ETR33003-003

85mΩ High Function Power Switch

■GENERAL DESCRIPTION

The XC8107 series is a P-channel MOSFET power switch IC with a low ON resistance. A current limit, reverse current prevention (prevents reverse current from V_{OUT} to V_{IN}), soft start, thermal shutdown, and an under voltage lockout (UVLO) are incorporated as protective functions. A flag function monitors the power switch status. The flag output has N-channel open drain configuration, and it outputs Low level signal when over-current or overheating is detected, or when the reverse current prevention is operated. The voltage level which is fed to CE pin determines the status of XC8107. The logic level of CE pin is selectable between either one of active high or active low.

■APPLICATIONS

- Set Top Boxes
- ●Digital TVs
- PCs
- ●USB Ports/USB Hubs
- ●HDMI

■FEATURES

Input Voltage : 2.5V~5.5V

Maximum Output Current : 2A

ON Resistance : $85m\Omega@V_{IN}=5.0V$ (TYP.) *USP-6C

 $100m\Omega@V_{IN}=5.0V$ (TYP.) *SOT-25

* At over-current detection

: 4ms(TYP.)

* At reverse voltage detection Protection Circuit : Reverse Current Prevention

Thermal Shutdown

Under Voltage Lockout(UVLO)

Soft-start

Functions : Flag Output

Current Limit Response Time

CE Pin Input Logic Selectable : 2µs(TYP.) *Reference value

Operating Ambient Temperature : -40°C~+105°C

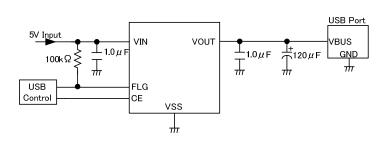
Packages : USP-6C, SOT-25

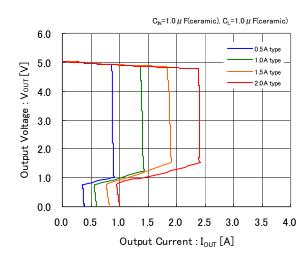
Environmentally Friendly : EU RoHS Compliant, Pb Free

■TYPICAL APPLICATION CIRCUIT

■TYPICAL PERFORMANCE CHARACTERISTICS

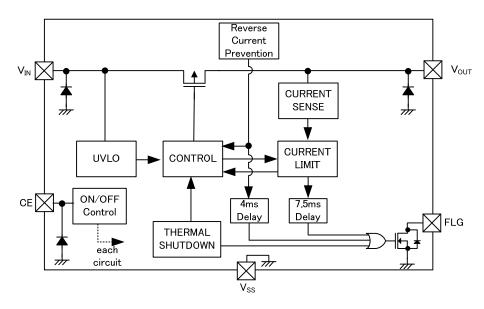
XC8107xCxxxR





■BLOCK DIAGRAM

XC8107 Series



^{*} Diodes inside the circuit are an ESD protection diode and a parasitic diode.

■PRODUCT CLASSIFICATION

Ordering Information

XC8107123456-7

DESIGNATOR	ITEM	SYMBOL	DESCRIPTION
(1)	CE Logio	Α	
U	CE Logic	В	Refer to Selection Guide
2	Protection Circuits Type	С	Refer to Selection Guide
∠	Protection Circuits Type	D	
		05	0.5A
34	Maximum Output Current	10	1.0A
3.4		15	1.5A
		20	2.0A
(F)(F)_(7) (*1)	Packagos	ER-G	USP-6C (3,000/Reel)
\$\(\text{6}-\bar{7}\) (*1)	Packages	MR-G	SOT-25 (3,000/Reel)

 $^{^{(1)}}$ The "-G" suffix denotes Halogen and Antimony free as well as being fully EU RoHS compliant.

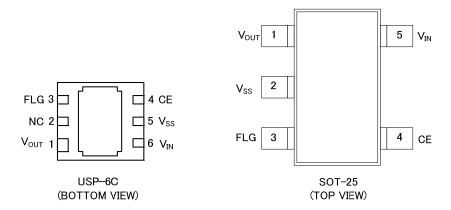
Selection Guide

TYPE	CE LOGIC SELECTABLE	SOFT-START	CURRENT LIMITTER
AC	Active High	Yes	Yes
AD	Active High	Yes	Yes
ВС	Active Low	Yes	Yes
BD	Active Low	Yes	Yes

TYPE	UVLO	FLG OUTPUT	REVERSE CURRENT PREVENTION
AC	Yes	Yes	Yes
AD	Yes	Yes	Yes
ВС	Yes	Yes	Yes
BD	Yes	Yes	Yes

TYPE	THERMAL SHUT DOWN	LATCH PROTECTION
AC	Yes	No
AD	Yes	Yes
ВС	Yes	No
BD	Yes	Yes

■PIN CONFIGURATION



^{*} The dissipation pad for the USP-6C packages should be solder-plated for mounting strength and heat dissipation.

Please refer to the reference mount pattern and metal masking. The dissipation pad should be connected to the V_{SS} (No. 5) pin.

■PIN ASSIGNMENT

PIN NUI	MBER	PIN NAME	FUNCTIONS
USP-6C	SOT-25	FIN NAIVIE	FUNCTIONS
1	1	Vout	Output
2	-	NC	No connection
3	3	FLG	Fault Report
4	4	CE	ON/OFF Control
5	2	V_{SS}	Ground
6	5	VIN	Power Input

■FUNCTION

TYPE	PIN NAME	SIGNAL	STATUS	
		Н	Active	
А		L	Stand-by	
	05	OF.	OPEN	Undefined State (*1)
	B CE	Н	Stand-by	
В		L	Active	
		OPEN	Undefined State (*1)	

^{*} Avoid leaving the CE pin open; set to any fixed voltage.

■ABSOLUTE MAXIMUM RATINGS

Ta=25°C

PARAMETE	PARAMETER		RATINGS	UNITS					
Input Voltag	ge	V _{IN}	-0.3~+6.0	٧					
Output Volta	ige	Vout	-0.3~+6.0	٧					
Output Curre	ent	Іоит	2.8	Α					
CE Input Volt	CE Input Voltage		-0.3~+6.0	٧					
FLG Pin Volt	FLG Pin Voltage		-0.3~+6.0	٧					
FLG Pin Curi	FLG Pin Current		15	mA					
	USP-6C		120						
Power Dissipation	037-60	USF-0C	03F-00	03F-00	03F-00	USF-0C	Pd	1000 (PCB mounted) (*2)	mW
Power Dissipation	SOT 25] Fu	250	IIIVV					
	SOT-25		600 (PCB mounted) (*2)						
Operating Ambient T	Operating Ambient Temperature		-40 ~ +105	°C					
Storage Tempe	rature	Tstg	-55 ∼ +125	°C					

 $^{^{\}star}\,\text{All}$ voltages are described based on the $V_{\text{SS}}.$

 $^{^{(^{\}star}1)}$ Use with I_{OUT} less than Pd/(V_{IN}\text{-V}_{\text{OUT}})\,.

^(*2) This is a reference data taken by using the test board. Please refer to page 24 and 25 for details.

■ELECTRICAL CHARACTERISTICS

Ta=25°C

PARAMETER	SYMBOL	C	ONDITIONS	MIN.	TYP.	MAX.	UNITS	CIRCUIT
Input Voltage	V _{IN}	-		2.5	-	5.5	V	1
		LICD CC	V _{IN} =3.3V (*1)	-	100	110	mΩ	
On Besistance		USP-6C	V _{IN} =5.0V (*1)	-	85	104	mΩ	①
On Resistance	Ron	007.05	V _{IN} =3.3V (*1)	-	115	135	mΩ	1
		SOT-25	V _{IN} =5.0V (*1)	-	100	120	mΩ	
Supply Current	Iss	V _{OUT} =OPE	ΞN	-	40	75	μA	2
		V _{IN} =5.5V,	V _{OUT} =OPEN					
Stand-by Current	Іѕтву	V _{CE} =V _{SS} (XC8107A series)	-	0.01	1.0	μA	2
		V _{CE} =V _{IN} ()	(C8107B series)					
		V _{IN} =5.5V,	V _{OUT} =0V					
Switch Leakage Current	ILEAK	V _{CE} =V _{SS} (XC8107A series)	-	0.01	1.0	μA	2
		V _{CE} =V _{IN} ()	(C8107B series)					
		V _{OUT} =V _{IN} -	0.3V,	0.01	0.90	0.00	_	
		XC8107xx	05 series	0.81	0.90	0.99	Α	
		V _{OUT} =V _{IN} -	0.3V,	1.26	1.40	1.54	_	
Current Limit	l	XC8107xx	(10 series	1.20	1.40	1.54	Α	1)
Current Limit	I _{LIMT}	V _{OUT} =V _{IN} -	0.3V,	1.71	1.90	2.09	_	U
		XC8107xx	<15 series	1.71	1.90	2.09	Α	
		V _{OUT} =V _{IN} -	V _{OUT} =V _{IN} -0.3V,		2.40	2.64	Α	
		XC8107xx	c20 series	2.16	2.40	2.04	^	
		V _{OUT} =0V,		_	0.45	_	Α	
		XC8107xx	(05 series		0.43		^	
		V _{OUT} =0V,		_	0.70	_	Α	
Short-Circuit Current	I _{SHORT}	XC8107xx	(10 series		0.70			1
Short Should Surrent	ISHORI	V _{OUT} =0V,		_	0.95	_	Α	•
		XC8107xx	(15 series		0.55			
		V _{OUT} =0V,		_	1.20	_	Α	
		XC8107xx			1.20		, ,	
			V _{OUT} : OPEN→0V					
Current Limit Circuit	t _{CLR}		rom V _{OUT} =0V	_	2.0	_	μs	1
Response Time (*2)	302.1		urrent falls below					O
		a certain I		4.5				
CE "H" Level Voltage	V_{CEH}		XC8107A series	1.5	-	5.5	V	1
-			XC8107B series	-	-	0.8		
CE "L" Level Voltage	V _{CEL}		XC8107A series	- 4.5	-	0.8	V	1
OF "H" Lovel Overser	1		XC8107B series	1.5	-	5.5	^	<u> </u>
CE "H" Level Current CE "L" Level Current	I _{CEH}	V _{IN} =5.5V, V _{CE} =5.5V		-0.1 -0.1	-	0.1	μΑ	1
CE L Level Current	I _{CEL}	V _{IN} =5.5V, V _{CE} =0V		-U. I	-	0.1	μA	\cup
UVLO Detected Voltage	V _{UVLOD}	V _{IN} : 2.2V→1.7V		1.8	1.9	2.0	V	1
UVLO Released Voltage	V _{UVLOR}	V _{IN} : 1.7V→2.2V		1.9	2.0	2.1	V	1
UVLO Hysteresis	Vuhys	-			0.1	_	V	1

NOTE:

Unless otherwise stated, V_{IN} =5.0V, I_{OUT} =1mA, V_{CE} = V_{IN} (XC8107A series) or V_{CE} = V_{SS} (XC8107B series)

 $^{^{(^{1})}} I_{OUT} = 0.25 A \ (XC8107xx05 \ series), \ I_{OUT} = 0.5 A \ (XC8107xx10 \ series), \ I_{OUT} = 0.75 A \ (XC8107xx15 series), \ I_{OUT} = 1.0 A \ (XC8107xx20 \ series)$

 $[\]ensuremath{^{(\mbox{\tiny{$^{\prime}}$2})}}$ Design reference value. This parameter is provided only for reference.

■ ELECTRICAL CHARACTERISTICS (Continued)

Ta=25°C

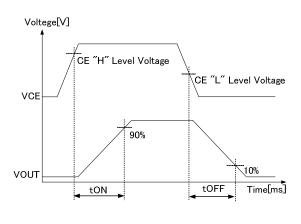
PARAMETER	SYMBOL	CONDITI	ONS	MIN.	TYP.	MAX.	UNITS	CIRCUIT
turn-on time	ton	R _{LOAD} =10Ω, V _{CE} =0)V→2.2V	-	0.60	1.00	ms	1
turn-off time	toff	R _{LOAD} =10Ω, V _{CE} =2	2.2V→0V	-	0.08	0.13	ms	1
FLG output FET On-resistance	R _{FLG}	I _{FLG} =10mA, V _{OUT} =	5.5V	-	15	20	Ω	3
FLG output FET Leakage Current	lfoff	V _{IN} =5.5V, V _{FLG} =5.5V	V, V _{OUT} =OPEN	-	0.01	0.1	μA	3
ELC delay time	t _{FD1}	over-current condition		6.5	7.5	8.5	ms	1
FLG delay time	t _{FD2}	reverse-voltage condition		2.7	4.0	4.7	ms	1
Reverse Current	I _{REV}	V _{IN} =0V, V _{OUT} =5.5V V _{CE} =5.0V (XC8107A series) V _{CE} =V _{SS} (XC8107B series)		-	0.1	1.0	μA	①
Reverse Current	.,	V _{IN} : 5.0V→4.7V	SOT-25	-	170	-	.,	0
Prevention Detect Voltage	V _{REV_D}	V _{OUT} =5.0V	USP-6C	-	140	-	mV	1
Thermal Shutdown Detect Temperature	T_{TSD}	Junction Temperature		-	150	ī	°C	1
Thermal Shutdown Release Temperature	T _{TSR}	Junction Temperature		-	130	i	°C	1
Thermal Shutdown Hysteresis Width	T _{HYS}	Junction Tempera	ture	-	20	-	°C	1

NOTE:

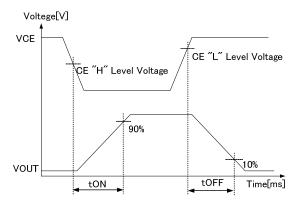
Unless otherwise stated, V_{IN} =5.0V, I_{OUT} =1mA, V_{CE} = V_{IN} (XC8107A series) or V_{CE} = V_{SS} (XC8107B series)

TIMING CHART

●turn-on time, turn-off time



XC8107 Series, Type A

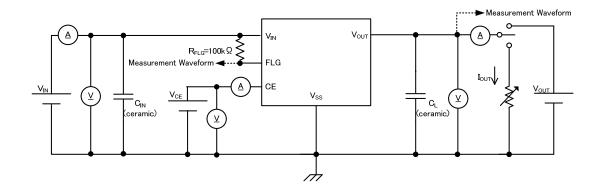


XC8107 Series, Type B

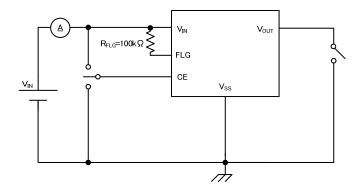
■TEST CIRCUITS

 C_{IN} =1.0 μ F, C_L =1.0 μ F

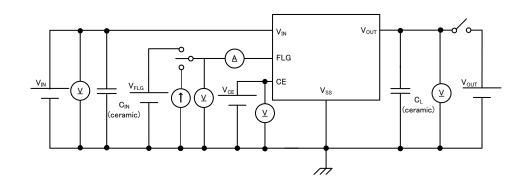
1) CIRCUIT①



2) CIRCUIT②



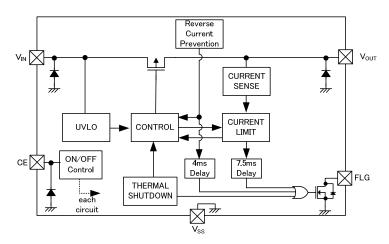
3) CIRCUIT®



■OPERATIONAL EXPLANATION

The XC8107 series is a P-channel MOSFET power switch IC.

The XC8107 series consists of a CE circuit, UVLO circuit, thermal shutdown circuit, current limiter circuit, reverse current prevention circuit, control block and others. The gate voltage of the power switch transistor is controlled with control block. The current limiter circuit and reverse current prevention circuit will operate based on the output voltage and output current. (See the BLOCK DIAGRAM below)



BLOCK DIAGRAM (XC8107 Series)

<CE Pin>

The voltage level which is fed to CE pin controls the status of this IC. If either "H" level or "L" level which is defined as the electrical specification is fed to CE pin, then XC8107 can operate in standard manner. However, if the middle voltage which is neither "H" level nor "L" level is fed to CE pin, the consumption current will increase due to the shoot-through current at internal circuits. Also if CE pin is open, the status of XC8107 cannot be fixed and the behavior will be unstable.

<Thermal Shutdown>

For protection against heat damage of the ICs, thermal shutdown function is built in. When the internal junction temperature reaches the temperature limit, the thermal shutdown circuit operates and the power switch transistor will turn OFF. The IC resumes its operation when the thermal shutdown function is released and the IC's operation is automatically restored because the junction temperature drops to the level of the thermal shutdown release temperature. When the thermal shutdown circuit detects higher junction temperature than the detect temperature, the voltage level of FLG pin is low level. When the thermal shutdown circuit detects lower junction temperature than the release temperature, the thermal shutdown function is released and the voltage level of FLG pin is high level.

<Under Voltage Lockout (UVLO) >

When the V_{IN} pin voltage goes down to lower voltage than UVLO detected voltage, the power switch transistor turns OFF by UVLO function in order to prevent false output caused by unstable operation of the internal circuitry. When the V_{IN} pin voltage goes up to higher voltage than UVLO released voltage, the UVLO function is released and the power switch transistor can turn ON.

<Soft-start Function>

The soft-start circuit can reduce the in-rush current charged on the output capacitor when IC starts up. Additionally, due to the reduction of the in-rush current, the circuit can reduce the fluctuation of the input voltage as well. The soft-start time is optimized internally and defined as turn-on time. (TYP: 0.6ms)

■ OPERATIONAL EXPLANATION (Continued)

<Current limiter, short-circuit protection>

When the output current reaches the current limit value, the constant current limiter circuit activates and as a result, the output voltage goes down.

If the short circuit comes at the V_{OUT} pin, the output current is limited to the current which is specified as the short-circuit current value. If the over-current state lasts for 7.5ms (TYP.), the FLG pin changes to Low level output.

Two types are available for the current limiter circuit: an auto recovery type (product type C) and a latch off type (product type D). After the current limiter circuit activates and the FLG pin outputs low level, the operation is different between these two types.

The auto recovery type continuously limits the output current by the current limit value.

When the over-current status finishes and the status of that the output current is less than the current limit value continues for 7.5ms (TYP.) or more, the voltage of FLG pin goes up "H" level again.

The latch off type turns off the power switch transistor after the FLG pin outputs Low level. The off state is maintained regardless of whether the over-current state is released.

Latch operation is released by turning off the IC with the CE pin signal and then restarting, or by lowering the input voltage below the UVLO detected voltage once and after that raising it higher than UVLO released voltage.

<Reverse current prevention>

An internal circuit is built in that prevents reverse current from the V_{OUT} pin to the V_{IN} pin.

When the difference between input voltage and V_{OUT} pin voltage is higher than the detect voltage set internally, the reverse current prevention circuit activates, and the power switch transistor turns off, then the reverse current from the V_{OUT} pin to the V_{IN} pin is reduced to $0.1\mu A$ (TYP.).

If the reverse-voltage state lasts for 4ms (TYP.), the FLG pin changes to Low level output.

Two types are available for the reverse current prevention circuit: the auto recovery type (product type C) and the latch off type (product type D). After the reverse current prevention circuit activates and the FLG pin outputs low level, the operation is different between these two types.

On the auto recovery type, when the output voltage drops below the input voltage, the reverse current prevention circuit stops immediately, and the power switch transistor turns on again. If the output voltage remains lower than the input voltage for 4ms (TYP.), the FLG pin returns to High level output.

On the latch off type, the power switch transistor remains in the off state even if the reverse voltage state is released. Latch operation is released by turning off the IC with the CE pin signal and then restarting, or by lowering the input voltage below the UVLO detected voltage once and after that raising it higher than UVLO released voltage.

■ OPERATIONAL EXPLANATION (Continued)

<Flag function>

The flag circuit is built in which monitors the state of the power switch.

The FLG pin outputs Low level when the reverse current prevention function is operating. A resistance of $10k\Omega$ to $100k\Omega$ is recommended for the FLG pin pull-up resistance.

Auto recovery type (product type C)

Protective function	FLG pin Low level output	Return to FLG pin High level output
Current limiter	7.5ms after over-current detection	7.5ms after over-current release
Reverse current prevention	4.0ms after reverse voltage detection	4.0ms after reverse voltage release
Thermal shutdown	Same time as overheat state is detected	Same time as overheat state is released

Latch off type (product type D)

Protective function	FLG pin Low level output	Return to FLG pin High level output
Current limiter	7.5ms after over-current detection	When latch operation is released
Reverse current prevention	4.0ms after reverse voltage detection	When latch operation is released
Thermal shutdown	Same time as overheat state is detected	Same time as overheat state is released

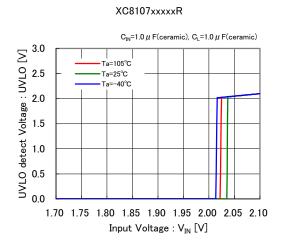
■NOTES ON USE

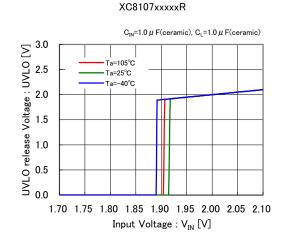
- 1. For the phenomenon of temporal and transitional voltage decrease or voltage increase, the IC may be damaged or deteriorated if IC is used beyond the absolute MAX. specifications.
- 2. Where wiring impedance is high, operations may become unstable due to noise depending on output current. Please keep the resistance low between V_{IN} and V_{SS} wiring in particular.
- 3. Please place the input capacitor (C_{IN}) and the output capacitor (C_L) as close to the IC as possible. For the input or output capacitor, a capacitance of 1.0µF or higher is recommended.
- 4. When the voltage which is higher than the maximum input voltage is fed to the V_{IN} pin, and V_{OUT} is shorted to the V_{SS} level, in this case the short circuit may cause a fatal impact to operation for the IC. Please use within the operational voltage range.
- 5. Torex places an importance on improving our products and its reliability.

 However, by any possibility, we would request user fail-safe design and post-aging treatment on system or equipment.

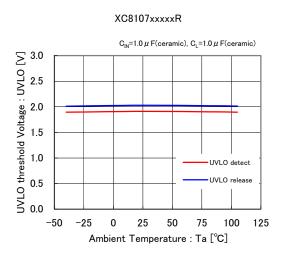
■TYPICAL PERFORMANCE CHARACTERISTICS

- (1) UVLO detect Voltage vs. Input Voltage
- (2) UVLO release Voltage vs. Input Voltage

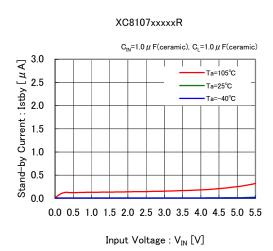




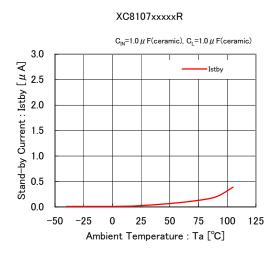
(3) UVLO threshold Voltage vs. Ambient Temperature



(4) Stand-by Current vs. Input Voltage



(5) Stand-by Current vs. Ambient Temperature



(6) Supply Current vs. Input Voltage (sweep up)

Input Voltage : V_{IN} [V]

 $0.0 \ 0.5 \ 1.0 \ 1.5 \ 2.0 \ 2.5 \ 3.0 \ 3.5 \ 4.0 \ 4.5 \ 5.0 \ 5.5$

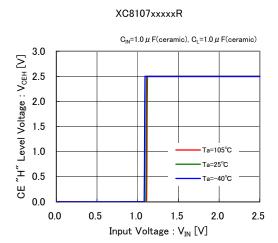
(8) CE "H" Level Voltage vs. Input Voltage

 C_{IN} =1.0 μ F(ceramic), C_L =1.0 μ F(ceramic) 50 45 Supply Current : $I_{SS} \left[\mu A \right]$ 40 35 30 25 20 15 10 5 0 -50 -25 0 25 50 75 100 125 Ambient Temperature : Ta [°C]

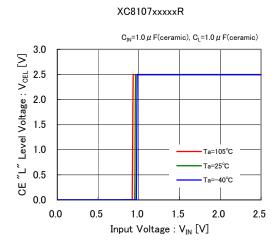
XC8107xxxxxR

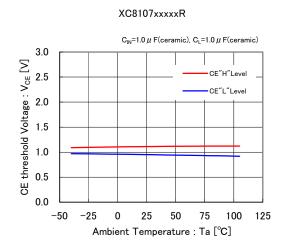
(7) Supply Current vs. Ambient Temperature

(9) CE "L" Level Voltage vs. Input Voltage

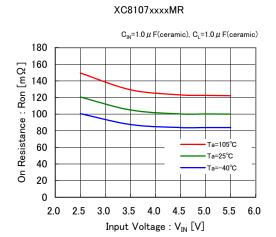


(10) CE threshold Voltage vs. Ambient Temperature

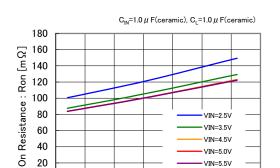




(11) On Resistance vs. Input Voltage (SOT-25)



(12) On Resistance vs. Ambient Temperature (SOT-25)



Ambient Temperature: Ta [°C]

75

100

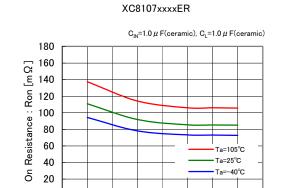
XC8107xxxxMR

c) (14) On Resistance

-50

-25

vs. Ambient Temperature (USP-6C)

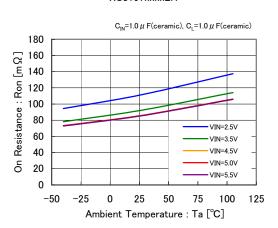


3.5 4.0 4.5 5.0 5.5

Input Voltage : V_{IN} [V]

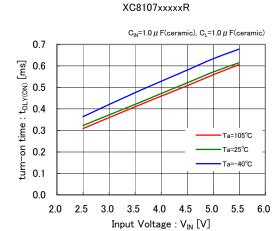
(13) On Resistance vs. Input Voltage (USP-6C)

XC8107xxxxER

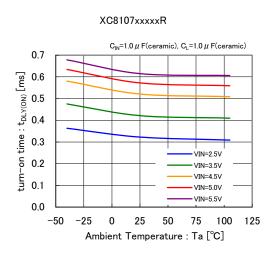


(15) turn-on time vs. Input Voltage

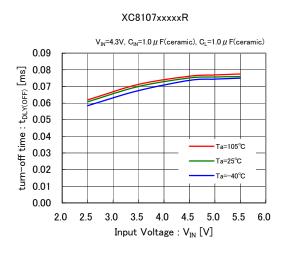
2.5



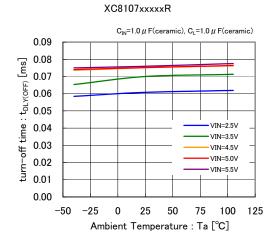
(16) turn-on time vs. Ambient Temperature



(17) turn-off time vs. Input Voltage

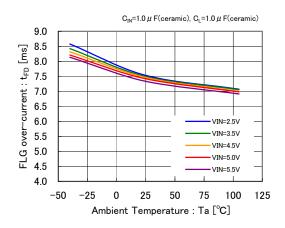


(18) turn-off time vs. Ambient Temperature



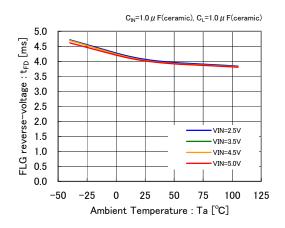
(19) FLG delay time over-current vs. Ambient Temperature





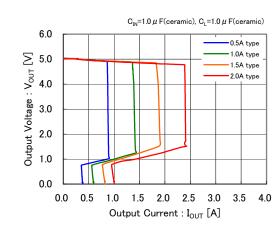
(20) FLG delay time reverse-voltage vs. Ambient Temperature

XC8107xxxxxR

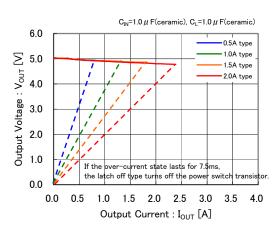


(21) Output Voltage vs. Output Current

XC8107xCxxxR

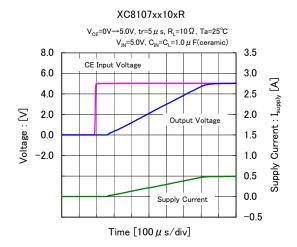


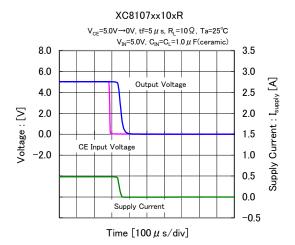
XC8107xDxxxR



(22) turn-on Delay vs. Rise Time ($C_L=1.0 \mu F$)

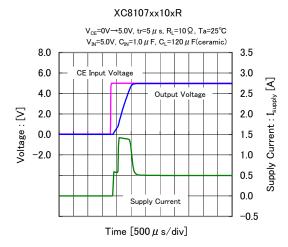
(23) turn-off Delay vs. Fall Time ($C_L=1.0 \mu F$)

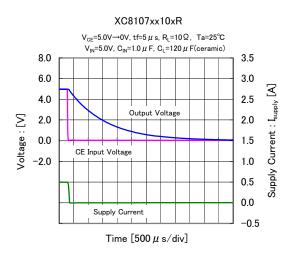




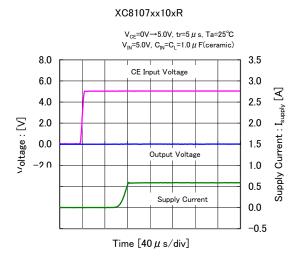
(24) turn-on Delay vs. Rise Time ($C_L=120 \mu F$)

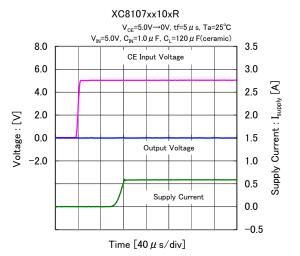
(25) turn-off Delay vs. Fall Time ($C_L=120 \mu F$)





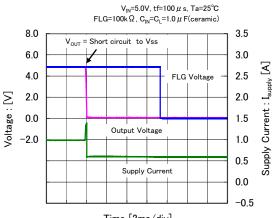
(26) Short Circuit Current, Device Enabled Into Short





(27) Short-Curcuit Transient Response $(V_{OUT}=5.0 \Omega \rightarrow short, C_L=1.0 \mu F)$

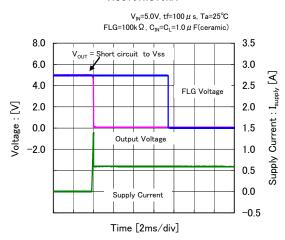
XC8107xC10xR



Time [2ms/div]

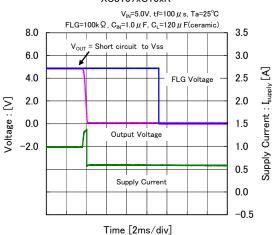
(29) Short-Curcuit Transient Response $(V_{OUT}=open \rightarrow short, C_L=1.0 \mu F)$

XC8107xC10xR

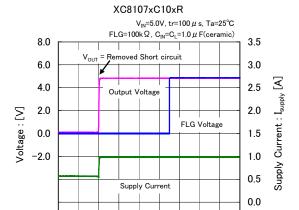


(31) Short-Curcuit Transient Response $(V_{OUT}=5.0 \Omega \rightarrow short, C_L=120 \mu F)$

XC8107xC10xR



(28) Short-Curcuit Transient Response $(V_{OUT}=short \rightarrow 5.0 \Omega, C_L=1.0 \mu F)$

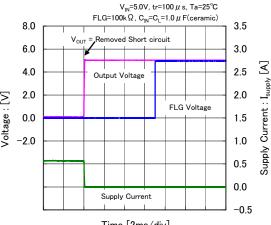


Time [2ms/div]

-0.5

(30) Short-Curcuit Transient Response $(V_{OUT}=short \rightarrow open, C_L=1.0 \mu F)$

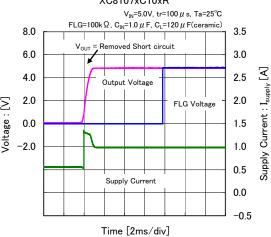




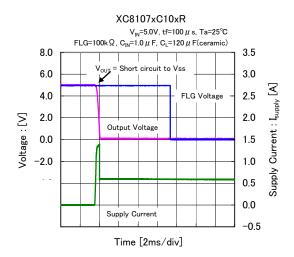
Time [2ms/div]

(32) Short-Curcuit Transient Response $(V_{OLIT}= short \rightarrow 5.0 \Omega, C_{I}= 120 \mu F)$

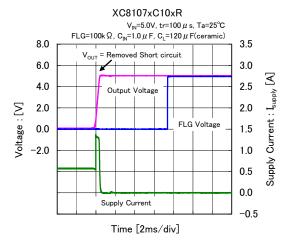
XC8107xC10xR



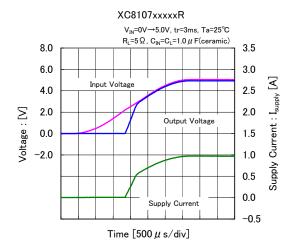
(33) Short-Curcuit Transient Response (V_{OUT}=open→short, C_L=120 μ F)

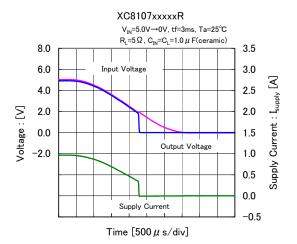


(34) Short-Curcuit Transient Response (V_{OUT}=short→open, C_L=120 μ F)

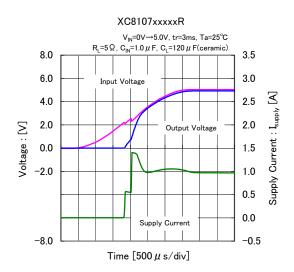


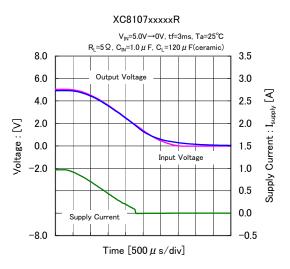
(35) UVLO Transient Response ($C_L=1.0 \mu F$)





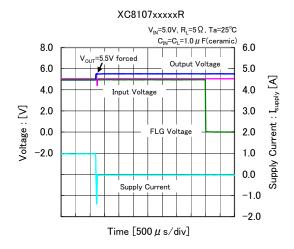
(36) UVLO Transient Response ($C_L=120 \mu F$)

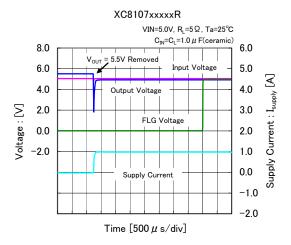




(37) Reverse Voltage Detected Voltage ($C_1 = 1.0 \mu F$)

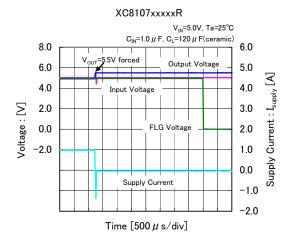
(38) Reverse Voltage Released Voltage ($C_1 = 1.0 \mu F$)

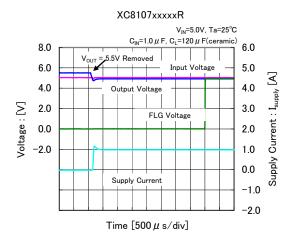




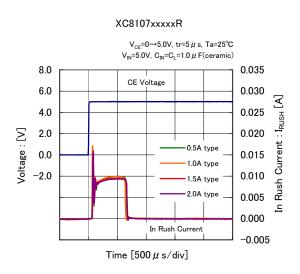
(39) Reverse Voltage Detected Voltage ($C_L=120 \mu F$)

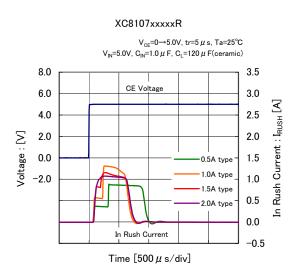
(40) Reverse Voltage Released Voltage (C_L =120 μ F)





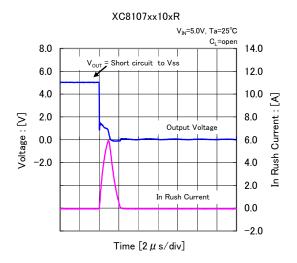
(41) CE Transient Response

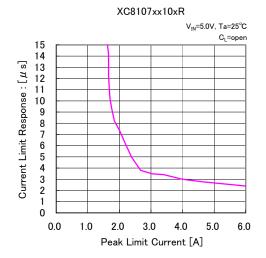




(42) Short Applied

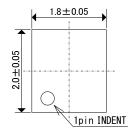
(43) Current Limit adapted time

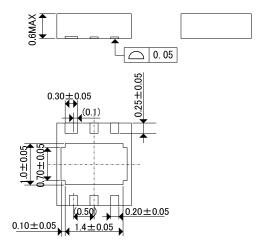




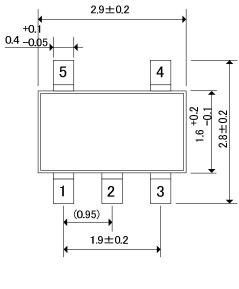
■PACKAGING INFORMATION

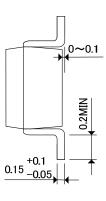
●USP-6C (unit:mm)





●SOT-25 (unit:mm)

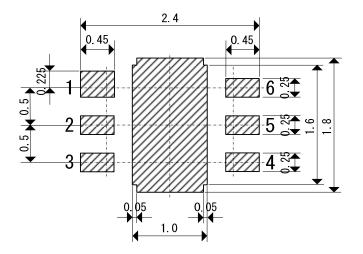


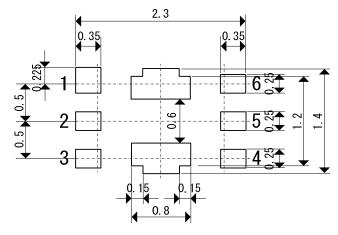




■ PACKAGING INFORMATION (Continued)

- ●USP-6C Reference Pattern Layout (unit: mm)
- ●USP-6C Reference Metal Mask Design (unit: mm)





■ PACKAGING INFORMATION (Continued)

SOT-25 Power Dissipation

Power dissipation data for the SOT-25 is shown in this page. The value of power dissipation varies with the mount board conditions. Please use this data as the reference data taken in the following condition.

1. Measurement Condition

Condition: Mount on a board

Ambient: Natural convection

Soldering: Lead (Pb) free

Board: Dimensions 40 x 40 mm (1600 mm² in one side)

Copper (Cu) traces occupy 50% of the board area

In top and back faces

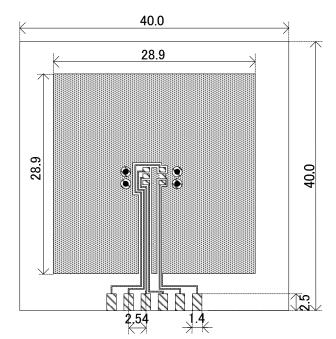
Package heat-sink is tied to the copper traces

(Board of SOT-26 is used)

Material: Glass Epoxy (FR-4)

Thickness: 1.6mm

Through-hole 4 x 0.8 Diameter

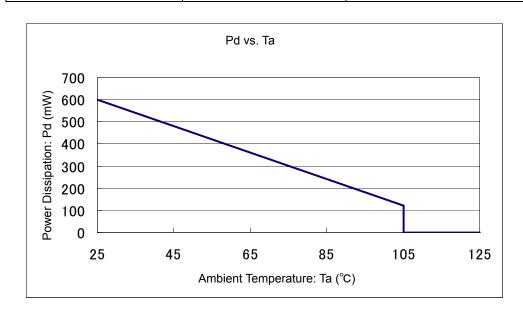


Evaluation Board (Unit: mm)

2. Power Dissipation vs. Ambient Temperature (105°C)

Board Mount (Tjmax=125°C)

Ambient Temperature (°C)	Power Dissipation Pd (mW)	Thermal Resistance (°C/W)
25	600	166.67
105	120	166.67



■ PACKAGING INFORMATION (Continued)

USP-6C Power Dissipation

Power dissipation data for the USP-6C is shown in this page. The value of power dissipation varies with the mount board conditions. Please use this data as the reference data taken in the following condition.

1. Measurement Condition

Condition: Mount on a board

Ambient: Natural convection

Soldering: Lead (Pb) free

Board: Dimensions 40 x 40 mm (1600 mm² in one side)

Copper (Cu) traces occupy 50% of the board area

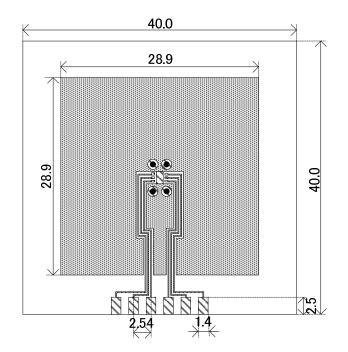
In top and back faces

Package heat-sink is tied to the copper traces

Material: Glass Epoxy (FR-4)

Thickness: 1.6mm

Through-hole 4 x 0.8 Diameter

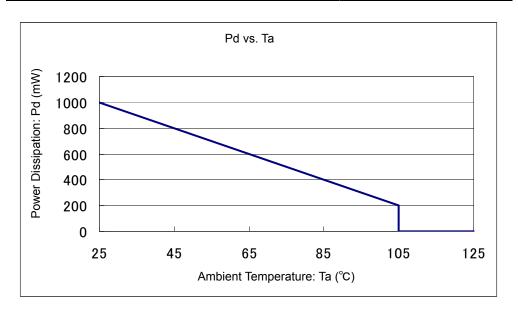


Evaluation Board (Unit: mm)

2. Power Dissipation vs. Ambient Temperature (105°C)

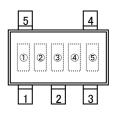
Board Mount (Tjmax=125°C)

Ambient Temperature (°C)	Power Dissipation Pd (mW)	Thermal Resistance (°C/W)	
25	1000	100.00	
105	200		

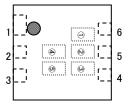


■ MARKING RULE

SOT-25



USP-6C



① represents products series

MARK	PRODUCT SERIES	
Z	XC8107*****-G	

2 represents product type

MARK	CE LOGIC	PROTECTION CIRCUIT TYPE	PRODUCT SERIES
1	Active High	Auto-recovery	XC8107AC****-G
2	Active High	Latch-off	XC8107AD****-G
3	Active Low	Auto-recovery	XC8107BC****-G
4	Active Low	Latch-off	XC8107BD****-G

③ represents maximum output current

MARK	CURRENT (A)	PRODUCT SERIES
1	0.5	XC8107**05**-G
2	1.0	XC8107**10**-G
3	1.5	XC8107**15**-G
4	2.0	XC8107**20**-G

45 represents production lot number

01~09, 0A~0Z, 11~9Z, A1~A9, AA~AZ, B1~ZZ in order.

(G, I, J, O, Q, W excluded)

^{*} No character inversion used.

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        XC8107AC15ER-G
        XC8107BC10MR-G
        XC8107BC15MR-G
        XC8107AC05MR-G
        XC8107BC05ER-G

        XC8107BD15ER-G
        XC8107AD10MR-G
        XC8107BC05MR-G
        XC8107BC10ER-G
        XC8107AC10MR-G

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