ECE 3750 Fundamentals of Electrical Engineering III

ECG Printed Circuit Board

May 8th, 2018

Honor Pledge:

On my honor as a student, I have neither given nor received unauthorized aid on this assignment.

Patrick Mahan, Andrew Powell, Patrick Rojas, Pierce Faraone

Group Member Responsibilities:

Patrick Mahan (phm4fv) - Soldering, Multisim schematics, mathematical verifications, board design and project leader

Andrew Powell (awp6rd) - Mathematical calculations, Multisim verifications, breadboard and final testing

Patrick Rojas (pjr2ea) - Mathematical calculations, mathematical verifications, board design, soldering, breadboard and final testing, and quadrilingual

Pierce Faraone (pf4tj) - Mathematical calculations, Multisim verifications, test subject, final testing, MyRIO connectivities

Section 1

1.1.1.Background

The aim of this project was to build a functional electrocardiograph (ECG) device using a printed circuit board (PCB). Electrocardiography (ECG) is the interpretation of the electrical activity of one's heart over a period of time. Generally, producing a valid ECG reading involves passing the heartbeat signal through various filters and amplifiers in order to get a usable output. Two of the electrodes used in ECG device measure a biopotential (a voltage produced in an organism) and the third acts as a reference.

For our specific project, the goal was to view a characteristic ECG signal on the V_{Out} measurement on the VirtualBench (VB). Subsystems were cascaded and soldered onto the PCB in order to create the majority of the device. These included: a shield driver, a power system, an instrumentation amplifier and a fourth-order Butterworth filter.

1.1.2. Explanation of expected signal levels and gain required

The expected input signal as measured from electrodes was on the order of magnitude of $100 - 1000\mu V$.

Power supply rails at through the circuit limited the voltages to half of 3.3 (1.65) V:

The gain is set in the AD627 instrumentation amplifier. The other stages such as the Butterworth filter and integrator were set to unity gain. Our group chose a gain in the AD627 of approximately 1000 or 60 dB. This value amplified the signal sufficiently to around ~1V which was useful, but not high enough to saturate at the power supply rails.

$$\text{Gain} = 5 + \frac{200000}{R_G} = 1000$$

$$R_G = 201\Omega,\ R_6 = R_1 + R_5 \Rightarrow R_1 = R_5 = 100\Omega$$

∗R1 and R5 are the values of the gain-setting resistors for AD627

1.1.3. Filtering Requirements

A fourth-order low-pass Butterworth filter in a Sallen-Key configuration was needed to satisfy the constraints of the ECG design. The Butterworth filter was chosen because it shows a characteristic maximally flat frequency response. In other words, the frequency response is as flat (no ripples) as possible from 0 Hz (DC) until the cut-off frequency at -3dB. Higher frequencies beyond the cut-off point rolls off down to zero in the stop band at 80 dB/Decade(20 □□/□□□□□□ $\times 4$). This is determined by the characteristic Butterworth quality factor of 0.707.

The requirements of the filter were:

1. Produce a gain of -72db/Decade at 500 Hz
2. Designed using resistor and capacitor values available
3. Act as an anti-aliasing filter to prevent aliasing of signals when measuring using the myRio DSP

As the filter required a gain of -72 dB/Dec at 500 Hz, the cutoff frequency (□□) had to be slightly after one decade before 500 Hz (i.e. 50 Hz). Since the achieved gain was 90 percent of the overall slope, we calculated 90 percent of the difference between the two decades, which was then taken into account by subtracting from the original frequency.

Using the Sallen-Key equations….These constraints were there to ensure sufficient attenuation of signal above 95 Hz (high frequency noise), while keeping the desired parts of the input signal.

Analytically, it was established that a 95Hz breakpoint and a -72 dB gain would occur at 500 Hz.

1.2. Schematics

This section details the functionality and design process for each functional block within the ECG device.

1.2.1. Power

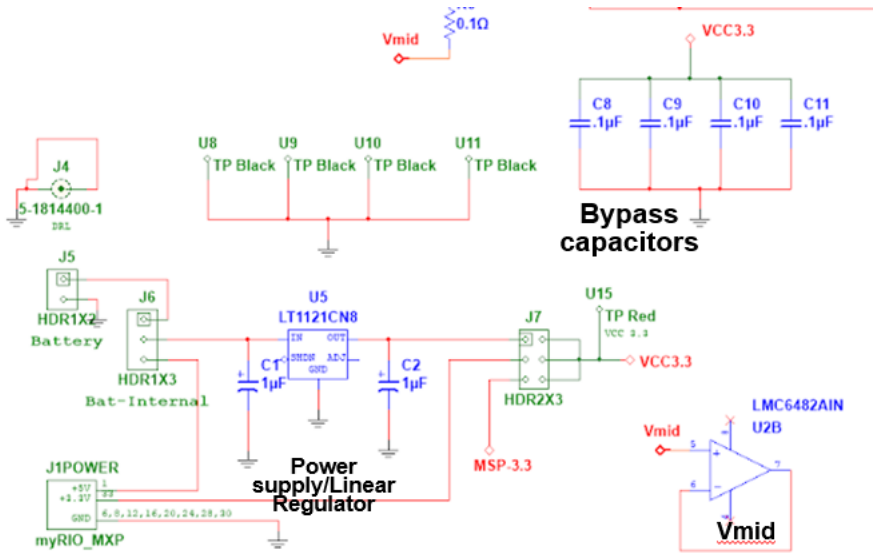


Figure 1: The Power Subsystem Sections

The bypass capacitors (C_8, C_9,C_{10}, C_{11}) were placed along active circuit elements. There purpose was to reduce the power supply noise and smooth the results of spikes on VCC3.3. Likewise, C_1 and C_2 acted as bypass capacitors for the power supply.

The different headers (J5, J1 Power etc.) were there to interface with different power supplies such as the 9V battery, the MSP430 and the myRIO.

The LTI1121CN8 linear regulator provides a constant output voltage of 3.3V when supplied by the potentially noisy and variable voltage of the 9V battery.

The $U2B\ V_{Mid}$was there to closed off used sections of the op-amp to prevent any unexpected behavior.

1.2.2. Fourth-order butterworth filter

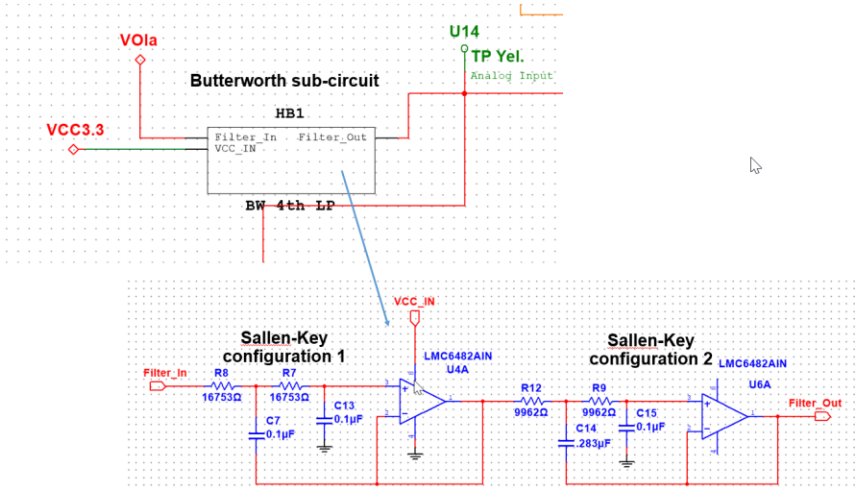


Figure 2: The Sallen Key Butterworth Filter

The design procedure involved these steps:

1. Identifying the overall quality factor of the 4th order BW: Q = 0.707
2. Selecting Q values for the cascaded stage 1 and stage 2 such that the component values using simplified equations where the filter components were ratios; calculating the component ratios and finally the values for each stage

Equations used:

$$\square = \frac{\sqrt{\square \times \square}}{\square + 1}$$

$$\omega_{\square} = \frac{1}{\square \cdot \square\sqrt{\square \cdot \square}}$$

$$\square 1 = \square\square, \square 2 = \square, \square 1 = \square, \square 2 = \square\square$$

Stage	**R8**	**R7**	**C7**	**C13**	**Q1**
1	16.753□□	16.753□□	0.1μ□	0.1μ□	0.5
Stage	**R12**	**R9**	**C14**	**C15**	**Q2**
2	0.9962□□	0.9962□□	0.283μ□	0.1μ□	1.414

∗Due to component restraints the values selected for values

1.2.3. Instrumentation Amplifier

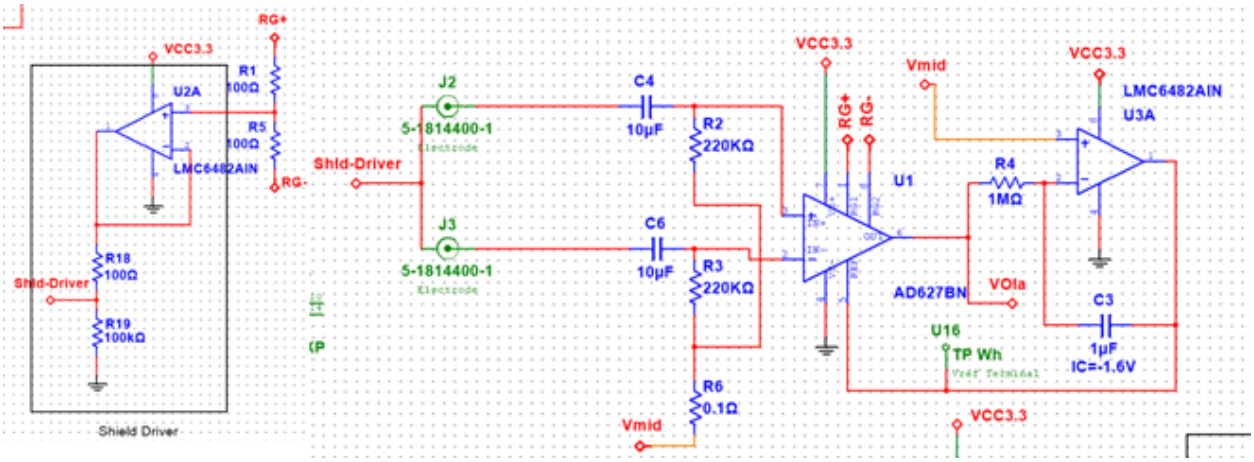


Figure 3: The Instrumentation Amplifier and Shield Driver Schematic

The purpose of the instrumentation amplifier is to buffer the output of centered around Vmid against offset changes.

The high pass filters on the left hand side of the subcircuit acted to remove DC signals entering instrumentation amplifier stage. They had a sufficiently low cutoff frequency (0.1Hz).

Using the conditions for the gain equation found in the AD627 specifications, we were able to solve for the total resistor gain from which we designed with the values of: ▯▯ = ▯▯ = ▯▯▯

The instrumentation amp provided a gain of about 1000, to amplify the difference of the two signals to around 10 - 100 mV and. Rg+ and Rg- were pins to the instrumentation amp, which were part of the shield driver circuit.

The integrator stage after was there to remove any remaining DC signals that may be present and center the output around V_{Mid} (1.65V).

The shield driver contained two gain-setting resistors (R1 and R5) in a voltage divider configuration that determine the gain of the IA. The midpoint voltage is the common mode voltage which ultimately provided a DC offset, therefore shielding the signal from interference as the signal travels.

1.2.4. Right-side driver

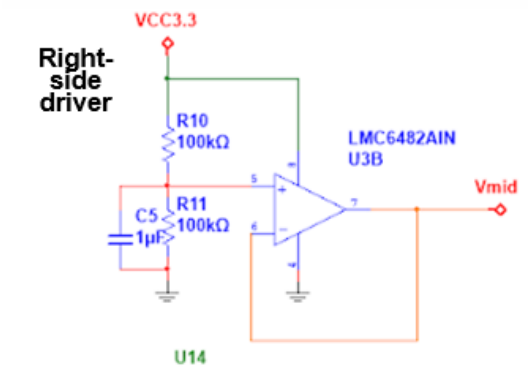


Figure 4: The Right Side Driver Schematic

The right-side driver acted as a voltage divider so that V_{Mid} was set at half of 3.3V or 1.65V which was the reference (ground) voltage. C_5 acted to smooth out noise coming in from VCC3.3

1.3. Multisim Simulations

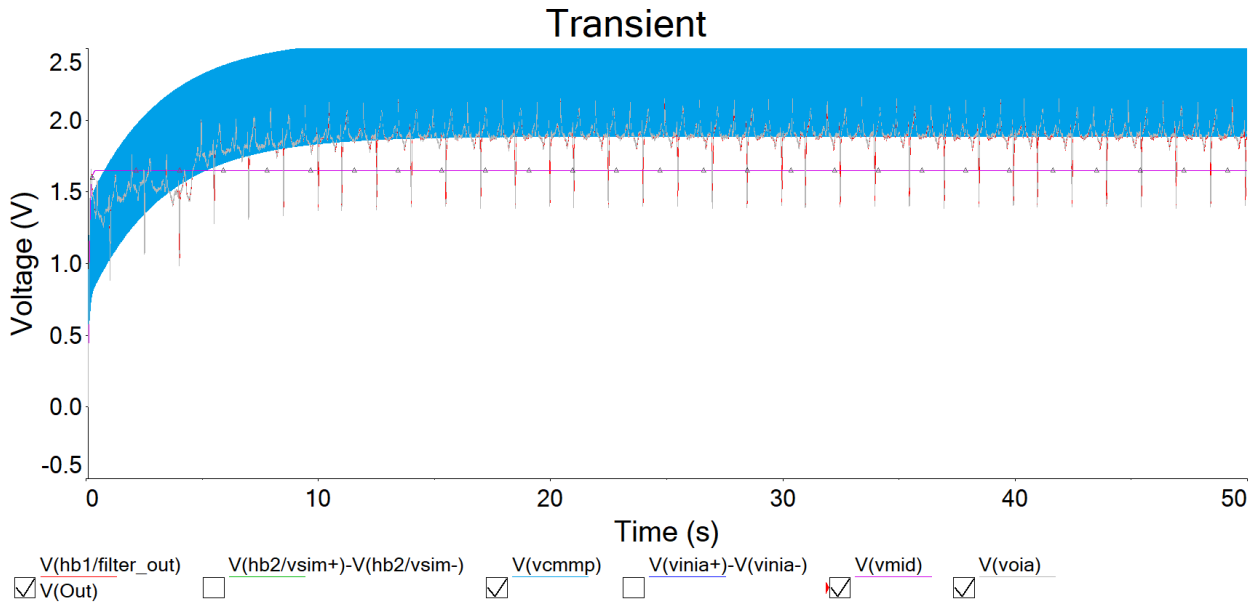


Figure 5: A Very Zoomed Out View of the System Over 50 Seconds

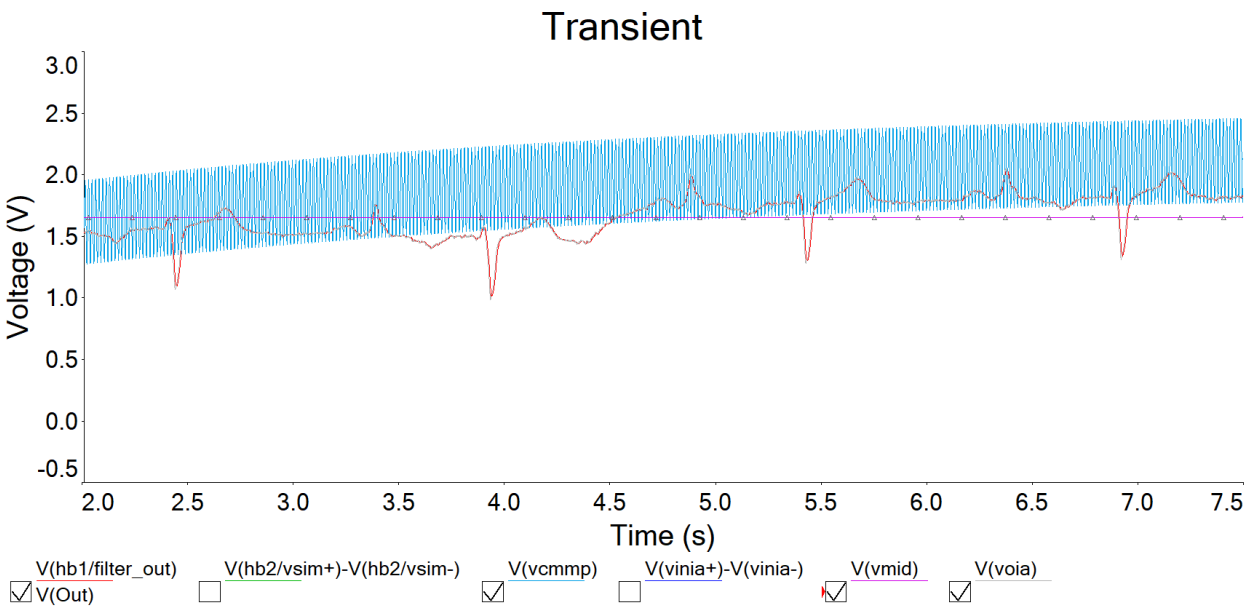


Figure 6: A Transient Analysis of Key Circuit Components at Scale

Figures 5 and 6 show the simulated system over time. The large spikes are the peaks and troughs of the heartbeat, the blue trace is common mode voltage. These simulations show a slight rise in values before leveling off, due to capacitive charging.

1.3.1. Frequency Domain Plots

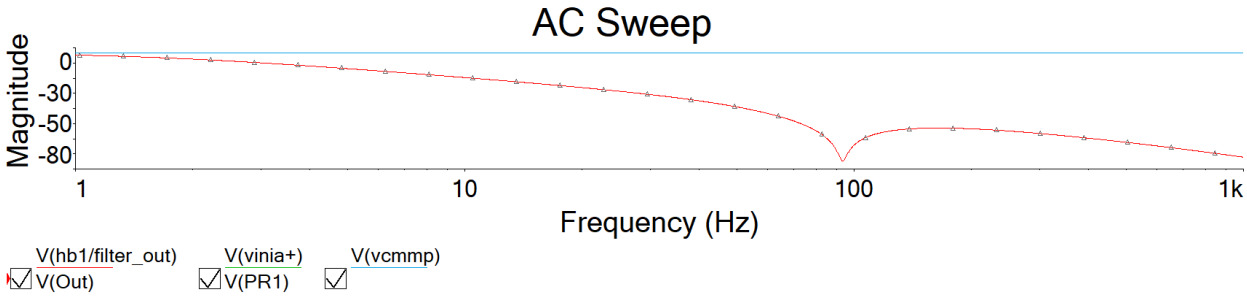


Figure 7: The System In the Frequency Domain

1.4. Layout

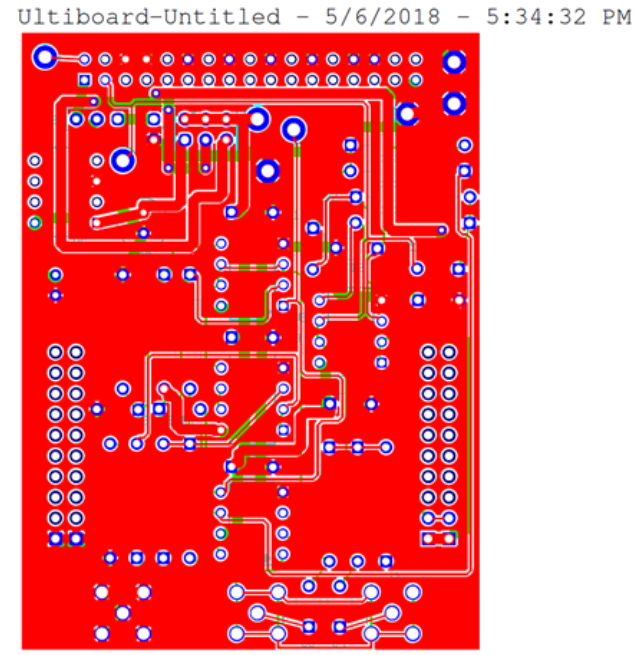


Figure 8: Top, Bottom, and Silk-Screen Overlay

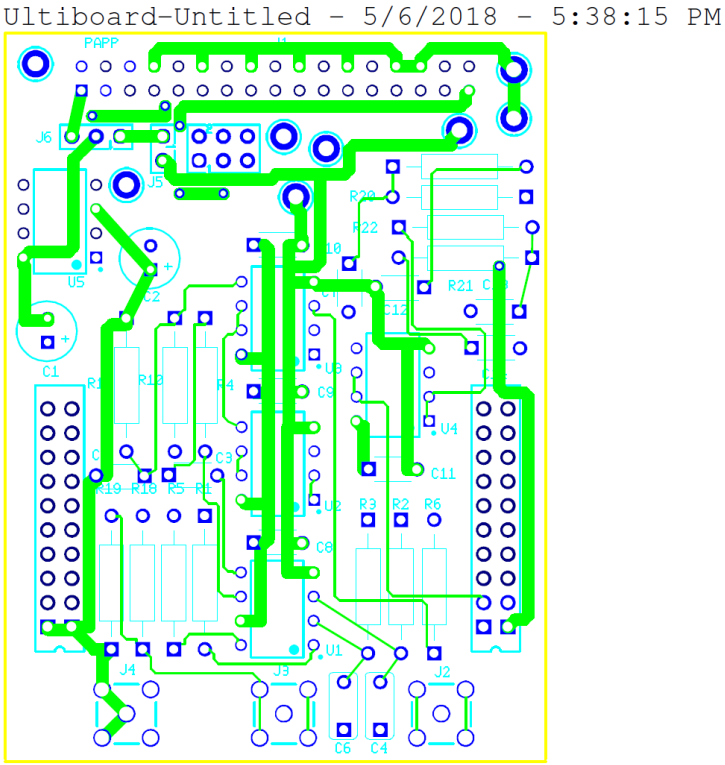


Figure 9: Top and Silk-Screen Overlay

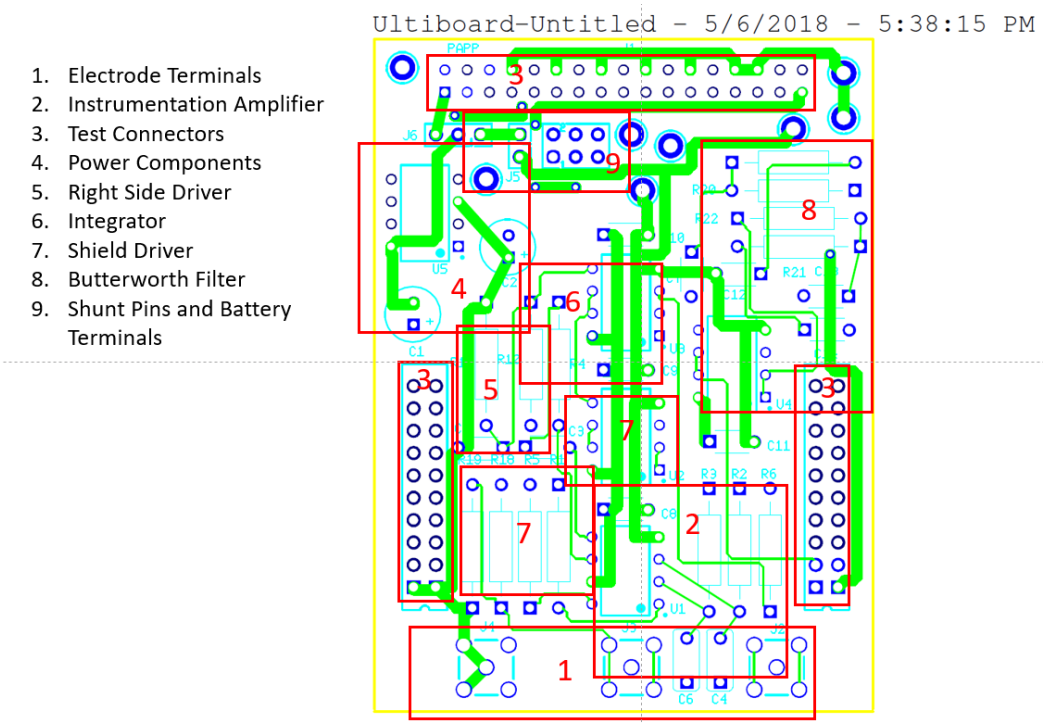


Figure 10: Annotated Board Layout Divided Into Subsections

1. The electrode terminals were placed for us by Professor Powell. There is enough space to comfortably add the connectors, and are easily accessible at the end of the board.
2. The natural place for the instrumentation amplifier is next to the electrode terminals to keep the signal traces short.
3. The test connectors were also placed for us by Professor Powell.
4. We grouped the power components in the top left corner of the board to keep them away from the signal components and to keep the 9 Volt traces as short as possible.
5. The Right-Side-Driver shares an Op-Amp with the Integrator, and both only require a few components. The middle of the board is already crowded with the Test Connectors and eventually the Butterworth Filter, so we squeezed the relatively small Right-Side-Driver and Integrator there.
6. See Number 5 Above.
7. The Shield Driver takes an input from the Instrumentation Amp, and its output shares a node with the Electrode Inputs to the Instrumentation Amp. Due to this, we placed the Shield Driver right above the Instrumentation Amp, to keep the traces short.
8. The Butterworth Filter is one of the largest sub-sections of the board, and takes up the majority of the right side of the board. This was where the majority of the remaining space was, so it was the natural place for the filter.
9. We placed the shunt pins and battery terminal next to the power components to keep the leads short, and to have all the connectors in one place.

We followed the usual CAM and FreeDFM process as outlined in the previous FUN classes. We encountered the same issue as usual, which is FreeDFM returns Ultiboard's default Silkscreen Font as a non-fatal error; thus it reported 500 silkscreen errors, despite nothing being wrong with the board. We did notice, however, that the FreeDFM sent its reports out much earlier, which was beneficial for receiving quick feedback and making adjustments in class.

Section 2

2.1. Assembly and Testing

Our team experienced a fair amount of difficulties with the assembly, all of which were due to our own negligence. We began by attaching the various test pins, followed by the power supply components. In order to test this, we used the Virtual Bench to supply 9 volts to the power input, and measured the readings on the VCC pins. At first, we measured 0 volts on the pin and after troubleshooting for a while, we realized that we forgot to put the shunts on the appropriate pins. A more potentially damaging problem involved the silkscreen for the bypass capacitors around the power supply. Due to an error when rotating the component in Ultiboard, the trace going to ground (Capacitor Negative) was marked with the + symbol. This could have had catastrophic effects on the power supply. Luckily, this error was caught before any soldering was done, and before power was supplied to the board.

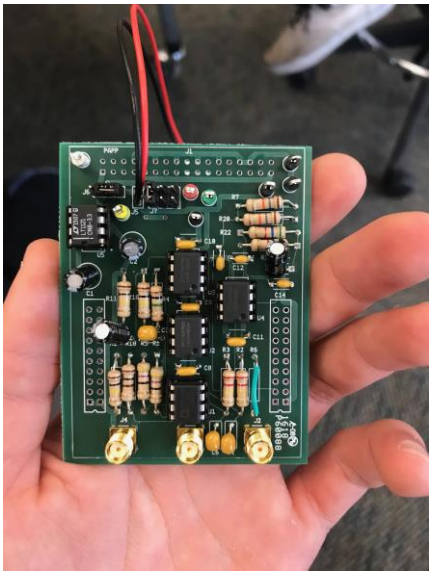
The next section to be assembled and tested was the section responsible for producing V_{Mid}. This section proved difficult for another assembly oversight. When soldering in the sockets, we applied solder to the corner pins in order to hold them in place. For the socket holding, the Op-Amp for the Right-Side Driver, we forgot to finish soldering the remaining pins. Once that was complete, we had no problems.

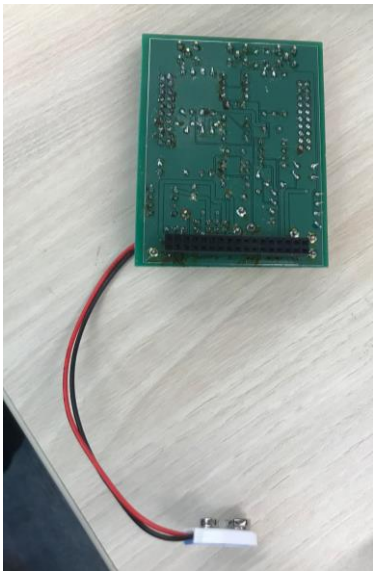
The remaining circuitry was fairly trivial to test. The Butterworth Filter simply required a signal sweep once we ascertained that the power was indeed connected to the Op-Amp. The instrumentation amplifier and shield driver were dependent on each other; thus after ensuring that power and ground were connected as expected, we assembled those sections in their entirety and tested the system as a whole.

We did not find many significant differences between testing on the breadboard and testing on the PCB. There were, however, fairly significant differences between our simulations and our physical testing. The simulations failed to account for 60 Hz interference from the electricity in the room, so at first we were surprised to see a wave on the output of our system before even attaching the electrodes. Once we saw that it was a fairly recognizable sine wave at 60 Hz, we quickly realized it was simply interference from the room, not a problem within our board.

Our final problem was, again, due to a lack of concentration during assembly. We soldered the female test pins onto the side of the board with the components, which made attaching to the myRio impossible. To remedy this, it took nearly half an hour of desoldering, and resulted in a somewhat unattractive connection. The analytical and simulated corner frequencies did not

match exactly but in conjunction with imperfections in the physical equipment, it was within an acceptable range for the purpose of our project.





2.2. Images

Figure 11: Front and Back of the PCB

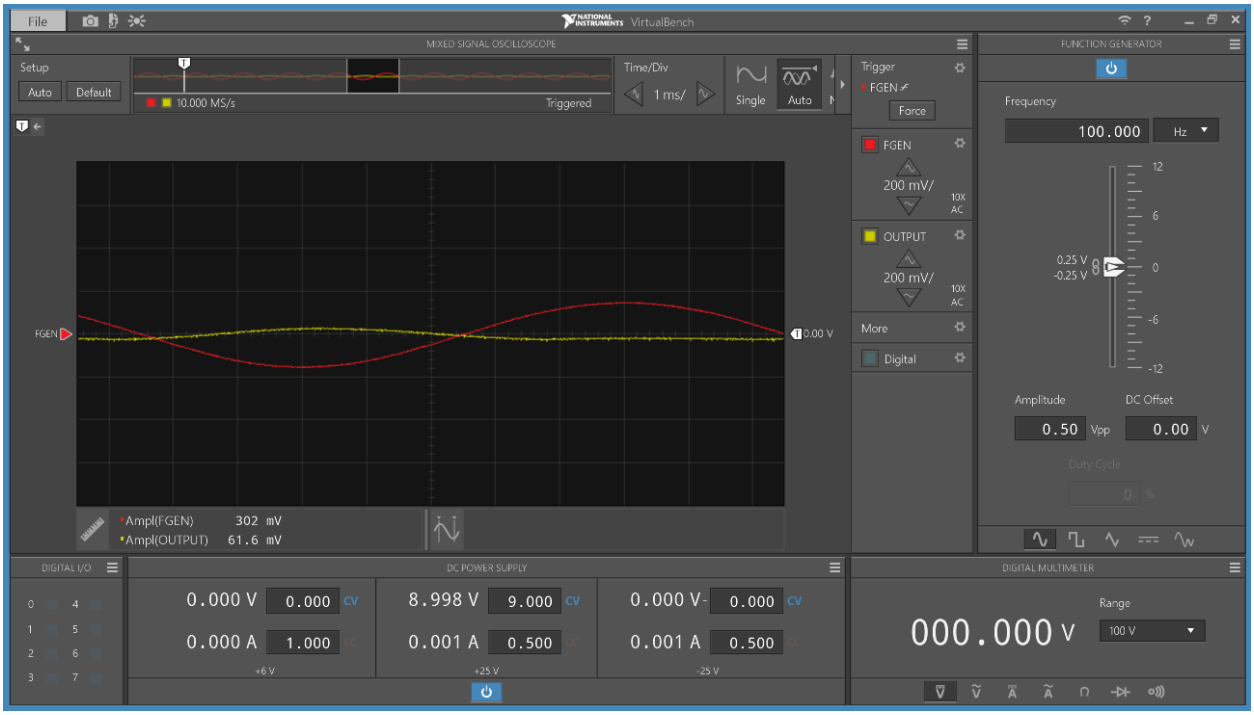


Figure 12: 4th Order Butterworth Filter at 100 Hz

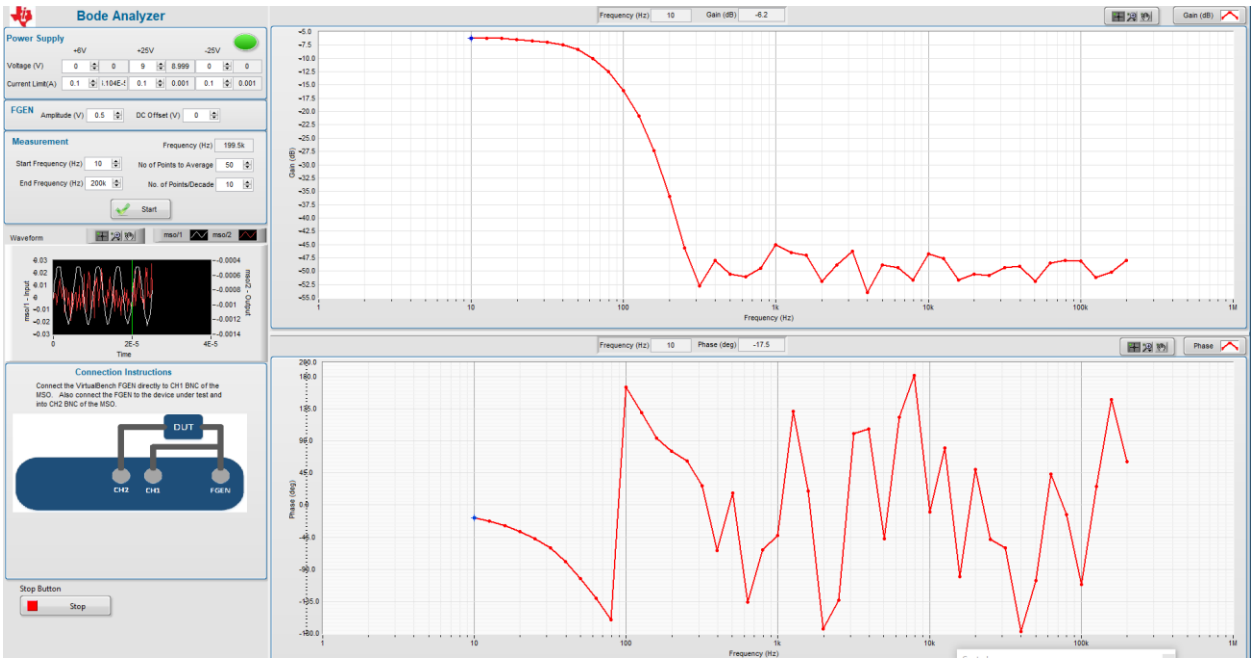


Figure 13: Frequency Response of the Butterworth Filter

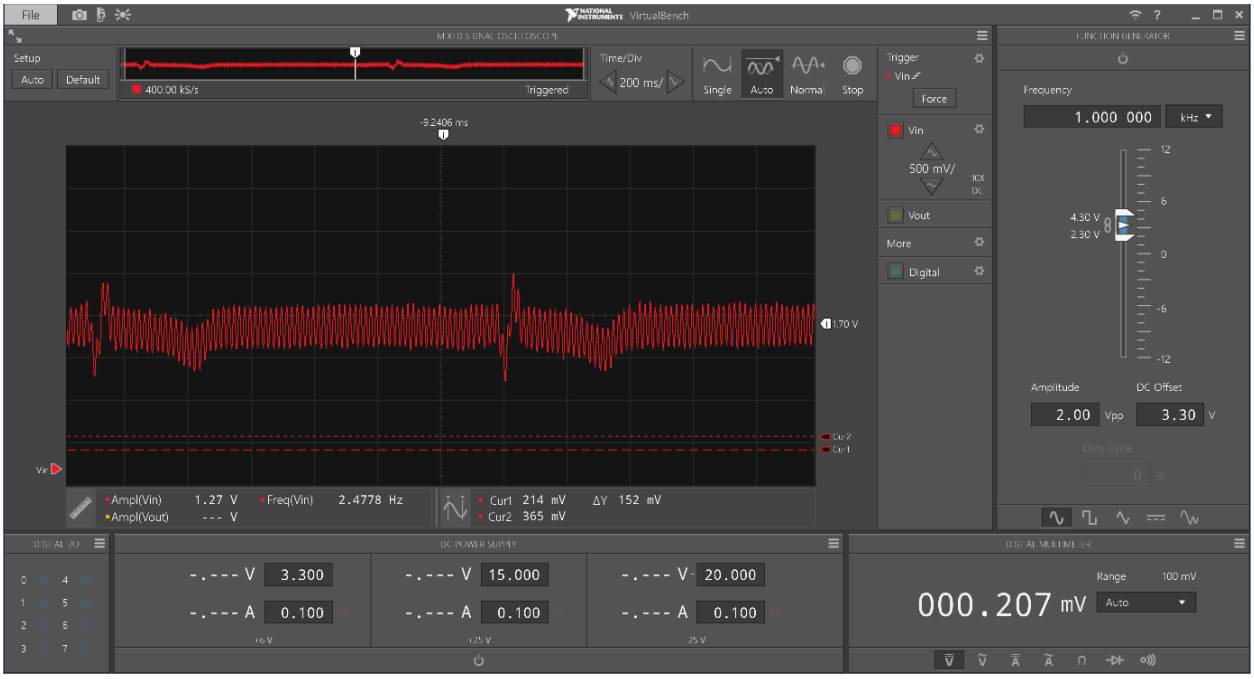


Figure 14: Pat Mahan's Heartbeat with 60 Hz Noise

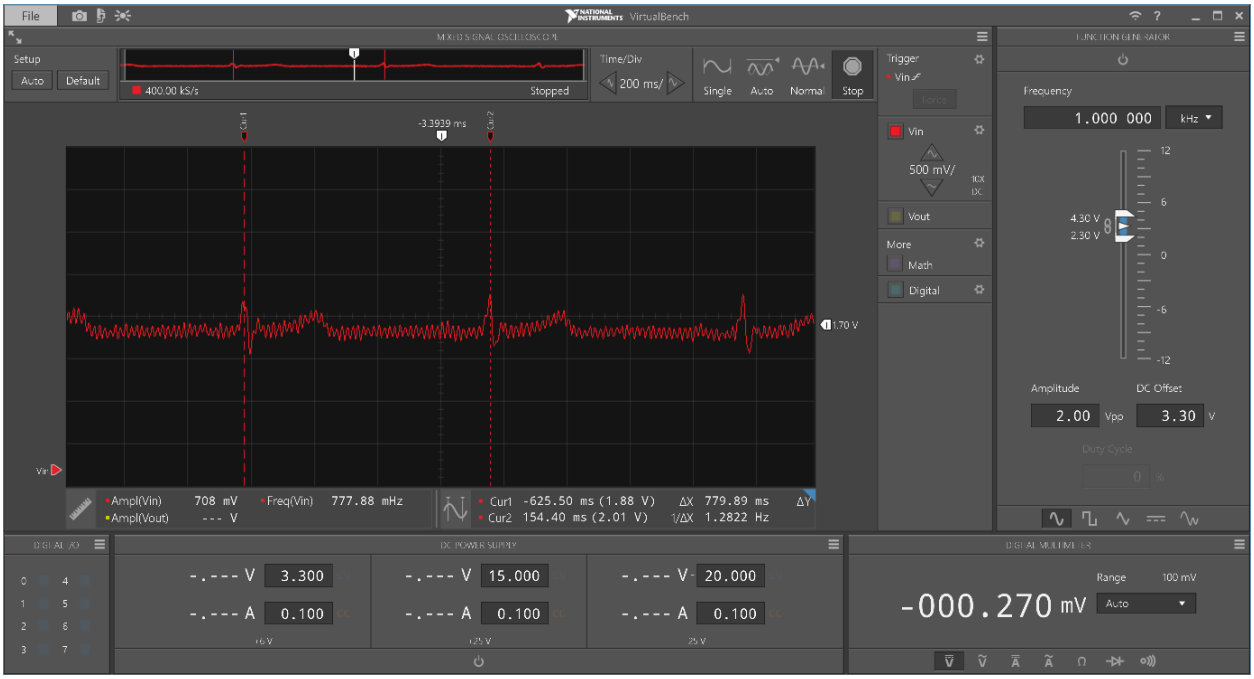


Figure 15: Pierce Faraone's Heartbeat

2.3. Conclusions

Completing the final ECG project involved applying subject matter knowledge and skills on a wide range of topics gained through the whole Fundamentals of Electrical Engineering (FUN) series. This provided us, the students, the opportunity to apply these areas to a practical problem, with particular emphasis on the basics of signals and system analysis.

There are; however, numerous improvements that could be carried out in order to make the project more fluid, straightforward, and to build a more accurate device that provided more valid readings. From our perspective, the printed circuit board used in the design for the ECG was accurate and precise, but not as exact as we had intended. This is due to the fact that there were certain aspects of the design process that could have allowed for greater development.

As mentioned before, there were not many significant differences in system behavior between testing on the breadboard and on the circuit board. This is a result of testing each subsystem individually before soldering the parts in their respective location. The same could not be said between our simulations and physical testing, as they were varied. External factors such as failure to account for the interference of electricity, among others, were reasonable explanations as to why the results in our simulations appeared the way they did. The time it took to realize such simple causes contributed to the loss of valuable in-class work. This is because the issues associated with the problem had nothing to do with both our design or components, but rather an independent source.

Human error was an additional factor that had an effect on the project. For instance, this was noticed in the assembly portion, where the female test pins were soldered onto the side of the board with the components. After desoldering and resoldering in the correct place, the components became slightly misaligned. Fortunately, this did not have substantial consequences. In general, the project served its purpose in producing a printed circuit board

that combined the elements that were taught in class, along with serving as an experience that consisted of a group effort.

2.4. MyRIO Appendix

Our myRio readings returned a value of 1/17, 17 times. In addition, our experimentation with the different filter varieties showed that an averaging filter worked best to eliminate 60 Hz noise. This was somewhat surprising, because we expected the 60 Hz comb filter to provide the best result.

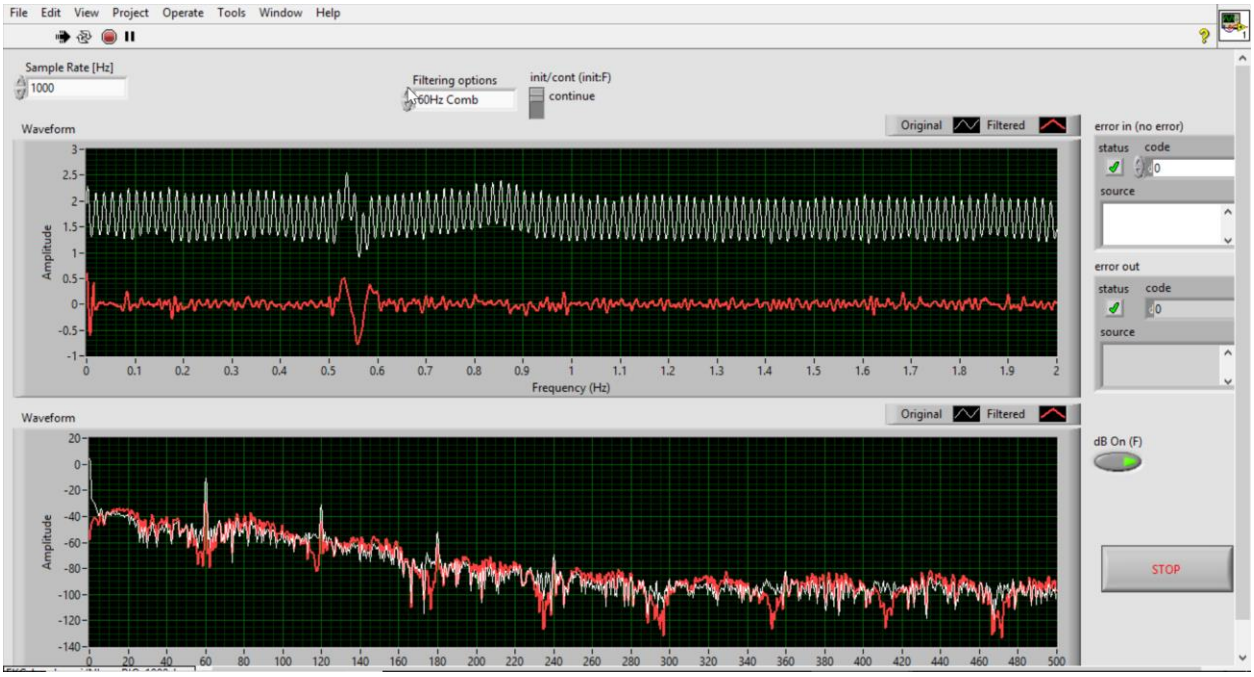


Figure 16: myRIO Digital 60 Hz Comb Filter

Our Mathscript code is shown below:

```
data = [1/17 1/17 1/17 1/17 1/17 1/17 1/17 1/17 1/17 1/17 1/17 1/
17 1/17 1/17 1/17 1/17 1/17];

freqz(data);
```

Figure 17: Mathscript Code

This returns:

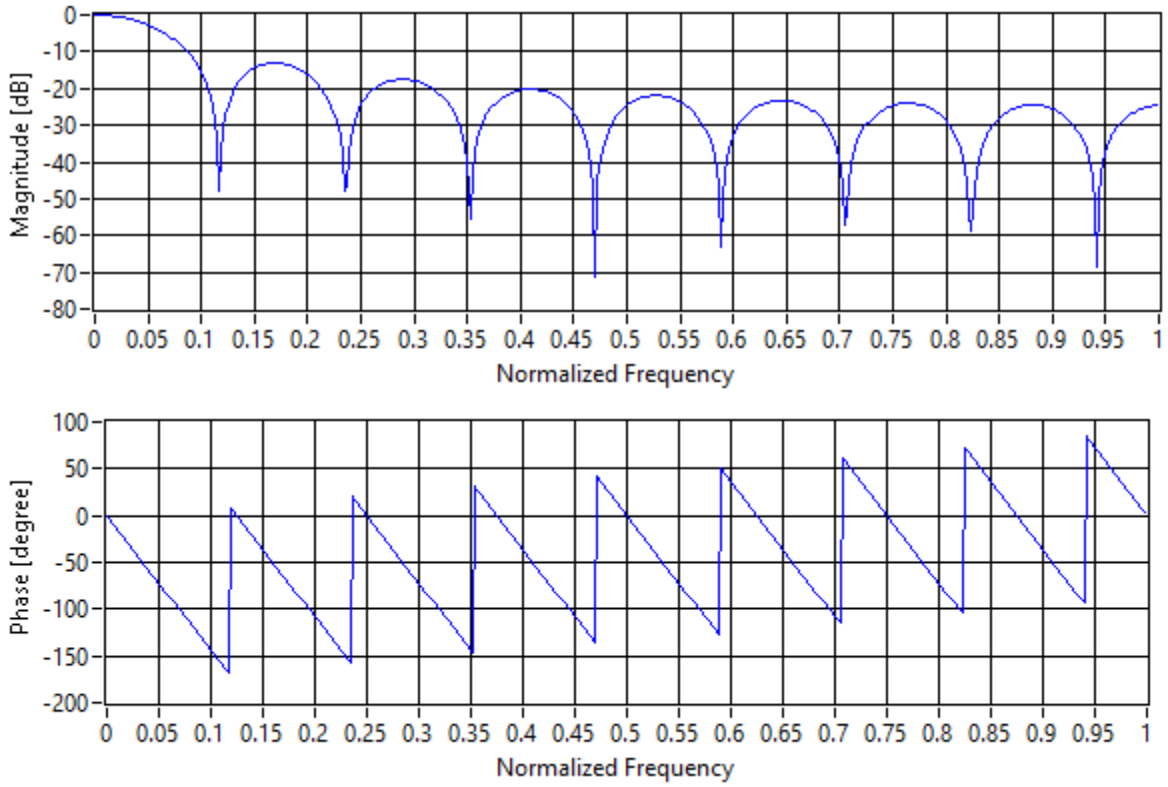


Figure 18: Mathscript Result