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Digital Circuits Design Project

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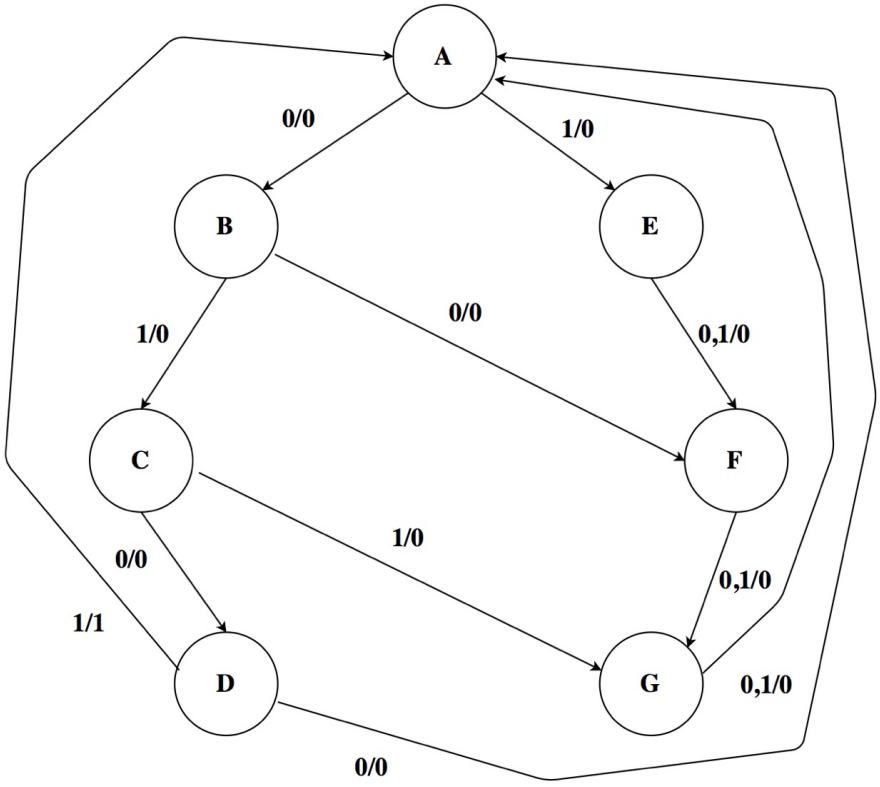
Purpose

To design a circuit that will examine exactly a four-bit sequence using the techniques we have learned this semester. It will examine a serial stream of bits to detect the sequence given to locate.

Pre Lab

STATE GRAPH



STATE TABLE

Present State	Next State X = 0	Next State X = 1	Output	
A	B	C	0	0
B	B	C	0	0
C	B	C	0	0
D	B	C	0	0
E	B	C	0	0
F	B	C	0	1
G	B	C	0	0

NEAR OPTIMUM APPROACH

I. ~~(B C)~~ ~~(F G)~~ ~~(D E)~~ ~~(F G)~~

II. ~~(B C)~~ ~~(E D)~~ ~~(E E)~~ ~~(F G)~~ ~~(G G)~~ ~~(A A)~~ ~~(A A)~~

III. (A B C D E F) (G)

Karnaugh Map

AB \ C	0	1
00	A	X
01	B	C
11	F	G
10	D	E

Once the optimized Karnaugh Map was created, we are able to create a new state table that consisted with the optimized present states and next states to achieve our goal of obtaining the sequence.

USING A D TYPE FLIP FLOP

A	B	C	X = 0 A^+	B^+	C^+	X = 1 A^+	B^+	C^+	X = 0 D_A	D_B	D_C	X = 1 D_A	D_B	D_C
0	0	0	0	1	0	0	1	1	0	1	0	0	1	1
0	0	1	X	X	X	X	X	X	X	X	X	X	X	X
0	1	0	1	0	1	1	0	0	1	0	1	1	0	0
0	1	1	1	0	1	1	0	1	1	0	1	1	0	1
1	0	0	1	1	0	1	1	1	1	1	0	1	1	1
1	0	1	1	1	1	1	1	1	1	1	1	1	1	1
1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0	0	0	0	0	0	0

XA \ BC	00	01	11	10
00	0	X	1	1
01	1	1	0	0
11	1	1	0	0
10	0	X	1	1

D_A = AB’ + A’B

XA \ BC	00	01	11	10
00	1	X	0	0
01	1	1	0	0
11	1	1	0	0
10	1	X	0	0

D_B = B’

XA \ BC	00	01	11	10
00	0	X	1	1
01	0	1	0	0
11	1	1	0	0
10	1	X	1	0

D_C = XB’ + B’C + A’BC + X’A’B

USING A JK FLIP FLOP

A B C	X = 0 $A^+ B^+ C^+$	X = 1 $A^+ B^+ C^+$	X = 0 $J_A K_A$ $J_B K_A$ $J_c K_c$	X = 1 $J_A K_A$ $J_B K_A$ $J_c K_c$
0 0 0	0 1 0	0 1 1	0 X 1 X 0 X	0 X 1 X 1 X
0 0 1	X X X	X X X	X X X X X X	X X X X X X
0 1 0	1 0 1	1 0 0	1 X X 1 1 X	1 X X 1 0 X
0 1 1	1 0 1	1 0 1	1 X X 1 X 0	1 X X 1 X 0
1 0 0	1 1 0	1 1 1	X 0 1 X 0 X	X 0 1 X 1 X
1 0 0	1 1 1	1 1 1	X 0 1 X X 0	X 0 1 X X 0
1 0 0	0 0 0	0 0 0	X 1 X 1 0 X	X 1 X 1 0 X
1 0 0	0 0 0	0 0 0	X 1 X 1 X 1	X 1 X 1 X 1

XA \ BC	00	01	11	10
00	0	X	1	1
01	X	X	X	X
11	X	X	X	X
10	0	X	1	1

J_A = B

XA \ BC	00	01	11	10
00	X	X	X	X
01	0	0	1	1
11	0	0	1	1
10	X	X	X	X

K_A = B

XA \ BC	00	01	11	10
00	1	X	X	X
01	1	1	X	X
11	1	1	X	X
10	1	X	X	X

J_B = 1

XA \ BC	00	01	11	10
00	X	X	1	1
01	X	X	1	1
11	X	X	1	1
10	X	X	1	1

K_B = 1

XA \ BC	00	01	11	10
00	0	X	X	1
01	0	X	X	0
11	1	X	X	0
10	1	X	X	0

J_C = X'A'B + XB'

XA \ BC	00	01	11	10
00	X	X	0	X
01	X	0	1	X
11	X	0	1	X
10	X	X	0	X

K_C = AB

TEST PLAN

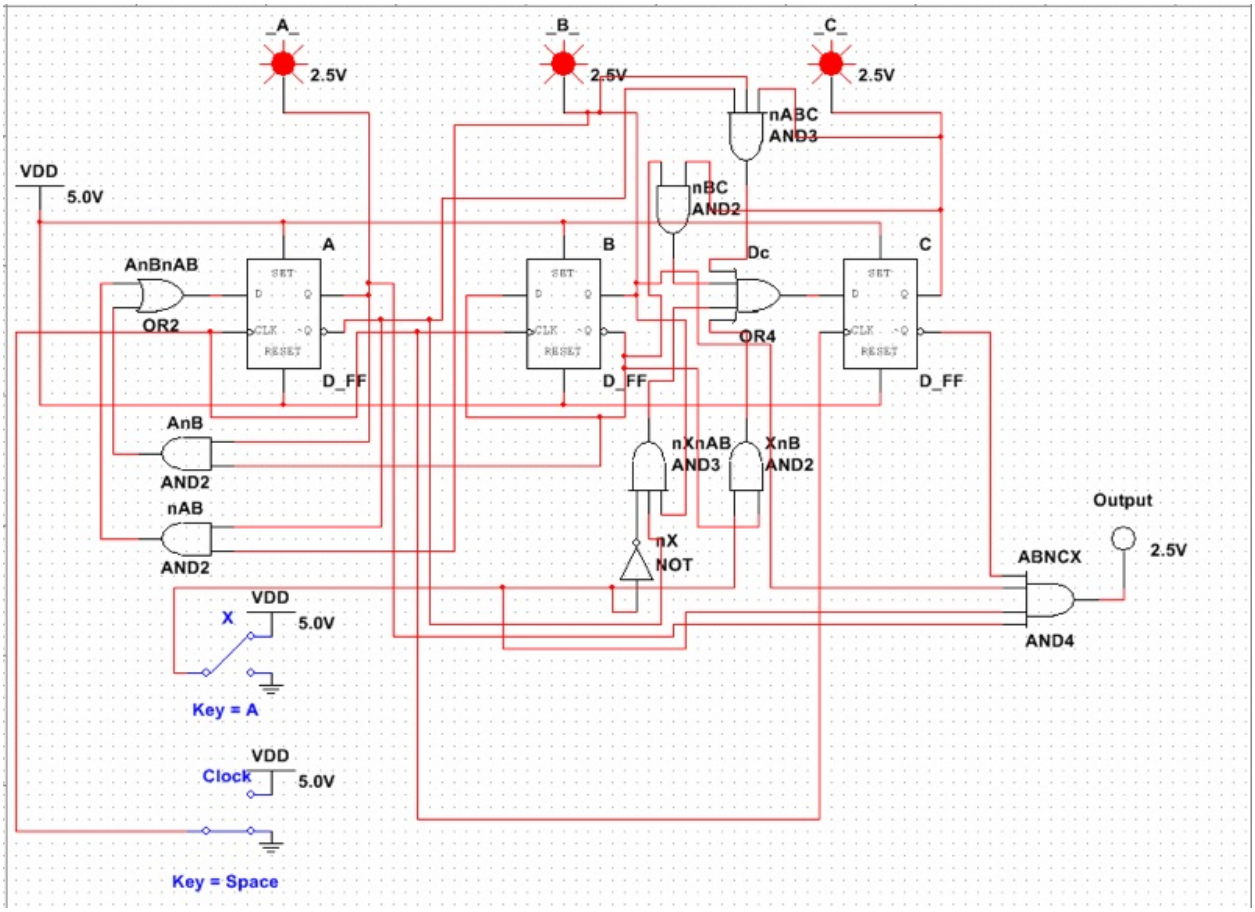
In order to test the JK Flip Flop, you need the necessary gates to wire in inputs for the JK flip flops. You will need the three JK flip flops, an inverter, two 2-input AND gates, a 2-input OR gate, and a 4-input AND gate. In order to control in inputs and the clock, you will need 2 switches. Connect the output for B to the input for both J_A and K_A. Connect power to both J_B and K_B. Connect the correct inputs to create the gates shown in the circuit to have the inputs for both J_C and K_C. In order to correctly identify if the input was detected, use the 4-input AND gate to AND XABC' and connect it to an LED. Once the sequence is correctly identified, the led will light. To test the sequence, use the switches to input the desired sequence of 1010 where 0 is the first bit to be received. Switch the clock respectively as each input is sent. Remember the circuit is designed to examine four bits at a time. No overlapping will occur.

Procedure

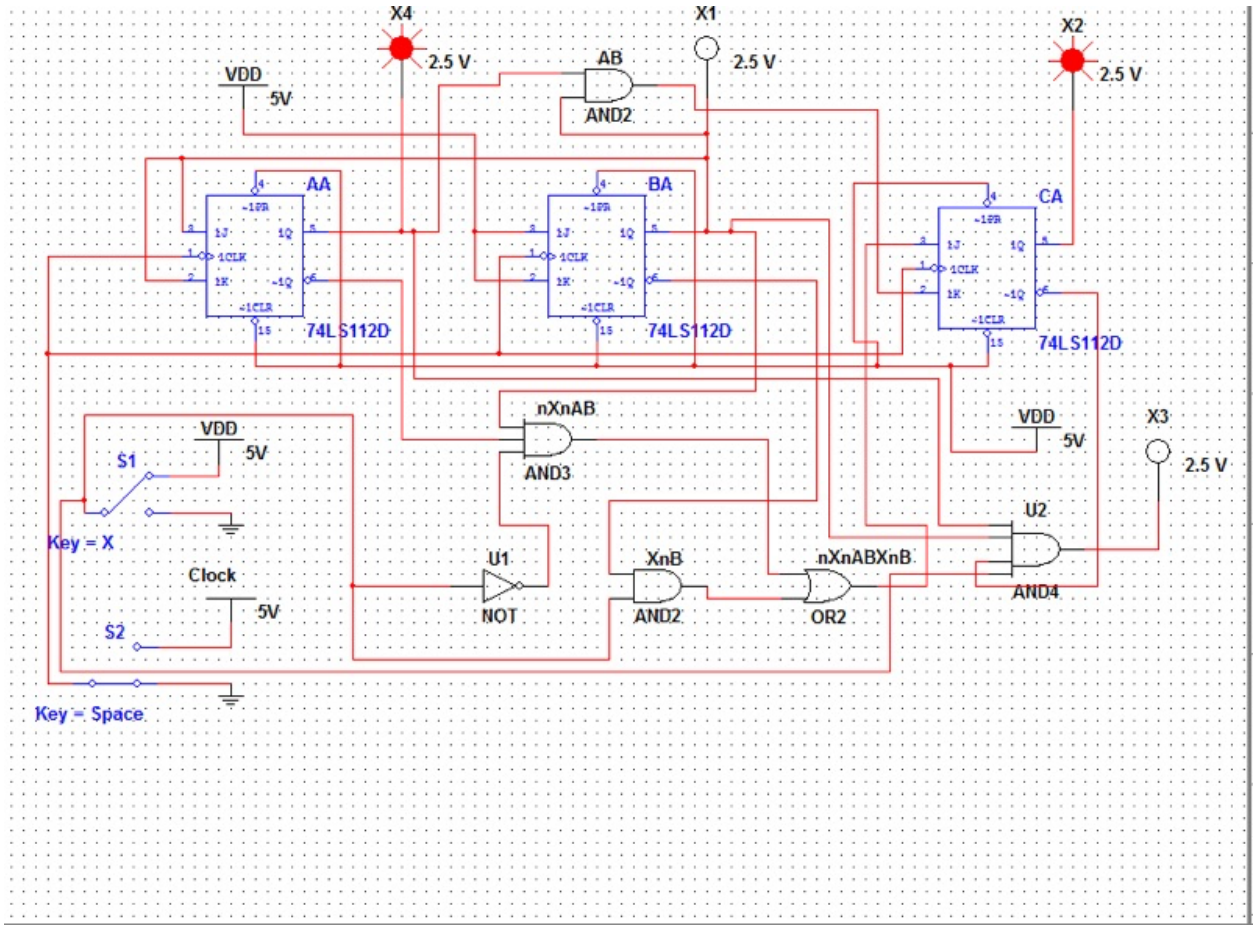
For the design state of the project, we listed all possible states and the two possible inputs that could occur. Since the circuit will examine exactly 4 bits, the state graph was set up so that it would finish with all correct inputs on one side and all incorrect on the other. Choosing the near optimum approach cut the amount of wiring down significantly. As shown above, it minimized the amount of work needed to both create the circuit and implement it with hardware. The two different type of flip flops were both implemented in design but the JK Flip Flop approach allowed the use of less and/or gates when creating the circuit. When doing research for cost online we examined that a D flip flop on average had a cost of $8.76 while a JK flip flop averaged a cost of $6.87. Because of these reasons we chose to go with the JK flip flop.

Data

CIRCUIT FOR USING D TYPE FLIP FLOP



CIRCUIT FOR USING A JK FLIP FLOP



RECORDED DATA

INPUT	STATUS OF LED
0000	OFF
0001	OFF
0010	OFF
0011	OFF
0100	OFF
0101	OFF
0110	OFF
0111	OFF
1000	OFF
1001	OFF
1010	ON
1011	OFF
1100	OFF
1101	OFF
1110	OFF
1111	OFF

Results

The circuits worked as expected. With the switches correctly utilized we input all possible combinations and observed the status of the LED. For the sequence of 1010, the LED turned on. While this was correct and as expected, we still inputted all other combinations as shown above in recorded data and tested to make sure the LED did not turn on for any other sequence.

Conclusion

By utilizing the material learned in lecture, we were able to create successfully a circuit that examined exactly a 4-bit sequence. We were able to successfully do this by using the near optimum method to reduce both time and cost to our circuit. We were able to create the circuit for both D and JK flip flop implementations. On both the multism and the physical implementation, we were able to test our results and verify that the circuit worked.