

# GPUShap: Massively Parallel Exact Calculation of SHAP Scores for Tree Ensembles

Rory Mitchell, Eibe Frank, and Geoffrey Holmes

**Abstract**—SHAP (SHapley Additive exPlanation) values [1] provide a game theoretic interpretation of the predictions of machine learning models based on Shapley values [2]. While exact calculation of SHAP values is computationally intractable in general, a recursive polynomial-time algorithm called TreeShap [3] is available for decision tree models. However, despite its polynomial time complexity, TreeShap can become a significant bottleneck in practical machine learning pipelines when applied to large decision tree ensembles. We present GPUShap, a modified TreeShap algorithm suitable for massively parallel computation on graphics processing units. Our approach first preprocesses each decision tree to isolate variable sized sub-problems from the original recursive algorithm, then solves a bin packing problem, and finally maps sub-problems to single-instruction, multiple-thread (SIMT) tasks for parallel execution with specialised hardware instructions. With a single NVIDIA Tesla V100-32 GPU, we achieve speedups of up to 19x for SHAP values, and speedups of up to 340x for SHAP interaction values, over a state-of-the-art multi-core CPU implementation executed on two 20-core Xeon E5-2698 v4 2.2 GHz CPUs. We also experiment with multi-GPU computing using eight V100 GPUs, demonstrating throughput of 1.2M rows per second—equivalent CPU-based performance is estimated to require 6850 CPU cores.

**Index Terms**—GPGPU, SHAP values, bin packing, decision tree ensembles

## 1 INTRODUCTION

EXPLAINABILITY and accountability are important for practical applications of machine learning, but the interpretation of complex models with state-of-the-art accuracy such as neural networks or decision tree ensembles obtained using gradient boosting is challenging. Recent literature [4], [5], [6] describes methods for “local interpretability” of these models, enabling the attribution of predictions for individual examples to component features. One such method calculates so-called SHAP (SHapley Additive exPlanation) values quantifying the contribution of each feature to a prediction. In contrast to other methods, SHAP values exhibit several unique properties that appear to agree with human intuition [3]. Although SHAP values generally take exponential time to compute exactly, the special structure of decision trees admits a polynomial-time algorithm. This algorithm, implemented alongside state-of-the-art gradient boosting libraries such as XGBoost [7] and LightGBM [8], enables complex decision tree ensembles with state-of-the-art performance to also output interpretable predictions.

However, despite improvements to algorithmic complexity and software implementation, computing SHAP values from tree ensembles remains a computational concern for practitioners, particularly as model size or size of test data increases: generating SHAP values can be more time-consuming than training the model itself. We address this problem by reformulating the recursive TreeShap algorithm, taking advantage of parallelism and increased computational throughput available on modern GPUs. We provide an open

source module named GPUShap implementing a high throughput variant of this algorithm using NVIDIA’s CUDA platform. GPUShap is integrated as a backend to the XGBoost library, providing significant improvements to runtime over its existing multicore CPU-based implementation.

## 2 BACKGROUND

In this section, we briefly review the definition of SHAP values for individual features and the TreeShap algorithm for computing these values from decision tree models. We also review an extension of SHAP values to second-order interaction effects between features.

### 2.1 SHAP Values

SHAP values are defined as the coefficients of the following additive surrogate explanation model  $g$ , a linear function of binary variables

$$g(z') = \phi_0 + \sum_{i=1}^M \phi_i z'_i \quad (1)$$

where  $M$  is the number of features,  $z' \in \{0, 1\}^M$ , and  $\phi_i \in \mathbb{R}$ .  $z'_i$  indicates the presence of a given feature and  $\phi_i$  its relative contribution to the model output. The surrogate model  $g(z')$  is a *local* explanation of a prediction  $f(x)$  generated by the model for a feature vector  $x$ , meaning that a unique explanatory model may be generated for any given  $x$ . SHAP values are defined by the following expression:

$$\phi_i = \sum_{S \subseteq M \setminus \{i\}} \frac{|S|!(|M| - |S| - 1)!}{|M|!} [f_{S \cup \{i\}}(x) - f_S(x)] \quad (2)$$

where  $M$  is the set of all features and  $f_S(x)$  describes the model output restricted to feature subset  $S$ . Equation 2

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considers all possible subsets, and so has runtime exponential in the number of features.

Given a trained decision tree model  $f$  and data instance  $x$ , it is not necessarily clear how to restrict model output  $f(x)$  to feature subset  $S$ —when feature  $j$  is not present in subset  $S$  along a given branch of the tree, and a split condition testing  $j$  is encountered, then how do we choose which path to follow to obtain a prediction for  $x$ ? [3] defines a conditional expectation for the decision tree model  $E[f(x)|x_S]$ , where the split condition on feature  $j$  is evaluated using a random variable with distribution estimated from the training set used to build the model. In effect, when a decision tree branch is encountered and the feature to be tested is not in the active subset  $S$ , we take the output of *both* the left and right branch. More specifically, we use the proportion of weighted instances that flow down the left or right branch during model training. This process is also how the C4.5 decision tree learner deals with missing values [9]. It is referred to as “cover weighting” in what follows.

Given this interpretation of missing features, [3] gives a polynomial time algorithm for efficiently solving Equation 2, named TreeShap. The algorithm exploits the specific structure of decision trees: the model is additive in the contribution of each leaf. Equation 2 can thus be independently evaluated for each unique path from root to leaf node. These unique paths are then processed using a quadratic-time dynamic programming algorithm. The intuition of the algorithm is to keep track of the proportion of all feature subsets that flow down each branch of the tree, weighted according to the length of each subset  $|S|$ , as well as the proportion that flow down the left and right branches when the feature is missing.

For ease of reference, Algorithm 1 shows this recursive polynomial-time algorithm, where  $m$  is a list representing the path of unique features split on so far. Each list element has four attributes:  $d$  is the feature index,  $z$  is the fraction of paths that flow through the current branch when the feature is not present,  $o$  is the corresponding fraction when the feature is present, and  $w$  is the proportion of feature subsets of a given cardinality that are present. The decision tree is represented by the set of lists  $\{v, a, b, t, r, d\}$ , where each list element corresponds to a given tree node, with  $v$  containing leaf values,  $a$  pointers to the left children,  $b$  pointers to the right children,  $t$  the split condition,  $r$  the weights of training instances, and  $d$  the feature indices.

At a high level, the algorithm proceeds by stepping through a path in the decision tree of depth  $D$  from root to leaf. According to Equation 2, we have a different weighting for the size of each feature subset, although we can accumulate feature subsets of the same size together. As the algorithm advances down the tree, it calls the method EXTEND, taking a new feature split and accumulating its effect on all possible feature subsets of length  $1, 2, \dots$  up to the current depth. The UNWIND method is used undo addition of a feature that has been added to the path via EXTEND. UNWIND and EXTEND are commutative and can be called in any order. UNWIND may be used to remove duplicate feature occurrences from the path and to compute the final SHAP values. When the recursion reaches a leaf, the SHAP values  $\phi_i$  for each feature present in the path are computed by calling UNWIND on feature  $i$  (line 7),

```

1: function TS( $x$ , tree)
2:    $\phi$  = array of  $\text{len}(x)$  zeroes
3:   function RECURSE( $j, m, p_z, p_o, p_i$ )
4:      $m = \text{EXTEND}(m, p_z, p_o, p_i)$ 
5:     if  $v_j == \text{leaf}$  then
6:       for  $i \leftarrow 2$  to  $\text{len}(m)$  do
7:          $w = \text{sum}(\text{UNWIND}(m, i).w)$ 
8:          $\phi_{m_i.d} = \phi_{m_i.d} + w(m_i.o - m_i.z)v_j$ 
9:     else
10:       $h, c = x_{d_j} \leq t_j?(a_j, b_j) : (b_j, a_j)$ 
11:       $i_z = i_o = 1$ 
12:       $k = \text{FINDFIRST}(m.d, d_j)$ 
13:      if  $k \neq \text{nothing}$  then
14:         $i_z, i_o = (m_k.z, m_k.o)$ 
15:         $m = \text{UNWIND}(m, k)$ 
16:        RECURSE( $h, m, i_z r_h / r_j, i_o, d_j$ )
17:        RECURSE( $c, m, i_z r_c / r_j, 0, d_j$ )
18:      function EXTEND( $m, p_z, p_o, p_i$ )
19:         $l = \text{len}(m)$ 
20:         $m = \text{copy}(m)$ 
21:         $m_{l+1}.(d, z, o, w) = (p_i, p_z, p_o, l = 0 ? 1 : 0)$ 
22:        for  $i \leftarrow l$  to  $1$  do
23:           $m_{i+1}.w = m_{i+1}.w + p_o \cdot m_i.w \cdot i / (l + 1)$ 
24:           $m_i.w = p_z \cdot m_i.w \cdot (l + 1 - i) / (l + 1)$ 
25:        return  $m$ 
26:      function UNWIND( $m, i$ )
27:         $l = \text{len}(m)$ 
28:         $n = m_l.w$ 
29:         $m = \text{copy}(m_{1..l-1})$ 
30:        for  $j \leftarrow l - 1$  to  $1$  do
31:          if  $m_i.o \neq 0$  then
32:             $t = m_j.w$ 
33:             $m_j.w = n \cdot l / (j \cdot m_i.o)$ 
34:             $n = t - m_j.w \cdot m_i.z \cdot (l - j) / l$ 
35:          else
36:             $m_j.w = (m_j.w \cdot l) / (m_i.z \cdot (l - j))$ 
37:        for  $j \leftarrow i$  to  $l - 1$  do
38:           $m_j.(d, z, o) = m_{j+1}.(d, z, o)$ 
39:        return  $m$ 
40:    RECURSE( $1, [], 1, 1, 0$ )
41:  return  $\phi$ 

```

**Algorithm 1:** TreeShap

temporarily removing it from the path; then, the overall effect of switching that feature on or off is adjusted by adding the appropriate term to  $\phi_i$ .

Given an ensemble of  $T$  decision trees, Algorithm 1 runs in time proportional to  $O(TLD^2)$ , using memory  $O(D^2 + M)$ , where  $L$  is the maximum number of leaves for each tree,  $D$  is the maximum tree depth, and  $M$  the number of features. In this paper, we adapt Algorithm 1 for massively parallel GPUs.

## 2.2 SHAP Interaction Values

In addition to the first-order feature relevance metric defined above, [3] also provides an extension of SHAP values to second-order relationships between features, termed SHAP Interaction Values. This method applies the game-theoretic

SHAP interaction index [10], defining a matrix of interactions as

$$\phi_{i,j} = \sum_{S \subseteq M \setminus \{i,j\}} \frac{|S|!(M - |S| - 2)!}{2(M - 1)!} \nabla_{ij}(S) \quad (3)$$

for  $i \neq j$ , where

$$\nabla_{ij}(S) = f_{S \cup \{i,j\}}(x) - f_{S \cup \{i\}}(x) - f_{S \cup \{j\}}(x) + f_S(x) \quad (4)$$

$$= f_{S \cup \{i,j\}}(x) - f_{S \cup \{j\}}(x) - [f_{S \cup \{i\}}(x) - f_S(x)] \quad (5)$$

with diagonals

$$\phi_{i,i} = \phi_i - \sum_{j \neq i} \phi_{i,j}. \quad (6)$$

Interaction values can be efficiently computed by connecting Eq. 5 to Eq. 2, for which we have the polynomial time TreeShap algorithm. To compute  $\phi_{i,j}$ , TreeShap should be evaluated twice for  $\phi_i$ , where feature  $j$  is alternately considered fixed to present and not present in the model. To evaluate TreeShap for a unique path conditioning on  $j$ , the path is extended as normal, but if feature  $j$  is encountered, it is *not included* in the path (the dynamic programming solution is not extended with this feature, instead skipping to the next feature). If  $j$  is considered not present, the resulting  $\phi_i$  is weighted according to the probability of taking the left or right branch (cover weighting) at a split on feature  $j$ . If  $j$  is considered present, we evaluate the decision tree split condition  $x_j < t_j$  and discard  $\phi_i$  from the path not taken.

To compute interaction values for all pairs of features, TreeShap can be evaluated  $M$  times, leading to time complexity of  $O(TLD^2M)$ . Interaction values are challenging to compute in practice, with runtimes and memory requirements significantly larger than decision tree induction itself. In Section 3.5, we show how to adapt this algorithm to the GPU and how to improve runtime to  $O(TLD^3)$  (tree depth  $D$  is normally much smaller than the number of features  $M$  present in the data).

### 2.3 GPU computing

GPUs are massively parallel processors optimised for throughput, in contrast to conventional CPUs which optimise for latency. GPUs in use today consist of many processing units with single-instruction, multiple-thread (SIMT) lanes that very efficiently execute a group of threads operating in lockstep. In modern NVIDIA GPUs such as the ones we use for the experiments in this paper, these processing units, called "streaming multiprocessors" (SMs), have 32 SIMT lanes and the corresponding group of 32 threads is called a "warp". Warps are generally executed on SMs without order guarantees, enabling latency in warp execution (e.g., from global memory loads) to be hidden by switching to other warps that are ready for execution [11].<sup>1</sup>

Large speed-ups in the domain of GPU computing commonly occur when the problem can be expressed as a balanced set of vector operations with minimal control flow. Notable examples are matrix multiplication [12], [13], [14], image processing [15], [16], deep neural networks [17], [18],

[19], and sorting [20], [21]. Prior work exists on decision tree induction [22], [23] and inference [24] on GPUs, but we know of no prior work on tree interpretability specifically tailored to GPUs. Related work also exists on solving dynamic programming type problems [25], [26], [27] but dynamic programming is a broad term and the referenced works discuss significantly different problem sizes and applications (e.g., Smith-Waterman for sequence alignment).

In Section 3 we discuss a unique approach to exploiting GPU parallelism, different from the above-mentioned works due to the unique characteristics of the TreeShap algorithm. In particular, our approach will efficiently deal with large amounts of branching and load imbalance that would normally inhibit performance on GPUs, leading to substantial improvements over a state-of-the-art multicore CPU implementation.

### 3 GPURTREESHAP

Algorithm 1 has properties that make it unsuitable for direct implementation on GPUs in a performant way. Conventional multithreaded CPU implementations of Algorithm 1 achieve parallel work distribution by instances [7], [8]. For example, interpretability results for input matrix  $X$  are computed by launching one parallel CPU thread per row (i.e., data instance being evaluated). While this approach is embarrassingly parallel, CPU threads do not correspond directly to the notion of GPU threads. If threads in a warp take divergent branches, performance is reduced, as all threads must execute identical instructions when they are active [28]. Moreover, GPUs can suffer from per-thread load balancing problems—if work is unevenly distributed between threads in a warp, finished threads stall until all threads in the warp are finished. Additionally, GPU threads are more resource constrained than their CPU counterparts, having a smaller number of available registers due to limited per-SM resources. Excessive register usage results in reduced SM occupancy by limiting the number of concurrent warps. It also results in register spills to global memory, causing memory loads at significantly higher latency.

To mitigate these issues, we segment the TreeShap algorithm to obtain fine-grained parallelism, observing that each unique path from root to leaf in Algorithm 1 can be constructed independently because the  $\phi_i$  obtained at each leaf are additive and depend only on features encountered on that unique path from root to leaf. Instead of allocating one thread per tree, we allocate a *group* of threads to cooperatively compute SHAP values for a given unique path through the tree. We launch one such group of threads for each (unique path, evaluation instance) pair, computing all SHAP values for this pair in a single GPU kernel. This method requires preprocessing to arrange the tree ensemble into a suitable form, avoid some less GPU-friendly operations of the original algorithm, and partition work efficiently across GPU threads. Our GPURTreeshap implementation can be summarised by the following high-level steps:

- 1) Preprocess the ensemble to extract all unique decision tree paths.
- 2) Combine duplicate features along each path.
- 3) Partition path subproblems to GPU warps by solving a bin packing problem.

1. AMD GPUs have similar basic processing units, called "compute units"; the corresponding term for a warp is "wavefront".

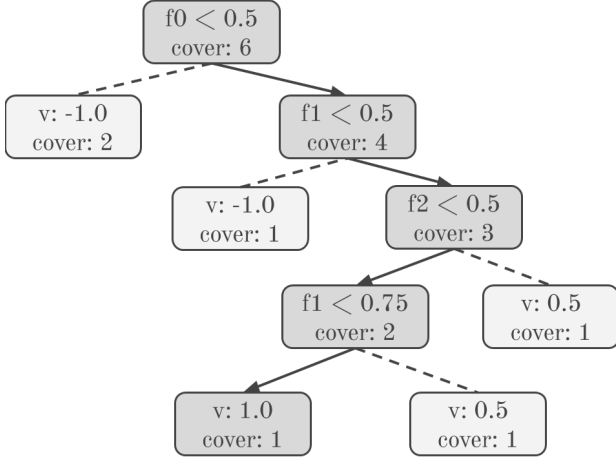


Fig. 1. Unique decision tree path

```

struct PathElement {
    // Unique path index
    size_t path_idx;
    // Feature of this split, -1 is root
    int64_t feature_idx;
    // Range of feature value
    float feature_lower_bound;
    float feature_upper_bound;
    // Probability of following this path
    // when feature_idx is missing
    float zero_fraction;
    // Leaf weight at the end of path
    float v;
};

```

Listing 1: Path element structure

- 4) Launch a GPU kernel solving the dynamic programming subproblems in batch.

These steps are described in more detail below.

### 3.1 Extract Paths

Figure 1 shows a decision tree model, highlighting a unique path from root to leaf. The SHAP values computed by Algorithm 1 are simply the sum of the SHAP values from every unique path in the tree. Note that the decision tree model holds information about the weight of training instances that flow down paths in the *cover* variable. To apply GPU computing, we first preprocess the decision tree ensemble into lists of path elements representing all possible unique paths in the ensemble. Path elements are represented as per Listing 1.

As paths share information that is represented in a redundant manner in the collection of lists representing a tree, reformulating trees increases memory consumption: assuming balanced trees, it increases space complexity from  $O(TL)$  to  $O(TDL)$  in the worst case. However, this additional memory consumption is not significant in practice.

Considering each path element, we use a lower and an upper bound to represent the range of feature values that can flow through a particular branch of the tree when the corresponding feature is present. For example, the root node in Figure 1 has split condition  $f_0 < 0.5$ . Therefore, if the feature is present, the left branch from this node contains instances where  $-\infty \leq f_0 < 0.5$ , and the right branch contains instances where  $0.5 \leq f_0 < \infty$ . This representation

is useful for the next preprocessing step where we combine duplicate feature occurrences along a decision tree path.

Figure 2 shows the unique paths extracted from Figure 1. An entire tree ensemble can be represented in this form. Crucially, this representation contains sufficient information to compute the ensemble’s SHAP values.

### 3.2 Remove Duplicate Features

Part of the complexity of Algorithm 1 comes from a need to detect and handle multiple occurrences of a feature in a single unique path. In Line 12, the candidate feature of the current recursion step is checked against existing features in the path. If a previous occurrence is detected, it is removed from the path using the UNWIND function. The  $p_z$  and  $p_o$  values for the old and new occurrences of the feature are multiplied, and the path extended with these new values.

Unwinding previous features to deal with multiple feature occurrences in this manner is problematic for GPU implementation because it requires threads to cooperatively evaluate FINDFIRST and then UNWIND, introducing branching as well as extra computation. Instead, we take advantage of our representation of a tree ensemble in path element form, combining duplicate features into a single occurrence. To do this, recognise that a path through a decision tree from root to leaf represents a single hypercube in the  $M$  dimensional feature space, with boundaries defined according to split conditions along the path. The boundaries of the hypercube may alternatively be represented with a lower and upper bound on each feature. Therefore, any number of decision tree splits over a single feature can be reduced to a single range, represented by these bounds. Moreover, note that the ordering of features within a path is irrelevant to the final SHAP values. As noted in [3], the EXTEND and UNWIND functions defined in Algorithm 1 are commutative; therefore, features may be added to or removed from a path in any order, and we can sort unique path representations by feature index, combining consecutive occurrences of the same feature into a single path element.

### 3.3 Bin Packing

Each unique path sub-problem identified above is mapped to GPU warps for hardware execution. A decision tree ensemble contains  $L$  unique paths, where  $L$  is the number of leaves, and each path has length between 1 and maximum tree depth  $D$ . To maximise throughput on the GPU, it is important to maximise utilisation of the processing units by saturating them with threads to execute. In particular, given a 32-thread warp, multiple paths may be resident and executed concurrently on a single warp. It is also important to assign all threads processing the same decision tree path to the same warp as we wish to use fast warp hardware intrinsics for communication between these threads and avoid synchronisation cost. Consequently, in our GPU algorithm, sub-problems are constrained to not overlap across warps. This implies that the maximum depth of a decision tree processed by our algorithm must be less than or equal to the GPU warp size of 32. Given that the number of nodes in a balanced decision tree increases exponentially with depth, and real-world experience showing  $D \leq 16$  in high-performance

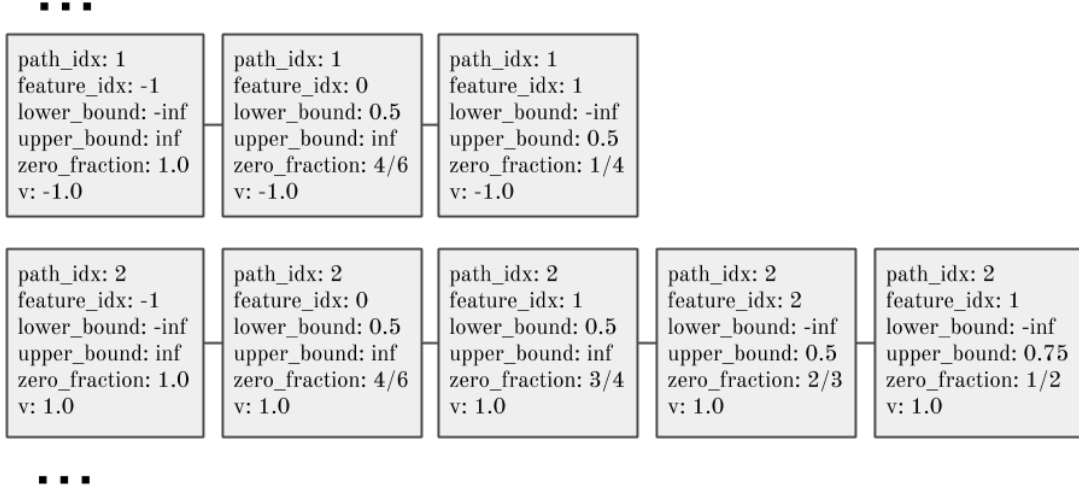


Fig. 2. Two unique paths from the decision tree in Figure 1

boosted decision tree ensembles almost always, we believe this to be a reasonable constraint.

To achieve the highest device utilisation, path sub-problems should be mapped to warps such that the total number of warps is minimised. Given the above constraint, this requires solving a bin packing problem. Given a finite set of items  $I$ , with sizes  $s(i) \in \mathbb{Z}^+$ , for each  $i \in I$ , and maximum bin capacity  $B$ ,  $I$  must be partitioned into the disjoint sets  $I_0, I_1, \dots, I_K$  such that the sum of sizes in each set is less than  $B$ . The partitioning minimising  $K$  is the optimal bin packing solution. In our case, the bin capacity,  $B = 32$ , is the number of threads per warp, and our item sizes,  $s(i)$ , are given by the unique path lengths from the tree ensemble. In general, finding the optimal packing is strongly NP-complete [29], although there are heuristics that can achieve close to optimal performance in many cases. In Section 4.1, we evaluate three standard heuristics for the off-line bin packing problem, *Next-Fit* (NF), *First-Fit-Decreasing* (FF), and *Best-Fit-Decreasing* (BFD), as well as a baseline where each item is placed in its own bin. We briefly describe these algorithms and refer the reader to [30] or [31] for a more in-depth survey.

*Next-Fit* is a simple algorithm, where only one bin is open at a time. Items are added to the bin as they arrive. If bin capacity is exceeded, the bin is closed and a new bin is opened. In contrast, *First-Fit-Decreasing* sorts the list of items by non-increasing size. Then, beginning with the largest item, it searches for the first bin with sufficient capacity and adds it to the bin. Similarly, *Best-Fit-Decreasing* also sorts items by non-increasing size, but assigns items to the feasible bin with the smallest residual capacity. FFD and BFD may be implemented in  $O(n \log n)$  time using a tree data structure allowing bin updates and insertions in  $O(\log n)$  operations (see [32] for specifics).

Existing literature gives worst-case approximation ratios for the above heuristics. For a given set of items  $I$ , let  $A(I)$  denote the number of bins used by algorithm  $A$ , and  $OPT(I)$  be the number of bins for the optimal solution. The approximation ratio  $R_A \leq \frac{A(I)}{OPT(I)}$  describes the worst-case

TABLE 1  
Bin packing time complexities and worst-case approximation ratios

ALGORITHM	TIME	$R_A$
NF	$O(n)$	2.0
FFD	$O(n \log n)$	1.222
BFD	$O(n \log n)$	1.222

performance ratio for any possible  $I$ . Time complexities and approximation ratios for each of the three above bin packing heuristic are listed in Table 1, as per [31].

As this paper concerns the implementation of GPU algorithms, we would ideally formulate the above heuristics in parallel. Unfortunately, the bin packing problem is known to be hard to parallelise. In particular, FFD and BFD are P-complete, indicating that it is unlikely that these algorithms may be sped up significantly via parallelism [33]. An efficient parallel algorithm with the same approximation ratio as FFD/BFD is given in [34], but the adaptation of this algorithm to GPU architectures is nontrivial and beyond the scope of this paper. Fortunately, as shown by our evaluation in Section 3.3, CPU-based implementations of the bin packing heuristics give acceptable performance for our task, and the main burden of computation still falls on the GPU kernels computing SHAP values in the subsequent step. We perform experiments comparing the three bin packing heuristics in terms of runtime and impact on efficiency for GPU kernels in Section 4.1.

### 3.4 GPU Kernel

Given a unique decision tree path extracted from a decision tree in an ensemble predictor, with duplicates removed, we allocate one path element per GPU thread and cooperatively evaluate SHAP values for each row in a test dataset  $X$ . The dataset  $X$  is assumed to be queryable from the device.

To enable non-recursive GPU-based implementation Algorithm 1, it remains to describe how to compute permutation weights for each possible feature subset with the

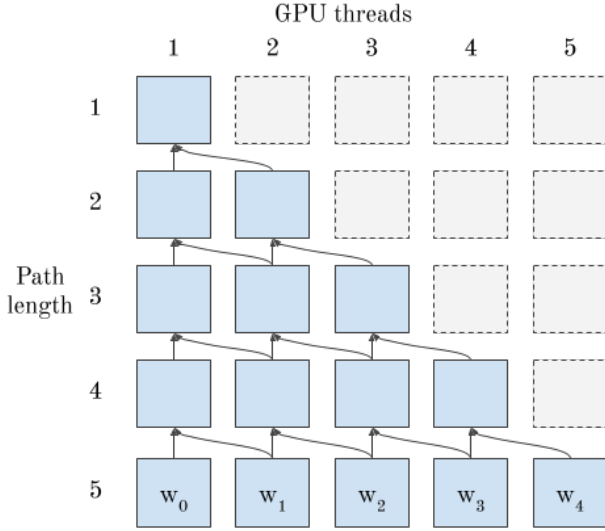


Fig. 3. Data dependencies of EXTEND

```

1: function PARALLEL_EXTEND( $m, p_z, p_o, p_i$ )
2:    $l = \text{len}(m)$ 
3:    $m_{l+1}.(d, z, o, w) = (p_i, p_z, p_o, l = 0 ? 1 : 0)$ 
4:   for  $i \leftarrow 2$  to  $l + 1$  in parallel, do
5:      $\text{left}_w = \text{shuffle}(m_i.w, i - 1)$ 
6:      $m_i.w = m_i.w \cdot p_z \cdot (l + 1 - i) / (l + 1)$ 
7:      $m_i.w = m_i.w + p_o \cdot \text{left}_w \cdot i / (l + 1)$ 
8:   return  $m$ 

```

**Algorithm 2: Parallel EXTEND**

EXTEND function (Line 4), as well as how to UNWIND each feature in the path and calculate the sum of permutation weights (Line 7). The EXTEND function represents a single step in a dynamic programming problem. In the GPU version of the algorithm, it processes a single path in a decision tree, represented as a list of path elements. As discussed above, all threads processing the same path are assigned to the same warp to enable efficient processing. Data dependencies between threads occur when each thread processes a single path element. Figure 3 shows the data dependency of each call to EXTEND on previous iterations when using GPU threads for the implementation. Each thread depends on its own previous result and the previous result of the thread to its "left".

This dependency pattern leads to a natural implementation using warp shuffle instructions, where threads directly access registers of other threads in the warp at considerably lower cost than shared or global memory. Algorithm 2 shows pseudocode for a single step of a parallel EXTEND function on the device. In pseudocode, we define a shuffle function analogous to the corresponding function in NVIDIA's CUDA language, where the first argument is the register to be communicated, and the second argument is the thread to fetch the register from—if this thread does not exist, the function returns 0, else it returns the register value at the specified thread index. In Algorithm 2, the shuffle function is used to fetch the element  $m_i.w$  from the current thread's left neighbour if this neighbour exists, and otherwise returns 0.

```

1: function PARALLEL_UNWOUNDSUM( $m, p_z, p_o, p_i$ )
2:    $l = \text{len}(m)$ 
3:    $\text{sum} = []$  array of  $l$  zeroes
4:   for  $i \leftarrow 1$  to  $l + 1$  in parallel, do
5:      $\text{next} = \text{shuffle}(m_i.w, l)$ 
6:     for  $j \leftarrow l$  to  $1$  do
7:        $w_j = \text{shuffle}(m_i.w, j)$ 
8:        $\text{tmp} = (\text{next} \cdot (l - 1) + 1) / j$ 
9:        $\text{sum}_i = \text{sum}_i + \text{tmp} \cdot p_o$ 
10:       $\text{next} = w_j - \text{tmp} \cdot (l - j) \cdot p_z / l$ 
11:       $\text{sum}_i = \text{sum}_i + (1 - p_o) \cdot w_j \cdot l / ((l - j) \cdot p_z)$ 
12:   return  $\text{sum}$ 

```

**Algorithm 3: Parallel UNWOUNDSUM**

Given the permutation weights for the entire path, it is also necessary to establish how to UNWIND the effect of each individual feature from the path to evaluate its relative contribution (Algorithm 1, Line 7). We distribute this task among threads, with each thread "unwinding" a unique feature. Pseudo-code for UNWOUNDSUM is given in Algorithm 3, where each thread  $i$  is effectively undoing the EXTEND function for a given feature and returning the sum along the path. Shuffle instructions are used to fetch weights  $w_j$  from other threads in the group. The result of UNWOUNDSUM is used to compute the final SHAP value as per Algorithm 1, Line 8.

### 3.5 Interaction values

Computation of SHAP interaction values makes use of the same preprocessing steps as above, and the same basic kernel building blocks, except that the thread group associated with each row/path pair evaluates SHAP values multiple times, iterating over each unique feature and conditioning on that feature being fixed to present or not present respectively. There are some difficulties in conditioning on features with our algorithm formulation so far—conditioning on a feature  $j$  requires ignoring it and not adding it to the active path. This introduces complexity when neighbouring threads are communicating via shuffle instructions (see Figure 3). Each thread must adjust its indexing to skip over a path element being conditioned on. We found a more elegant solution is to swap a path element used for conditioning to the end of the path, then simply stop before adding it to the path (taking advantage of the fact that the ordering of path elements is irrelevant). Thus, to evaluate SHAP interaction values, we use a GPU kernel similar to the one used for computing per-feature SHAP values, except that we loop over each unique feature, conditioning on that feature as on or off.

One major difference that arises between our GPU algorithm and the CPU algorithm of [3], is that we can easily avoid conditioning on features that are not present in a given path. It is clear from Equation 5 that  $f_{S \cup \{i, j\}}(x) = f_{S \cup \{i\}}(x)$ ,  $f_{S \cup \{j\}}(x) = f_S(x)$  and  $\nabla_{ij}(S) = 0$  if we condition on feature  $j$  that is not present in the path. Therefore, our approach has runtime proportional to  $O(TLD^3)$  instead of  $O(TLD^2M)$  by exploiting the limited subset of possible feature interactions in a tree branch. This modification has a significant impact on runtime in practice (because, normally,  $M \gg D$ ).



TABLE 2  
Datasets

NAME	ROWS	COLS	TASK	CLASSES	REF
COVTYPE	581012	54	CLASS	8	[35]
CAL_HOUSING	20640	8	REGR	-	[36]
FASHION_MNIST	70000	785	CLASS	10	[37]
ADULT	48842	14	CLASS	2	[38]

TABLE 3  
Models

MODEL	TREES	LEAVES	MAX_DEPTH
COVTYPE-SMALL	80	560	3
COVTYPE-MED	800	113888	8
COVTYPE-LARGE	8000	6636440	16
CAL_HOUSING-SMALL	10	80	3
CAL_HOUSING-MED	100	21643	8
CAL_HOUSING-LARGE	1000	3317209	16
FASHION_MNIST-SMALL	100	800	3
FASHION_MNIST-MED	1000	144154	8
FASHION_MNIST-LARGE	10000	2929521	16
ADULT-SMALL	10	80	3
ADULT-MED	100	13074	8
ADULT-LARGE	1000	642035	16

## 4 EVALUATION

We train a range of decision tree ensembles using XGBoost on the datasets listed in Table 2. Our goal is to evaluate a wide range of models representative of different real-world settings, from simple exploratory models to large ensembles of thousands of trees. For each dataset, we train a small, medium, and large variant by adjusting the number of boosting rounds (10, 100, 1000) and maximum tree depth (3, 8, 16). The learning rate is set to 0.01 to prevent XGBoost learning the model in the first few trees and producing only stumps in subsequent iterations. Using a low learning rate is also common in practice to minimise generalisation error. Other hyperparameters are left as default. Summary statistics for each model variant are listed in Table 3, and our testing hardware is listed in Table 4.

### 4.1 Bin packing

We first evaluate the performance of the NF, FFD and BFD bin packing algorithms from Section 3.3. We also include “none” as a baseline, where no packing occurs and each unique path is allocated to a single warp. All bin packing heuristics are single-threaded and run on the CPU. We report the execution time (in seconds), utilisation, and number of bins used ( $K$ ). Utilisation is defined as  $\frac{\sum_{i \in I} s(i)}{32K}$ , the total weight of all items divided by the bin space allocated, or for our purposes, the fraction of GPU threads that are active for a given bin packing. Poor bin packings waste space on each warp and underutilise the GPU.

Results are summarised in Table 5. “None” is clearly a poor choice, with utilisation between 0.1 and 0.3, with worse utilisation for smaller tree depths—for example, small models with maximum depth three allocate items of size three to warps of size 32. The simple NF algorithm often provides competitive results with fast runtimes, but it can lag behind FFD and BFD when item sizes are larger, exhibiting utilisation as low as 0.79 for *fashion\_mnist-large*. FFD and BFD

TABLE 4  
Hardware - Nvidia DGX-1

PROCESSOR	DETAILS
CPU	2X 20-CORE XEON E5-2698 v4 2.2 GHZ
GPU	8X TESLA V100-32

achieve better utilisation than NF in all cases, reflecting their superior approximation guarantees. Interestingly, FFD and BFD achieve the same efficiency on every example tested. We have verified they can produce different packings on contrived examples, but there is no discernible difference for our application. FFD and BFD have longer runtimes than NF due to their  $O(n \log n)$  time complexity. FFD is slightly faster than BFD because it uses a binary tree packed into an array, yielding greater cache efficiency, but its implementation is more complicated. In contrast, BFD is implemented easily using `std::set`.

Based on these results, we recommend BFD for its strong approximation guarantee, simple implementation, and acceptable runtime when packing jobs into batches for GPU execution. Its runtime is at most 1.6s in our experiments, for our largest model (*covtype-large*) with 6.7M items, and is constant with respect to the number of test rows because the bin packing occurs once per ensemble and is reused for each additional data point, allowing us to amortise its cost over improvements in end-to-end runtime from improved kernel efficiency. The gains in GPU thread utilisation from using BFD over NF directly translate into performance improvements, as fewer bins used means fewer GPU warps are launched. On our large size models, we see improvements in utilisation of 10.1%, 3.2%, 16.7% and 9.6% from BFD over NF. We use BFD in all subsequent experiments.

### 4.2 SHAP Values

We evaluate the performance of GPUtreeShap as a backend to the XGBoost library [7], comparing its execution time against the existing CPU implementation of Algorithm 1<sup>2</sup>. The baseline CPU algorithm is efficiently multithreaded using OpenMP, with a parallel for loop over all test instances. See <https://github.com/dmlc/xgboost> for exact implementation details for the baseline and <https://github.com/rapidsai/gputreeshap> for GPUtreeShap implementation details.

Table 6 reports the runtime of GPUtreeShap on a single V100 GPU compared to TreeShap on 40 CPU cores. Results are averaged over five runs and standard deviations are also shown. We observe speedups between 13-18x for medium and large models evaluated on 10,000 test rows. We observe little to no speedup for the small models as insufficient computation is performed to offset the latency of launching GPU kernels.

Figure 4 plots the time to evaluate varying numbers of test rows for the *cal\_housing-med* model. We plot the average of five runs; the shaded area indicates the 95% confidence interval. This illustrates the throughput vs. latency trade-off

2. We do not benchmark against TreeShap implementations in the Python SHAP package or LightGBM because they are written by the same author, also in C++, and are functionally equivalent to XGBoost’s implementation.

TABLE 5  
Bin packing performance

MODEL	ALG	TIME(S)	UTILISATION	BINS	MODEL	ALG	TIME(S)	UTILISATION	BINS
COVTYPE-SMALL	NONE	0.0018	0.105246	560	FASHION_MNIST-SMALL	NONE	0.0022	0.123906	800
COVTYPE-SMALL	NF	0.0041	0.982292	60	FASHION_MNIST-SMALL	NF	0.0082	0.991250	100
COVTYPE-SMALL	FFD	0.0064	0.998941	59	FASHION_MNIST-SMALL	FFD	0.0116	0.991250	100
COVTYPE-SMALL	BFD	0.0086	0.998941	59	FASHION_MNIST-SMALL	BFD	0.0139	0.991250	100
COVTYPE-MED	NONE	0.0450	0.211187	113533	FASHION_MNIST-MED	NONE	0.0439	0.264387	144211
COVTYPE-MED	NF	0.0007	0.913539	26246	FASHION_MNIST-MED	NF	0.0008	0.867580	43947
COVTYPE-MED	FFD	0.0104	0.940338	25498	FASHION_MNIST-MED	FFD	0.0130	0.880279	43313
COVTYPE-MED	BFD	0.0212	0.940338	25498	FASHION_MNIST-MED	BFD	0.0219	0.880279	43313
COVTYPE-LARGE	NONE	0.0346	0.299913	6702132	FASHION_MNIST-LARGE	NONE	0.0140	0.385001	2929303
COVTYPE-LARGE	NF	0.0413	0.851639	2360223	FASHION_MNIST-LARGE	NF	0.0132	0.791948	1424063
COVTYPE-LARGE	FFD	0.8105	0.952711	2109830	FASHION_MNIST-LARGE	FFD	0.3633	0.958855	1176178
COVTYPE-LARGE	BFD	1.6702	0.952711	2109830	FASHION_MNIST-LARGE	BFD	0.8518	0.958855	1176178
CAL_HOUSING-SMALL	NONE	0.0015	0.085938	80	ADULT-SMALL	NONE	0.0016	0.125000	80
CAL_HOUSING-SMALL	NF	0.0025	0.982143	7	ADULT-SMALL	NF	0.0023	1.000000	10
CAL_HOUSING-SMALL	FFD	0.0103	0.982143	7	ADULT-SMALL	FFD	0.0061	1.000000	10
CAL_HOUSING-SMALL	BFD	0.0001	0.982143	7	ADULT-SMALL	BFD	0.0060	1.000000	10
CAL_HOUSING-MED	NONE	0.0246	0.181457	21641	ADULT-MED	NONE	0.0050	0.229014	13067
CAL_HOUSING-MED	NF	0.0126	0.931429	4216	ADULT-MED	NF	0.0066	0.913192	3277
CAL_HOUSING-MED	FFD	0.0016	0.941704	4170	ADULT-MED	FFD	0.0575	0.950010	3150
CAL_HOUSING-MED	BFD	0.0031	0.941704	4170	ADULT-MED	BFD	0.1169	0.950010	3150
CAL_HOUSING-LARGE	NONE	0.0089	0.237979	3370373	ADULT-LARGE	NONE	0.0033	0.297131	642883
CAL_HOUSING-LARGE	NF	0.0225	0.901060	890148	ADULT-LARGE	NF	0.0035	0.858728	222446
CAL_HOUSING-LARGE	FFD	0.3534	0.933114	859570	ADULT-LARGE	FFD	0.0684	0.954377	200152
CAL_HOUSING-LARGE	BFD	0.8760	0.933114	859570	ADULT-LARGE	BFD	0.0954	0.954377	200152

TABLE 6  
V100 vs. 40 CPU cores - 10000 test rows

MODEL	CPU(S)	STD	GPU(S)	STD	SPEEDUP
COVTYPE-SMALL	0.04	0.02	0.02	0.01	2.27
COVTYPE-MED	8.25	0.07	0.45	0.03	18.23
COVTYPE-LARGE	930.22	0.56	50.88	0.21	18.28
CAL_HOUSING-SMALL	0.01	0.01	0.01	0.01	0.96
CAL_HOUSING-MED	1.27	0.02	0.09	0.02	14.59
CAL_HOUSING-LARGE	315.21	0.30	16.91	0.34	18.64
FASHION_MNIST-SMALL	0.35	0.14	0.17	0.04	2.09
FASHION_MNIST-MED	15.10	0.07	1.13	0.08	13.36
FASHION_MNIST-LARGE	621.14	0.14	47.53	0.17	13.07
ADULT-SMALL	0.01	0.00	0.01	0.01	1.08
ADULT-MED	1.14	0.00	0.08	0.01	14.59
ADULT-LARGE	88.12	0.20	4.67	0.00	18.87

for this particular model size. The CPU is more effective for < 180 test rows due to lower latency, but the throughput of the GPU is significantly higher at larger batch sizes.

SHAP value computation is embarrassingly parallel over dataset rows, so we expect to see linear scaling of performance with respect to the number of GPUs or CPUs, given sufficient data. We set the number of rows to 1 million and evaluate the effect of additional processors for the *cal\_housing-med* model, measuring throughput in rows per second. Figure 5 reports throughput up to the eight GPUs available on the DGX-1 system, showing the expected close to linear scaling and reaching a maximum throughput of 1.2M rows per second. Reported throughputs are from the average of five runs—error bars are too small to see due to relatively low variance. Figure 6 shows linear scaling with respect to CPU cores up to a maximum throughput of 7000 rows per second. The shaded area indicates the 95% confidence interval from 5 runs. We speculate that the dip at 40 cores is due to contention with the operating system requiring threads for other system functions, and so ignore

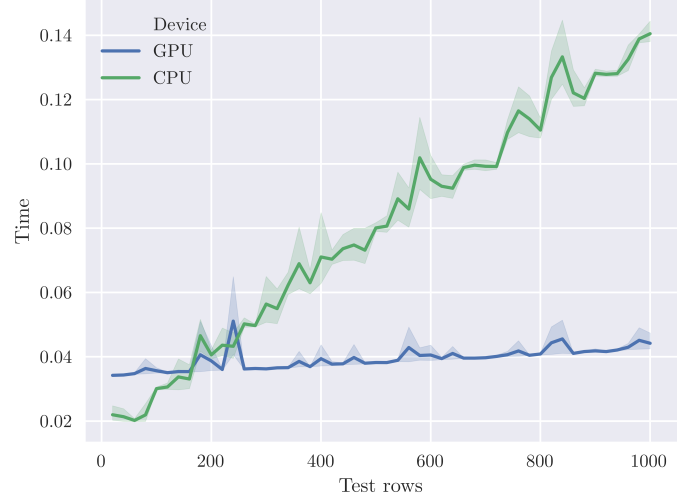


Fig. 4. V100 vs. 40 CPU cores - *cal\_housing-med*

it for this scaling analysis. We can reasonably approximate from Figure 6, using a throughput of 7000 rows/s per 40 cores, that it would require 6850 Xeon E5-2698 v4 CPU cores, or 343 sockets, to achieve the same throughput as eight V100 GPUs for this particular model.

### 4.3 SHAP Interaction Values

Table 7 compares single GPU vs. 40 core CPU runtime for SHAP interaction values. For this experiment, we lower the number of test rows to 200 due to the significantly increased computation time over per-feature SHAP values. Computing interaction values is challenging for datasets with larger numbers of features, in particular for *fashion\_mnist* (785 features). Our GPU implementation achieves moderate speedups on *cal\_housing* and *adult* due to the relatively low



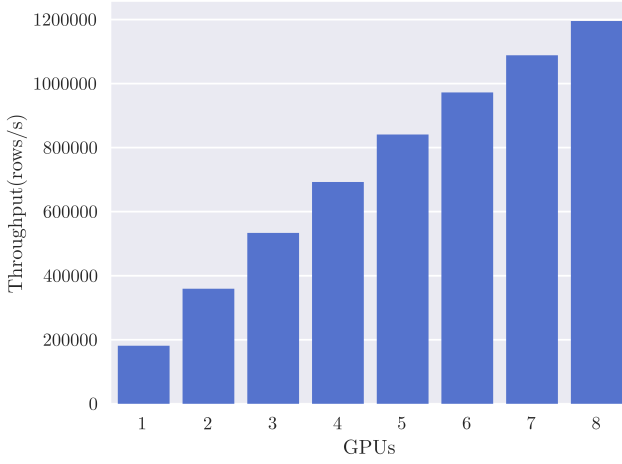


Fig. 5. Up to eight V100 GPUs - *cal\_housing-med*

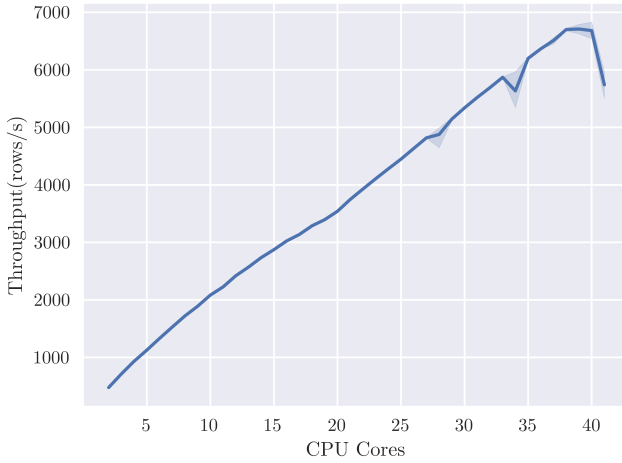


Fig. 6. Up to 40 CPU cores - *cal\_housing-med*

number of features; these speedups are roughly comparable to those obtained for standard SHAP values (Table 6). In contrast, for *covtype-large* and *fashion\_mnist-large*, we see speedups of 114x and 340x, in the most extreme case reducing runtime from six hours to one minute. This speedup comes from both the increased throughput of the GPU over the CPU and the improvements to algorithmic complexity due to omission of irrelevant features described in Section 3.5. Note that it may be possible to reformulate the CPU algorithm to take advantage of the improved complexity with similar preprocessing steps, but investigating this is beyond the scope of this paper.

## 5 CONCLUSION

SHAP values have proven to be a useful tool for interpreting the predictions of decision tree ensembles. We have presented GPUtreeShap, an algorithm obtained by modifying the TreeShap algorithm to enable efficient computation on GPUs. Our modifications exploit warp-level parallelism by cooperatively evaluating dynamic programming problems for each path in a decision tree ensemble, thus providing

TABLE 7  
Feature interactions - 200 test rows

MODEL	CPU(s)	STD	GPU(s)	STD	SPEEDUP
COVTYPE-SMALL	0.14	0.01	0.02	0.01	8.32
COVTYPE-MED	21.50	0.32	0.19	0.02	114.41
COVTYPE-LARGE	2055.78	4.19	28.85	0.06	71.26
CAL_HOUSING-SMALL	0.01	0.00	0.01	0.00	1.44
CAL_HOUSING-MED	0.53	0.04	0.04	0.01	12.05
CAL_HOUSING-LARGE	93.67	0.28	8.55	0.04	10.96
FASHION_MNIST-SMALL	11.35	0.87	4.04	0.67	2.81
FASHION_MNIST-MED	578.90	1.23	4.91	0.71	117.97
FASHION_MNIST-LARGE	21603.53	622.60	63.53	0.78	340.07
ADULT-SMALL	0.06	0.09	0.01	0.00	11.25
ADULT-MED	1.74	0.30	0.04	0.01	39.38
ADULT-LARGE	67.29	6.22	2.76	0.00	24.38

massive parallelism for large ensemble predictors. We have shown how standard bin packing heuristics can be used to effectively schedule problems at the warp level, maximising GPU utilisation. Additionally, our rearrangement leads to improvement in the algorithmic complexity when computing SHAP interaction values, from  $O(TLD^2M)$  to  $O(TLD^3)$ . Our library GPUtreeShap provides significant improvement to SHAP value computation over currently available software, allowing scaling onto one or more GPUs and reducing runtime by one to two orders of magnitude.

## REFERENCES

- [1] S. M. Lundberg and S.-I. Lee, “A unified approach to interpreting model predictions,” in *NIPS*. Curran Associates, 2017, pp. 4765–4774.
- [2] L. S. Shapley, “A value for  $n$ -person games,” *Contributions to the Theory of Games*, vol. 2, no. 28, pp. 307–317, 1953.
- [3] S. M. Lundberg, G. Erion, H. Chen, A. DeGrave, J. M. Prutkin, B. Nair, R. Katz, J. Himmelfarb, N. Bansal, and S.-I. Lee, “From local explanations to global understanding with explainable ai for trees,” *Nature Machine Intelligence*, vol. 2, no. 1, pp. 2522–2539, 2020.
- [4] M. T. Ribeiro, S. Singh, and C. Guestrin, “‘Why Should I Trust You?’: Explaining the predictions of any classifier,” in *KDD*. ACM, 2016, pp. 1135–1144.
- [5] R. R. Selvaraju, M. Cogswell, A. Das, R. Vedantam, D. Parikh, and D. Batra, “Grad-CAM: Visual explanations from deep networks via gradient-based localization,” in *ICCV*. IEEE, 2017, pp. 618–626.
- [6] R. Guidotti, A. Monreale, S. Ruggieri, F. Turini, F. Giannotti, and D. Pedreschi, “A survey of methods for explaining black box models,” *ACM Comput. Surv.*, vol. 51, no. 5, 2018.
- [7] T. Chen and C. Guestrin, “XGBoost: A scalable tree boosting system,” in *KDD*. ACM, 2016, pp. 785–794.
- [8] G. Ke, Q. Meng, T. Finley, T. Wang, W. Chen, W. Ma, Q. Ye, and T.-Y. Liu, “LightGBM: A highly efficient gradient boosting decision tree,” in *NIPS*. Curran Associates, 2017, pp. 3149–3157.
- [9] J. R. Quinlan, *C4.5: Programs for Machine Learning*. San Francisco, CA, USA: Morgan Kaufmann Publishers Inc., 1993.
- [10] K. Fujimoto, I. Kojadinovic, and J.-L. Marichal, “Axiomatic characterizations of probabilistic and cardinal-probabilistic interaction indices,” *Games and Economic Behavior*, vol. 55, pp. 72–99, 2006.
- [11] NVIDIA Corporation, “CUDA C++ programming guide,” 2020, version 11.1.
- [12] K. Fatahalian, J. Sugerman, and P. Hanrahan, “Understanding the efficiency of gpu algorithms for matrix-matrix multiplication,” in *Proceedings of the ACM SIGGRAPH/EUROGRAPHICS Conference on Graphics Hardware*, ser. HWW ’04. New York, NY, USA: Association for Computing Machinery, 2004, p. 133–137. [Online]. Available: <https://doi.org/10.1145/1058129.1058148>
- [13] J. D. Hall, N. A. Carr, and J. C. Hart, “Cache and bandwidth aware matrix multiplication on the gpu,” 2003.
- [14] Changhao Jiang and M. Snir, “Automatic tuning matrix multiplication performance on graphics hardware,” in *14th International Conference on Parallel Architectures and Compilation Techniques (PACT’05)*, 2005, pp. 185–194.

- [15] Bo Fang, Guobin Shen, Shipeng Li, and Huifang Chen, "Techniques for efficient dct/idct implementation on generic gpu," in *2005 IEEE International Symposium on Circuits and Systems*, 2005, pp. 1126–1129 Vol. 2.
- [16] K. Moreland and E. Angel, "The fft on a gpu," in *Proceedings of the ACM SIGGRAPH/EUROGRAPHICS Conference on Graphics Hardware*, ser. HWWS '03. Goslar, DEU: Eurographics Association, 2003, p. 112–119.
- [17] M. Perry, H. B. Prosper, and A. Meyer-Baese, "GPU implementation of bayesian neural network construction for data-intensive applications," *Journal of Physics: Conference Series*, vol. 513, no. 2, p. 022027, jun 2014. [Online]. Available: <https://doi.org/10.1088/1742-6596/513/2/022027>
- [18] A. Coates, B. Huval, T. Wang, D. J. Wu, A. Y. Ng, and B. Catanzaro, "Deep learning with cots hpc systems," in *Proceedings of the 30th International Conference on International Conference on Machine Learning - Volume 28*, ser. ICML'13. JMLR.org, 2013, p. III-1337–III-1345.
- [19] S. Chetlur, C. Woolley, P. Vandermersch, J. Cohen, J. Tran, B. Catanzaro, and E. Shelhamer, "cudnn: Efficient primitives for deep learning," 2014.
- [20] O. Green, R. McColl, and D. A. Bader, "Gpu merge path: A gpu merging algorithm," in *Proceedings of the 26th ACM International Conference on Supercomputing*, ser. ICS '12. New York, NY, USA: Association for Computing Machinery, 2012, p. 331–340. [Online]. Available: <https://doi.org/10.1145/2304576.2304621>
- [21] N. Satish, C. Kim, J. Chhugani, A. D. Nguyen, V. W. Lee, D. Kim, and P. Dubey, "Fast sort on cpus and gpus: A case for bandwidth oblivious simd sort," in *Proceedings of the 2010 ACM SIGMOD International Conference on Management of Data*, ser. SIGMOD '10. New York, NY, USA: Association for Computing Machinery, 2010, p. 351–362. [Online]. Available: <https://doi.org/10.1145/1807167.1807207>
- [22] T. Sharp, "Implementing decision trees and forests on a gpu," in *Computer Vision – ECCV 2008*, D. Forsyth, P. Torr, and A. Zisserman, Eds. Berlin, Heidelberg: Springer Berlin Heidelberg, 2008, pp. 595–608.
- [23] R. Mitchell and E. Frank, "Accelerating the xgboost algorithm using gpu computing," *PeerJ Computer Science*, vol. 3, p. e127, 2017.
- [24] T. Sharp, "Evaluating decision trees on a gpu," Oct. 16 2012, uS Patent 8,290,882.
- [25] Y. Liu, W. Huang, J. Johnson, and S. Vaidya, "Gpu accelerated smith-waterman," in *Computational Science – ICCS 2006*, V. N. Alexandrov, G. D. van Albada, P. M. A. Sloot, and J. Dongarra, Eds. Berlin, Heidelberg: Springer Berlin Heidelberg, 2006, pp. 188–195.
- [26] P. Steffen, R. Giegerich, and M. Giraud, "Gpu parallelization of algebraic dynamic programming," in *Parallel Processing and Applied Mathematics*, R. Wyrzykowski, J. Dongarra, K. Karczewski, and J. Wasniewski, Eds. Berlin, Heidelberg: Springer Berlin Heidelberg, 2010, pp. 290–299.
- [27] V. Boyer, D. El Baz, and M. Elkihel, "Solving knapsack problems on gpu," *Computers & Operations Research*, vol. 39, no. 1, pp. 42–47, 2012, special Issue on Knapsack Problems and Applications. [Online]. Available: <https://www.sciencedirect.com/science/article/pii/S0305054811000876>
- [28] M. Harris and I. Buck, "GPU flow-control idioms," in *GPU Gems 2*, M. Pharr, Ed. Addison-Wesley, 2005, pp. 547–555.
- [29] M. R. Garey and D. S. Johnson, *Computers and Intractability: A Guide to the Theory of NP-Completeness*. W. H. Freeman & Co., 1979.
- [30] S. Martello and P. Toth, *Knapsack Problems: Algorithms and Computer Implementations*. John Wiley & Sons, 1990.
- [31] E. G. Coffman, M. R. Garey, and D. S. Johnson, "Approximation algorithms for bin packing: A survey," in *Approximation Algorithms for NP-Hard Problems*, D. S. Hochbaum, Ed. PWS Publishing, 1997, pp. 46–93.
- [32] D. S. Johnson, "Fast algorithms for bin packing," *J. Comput. Syst. Sci.*, vol. 8, no. 3, pp. 272–314, 1974.
- [33] R. Anderson and E. Mayr, "Parallelism and greedy algorithms," Computer Science Department, Stanford University, Tech. Rep. 1003, 1984.
- [34] R. J. Anderson, E. W. Mayr, and M. K. Warmuth, "Parallel approximation algorithms for bin packing," *Inf. Comput.*, vol. 82, no. 3, p. 262–277, 1989.
- [35] J. A. Blackard, "Comparison of neural networks and discriminant analysis in predicting forest cover types," Ph.D. dissertation, Colorado State University, 1998.
- [36] R. K. Pace and R. Barry, "Sparse spatial autoregressions," *Statistics & Probability Letters*, vol. 33, no. 3, pp. 291–297, 1997.
- [37] H. Xiao, K. Rasul, and R. Vollgraf, "Fashion-MNIST: a novel image dataset for benchmarking machine learning algorithms," *arXiv*, vol. abs/1708.07747, 2017.
- [38] R. Kohavi, "Scaling up the accuracy of naive-bayes classifiers: A decision-tree hybrid," in *KDD*. AAAI Press, 1996, pp. 202–207.