Notes on transport measurements using a lock-in

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This document is an account of the lessons the authors learned while examining possible circuit artifacts that might exist in data gathered in real experiments. It aims at providing new users of cryogenic electronic setups for transport measurements with some coarse guidelines and reminders regarding how to mitigate unwanted artifacts while measuring with a lock-in amplifier. We make no attempt at comprehensiveness, but rather focus on the most commonly occuring mistakes in our specific experiment setups in the Topo group within QuTech.

1 Using a lock-in to measure conductance

Mesoscopic transport devices are often measured with the "standard DC + lock-in technique" even when the device itself is modeled as a purely resistive circuit component. Since major parts of this document are devoted to the caveats of measuring resistance/conductance with a lock-in, we would like to briefly discuss why the lock-in is useful at all for such purposes. After all, purely DC circuits are perfectly capable of measuring conductance and do not suffer from any L, C in the circuit, intentional (filtering, amp design) or parasitic, which we will address at length below.

The most noticeable drawback of DC $I - V$ measurements is noise: it is often the *differential* conductance that is the quantity of most interest to us and taking numerical derivative is a procedure that is bound to be noisy. Lock-in also filters out noise outside of a narrow band ($f \pm \tau^{-1}$, with τ being the integration time and f measurement frequency) while DC is exposed to $1/f$ noise all the way down to zero frequency.

However, lock-in conductance measurements can easily introduce systematic errors on the order of 10% of the total signal if operated with the wrong settings as we will show below, while DC current measurements do not suffer easily from these complicated circuit artifacts. Thus, although the lock-in is a very useful tool especially when we care more about *features* than accurate conductance *values*, extra attention should be paid if the accurate values do concern you. Here are some simplest rules to keep in mind to make sure your experiment is not affected by the artifacts addressed in this document:

- **Perform the same measurement again in DC** and check whether the values you obtain agree with each other up to the error margin you are willing to accept.
- Then, if the two do not agree, repeat the same measurement with various circuit settings that are expected to be irrelevant to your physics. Try another lock-in frequency (*e.g.* 2x and 0.5x the original) and check if your results are strongly frequency-dependent. Reduce the filtering strength and see if it does more than simply increasing the noise, etc.
- Beware of a large lock-in phase: you may not be able to recover correct values from your data when the angle is too large.

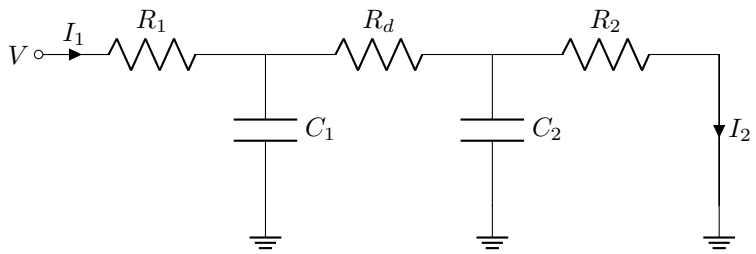

Figure 1: Example circuit consisting of two RC filters and one sample resistor in series, under a voltage bias V.

If the results do not agree, that means your lock-in measurement probably suffered from circuit artifacts. Next we analyze in more detail how to avoid these.

2 Fridge line filters at finite frequency

The first question a newcomer to lock-in measurements might ask is whether they should use the X or R component to compute their device resistance. We can take a look at what the X and R are in this very simple circuit in Fig 1, representing a sample R_d in the fridge and two RC low-pass filters in the fridge line (or on PCB), R_1, C_1, R_2, C_2, under voltage bias V. We assume for now there is a perfect current meter (meaning no input resistance, $Z_{\text{in}} = 0$) inserted at the position of either I_1 or I_2 which reads out the corresponding current. The latter configuration is most frequently used so we'll focus on it more next. The former is most typically seen in a 3-terminal nonlocal conductance measurement.

2.1 When things are right

In DC, this circuit is trivial. $I_1 = I_2 = I$ and the measured resistance is $V/I = R_1 + R_2 + R_d$ as expected. We simply need to deduct $R_1 + R_2$ from the total and obtain the device resistance.

At finite frequencies $\omega = 2\pi f$, we need to take all circuit parameters to be complex. Despite this change, the validity of the above procedure will continue to hold *so long as the two capacitors do not draw any current.* This requirement can be written as

$$R_i \ll (\omega C_k)^{-1},\ \forall i, k \tag{1}$$

The subscripts take a looser form than depicted in the circuit because in real fridge lines filters often come in several stages and this is just an illustration to showcase the basic principles.

Equivalently, this is requiring we *stay well below the cutoff frequencies* defined by any R_i, C_k combination:

$$f \ll f_{ik} \equiv \frac{1}{2\pi R_i C_k} \tag{2}$$

To get a quick estimation on what this means, we only need to be familiar with the fridge line bandwidth and resistance values. Here we assume $R_1 = R_2 = R_f$ is the total line resistance, $C_1 = C_2 = C_f$ and they define the fridge line bandwidth $f_0 \equiv 1/(2\pi R_f C_f)$.

- If $R_d < R_f$, we simply need to stay well below f_0, which is typically $> 1\,\text{kHz}$ and very easily satisfied.
- If $R_d \gg R_f$, we need to stay well below $f_0 \cdot \frac{R_f}{R_d}$. Note that this necessarily breaks down when $R_d \to \infty$, *e.g.* when measuring inside the Coulomb or superconducting gap.

In the next section we see what happens when the capacitors do draw currents.

2.2 When things go wrong

Now we calculate I_1, I_2 without any assumptions on C_1, C_2 and see what are the currents measured by the current meters in either situation. The total load impedance of this network Z_{tot} is ($||$ denotes the resistance shunt operation and $\tau_i \equiv R_i C_i$):

$$Z_{\text{tot}} = \left(R_2 || \frac{1}{j\omega C_2} + R_d\right) || \frac{1}{j\omega C_1} + R_1 \tag{3}$$

$$= \frac{(R_1 + R_d + R_2) - \omega^2 \tau_1 \tau_2 R_d + j\omega[\tau_1(R_d + R_2) + \tau_2(R_1 + R_d)]}{1 - \omega^2 \tau_2 R_d C_1 + j\omega[C_1(R_d + R_2) + \tau_2)]} \tag{4}$$

If we have a meter measuring I_1, the total measured response is $V/I_1 = Z_{\text{tot}}$. See Appendix for derivations and more discussions on this situation.

If we have a meter measuring I_2, the final expression of the measured response is simpler:

$$\frac{V}{I_2} = (R_1 + R_d + R_2) - \omega^2 \tau_1 \tau_2 R_d + j\omega[\tau_1(R_d + R_2) + \tau_2(R_d + R_1)] \tag{5}$$

- It looks as if we are measuring an *inductive* load even though there are only capacitors in this network. This is merely a result of comparing the voltage and current at two separate locations in the circuit.
- Neither X nor R on the lock-in is the right value to use if the angle is large, but the *real part of the inverse* of the lock-in reading (which is different from the *inverse of the real part*). The device resistance is obtained as

  $$\Re\left[\frac{V}{I_2}\right] - R_1 - R_2 = (1 - \omega^2 \tau_1 \tau_2) R_d \tag{6}$$

  Since $\omega^2 \tau_1 \tau_2$ is typically < 0.01, the result is close to R_d if all other elements of the circuit are ideal (the current meters having infinite bandwidth etc).
- Diverging R_d in this setup does not pose an intractable problem, since if we set $R_1 = R_2 \to 0$, I_2 is in fact not affected by the capacitors.
- Real fridge line filters come in stages, so the formulas here only serve to illustrate the complexity of the situation *if* we begin to notice a large phase in the signal. The right approach is to try to make sure this does not happen and beware to not treat the values as exact if we cannot avoid it.

To summarize, as soon as the capacitors begin to draw appreciable currents, *i.e.* the total load is not almost purely real, R_d becomes tangled up with other (likely not precisely-known) circuit elements in the final expression and in general cannot be recovered.

In the next sections, we assume this unwanted situation does not occur and ignore the fridge line capacitors.

3 Amplifiers at finite frequency

3.1 An example

Current-to-voltage converters, such as `I-measure` modules on IVVI and Ithaco ones in the MS setup, are one of the most common reasons lock-in measurements go wrong because of its complex circuitry and abundance of configuration possibilities. In this section we show an example to illustrate the severity of the problem.

The most commonly used `M1b` current amplifier on the IVVI rack is especially susceptible to lock-in finite-frequency problems because of its low bandwidth of roughly 200 Hz only. Slower amps draw less current in order to operate, so the design goal of this amp is to minimize its back-action on the sample. However, this also limits the operating frequency to about < 20 Hz. If this is not respected, one must only look at *features* of the measurement results and not exact *values*. Figure 2 is an example that illustrates this particular problem. We measured a 10 kΩ resistor in the fridge (K4) using the usual voltage-bias DC + lock-in circuit with different `M1b`/`M1h` current amps under various gain settings and lock-in frequencies. Note how the (wrongly) measured value can deviate from the truth by ∼10% even at a moderate frequency of 60 Hz and using the R component of the lock-in (using X would lead to another ∼10% of error on top of this).

There are other voltage amplifiers present in the IVVI circuit with configurable bandwidths such as the `Iso-in` and `Iso-out`. The same characterization principles in the next subsection apply to them as well: measure the input and output of these amps at the frequency you use and check if they are what you expect.

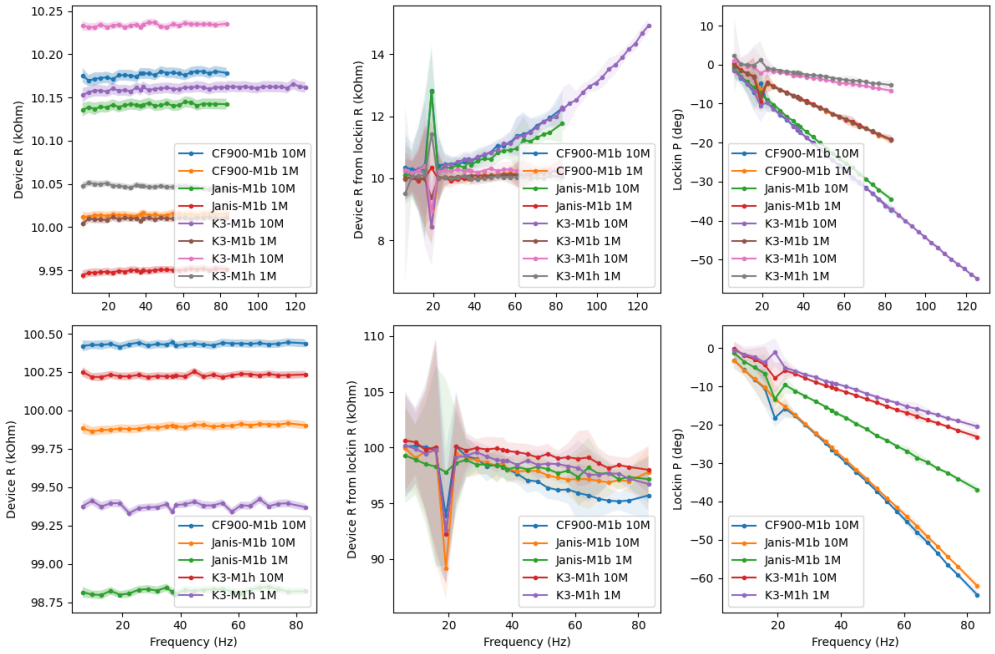

Figure 2: Measuring a 10 kΩ (top row) and 100 kΩ (bottom row) resistor using DC (left column) and lock-in (middle and right columns) with different current amplifiers and gain settings. Note the difference in y axis scales.

3.2 Characterizing a current amplifier

What we colloquially call current amps should, in fact, be called current-to-voltage converters (or current-controlled voltage sources). The two most important parameters of such a converter for our measurements are its input impedance Z_{in} and gain impedance Z_{g}. These two are internally related (see caption), but as users it is usually not necessary to consider their relation and enough to treat them as two independent values. Figure 3 illustrates a simplified internal circuit of such a converter and its equivalent circuit that is most useful for users.

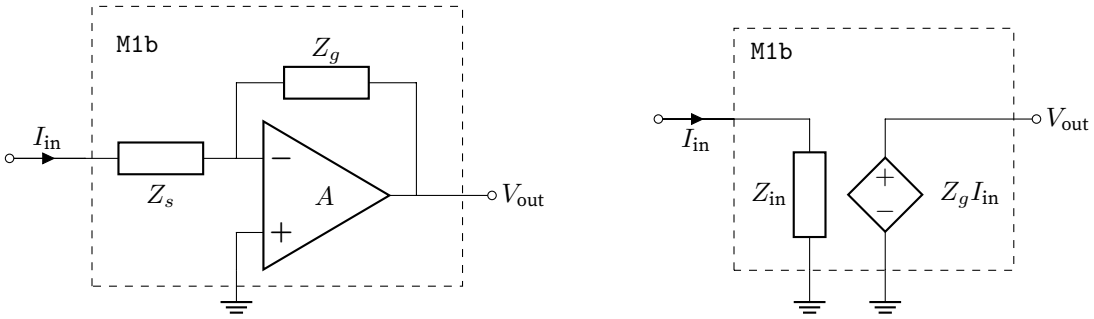

Figure 3: A simplified current-to-voltage converter (left) and its equivalent circuit (right). In the case of `M1b` in DC, $Z_s = 2\,\text{k}\Omega$, Z_{g} is configurable from $1\,\text{M}\Omega$ to $1\,\text{G}\Omega$, $Z_{\text{in}} = Z_s + \frac{Z_{\text{g}}}{1+A}$ and $A \approx 1000$. Parameters of other amplifiers can be looked up in their datasheets.

Fig 4 shows the measurement circuit used to determine these two parameters according to their definition:

$$Z_{\text{g}} = \frac{V_{\text{out}}}{I_{\text{in}}}, \quad Z_{\text{in}} = \frac{V_{\text{in}}}{I_{\text{in}}} \tag{7}$$

As long as we use relatively ideal current sources and voltage meters (IVVI `S4m` and Keithley multimeters will do), this measurement provides an accurate description about the most important behaviors of any `I-measure` or Ithaco. From then on, we can plug these two numbers along with the equivalent circuit of Fig 3-right into our measurement circuit and carry out any analysis.

Note that the current supplied and voltages measured can be either in DC or at any lock-in frequency. To measure both at the same time, it is easiest to perform a DC+lockin measurement and sweep in DC bias. The resulting $V(I)$ slopes determine $R_{\text{g}}, R_{\text{in}}$ in DC and the averaging of lock-in signals removes possible interference with nearby frequencies.

3.3 Input resistance and gain at finite frequency

The results of these $Z_{\text{g}}, Z_{\text{in}}$ at finite frequencies are shown on the complex plane in Fig 5 for one of the `M1b` units we tested. The spec values are $R_{\text{g}} = 1\,\text{M}\Omega$ and $R_{\text{in}} = 12\,\text{k}\Omega$, but they begin to deviate from these purely resistive values quickly for even very low frequencies.

Fig 6 then shows the diagram of the entire voltage-biased circuit used to measure the device simulators in the fridge, if we omit the presence of any filters or parasitic L, C except those already included in $Z_{\text{g}}, Z_{\text{in}}$. The device resistance, following this circuit, should be obtained from the measurement results as

$$R_d = \frac{V_{\text{in}}}{V_{\text{out}}/Z_{\text{g}}} - Z_{\text{in}} - R_1 - R_2 \tag{8}$$

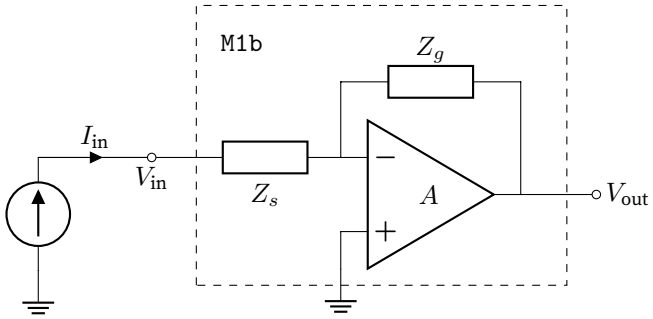

Figure 4: Using an ideal current source to characterize a current amplifier.

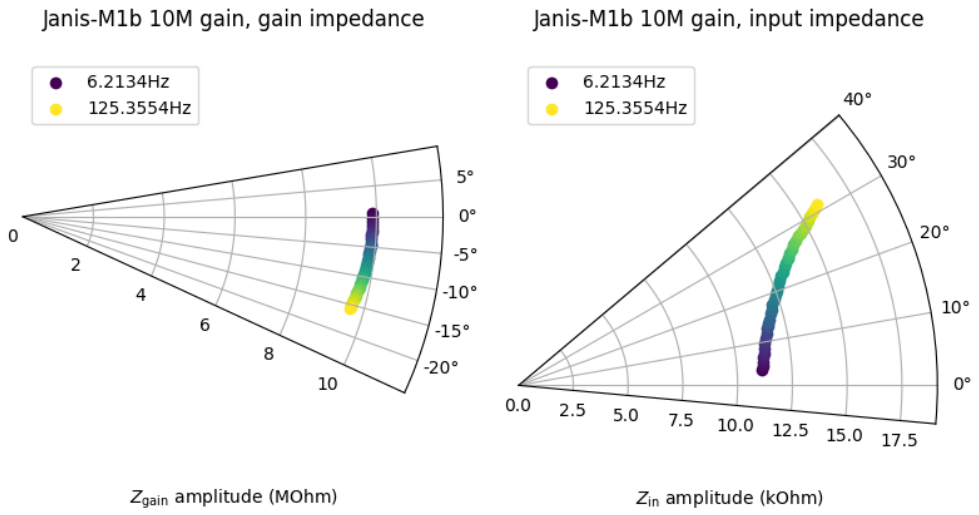

Figure 5: Z_{g} and Z_{in} measured for the `M1b` unit labeled `Janis` at finite lock-in frequencies. Both of these complex impedance components contribute to the final phase showing up on the lock-in measured signal.

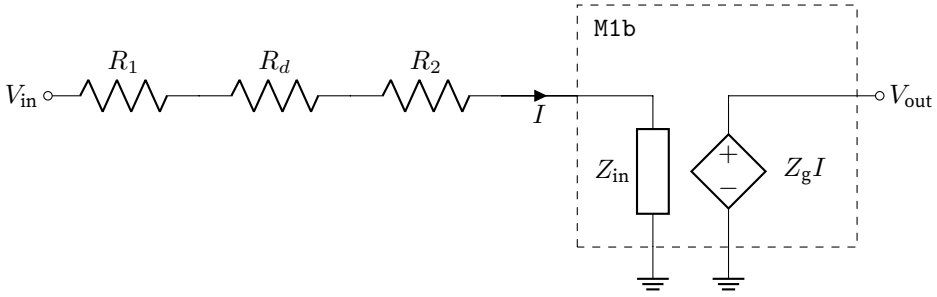

Figure 6: Circuit diagram of voltage-biased sample in fridge measured by a current-to-voltage-converter at the end. It is assumed the fridge line filter capacitors do not play a role because $R_d < \infty$ and the operating frequency is well below the line bandwidth.

Plug the measured values of $Z_{\text{in}}, Z_{\text{g}}$ at each corresponding frequency into the calculation above and we get the results shown in Fig 7. The resulting impedance is still not purely real so both the real part and the phase are plotted. Although the resistance values still deviate from the known value of 10 kΩ, the frequency dependence and large inductive phases are largely removed. The residual systematic errors may be attributed to several different sources: insufficient waiting time at the lowest frequencies, unaccounted-for L, C components in the circuit, *etc*.

Again, this example does *not* serve to demonstrate how to recover the correct measurement result from an imperfect measurement. Rather the contrary, it reiterates the two points we've made above:

- Make sure your desired circuit approximations hold *before* you start the measurement (*e.g.* by operating in low enough frequencies and using the correct amplifier settings).
- Trust your DC measurements more than the lock-in when it comes to accuracy of the values in most cases.

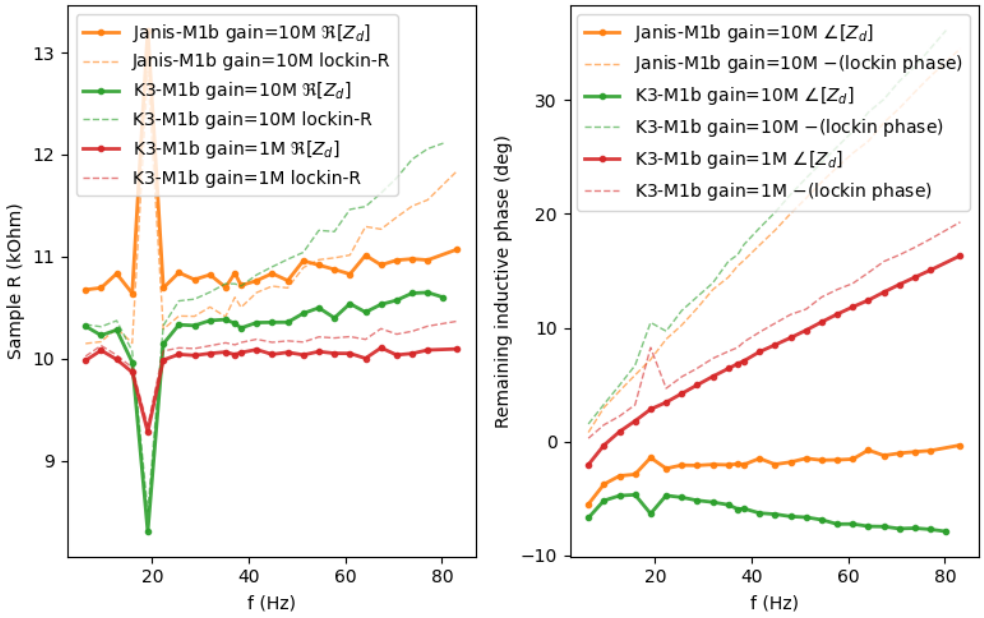

Figure 7: Results of device resistance calculation using measured gain and input impedances of `M1b`. Solid lines are the real parts of device resistance (left) and its phase (right) calculated using Eq 8. Dashed lines of corresponding colors are the same results as in Fig 2, *i.e.* using the lock-in R component to calculate the current and subtracting a purely real input resistance. (A minus sign is added to the raw lock-in phase to make positive phases indicate an inductive result in both cases.)

4 Appendix

4.1 Fridge line filter effects on 3-terminal setup

Section 2.2 mentioned an alternative circuit is possible when it comes to voltage-biased resistance measurements: placing a current meter on the same side of the fridge as the voltage meter, which is a setup typically seen in 3-terminal nonlocal conductance experiments. This section discusses the role the fridge line filter plays in this scenario.

The RC network present in the circuit is the same and still has a total impedance Z_{tot} defined in Eq 3. However, it is I_1 instead of I_2 that is measured this time and therefore it is simply $I_1 = V/Z_{\text{tot}}$.

Now we need to make some simplifications based on assumptions of the values in the expression for Z_{tot}. We first throw away any second-order term in ω since the cutoff frequency of the filters is typically > 5kHz and typical lock-in operation frequency is $f = \omega/2\pi < 50$ Hz. This means the product $\omega\tau_i < 0.1$ and the second order term is negligible. This simplifies the above expression to ($R_\Sigma \equiv R_1 + R_d + R_2$):

$$Z_{\text{tot}} \approx \frac{(R_1 + R_d + R_2) + j\omega[\tau_1(R_d + R_2) + \tau_2(R_1 + R_d)]}{1 + j\omega[C_1(R_d + R_2) + \tau_2]} \tag{9}$$

$$= R_\Sigma \cdot \frac{1 + j\omega\left[\tau_1\left(1 - \frac{R_1}{R_\Sigma}\right) + \tau_2\left(1 - \frac{R_2}{R_\Sigma}\right)\right]}{1 + j\omega\left[\tau_1\left(\frac{R_\Sigma}{R_1} - 1\right) + \tau_2\right]} \tag{10}$$

We can move all imaginary parts to the denominator in order to illustrate the behavior of this network more clearly and again throw away the resulting second order terms in ω. The final expression is

$$Z_{\text{tot}} \approx R_\Sigma \cdot \frac{1}{1 + j\omega\left[\tau_1\left(\frac{R_\Sigma}{R_1} + \frac{R_1}{R_\Sigma} - 2\right) + \tau_2\frac{R_2}{R_\Sigma}\right]} \tag{11}$$

At finite frequency, the load impedance is the DC resistance with a low-pass filter applied. As a quick estimation, such a filter introduces 6° of rotation of the signal on the complex plane when the operating frequency is 0.1x the cutoff. The cutoff frequency of this low-pass filter is

$$f_{\text{eff}} = \frac{1}{2\pi}\left[\tau_1\left(\frac{R_\Sigma}{R_1} + \frac{R_1}{R_\Sigma} - 2\right) + \tau_2\frac{R_2}{R_\Sigma}\right]^{-1} \tag{12}$$

We can learn a few things from this expression:

- The cutoff is R_d-dependent. This means if one starts to see an appreciable effect of the fridge line filtering in their measurement (*e.g.* phase $> 10^\circ$ even when all other parts of circuit settings are correct) and wish to then recover the correct value of R_Σ from this total expression, they would need to know the capacitance values and numerically solve this equation. This is hardly what we want, especially considering the filtering in fridge lines usually come in stages, whereas here we're looking at one stage alone, and numerous parasitic components exist. This can be avoided by ensuring the capacitors do not draw any current, *i.e.* $(\omega C_i)^{-1} \to \infty$ compared to any R. Otherwise, the amount of current each capacitor draws depends on all the other components in the circuit and we would have no way of knowing how much current was actually flowing through the device.

- The imaginary part does not in general assume a simple form that's predictable from the filtering parameters alone (*e.g.* $\omega \sum C_i$).
- If all resistors are of the same order of magnitude, f_{eff} is also of the same order as the designed filter cutoff. However, if the device resistance is very high, $R_\Sigma \gg R_1$ and through the first term in the bracket, f_{eff} becomes much lower than the fridge line bandwidth.[1] This is also easily understood as having a filter $R_d C_1$ instead of $R_1 C_1$ playing the biggest role and therefore severely modifying the designed bandwidth. In the limit of $R_d \to \infty$, we can treat R_1, R_2 as shorts (can be verified in the expression) and the imaginary part (Y component) is proportional to ωC_1.

To summarize, **we need to make sure the fridge line filters do not introduce any appreciable phase rotation to the signal**. Otherwise, we do not have a good way of removing the effects of this artifact. Fortunately, this is usually satisfied because the fridge line bandwidth is quite high compared to the usual lock-in operation frequency so this does not happen too often. The most common situation where this assumption fails is **when the device has infinite resistance** (inside the Coulomb or superconducting gap). In those situations, think twice before you decide you can trust the lock-in value (*e.g.* if you want to use it to calculate the subgap conductance suppression).

4.2 DC circuit artifacts

We have seen that as soon as non-ideal circuit components L, C are present in lock-in measurements, they begin to play a role in the measured values. Do DC signals also suffer from artifacts when we consider the reality that some of the circuit components are less ideal than the most simplistic models? If so, how much? We can examine the DC circuit in more detail regarding these questions.

We have either active or passive components in circuits. In DC, the only passive elements are resistors. To know them well, we only need to measure their values accurately. [2]

The active components are sources and amplifiers, the former of which can also be characterized very easily and accurately via Thévenin's theorem. The most tricky component in DC, then, is the amplifier. The basic properties of them are also easily characterized: the gain factor, offset and input/output impedance. [3] The two things that are usually omitted, however, are finite common mode suppression and finite open-loop gain.

4.2.1 Common mode suppression

An ideal differential amplifier only amplifies the difference of the two input signal voltages: $V_{\text{out}} = A(V_+ - V_-)$. The "common mode" $(V_+ + V_-)/2$ component of the input should be entirely rejected. However, real amplifiers are not completely immune to the common mode voltage. This problem usually manifests itself when V_+, V_- are close to each other but both at a very high/low voltage relative to the circuit ground of the amplifier.

[1] To put numbers to these quantities, we take K3/K4 as an example. The largest fridge filter there is 22 nF and for a resistance on the order of 13 kΩ this translates to a characteristic frequency of 556 Hz. A reader may feel that 556 Hz $\gg$ 40 Hz, but at 40 Hz the current is already reduced by >2% and a phase shift of 5° is introduced, according to a very simple SPICE model.

[2] The measured values for K3/K4 fridge lines can be found in a separate document that will be published online soon. We will include a link in a newer version of this document once it is published.

[3] These data for several M1b's and M1h are similarly available in the aforementioned document.

A concrete example is when measuring a device of very low resistance (*e.g.* supercurrent) in the fridge using a four-probe setup. Due to currents running through the fridge line resistors, both voltage probes attached to the device will be at an elevated voltage relative to fridge ground, although the voltage difference between them is small. The voltage measurement amplifier might be picking up the common mode voltage if its supression thereof is not strong enough. The IVVI `I-source` module is thus equiped with a `V2=V4` mode to combat this problem: it supplies currents in a way that allows the device to still sit at roughly the fridge ground, thus eliminating the large common-mode component.

Since there is an easy fix to the problem (using the symmetric biasing mode), we leave out more detailed discussions in this lock-in-focused document but only alert users to its existence in practice. For further reading on this and all of the other non-idealities, §4.11 of the book *The Art of Electronics* by Horowitz and Hill treats them in detail.

4.2.2 Amplifier at finite open-loop gain

In this section, we address the second non-ideality, namely the finite op-amp open-loop gain $A < \infty$ and check how the measurement is affected when we do take it into account. The following paragraphs assume a basic understanding of the two golden rules of op-amps.

The two op-amp golden rules result from the approximation that A is usually very large ($> 10^3$) and can be treated as infinite. In the case of `M1b` low-noise mode, this value is configured to be around 1000 and therefore neglecting it could introduce errors on the order of $1/A$.

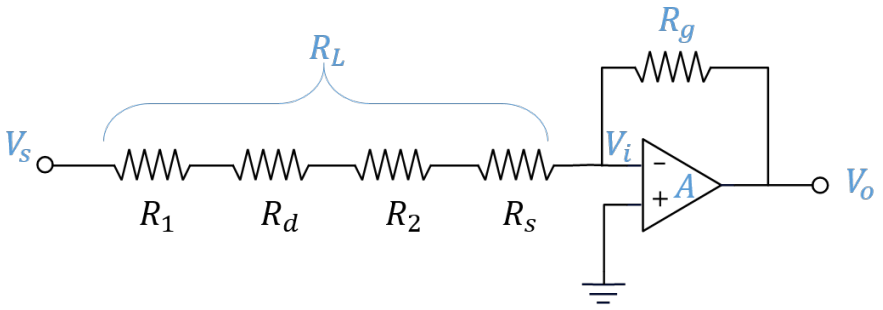

Figure 8: Circuit with finite gain

R_1 is the source and total line resistance before sample, R_d the device under test, R_2 the line resistance after the sample. R_s is the part of the input impedance of the current meter that is gain-independent (for `M1b` this is 2 kΩ). The total input impedance of a current preamp including that of `M1b` is $R_s + R_g/(1 + A)$ where R_g is the gain factor, *e.g.* 10M V/A = 10MOhm.

$$\frac{V_o - V_i}{R_L} = \frac{V_i - V_o}{R_g} \tag{13}$$

$$V_o = -AV_i \tag{14}$$

Solving this (expressing V_o in R_L, R_g, A, V_s) gives

$$V_o = -A\frac{R_L || \frac{R_g}{1+A}}{R_L} V_s = -\frac{A}{1+A}\frac{V_s}{R_L + R_g/(1+A)} R_g \tag{15}$$

($R_a||R_b \equiv R_a R_b/(R_a+R_b)$.) When the gain-dependent part of the input resistance $R_g/(1+A)$ is far smaller than the total load R_L, the load term will dominate and we recover

$$V_o = -\frac{A}{1+A}\frac{V_s}{R_L}R_g \tag{16}$$

which is a good current-to-voltage converter up to a factor of $A/(1+A)$. This number is typically very close to 1 (0.999 for `M1b` low noise, 0.9999 for `M1b` low-Rin and `M1h` low noise, 0.99999 for `M1h` low-Rin).

Even if we do not make the approximation that the load term dominates, we see that dividing the ideal voltage output V_s by what we think is the current ($-V_o/R_g$) gives us

$$\frac{V_s}{-V_o/R_g} = \frac{1+A}{A}\left(R_L + \frac{R_g}{1+A}\right) \tag{17}$$

Apart from a small addition of $1/A$ factor, this is exactly what we use to calculate the real device resistance with.

Writing out the full expression,

$$R_d = \frac{V_s}{-V_o/R_g}\frac{A}{1+A} - \frac{R_g}{1+A} - R_s - R_1 - R_2 \tag{18}$$

Compare this to the naïve expression:

$$R_{d,\text{wrong}} = \frac{V_s}{-V_o/R_g} - \frac{R_g}{1+A} - R_s - R_1 - R_2 \tag{19}$$

This means our error

$$\frac{R_{d,\text{wrong}} - R_d}{R_d} = \frac{1}{1+A}\frac{R_\text{tot}}{R_d} \tag{20}$$

where R_tot is the total resistance we think we measure in the naïve picture.

In summary, the influence of finite open-loop gains of op-amps, although real and present, is very small (generally $\ll$1%) on the reliability of the DC measurement results in our context, provided that the device resistance constitutes the majority of total resistance in the circuit.

5 Acknowledgements and further reading

Measurements, analysis, and documentation was done by Jouri Bommer, Guanzhong Wang and Michiel de Moor, with valuable input from Bernard van Heck, Gijs de Lange, and Raymond Schouten. The analysis has further been discussed with Leo Kouwenhoven, Hao Zhang, Di Xu, and Nick van Loo.

For further understanding of current-to-voltage converters, including what design choices there are and some basic principles of its noise and back-action, we refer readers to a set of slides by Raymond Schouten sent along with this document.