Jade Computer Note No. 30
15.11.1979
Y. Watanabe

"SPINNING LEAD GLASS" ANALYSIS

Having a compact system of about 3000 ADC channels, it is next to impossible to make the operation perfect. This is a description of the nature of "spinning blocks" and of the method developed in handling them.

I. The nature of "spinning blocks"

The problem of "spinning blocks" originates from various hardware causes.

(1) Hot channels

There are 2 to 3 ADC channels which are always on with pulse heights of more than 3000 counts. The FAST CLEAR of these channels has ceased functioning and charges on a capacitor keep accumulating, thus giving overflow.

(2) Change of pedestals

Pedestals for each ADC channel are measured at the beginning of each run and are subtracted. To be written into IBM, channels have to have more than 5 counts. The pedestal values could change gradually or suddenly during a run by some defective operations of ADC as described in Appendix.

(3) Faulty ADC modules

During runs 1500 and 1521, one of the ADC modules behaved crazily. This was due to a drift of one of power voltages. Much less drastic drifts of pedestals may also happen due to a momentary change of power voltages.

(4) Faulty crates

During summer runs, the pedestals of a whole crate shifted time to time. This seems to have been cured by the installation of an AVR in the 220 V line. Similar effect may be still with us because one of the power voltages is overloaded and just at the edge of regulation.

(5) "monopole" events

Sometimes more than 2000 channels fire, each having typically 5 ~ 10 counts. Were these events real, they may be caused by the production and the fusion of a pair of monopoles. Some of these events are believed to be associated with spurious triggers, which are likely to occur right after accepted events. The linear sum output for the trigger could shift up to ± 100 mV, equivalent of about 3 GeV. The pedestals also shift because the steady repetition of gates and FAST CLEAR's is interrupted. This situation is illustrated in Fig. 1 reproducing the explanation given by Y. Totsuka. According to P. Dittmann, the step observed in on-line histogram of lead glass hitmap I is due to these "monopole" events, because he displays "only" up to 500 hit channels.

These hardware problems are no doubt to be improved, by replacing the whole ADC's as recommended by LeCroy, by increasing the power capacity of crates, by installing a separate circuit for the linear sum trigger to avoid the pickup of gates, and so on. Probably even then, the "spinning block" analysis described in the next section may still be necessary.

II. The analysis of "spinning blocks"

As a part of reformatting job, "spinning blocks" are listed run by r and are written into disk. The analysis reflects the nature of "spinning blocks" described in the previous section, and divides them into the following categories:

(1) "monopole" (# hit channels ≥ 600 out of 2880 channels total)
(2) each crate (# hit channels ≥ 80 out of 960 channels)
(3) each ADC (# hit channels ≥ 24 out of 48 channels)
(4) each channel

For each category, the following quantities are obtained:

f = frequency of occurance
aph = average pulse heigths
σ = average sigma of pulse heigths

In histogramming the quantities for each channel, only the events where none of the energy bits for lead glass are set (i.e. $E_{LG} < 1$ GeV) are used to reduce biases from rather frequent Bhabhas and energetic beam gas events. When an event is of type (1), (2) or (3), then the rest of analysis is not done for the event to avoid double counting.
Those quantities above some thresholds are written to disk. The values for the thresholds are empirically decided and are summarized in Table I.

III. The use of the "spinning block data"

The data of "spinning blocks" written on disk are added into 'F11LHO.AUPDAT1', one of the general constant files of O'Neill's. Then in the stage of reduction 1, a subroutine LGCALB is called, whose primary function is to create a calibrated bank of 'ALGN'/1 out of 'ALGL'/1, i.e. counts are converted to MeV. On the process of doing so, a subroutine LGERSE is called, which subtracts some constants from "spinning blocks". These constants are prepared at the beginning of a new run, obtaining the information from the common CALIBR, which is updated at a new run, reading the file 'F11LHO.AUPDAT1'. The constants to be subtracted depend on the "spinningness", and are again decided empirically as summarized in Table II. When the pulse heights after subtraction are zero or negative, then the blocks are deleted in creating 'ALGN'/1 bank. Also deleted are the ADC channels corresponding to the ring 1 and 32, and two dead channels, where high voltage cables have been shorted. In this case the calibration factors in the common CALIBR are zero, thus the deletion is automatic. Typical subtraction constants are 10 to 15 counts (about 5.4 MeV/count), and only 2 to 3 channels are really killed.

If a run is too short (# events < 500), the information of "spinning blocks" for that run is <u>not</u> included in AUPDAT1. Then Reduction 1 jobs use that of the previous run which contains statistically more meaningful quantities.

The treatment of "spinning blocks" has to be effective, but at the same time safe enough not to distort the real events. The procedure described here is still primitive and any constructive criticisms and advices are most welcome.

Appendix defective ADC operations

Some of the characteristics of LeCroy 2282 have been identified as defective. Those relevant to us are listed below.

(1) Pre-gate feedthrough

Any input signal of amplitude greater than -50 mV that is present 0-5 msec before a gate causes a pedestal change of up to 70 counts. The closer the signal is to the gate, the larger the pedestal shifts. This case may be realized by e.g. cosmic rays which come randomly.

(2) Fast clear rate effect

A pedestal value depends on the time between the gate and the fast clear signal. The pedestal is shifted by 7 to 10 counts if this time is decreased from 1 second to 1 μsec. The situation could be realized after a pause, ID trip or each event. There is also a pedestal shift of 3-5 counts if fast clears come too rapidly in succession. This probably is very seldom.

(3) Ground loop problem?

Because of the ground loop problem, the input to ADC may shift coherently, which may be another cause of "monopole" events.

TABLE I Thresholds to write to disk

CATEGORY	#hits	f	APH
"monopole"	>600	0.2%	0
each crate	> 80	0.2	0
each ADC	> 24	0.2	0
each channel	-	5.0	5 counts
	-	0.5	20 counts.

where f = frequency

APH = average pulse heights

TABLE II Subtraction Constants

CATEGORY	CASE	subtraction constants
"monopole"	f > 0.2%	APH + 3σ
(#hits > 600)	f < 0.2	0
each crate	f > 0.2	APH + 3σ
(#hits > 80)	f < 0.2	0
each ADC	f > 0.2	APH + 3σ
(#hits > 24)	f < 0.2	0
each channel	f > 5%.AND.APH > 5	APH + 3σ
	f > 1%.AND.APH > 100	APH + 3σ
	f > 5%.AND.APH > 100	9999 (i.e. to kill)

Note For safety reason, σ is arbitrarilly limited to

$6 < \sigma < 60$ counts.

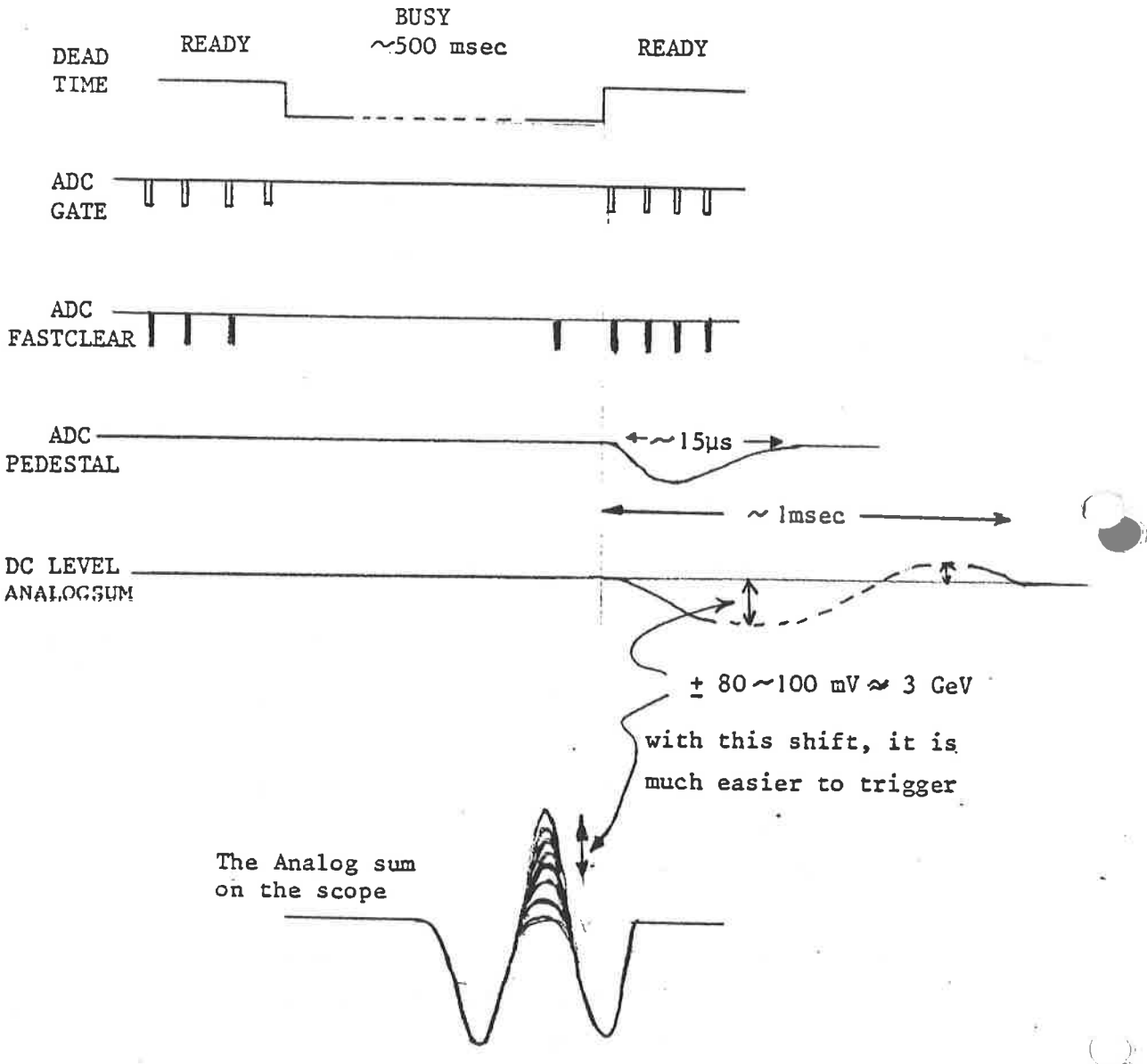

Fig. 1 Timing diagram of spurious triggers and "monopole" events