Universidad Politécnica de Valencia

Redes en Chip

The Spidergon Network-on-Chip

Author:
Andrew Fecheyr Lippens

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Abstract

TODO: write an abstract

Contents

1 Introduction

A network-on-chip or NoC has become one of the key components in digital chips. As the number of components and transistors per chip grows continuously, most chips have become multi-core. These chips consist of a number of separate cores, often with fixed-function accelerators, memory arrays and input/output units.

Historically buses or crossbar switches were used to connect the functional components of a chip. Above four cores, however, the limited bandwidth of a bus becomes a major limitation, and above 8 or 16 cores, crossbar switches become very expensive. Only a NoC provides the scalability needed for emerging multicore chips. The NoC bounds the performance potential of these chips and accounts for a substantial fraction of the power and area consumption.

TODO: introduce Spidergon

2 Background

2.1 Technical Terms

This paper uses technical terms from the domain of computer networks. Some of them are explained here to help the reader.

System on Chip (SoC) refers to the integration of all components of a computer or electronic system into a single integrated circuit (chip) [6]. SoCs are often used in space and power constrained devices.

A Network on Chip (NoC) is a packet-switched on-chip micronetwork. It is the natural evolution of traditional circuit-switched bus solutions.

An Interconnect Processing Unit (IPU) is a configurable and extensible communication component that implements system services and core communication. It is essentially an on-chip communication network with hardware and software elements which jointly implement key functions of different SoC programming models through a set of communication and synchronization primitives and provide low-level platform services to enable advanced features in modern heterogeneous multi-core SoCs.[1]

A Chip multiprocessor (CMP) is a multi-core processor in which the distinct cores are integrated onto a single integrated circuit die.

IP block: In electronic design a semiconductor intellectual property core or IP block is a reusable unit of logic, cell, or chip layout design that is the intellectual property of one party. They are often used as building blocks in SoC designs.

2.2 Bus vs. Network-on-Chip

SoC communication has traditionally been done using on-chip busses. A diagram of an early bus architecture is depicted on figure 1. This allowed designers of early SoCs to select IP blocks, place them onto the silicon, and connect them together with a standard on-chip bus.

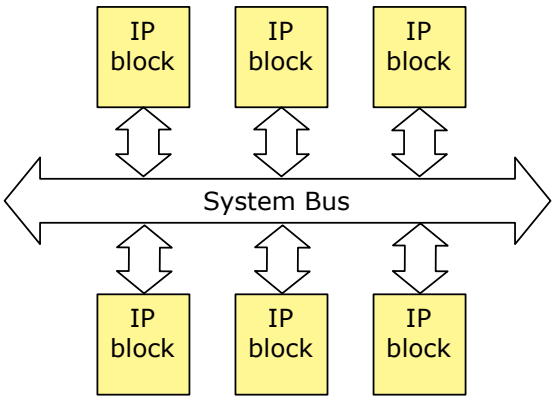

Figure 1: Early SoC structure based on a single shared bus

Buses are well understood and have been successfully implemented in many complex SoCs focusing on both application-based and processor-specific features, thus providing compatibility with most available IP and processor cores, and SoC communication requirements. Examples of more modern on-chip buses include ST Microelectronics' STBus [4], ARM's AMBA AHB and IBM's Core-connect [3].

However, buses do not scale well. With the rapid rise in the number of blocks to be connected and the increase in performance demands, today's SoCs cannot be built around a single bus. Instead, complex hierarchies of buses are sometimes used, with sophisticated protocols and multiple bridges between them. Communication between two remote blocks can go via several buses, and every section of every path must be carefully verified [2].

Moreover, the increase in the number of connected IP and processor cores causes the bus to become a communication bottleneck due to sharing of aggregate bandwidth by all attached units, and worsens arbiter delay, thus introducing

variation, limiting scalability and making the arbiter instance-specific. Additional concerns regarding reachable clock frequency and time closure arise, since every bus transaction involves all connected cores and unnecessarily consumes significant power [1].

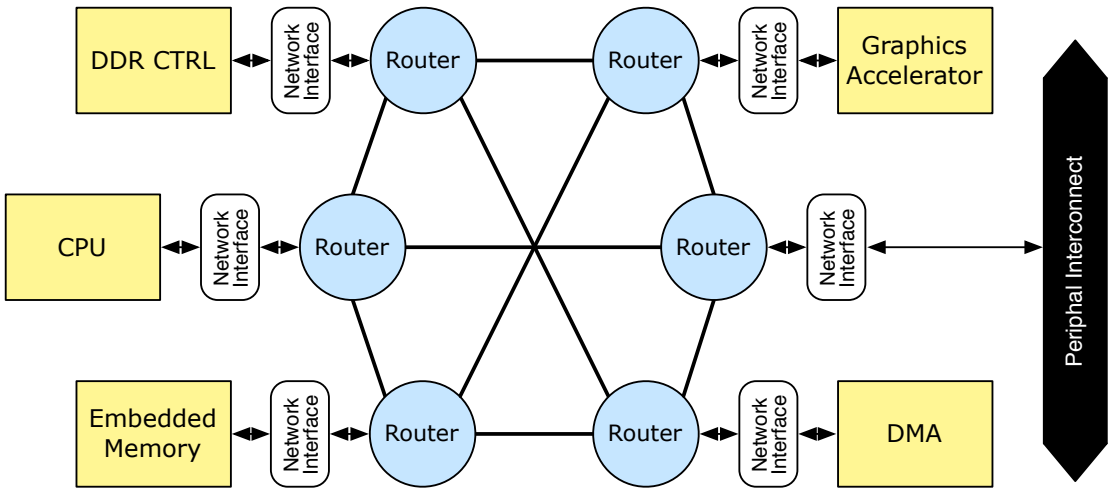

Figure 2: SoC equipped with a Network-on-Chip

3 Spidergon STNoC

3.1 Spidergon Topology

The proprietary Spidergon topology provides an interesting price/performance trade-off for SoC devices. In the Spidergon topology, all of the IP blocks are arranged in a ring where each IP block is connected to its clockwise and its counter-clockwise neighbour and directly to its diagonal counterpart in the network. This allows the routing algorithm to minimise the number of nodes that a data packet has to traverse before reaching its destination. A particularly important advantage is that the functional diagram (shown below on the left of figure 3 for a network of 16 nodes) corresponds to a simple planar implementation (shown on the right side of figure 3) in which the wiring only needs to cross itself at one point. This is a key benefit in delivering high price/performance [5].

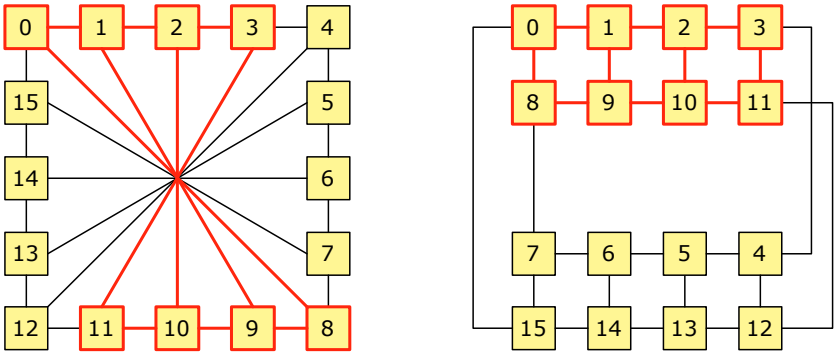

Figure 3: Equivalent representations of the Spidergon topology for $N = 16$

4 Conclusion

TODO: write a conclusion

References

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