**БЕЛОРУССКИЙ ГОСУДАРСТВЕННЫЙ УНИВЕРСИТЕТ**

**ИНФОРМАТИКИи РАДИОЭЛЕКТРОНИКИ**

**Факультет КСиС**

**Кафедра ЭВМ**

**АПВМиС**

Лабораторная работа № 4

Вариант № 29

**Описание и моделирование цифрового устройства на языке VHDL в потоковом виде**

**Выполнил: Проверила:**

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Структурная схема устройства.

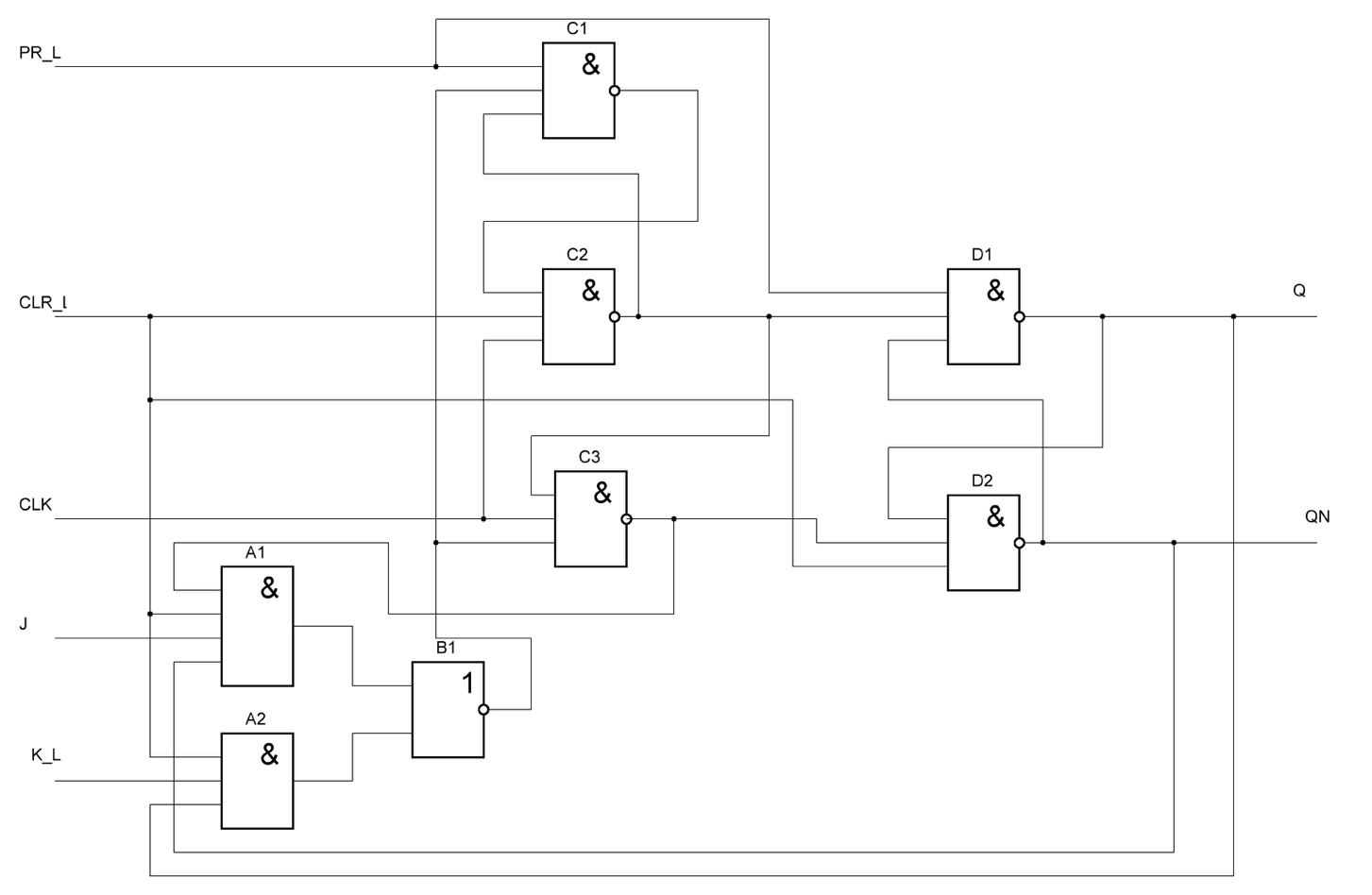
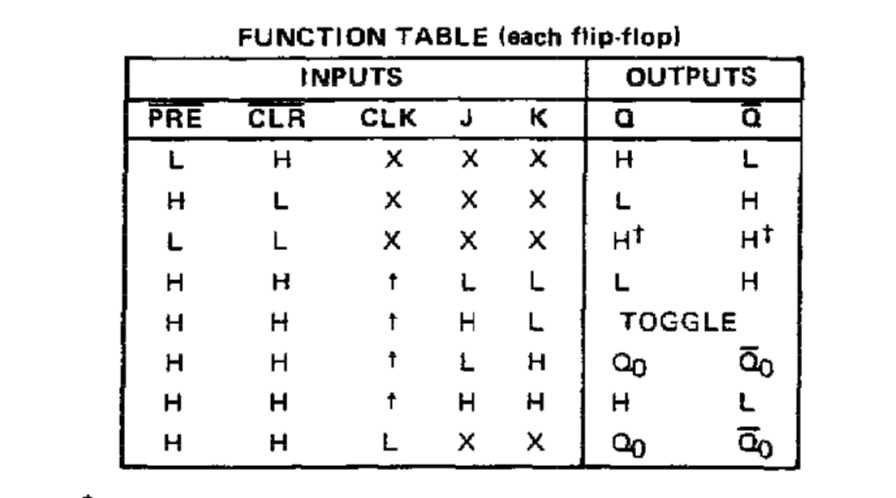


Таблица функционирования:



По результатам анализа определили, что схема комбинационного типа и имеет линии обратной связи, при это устройство принадлежит к устройствам с памятью.

1. Описание цифрового устройства на языке системы VLSI-SIM

CIRCUIT Lab3Code;

INPUTS PRL(1),CLRL(1),CLK(1),J(1),KL(1);

OUTPUTS D1(1),D2(1);

GATES

A1 'A4' (1) C3(1),CLRL(1),J(1),D2(1);

A2 'A3' (1) CLRL(1),KL(1),D1(1);

B1 'O2' (1) A1(1),A2(1);

C1 'NA3' (1) PRL(1),B1(1),C2(1);

C2 'NA3' (1) C1(1),CLRL(1),CLK(1);

C3 'NA3' (1) C2(1),CLK(1),B1(1);

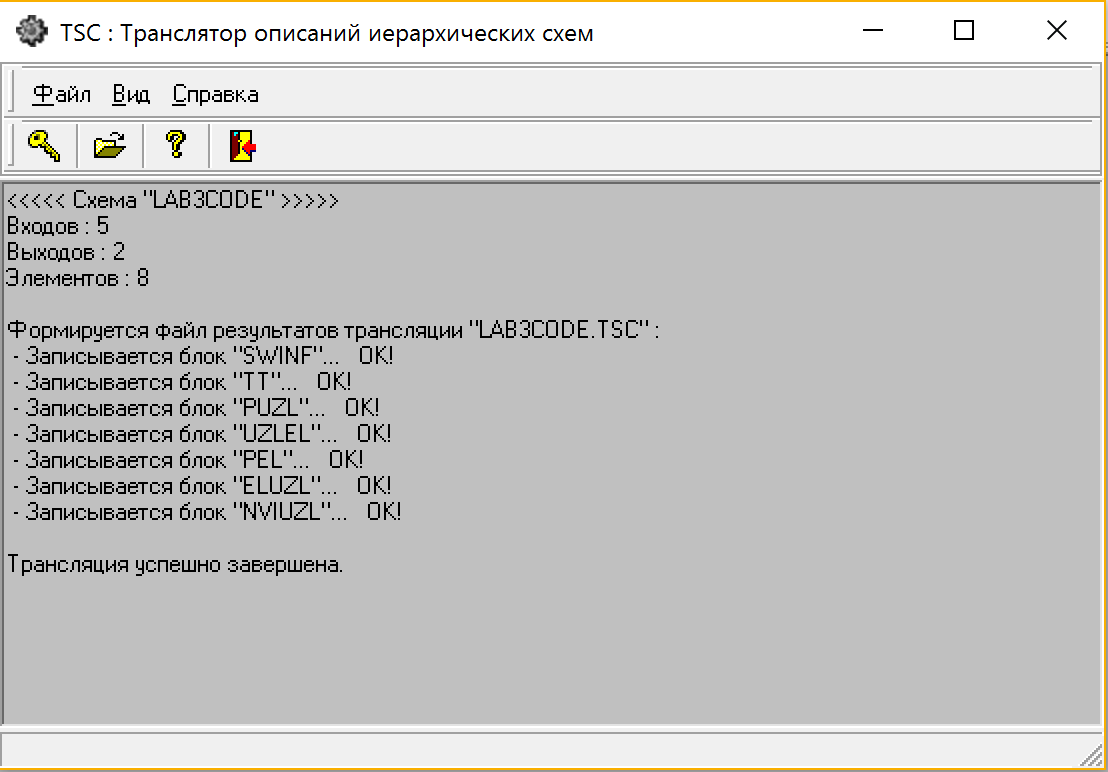
D1 'NA3' (1) PRL(1),C2(1),D2(1);

D2 'NA3' (1) D1(1),C3(1),CLRL(1);

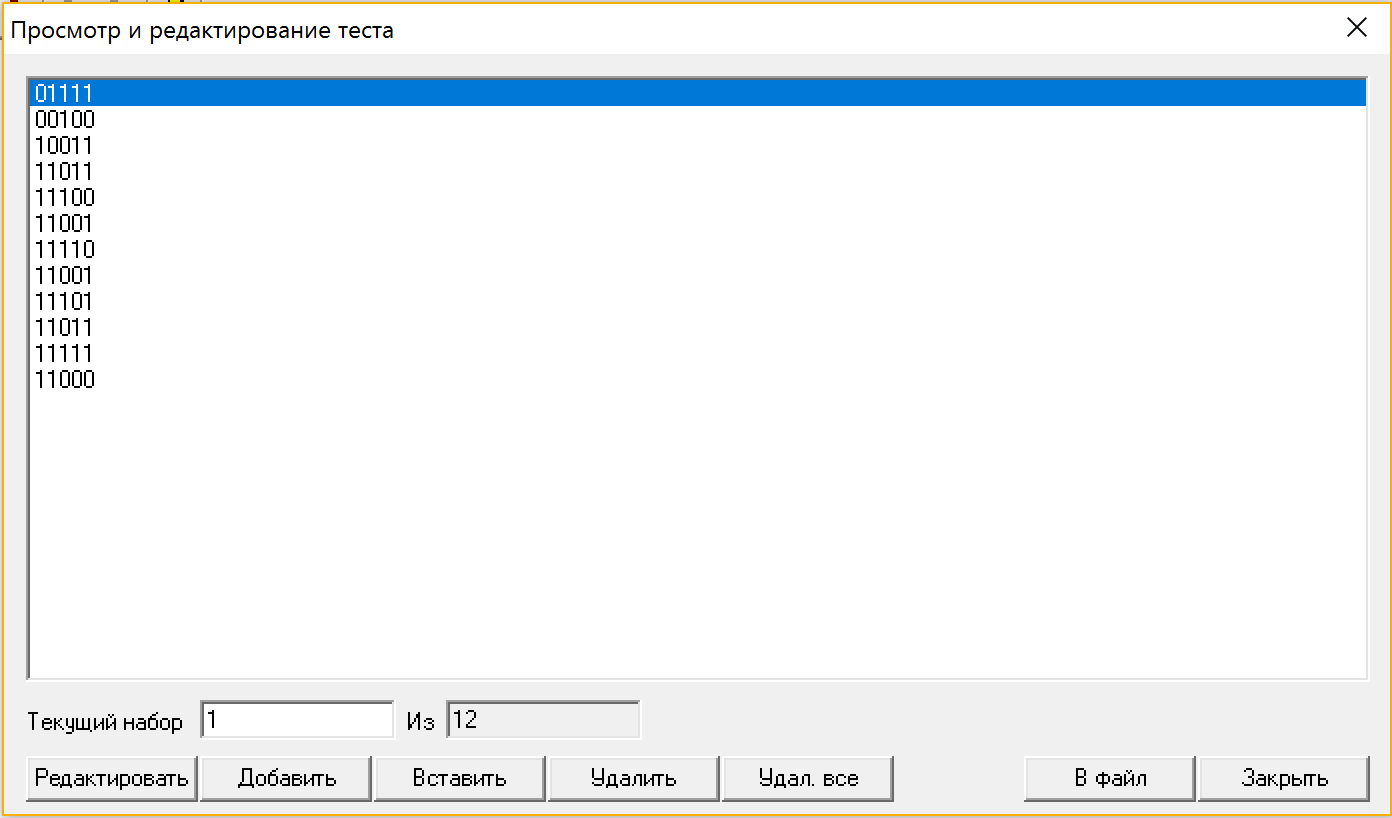
ENDGATES

END

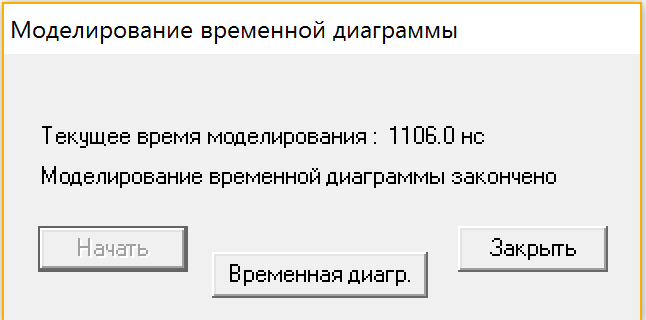
Трансляция описания:



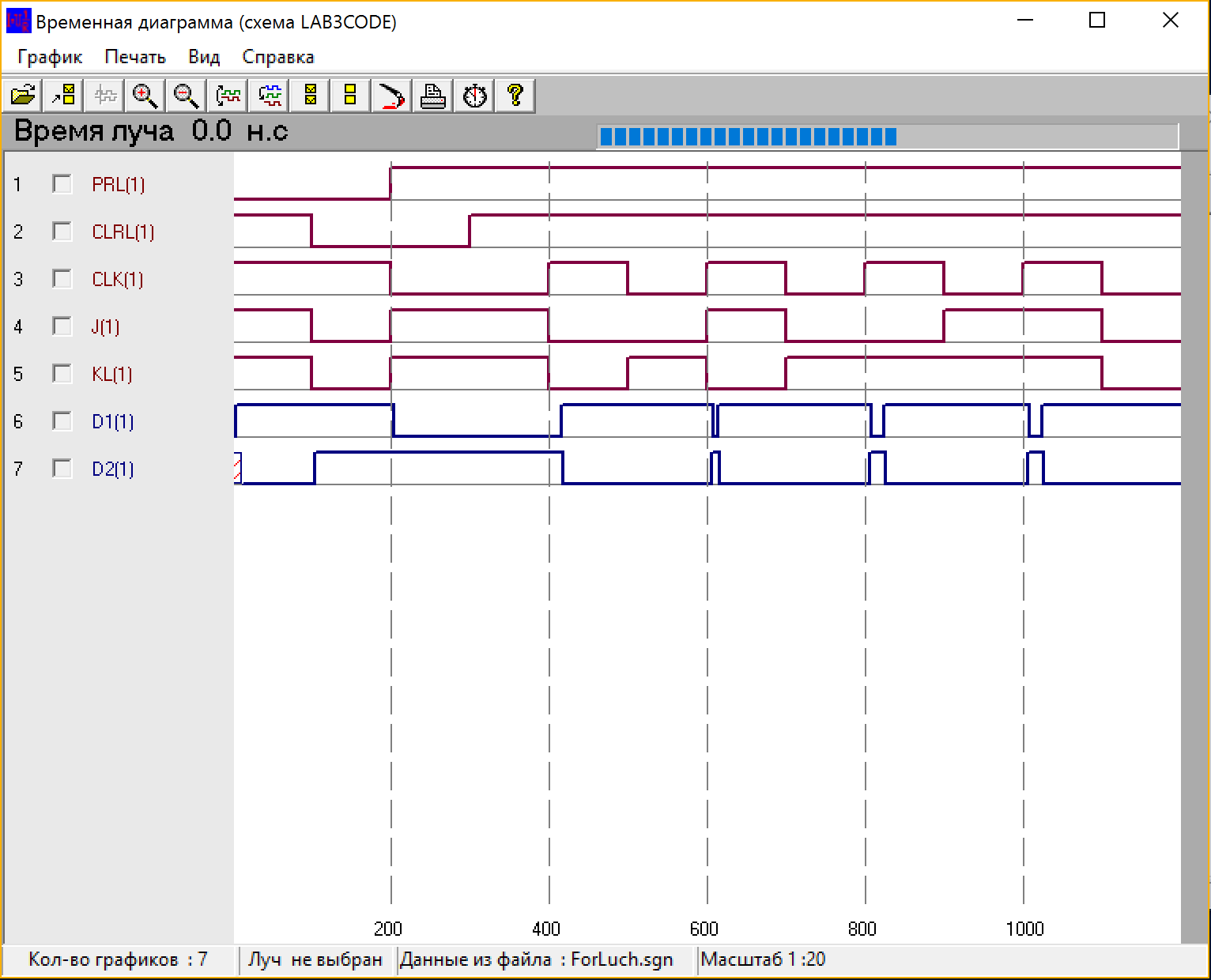
1. Провести моделирование схемы в программе SCA-TIME



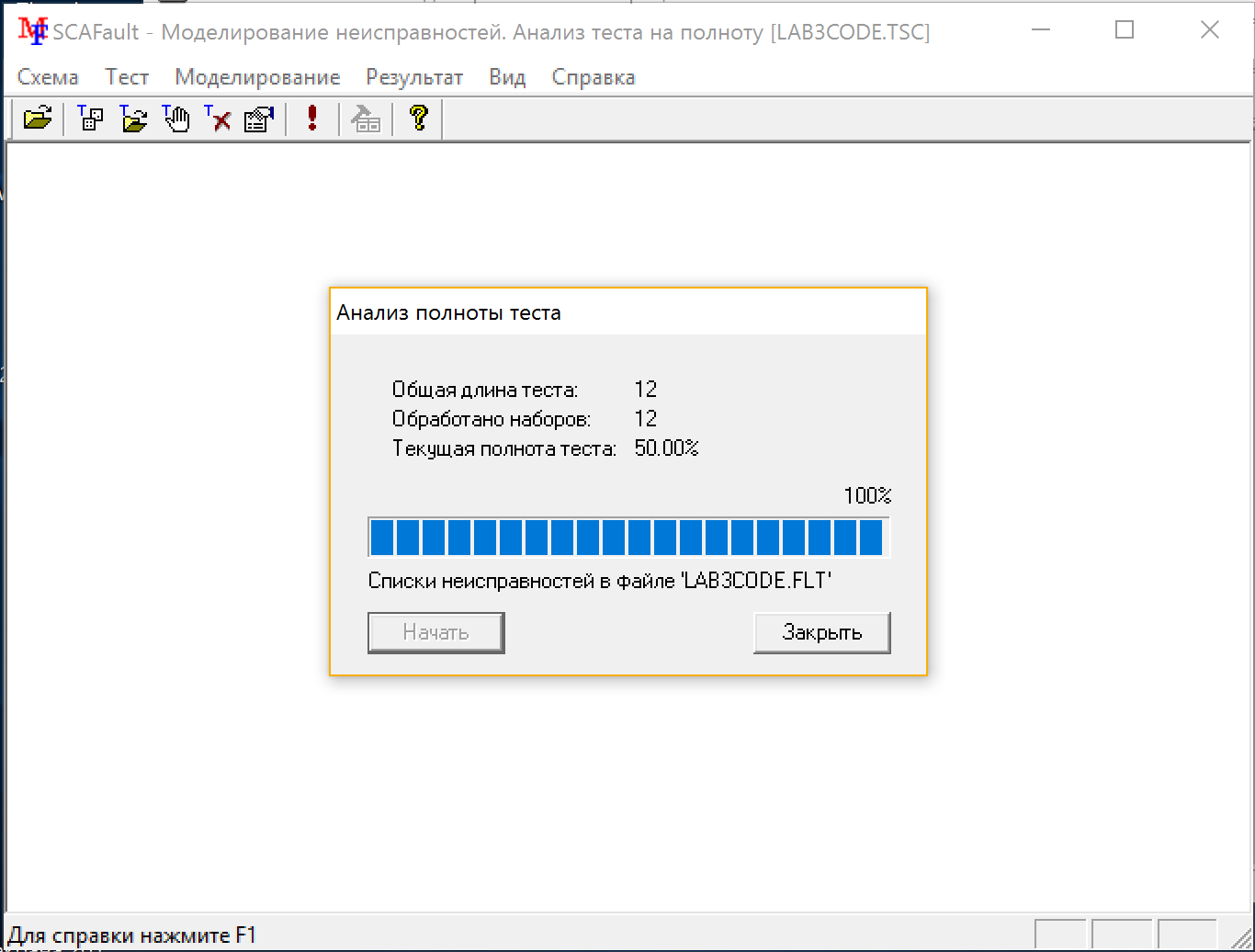
Моделирование теста:



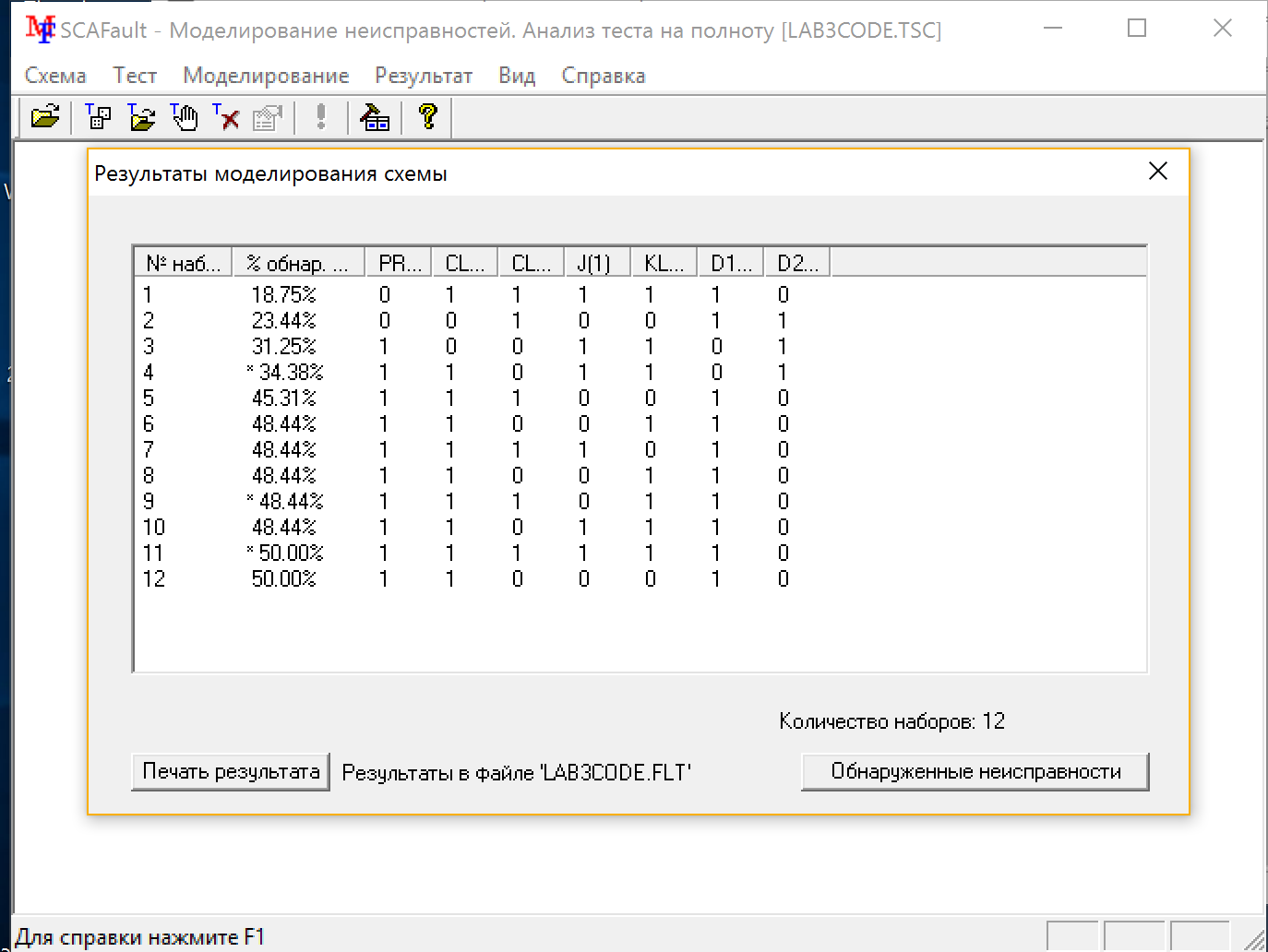
Временная диаграмма:



1. Определить контролирующую способность теста (SCAFault)

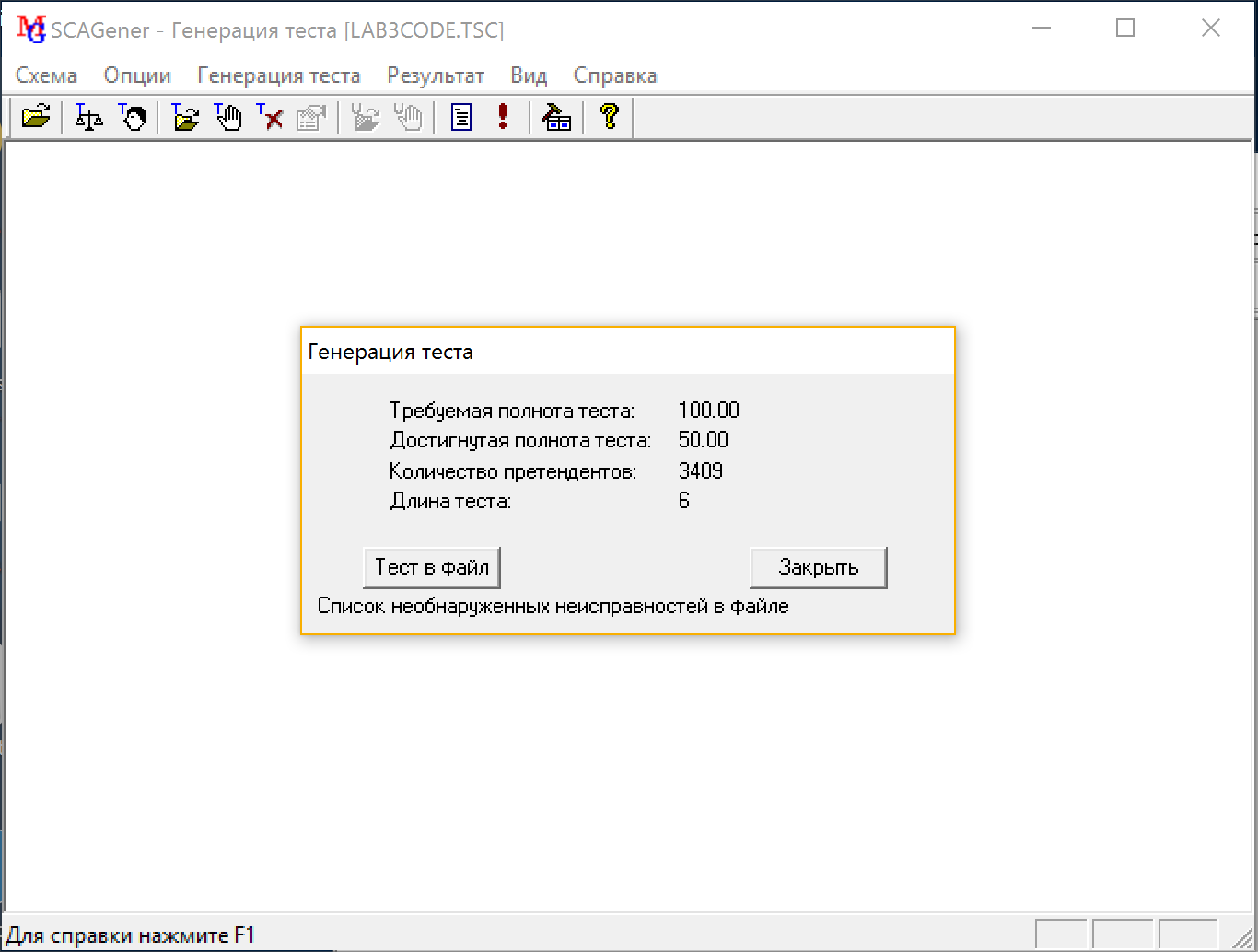


Результат моделирования:

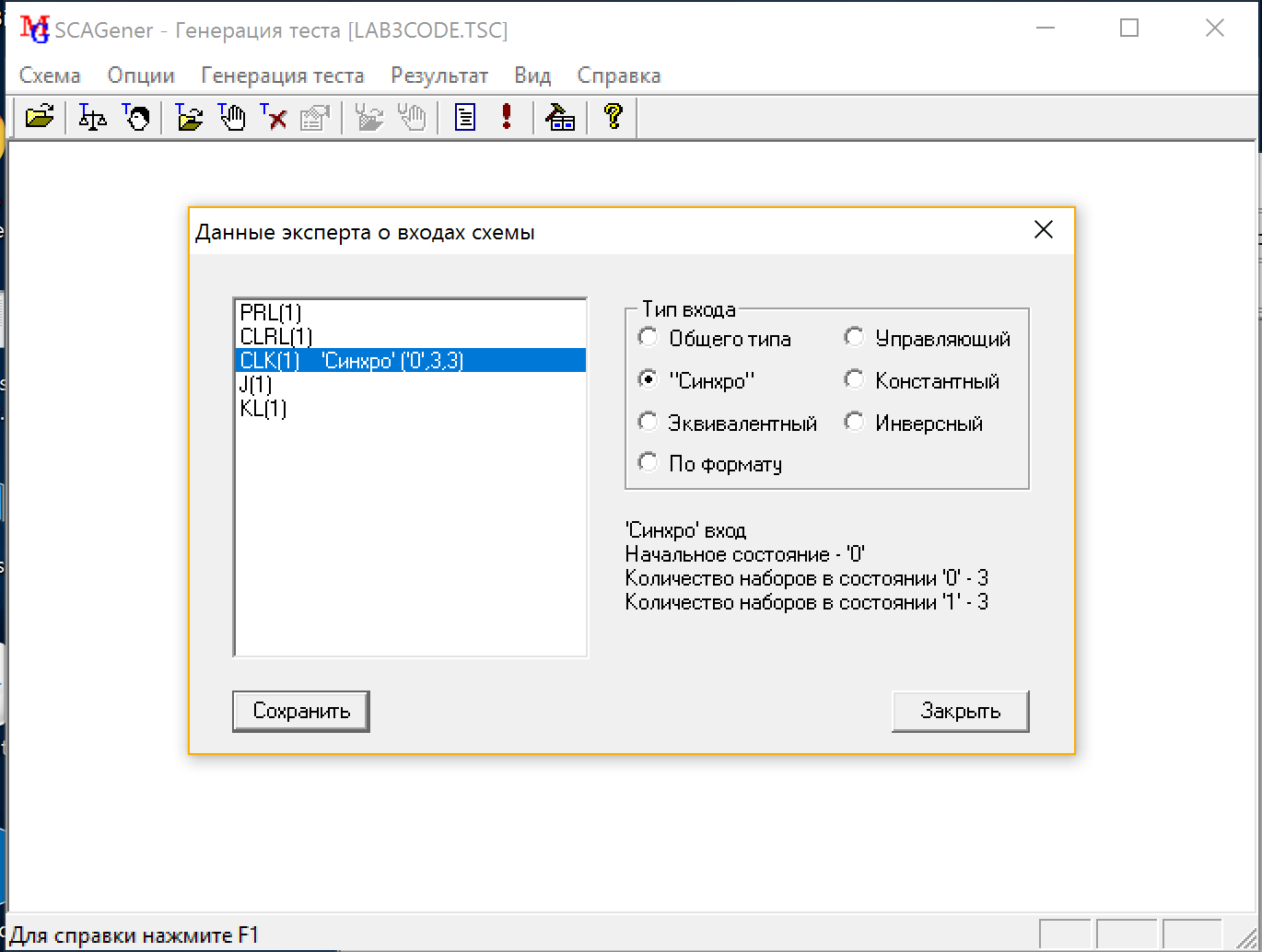


1. Проведение автоматического и автоматизированного теста при помощи программы SCAGener и функции «Данные эксперта»

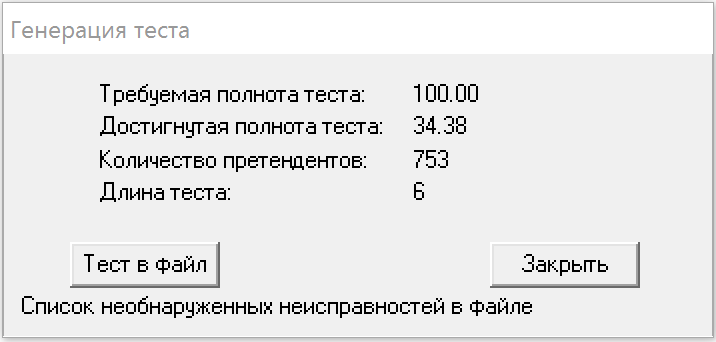
Автоматический тест:



Автоматизированный тест:



Генерация теста:



Вывод: под данному эксперименту видно, что для данной схемы автоматический и автоматизированный тесты не подходят.

1. Описание цифрового устройства в структурном виде на языке системы ModelSim

library IEEE;

use IEEE.STD\_LOGIC\_1164.all;

ENTITY A4 IS

port(

A, B, C, D: in STD\_LOGIC;

F: out STD\_LOGIC);

END A4;

ARCHITECTURE Arch\_A4 OF A4 IS

Begin

F <= A AND B AND C AND D after 4 ns;

END Arch\_A4;

library IEEE;

use IEEE.STD\_LOGIC\_1164.all;

ENTITY A3 IS

port(

A, B, C: in STD\_LOGIC;

F: out STD\_LOGIC);

END A3;

ARCHITECTURE Arch\_A3 OF A3 IS

Begin

F <= A AND B AND C after 3 ns;

END Arch\_A3;

library IEEE;

use IEEE.STD\_LOGIC\_1164.all;

ENTITY O2 IS

port(

A, B: in STD\_LOGIC;

F: out STD\_LOGIC);

END O2;

ARCHITECTURE Arch\_O2 OF O2 IS

Begin

F <= A OR B after 2 ns;

END Arch\_O2;

library IEEE;

use IEEE.STD\_LOGIC\_1164.all;

ENTITY NA3 IS

port(

A, B, C: in STD\_LOGIC;

F: out STD\_LOGIC);

END NA3;

ARCHITECTURE Arch\_NA3 OF NA3 IS

Begin

F <= NOT (A AND B AND C) after 3 ns;

END Arch\_NA3;

library IEEE;

use IEEE.STD\_LOGIC\_1164.all;

ENTITY hohoh IS

port (PRL, CLRL, CLK, J, KL: in STD\_LOGIC;

D1, D2 : inout STD\_LOGIC);

END hohoh ;

ARCHITECTURE ha OF hohoh IS

component A4

port(

A, B, C, D: in STD\_LOGIC;

F: out STD\_LOGIC);

end component;

component A3

port(

A, B, C: in STD\_LOGIC;

F: out STD\_LOGIC);

end component;

component O2

port(

A, B: in STD\_LOGIC;

F: out STD\_LOGIC);

end component;

component NA3

port(

A, B, C: in STD\_LOGIC;

F: out STD\_LOGIC);

end component;

signal A1, A2, B1, C1, C2, C3: STD\_LOGIC;

BEGIN

sA1: A4 port map (C3, CLRL, J, D2, A1);

sA2: A3 port map (CLRL, KL, D1, A2);

sB1: O2 port map (A1, A2, B1);

sC1: NA3 port map (PRL, B1, C2, C1);

sC2: NA3 port map (C1, CLRL, CLK, C2);

sC3: NA3 port map (C2, CLK, B1, C3);

sD1: NA3 port map (PRL, C2, D2, D1);

sD2: NA3 port map (D1, C3, CLRL, D2);

END ha;

1. Теста цифрового устройства на языке системы ModelSim

entity TEST\_Test is

end;

library IEEE;

use IEEE.STD\_LOGIC\_1164.all;

architecture BENCH of TEST\_Test is

component hohoh

port (PRL, CLRL, CLK, J, KL: in STD\_LOGIC;

D1, D2 : inout STD\_LOGIC);

end component;

signal PRL, CLRL, CLK, J, KL, D1, D2: STD\_LOGIC;

begin

PRL <= '0', '0' after 100 NS, '1' after 200 NS, '1' after 300 NS, '1' after 400 NS, '1' after 500 NS, '1' after 600 NS, '1' after 700 NS, '1' after 800 NS, '1' after 900 NS, '1' after 1000 NS, '1' after 1100 NS;

CLRL <= '1', '0' after 100 NS, '0' after 200 NS, '1' after 300 NS, '1' after 400 NS, '1' after 500 NS, '1' after 600 NS, '1' after 700 NS, '1' after 800 NS, '1' after 900 NS, '1' after 1000 NS, '1' after 1100 NS;

CLK <= '1', '1' after 100 NS, '0' after 200 NS, '0' after 300 NS, '1' after 400 NS, '0' after 500 NS, '1' after 600 NS, '0' after 700 NS, '1' after 800 NS, '0' after 900 NS, '1' after 1000 NS, '0' after 1100 NS;

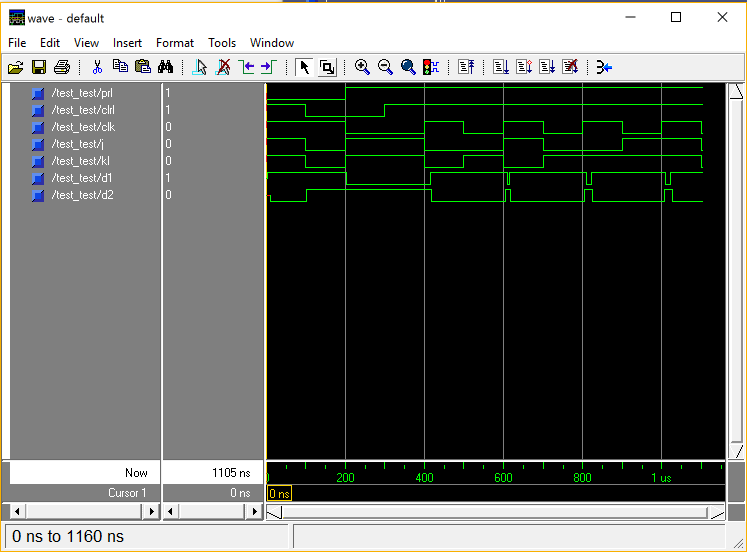
J <= '1', '0' after 100 NS, '1' after 200 NS, '1' after 300 NS, '0' after 400 NS, '0' after 500 NS, '1' after 600 NS, '0' after 700 NS, '0' after 800 NS, '1' after 900 NS, '1' after 1000 NS, '0' after 1100 NS;

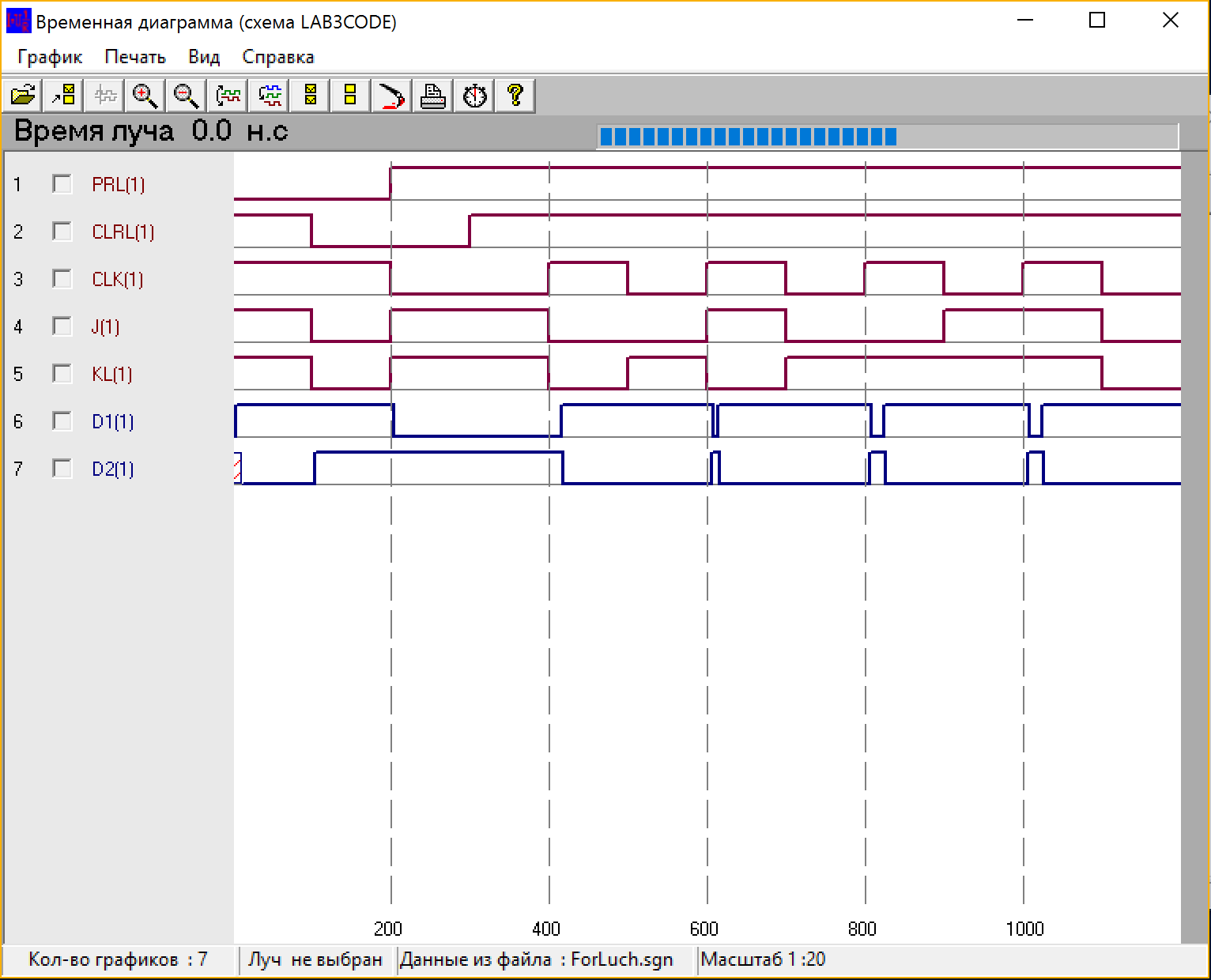
KL <= '1', '0' after 100 NS, '1' after 200 NS, '1' after 300 NS, '0' after 400 NS, '1' after 500 NS, '0' after 600 NS, '1' after 700 NS, '1' after 800 NS, '1' after 900 NS, '1' after 1000 NS, '0' after 1100 NS;

M: hohoh port map (PRL, CLRL, CLK, J, KL, D1, D2);

end BENCH;

1. Сравнение графиком, полученных в средах ModelSim и VLSI-SIM





1. Описание цифрового устройства в поведенческом виде на языке системы ModelSim

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

entity lab4\_3 is

port (PRL, CLRL, CLK, J, KL: in STD\_LOGIC;

D1, D2 : inout STD\_LOGIC);

end lab4\_3;

architecture V1 of lab4\_3 is

signal tempD1, tempD2: STD\_LOGIC;

begin

process (PRL, CLRL, CLK, J, KL, D1, D2)

begin

assert not(PRL='1' and CLRL='1' and CLK'event and CLK='1' and J'event and KL'event) report "Error :(" severity error;

if (PRL='1' and CLRL='1') then

if (CLK'event and CLK='1' and J='0' and KL='0') then

tempD1 <= '0';

tempD2 <= '1';

elsif (CLK'event and CLK='1' and J='1' and KL='0') then

tempD1 <= not D1;

tempD2 <= not D2;

elsif (CLK'event and CLK='1' and J='0' and KL='1') then

tempD1 <= D1;

tempD2 <= D2;

elsif (CLK'event and CLK='1' and J='1' and KL='1') then

tempD1 <= '1';

tempD2 <= '0';

else

tempD1 <= D1;

tempD2 <= D2;

end if;

elsif (PRL='0' and CLRL='1') then

tempD1 <= '1';

tempD2 <= '0';

elsif (PRL='1' and CLRL='0') then

tempD1 <= '0';

tempD2 <= '1';

else

tempD1 <= '1';

tempD2 <= '1';

end if;

end process;

D1 <= tempD1;

D2 <= tempD2;

end V1;

1. Тест цифрового устройства на языке системы ModelSim

entity TEST\_Test2 is

end;

library IEEE;

use IEEE.STD\_LOGIC\_1164.all;

architecture BENCH of TEST\_Test2 is

component lab4\_3

port (PRL, CLRL, CLK, J, KL: in STD\_LOGIC;

D1, D2 : inout STD\_LOGIC);

end component;

signal PRL, CLRL, CLK, J, KL, D1, D2: STD\_LOGIC;

begin

PRL <= '0', '0' after 100 NS, '1' after 200 NS, '1' after 300 NS, '1' after 400 NS, '1' after 500 NS, '1' after 600 NS, '1' after 700 NS, '1' after 800 NS, '1' after 900 NS, '1' after 1000 NS, '1' after 1100 NS;

CLRL <= '1', '0' after 100 NS, '0' after 200 NS, '1' after 300 NS, '1' after 400 NS, '1' after 500 NS, '1' after 600 NS, '1' after 700 NS, '1' after 800 NS, '1' after 900 NS, '1' after 1000 NS, '1' after 1100 NS;

CLK <= '1', '1' after 100 NS, '0' after 200 NS, '0' after 300 NS, '1' after 400 NS, '0' after 500 NS, '1' after 600 NS, '0' after 700 NS, '1' after 800 NS, '0' after 900 NS, '1' after 1000 NS, '0' after 1100 NS;

J <= '1', '0' after 100 NS, '1' after 200 NS, '1' after 300 NS, '0' after 400 NS, '0' after 500 NS, '1' after 600 NS, '0' after 700 NS, '0' after 800 NS, '1' after 900 NS, '1' after 1000 NS, '0' after 1100 NS;

KL <= '1', '0' after 100 NS, '1' after 200 NS, '1' after 300 NS, '0' after 400 NS, '1' after 500 NS, '0' after 600 NS, '1' after 700 NS, '1' after 800 NS, '1' after 900 NS, '1' after 1000 NS, '0' after 1100 NS;

M: lab4\_3 port map (PRL, CLRL, CLK, J, KL, D1, D2);

end BENCH;

1. Результат работы программы

