國立高雄大學資訊工程學系 計算機結構考卷

姓名： 學號：

1. (15%) Please explain the three kinds of hazards：
   A. Structural hazards
   B. Data hazards
   C. Control hazards

   - **Structural hazards: HW cannot support this combination of instructions (single person to fold and put clothes away)**
   - **Data hazards: Instruction depends on result of prior instruction still in the pipeline (missing sock)**
   - **Control hazards: Caused by delay between the fetching of instructions and decisions about changes in control flow (branches and jumps).**

2. (15%) Please describe data hazards between which two instructions.

L.D	**F0, 10(R1)**
ADD.D	**F0, F4, F6**
SUB.D	**F10, F0, F8**
MUL.D	**F2, F8, F10**
DIV.D	**F8, F2, F6**
S.D	**F2, 0(R1)**

RAW:

L.D and SUB.D
ADD.D and SUB.D
SUB.D and MUL.D
MUL.D and DIV.D
MUL.D and S.D

WAW:

L.D and ADD.D

WAR:

MUL.D and DIV.D
SUB.D and DIV.D

3. (10%) Please explain the difference between Basic Branch Prediction Buffer and Correlating Branch Predictors.

- **The previous schemes use only the recent behavior of a signal branch to predict the future behavior of the branch.**
- **Correlating Branch Predicator**
  - **Branch predictors that use the behavior of other branches to make a predication.**

4. (10%) Please explain Moore's Law and Amdahl's Law.

 # on transistors / cost-effective integrated circuit double every N months

$$\text{Speedup}_{\text{overall}} = \frac{\text{ExTime}_{\text{old}}}{\text{ExTime}_{\text{new}}} = \frac{1}{\left(1 - \text{Fraction}_{\text{enhanced}}\right) + \frac{\text{Fraction}_{\text{enhanced}}}{\text{Speedup}_{\text{enhanced}}}}$$

5. (10%) Please explain Temporal Locality and Spatial Locality.

Temporal Locality (Locality in Time): If an item is referenced, it will tend to be referenced again soon (e.g., loops, reuse)
Spatial Locality (Locality in Space): If an item is referenced, items whose addresses are close by tend to be referenced soon
(e.g., straight-line code, array access)

6. (10%) Please compare the difference between dynamic scheduling and static scheduling.
   A. With static scheduling the compiler tries to reorder these instructions during compile time to reduce pipeline stalls.
      i. Uses less hardware
      ii. Can use more powerful algorithms
   B. With dynamic scheduling the hardware tries to rearrange the instructions during run-time to reduce pipeline stalls.
      i. Simpler compiler
      ii. Handles dependencies not known at compile time
      iii. Allows code compiled for a different machine to run efficiently.

7. (12%) Assume that there are 16K bits in the Correlating Branch Prediction Buffer. Please derive the numbers of entries in (0,1), (0,2), (2,2), and (12,2) predicators.

A. (0,1): 16K entries
B. (0,2): 8K entries
C. (2,2): 2K entries
D. (12,2): 2 entry

8. (10%) Please describe the Drawbacks of Tomasulo.

(1)Many associative stores (CDB) at high speed, Performance limited by Common Data Bus
(2)Non-precise interrupts

9. (8%) In Hardware-Based Speculation design, a specific reorder buffer is needed. Please describe the purpose of the buffer as detail as possible.
   A. In Tomasulo's algorithm, once an instruction writes its result, any subsequently issued instructions will find result in the register file
   B. With speculation, the register file is not updated until the instruction commits
      i. (we know definitively that the instruction should execute)
   C. Thus, the ROB supplies operands in interval between completion of instruction execution and instruction commit
      i. ROB is a source of operands for instructions, just as reservation stations (RS) provide operands in Tomasulo's algorithm
      ii. ROB extends architectured registers like RS

10. (20%) Please write the contents of Instruction Status, Reservation Stations, and Register result status at clock cycle 15.

Instruction status:

Instruction		j	k	Issue	Exec Comp	Write Result
LD	F6	34+	R2	1	3	4
LD	F2	45+	R3	2	4	5
MULTD	F0	F2	F4	3	15	
SUBD	F8	F6	F2	4	7	8
DIVD	F10	F0	F6	5		
ADDD	F6	F8	F2	6	10	11

	Busy	Address
Load1	No	
Load2	No	
Load3	No	

Reservation Stations:

Time	Name	Busy	Op	S1 Vj	S2 Vk	RS Qj	RS Qk
	Add1	No					
	Add2	No					
	Add3	No					
0	Mult1	Yes	MULTD	M(A2)	R(F4)		
	Mult2	Yes	DIVD		M(A1)	Mult1	

Register result status:

Clock		F0	F2	F4	F6	F8	F10	F12	...	F30
15	FU	Mult1	M(A2)		(M-M+M	(M-M)	Mult2			

Note：FP multiply (10 EX cycles)、FP add (2 EX cycles)、and FP divide (40 EX cycles)、load (2 EX cycles)