資訊工程學系 計算機結構

姓名： 學號：

[Fundamentals of Computer Design] (22%)

1. (6%) What is an "Instruction Set Architecture"?

An interface between the software and hardware including

- **Memory addressing**
- **Addressing modes**
- **Instructions**
- **Types and size of operands**
- **Operations**
- **Control flow instructions**
- **Encoding an ISA**

2. (10%) Please explain Moore's Law and Amdahl's Law.

 # on transistors / cost-effective integrated circuit double every N months

$$\text{Speedup}_{\text{overall}} = \frac{\text{ExTime}_{\text{old}}}{\text{ExTime}_{\text{new}}} = \frac{1}{\left(1 - \text{Fraction}_{\text{enhanced}}\right) + \frac{\text{Fraction}_{\text{enhanced}}}{\text{Speedup}_{\text{enhanced}}}}$$

3. (6%) Please explain Temporal Locality and Spatial Locality.

Temporal Locality (Locality in Time): If an item is referenced, it will tend to be referenced again soon (e.g., loops, reuse)

Spatial Locality (Locality in Space): If an item is referenced, items whose addresses are close by tend to be referenced soon (e.g., straight-line code, array access)

[Instruction Level Parallelism and Its Exploitation] (82%)

4. (5%) Why is it very difficult to deal with dependence through memory location?

A. two addresses may refer to the same location but look different

i. 100(R4) and 20(R6)

B. or may look the same but locate different addresses.

i. 20(R4) and 20(R4)

5. (6%) There are several types of limits to the gains that can be achieved by loop unrolling. Please illustrate three types.
   - **A. Decrease in amount of overhead amortized with each extra unrolling**
   - **B. Growth in code size**
     - **i. For larger loops, concern it increases the instruction cache miss rate**
   - **C. Compiler**
   - **D. Register pressure: potential shortfall in registers created by aggressive unrolling and scheduling**

6. (6%) Please illustrate two techniques which can achieve CPI<1.

   multiple-issue

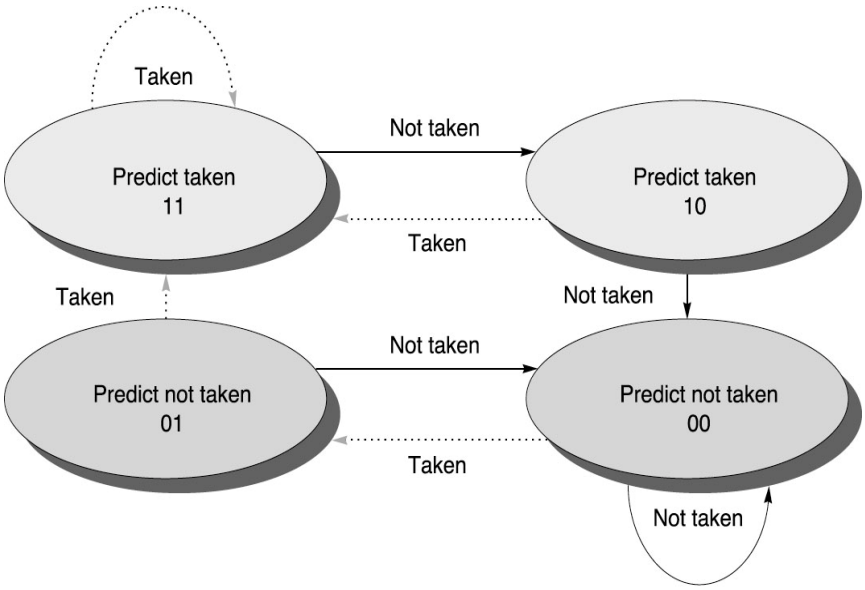
   VLIW

   superscalar

7. (5%) Please discuss 2-bit branch predictor.

   Predict incorrectly twice

   - **If (counter >= 2), predict taken, else predict not taken**
   - **Advantage: a few atypical branches will not influence the prediction (a better measure of "the common case")**



8. (6%) Please explain the difference between Basic Branch Prediction Buffer and Correlating Branch Predictors.

- **The previous schemes use only the recent behavior of a signal branch to predict the future behavior of the branch.**
- **Correlating Branch Predicator**
  - **Branch predictors that use the behavior of other branches to make a predication.**

9. (6%) How many bits are in the (0,2) branch predictor with 4K entries? How many entries are in a (2,2) predictor with the same number of bits?.

   8K bits

   1K entries

10. (5%) How can a processor with the Reorder Buffer maintain a precise exception model while dynamically execute code?

    We could simply wait until it reached the head of the ROB and take the interrupt, flushing any other pending instructions from the ROB. Because instruction commit happens in order, this yields a precise exception.

11. (8%) How can the scheme of Tomasulo's approach can minimize RAW hazard and eliminate the stalls for WAW, and WAR hazards?

    A. tracks when operands for instructions are available, to minimize RAW hazards (listen common data bus)

    B. introduces register renaming to minimize WAW and WAR hazards with reservation station and register status

12. (6%) Please illustrate three drawbacks of Tomasulo.

    Complexity

    Performance limited by Common Data Bus

    Non-precise interrupts

13. (6%) What situations does a branch-target buffer take penalties?

    A. An instruction is in the buffer and we predict taken. However, the actual branch is not taken.

    B. **The instruction is not in the buffer.**

14. (5%) What interval does the Reorder Buffer supply operands in the Speculative Tomasulo?

    Interval between *completion of instruction execution* and *instruction commit*

15. (18%) Please write the contents of Instruction Status, Reservation Stations, and Register result status at clock cycle 12.

Instruction status:

Instruction		*j*	*k*	*Issue*	*Exec Comp*	*Write Result*
LD	F6	34+	R2	1	3	4
LD	F2	45+	R3	2	4	5
MULTD	F0	F2	F4	3		
SUBD	F8	F6	F2	4	7	8
DIVD	F10	F0	F6	5		
ADDD	F6	F8	F2	6	10	11

	Busy	Address
Load1	No	
Load2	No	
Load3	No	

Reservation Stations:

Time	*Name*	*Busy*	*Op*	*S1 Vj*	*S2 Vk*	*RS Qj*	*RS Qk*
	Add1	No					
	Add2	No					
	Add3	No					
3	Mult1	Yes	MULTD	M(A2)	R(F4)		
	Mult2	Yes	DIVD		M(A1)	Mult1	

Register result status:

Clock		*F0*	*F2*	*F4*	*F6*	*F8*	*F10*	*F12*	...	*F30*
12	*FU*	Mult1					Mult2			

Note：FP multiply (10 EX cycles)、FP add (2 EX cycles)、and FP divide (40 EX cycles)、load (2 EX cycles)