Computer Architecture
Fall, 2018
Week 15
2018.12.17

[group1]

1.

Supposing: a 4-Way Set-Associative Cache with 1KB of data,4 word per block and 4bytes per word, a 32-bit address. Cache block has a dirty bit, tag bits, and data bits. What's the total bits in the cache?

Ans:

4-way, so it has 4 blocks/set

16bytes per block

2^10/2^4=2^6=64 blocks

64blocks/4 blocks/set=16 sets.

So index 4 bits, tag 24 bits, offset 4 bits

total bits: (1+24+2^4*8) *16 * 4 = 9792 bits

[group7]

2.

Give two examples that move a process(thread) from the state of running to waiting

1. I/O request (e.g:print)
2. sleep (put the process(thread) to sleep)

[group2]

3.

Referring to ShareCourse video 6-2-4 and 6-3, please choose the correct statement(s) and explain the wrong.

(a) Generally, CPU time contains two components: program execution cycles, which includes cache hit time, and memory stall cycles.

(b) For all R-type instructions, memory stall cycles are always 0.

(c) Only I-type instructions need to access I-cache.

(d) Load and store instructions need to access D-cache.

(e) Given I-cache miss rate 2%, D-cache miss rate 5%, base CPI=3. If load and store are 87% instructions. Using four-word wide bank memory organization, where transfer time isn't overlapped with (memory) cycle time. Assuming 1 memory bus clock to send the address, 15 memory bus clocks for each DRAM access initiated, 2 memory bus clock to send a 4-word data, and a cache block = 16 words. Then miss penalty = 1+4*15+4*2=69 Memory bus clock cycles.

(f) Following (e), if memory bus clock time = (CPU) cycle time then actual CPI = 3+0.02*69+0.87*0.05*69

ANS:

(a)對 r

(b)錯，R-type instruction 也要 access I-cache，如果 I-cache 的 miss rate 不為 0，則就會有 memory stall cycle。錯在 always 0.

(c)錯，every instruction needs to access I-cache.

(d)對 r

(e)對 r

(f)對 r

[group5]

4.

Suppose we use a 2-way Set-Associative Cache of 8 blocks and LRU to replacement.
Size of each block = 1 word (4 bytes) and all blocks are empty initially.
Now we want to access the memory from the following byte address sequentially.
Please determine each access is cache hit or cache miss.

-> 0x0036
-> 0x028D
-> 0x7A57
-> 0x291F
-> 0x0034
-> 0x32C5
-> 0x291C
-> 0x7A54
-> 0x0037

A2:
0x0036 -> Miss -> Allocate a block in set 01, tag = 003
0x028D -> Miss -> Allocate a block in set 11, tag = 028
0x7A57 -> Miss -> Allocate a block in set 01, tag = 7A5
0x291F -> Miss -> Allocate a block in set 11, tag = 291
0x0034 -> Hit
0x32C5 -> Miss -> Replace LRU block in set 01 (tag = 7A5) -> Allocate a block in set 01, tag = 32C
0x291C -> Hit
0x7A54 -> Miss -> Replace LRU block in set 01 (tag = 003) -> Allocate a block in set 01, tag = 7A5
0x0037 -> Miss -> Replace LRU block in set 01 (tag = 32C) -> Allocate a block in set 01, tag = 003

[group4]

5.

Given the following information, please compute how many times is Ideal CPI faster than Actual CPI?

I-cache miss rate = 1%, D-cache miss rate = 5%, Miss penalty = 50 cycles

Base CPI (ideal cache) = 2, Load & stores are 40% of instructions

A：

Miss cycles per instruction

I-cache: 0.01*50 = 0.5

D-cache: 0.4*0.05*50 = 1

Actual CPI = 2 + 0.5 + 1 = 3.5

Ideal CPI is 3.5/2 = 1.75 times faster than Actual CPI.

[group8]

6.

下列對於 Multilevel caches 敘述哪些是錯的並且說明原因(多選)?

(a) 在設計 Multilevel caches 時 我們在 primary cache 時主要會盡量降低 miss rate

(b) Level 2 的 block size 通常比 primary cache 的 block size 來的大

(c) Multilevel caches 可以增加 cache 的 performance

(d) 在設計 Multilevel caches 時 在 level 2 我們主要會盡量降低 hit time

Ans: A, D

A. 在設計 Multilevel caches 時 我們在 primary cache 時主要會盡量降低 hit time

D. 在設計 Multilevel caches 時 在 level 2 我們主要會盡量降低 miss rate

[group10]

7.

State at least two reasons why we need virtual memory and elaborate your answer.

Ans:

1. allow a single user program to exceed the size of primary memory.
2. allow efficient and safe sharing of memory among multiple programs.

當程式的 address space 大於 RAM 的 address space 的時候，如果沒有利用 virtual memory 則可能造成 crash.而利用 virtual memory 則可以將部分資料存放到 disk 裡，需要的時候再經由 address mapping 找回。而且 virtual memory 可以經由 address mapping 有效的保護資料不被不同程式經由讀取相同地址汙染，不只如此，如果要更有效率地運用儲存空間，可以將 mapping 改為指向同一個 RAM 地址，以達到不同程式共同存取相同地址的目的。

[group11]

8.

The Average Memory Access Time equation (AMAT) has three components: hit time, miss rate, and miss penalty. For each of the following cache optimizations, indicate which component of the AMAT equation is improved.

- Using a second-level cache
- Using a direct-mapped cache
- Using a 4-way set-associative cache

1.Using a second-level cache improves miss rate

2.Using a direct-mapped cache improves hit time

3. Using a 4-way set-associative cache improves miss rate

[group12]

9.

Find the AMAT (average memory access time) for a processor with a 2 ns clock cycle time, a miss penalty of 30 clock cycles, a miss rate of 0.02 misses per instruction, and a cache access time (including hit detection) of 2 clock cycles. Assume that the read and write miss penalties are the same and ignore other write stalls.

Ans.

AMAT=2+0.02*30 = 2.6 clock cycles or 5.2 ns