**計算機結構**

**小考1(Snooping)**

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(70 pnts) A write-back cache use the write-invalidate cache coherence protocol. In the snooping protocol, the cache controller must maintain the state transition for each cache block. Besides, we assume that the memory addresses X1 and X2 are in different memory blocks and map to the same cache block. Their initial values are 0. The initial stat of each cache block is Invalid. (cache block狀態請用所寫I、S、E)



Please describe

* 1. the stat change of each corresponding cache block (X🡪Y)
  2. the values of X1 and X2 in the memory and cache (X1=? X2=?)
  3. what message is placed in the bus
     1. P0 reads X1 (10 pnts)

In P0, cache block: I🡪S X1=0 read miss

Memory block: X1=0

* + 1. P1 reads X1 (10 pnts)

In P0, cache block: S🡪S X1=0

In P1, cache block: I🡪S X1=0 read miss

Memory block: X1=1

* + 1. P2 writes 1 to X1 (15 pnts)

In P0, cache block: S🡪I

In P1, cache block: S🡪I

In P2, cache block: I🡪E X1=1 write miss

Memory block: X1=0

* + 1. P0 reads X1 (15 pnts)

In P0, cache block: I🡪S X1=1 read miss

In P2, cache block: E🡪S X1=1 write back the dirty block, abort the memory access

Memory block: X1=1

* + 1. P2 writes 2 to X2 (10pnts)

In P2, cache block: S🡪E X2=2 write miss

Memory block: X2=0

* + 1. P0 writes 3 to X1 (10 pnts)

In P0, cache block: S🡪E X1=3 invalidate

Memory block: X1=1