**計算機結構 隨堂練習**

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(70 pnts) A write-back cache use the write-invalidate cache coherence protocol. In the directory protocol, the cache controller must maintain the state transitions for each cache block and each memory block. Besides, we assume that the memory addresses X1 and X2 are in different memory blocks on the processor P2 and map to the same cache block. Their initial values are 0. The initial stats of each cache block and each memory block are Invalid an Uncached. (cache block狀態請用所寫I、S、E。memory block狀態請用U、S、E )



Please describe

* 1. the stat change of each corresponding cache block and memory bock
  2. the sharer set for the memory block
  3. the values of X1 and X2 in the memory and cache
  4. what message is placed in the bus

When the following requests are issued under the directory protocol. (Hint: home node, local node, and remote node)

* + 1. P0 reads X1 (10 pnts)

In P0, cache block: Invalid🡪Shared X1=0 read miss

In P2, X1 memory block: Uncahed🡪Shared Sharer={P0} X1=0 Data value reply

* + 1. P1 reads X1 (10 pnts)

In P1, cache block: Invalid🡪Shared X1=0 read miss

In P2, X1 memory block: Shared🡪Shared Sharer={P0,P1} X1=0 Data value reply

* + 1. P0 writes 1 to X1 (15 pnts)

In P0, cache block: Shared🡪 Exclusive X1=1 Invalidation

In P1, cache block: Shared🡪Invalid

In P2, X1 memory block: Shared🡪Exclusive Sharer={P0} X1=0 Invalidation

* + 1. P1 read X1 (15 pnts)

In P1, cache block: Invalid🡪 Shared X1=1 read miss

In P0, cache block: Exclusive🡪 Shared X1=1

In P2, X1 memory block: Exclusive🡪 Shared Sharer={P0,P1} X1=1 Fetch, Data value reply

* + 1. P1 writes 1 to X2 (20pnts)

In P1, cache block: Shared🡪Exclusive X2=1 write miss

n P0, cache block: Shared X1=1

In P2, X1 memory block: Shared Sharer={P0} X1=1,

X2 memory block: Uncached🡪Exclusive Sharer={P1} X2=0