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SAML10-QT8 Low Power

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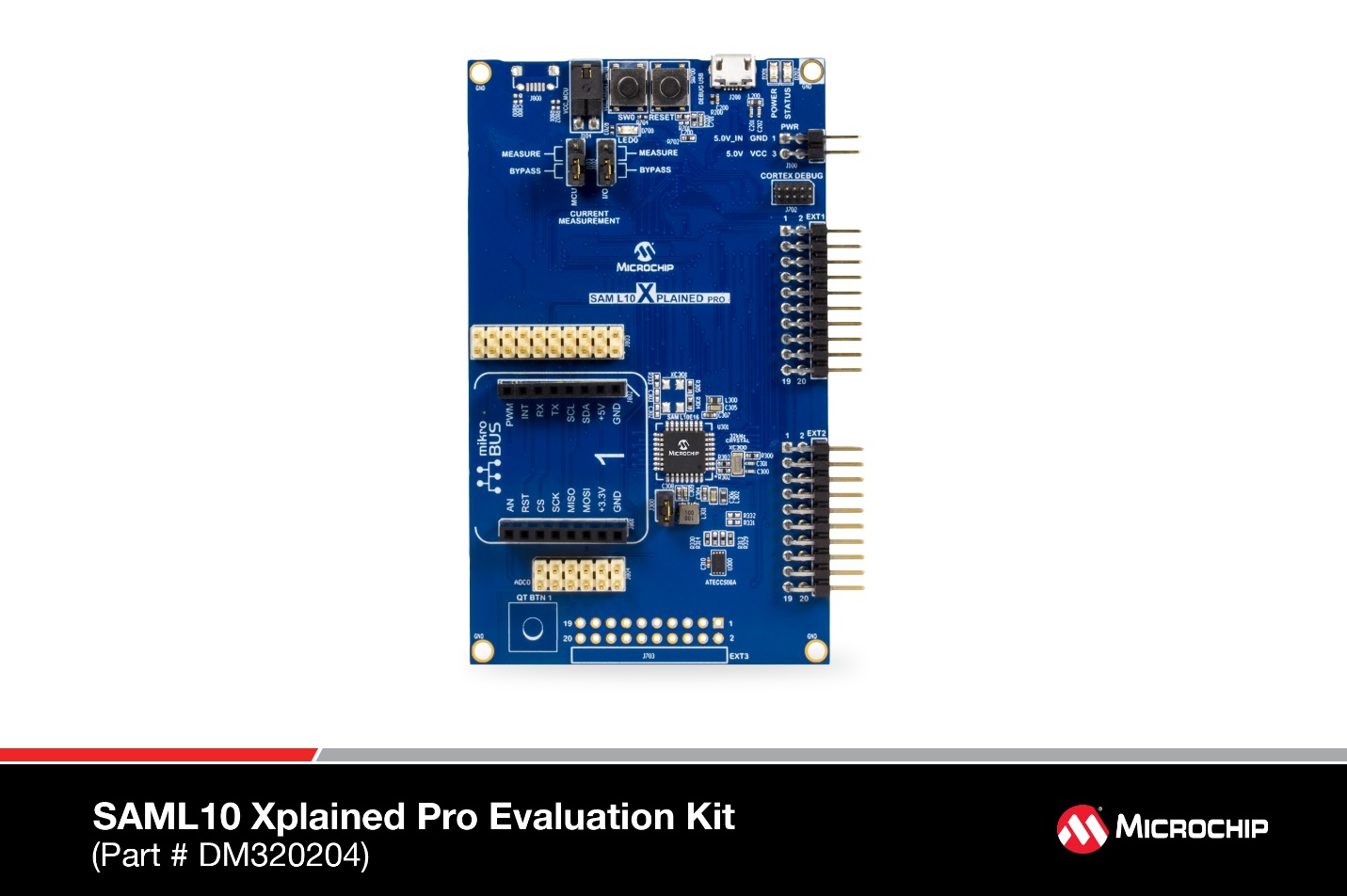
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ATSAML10 XPRO using QT8 2D Sensor Board

# Hardware

## [SAML10 XPRO](https://www.microchip.com/DevelopmentTools/ProductDetails/dm320204)



## [QT8 XPRO Eval Kit](https://www.microchip.com/DevelopmentTools/ProductDetails/PartNO/AC164161)

Machine generated alternative text:

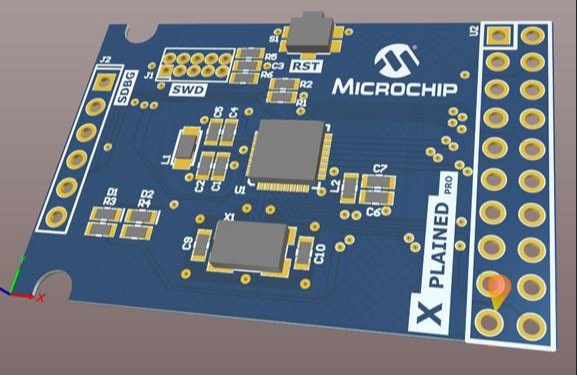


## System Block Diagram

Machine generated alternative text:



Custom Cap Controller Board



# SAML10 Low Power Single Button Demo

Hardware: SAML10 XPRO

Running: QTouch-SAML10-XPro-Low-power-Touch-Project from START

Sensor: on XPRO

Using as a reference for lowest possible power consumption of SAML10

## Active Mode Performance @ 3.3Vdc:

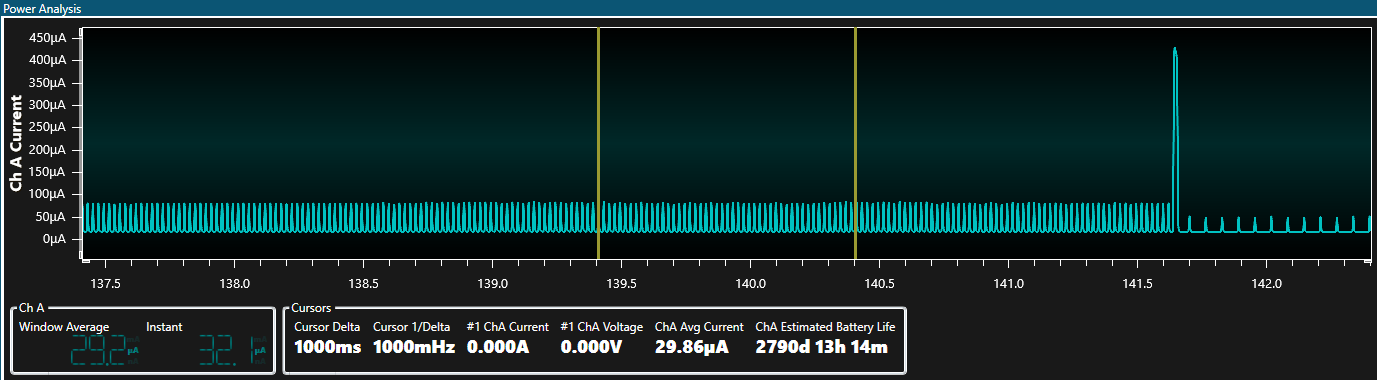
16MHz Internal OSC, 32.768kHz LPINTOSC

No serial debug enabled

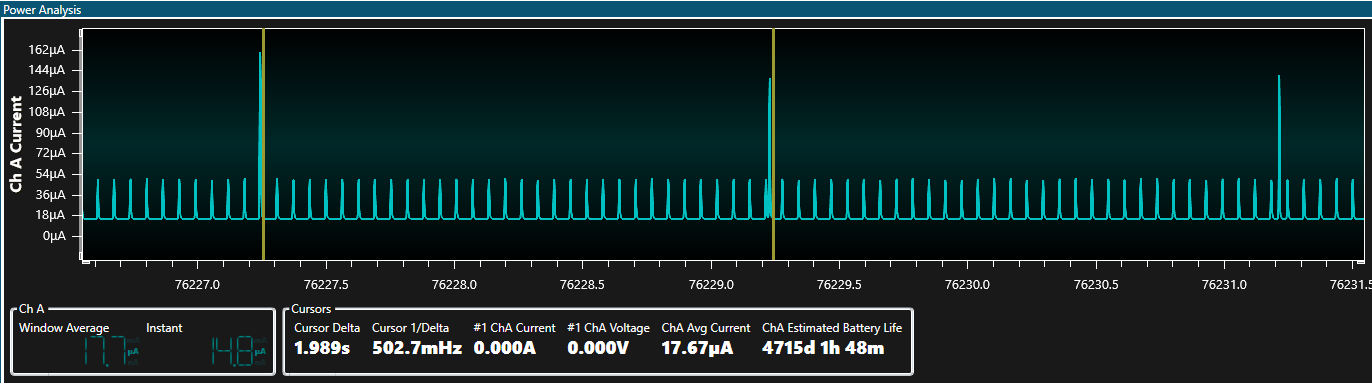
Using SAML10 XPRO

CPU @ 16MHz (GCLK DIVSEL = 1)

Avg Active Current: 29.86uA

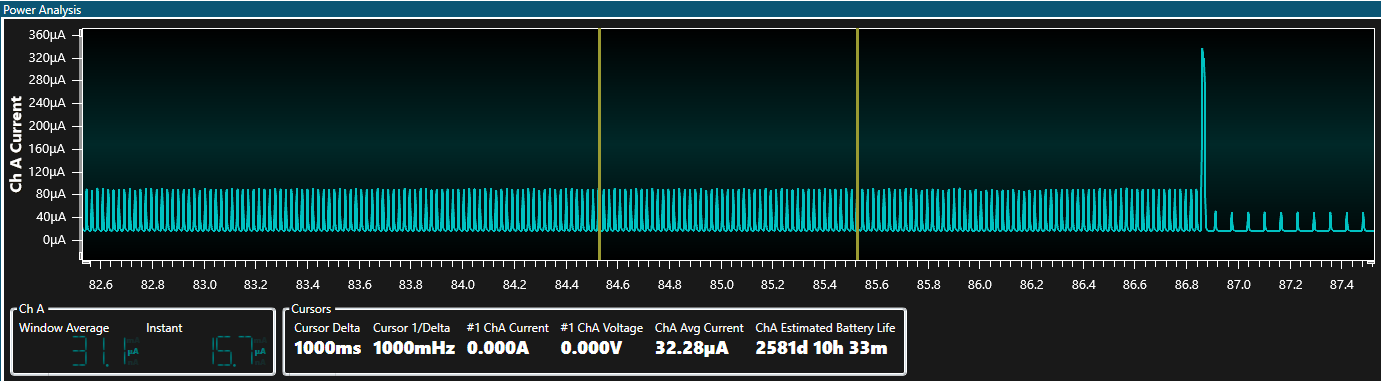


Avg Sleep Current: 17.7uA



CPU @ 8MHz (GCLK DIVSEL = 2)

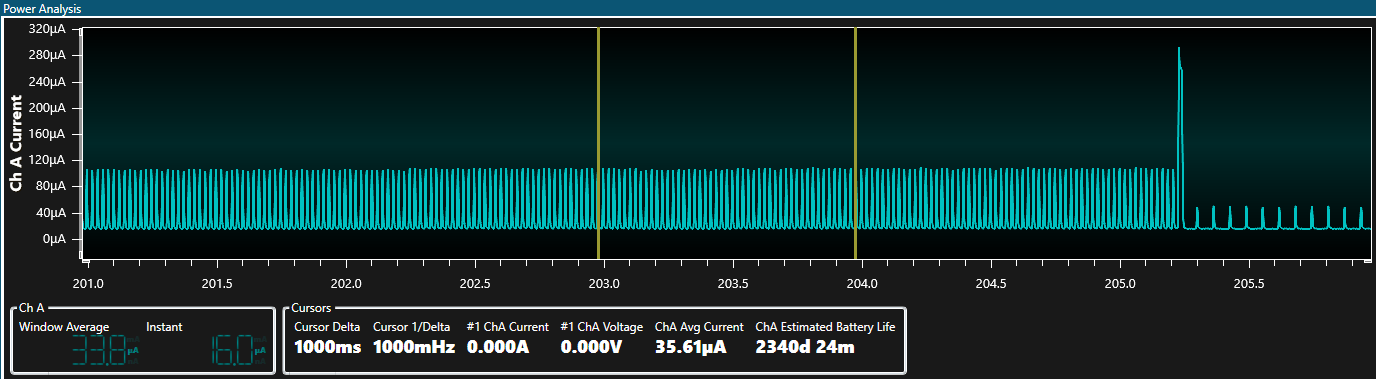
Avg Active Current:



Avg Sleep Current: unchanged due to turning off POSC

CPU @ 4MHz (GCLK DIVSEL = 4)

Avg Active Current: 35.61uA



Avg Sleep Current: unchanged due to turning off POSC

## Active Mode Performance @ 1.8Vdc:

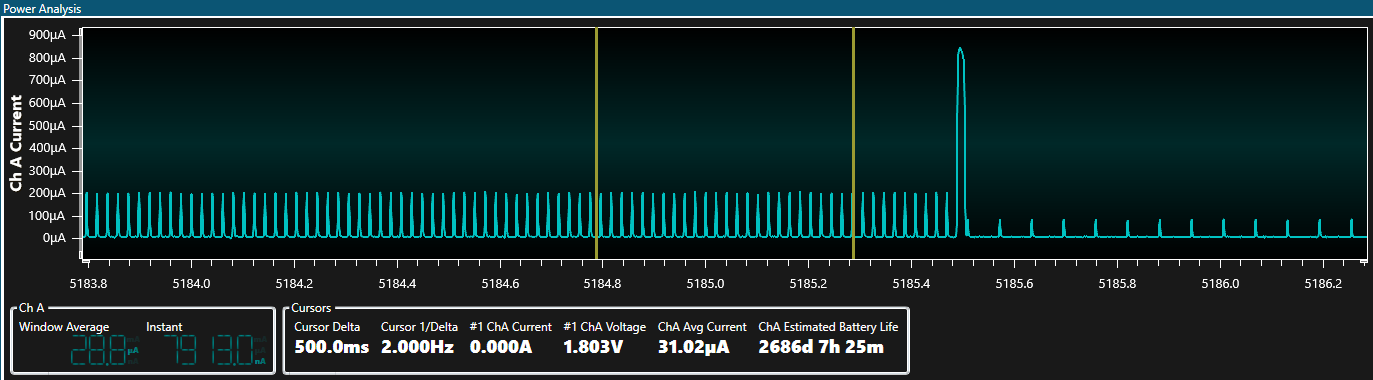
16MHz Internal OSC, 32.768kHz LPINTOSC

No serial debug enabled

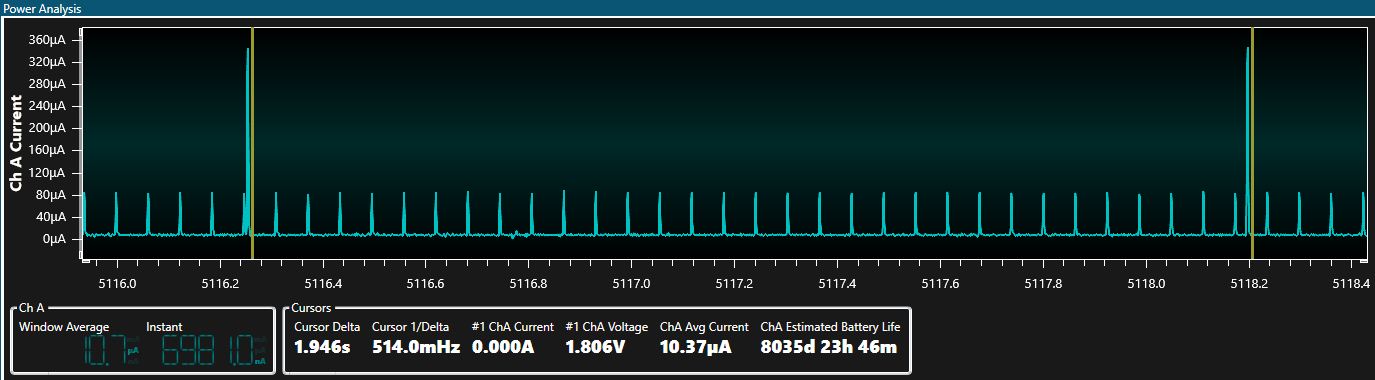
Using custom SAML10 cap controller board

CPU @16MHz (GCLK DIVSEL = 1)

Avg Active Current: 31.02uA

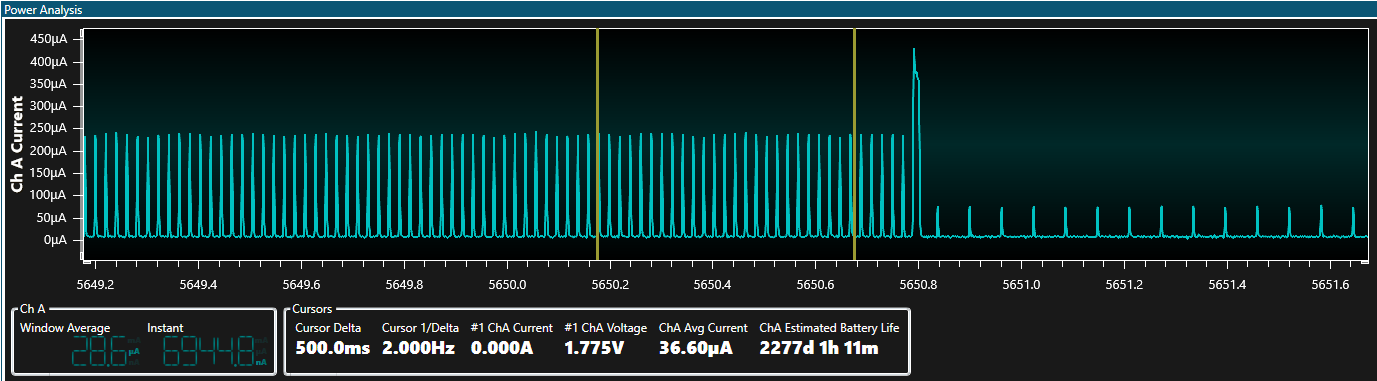


Avg Sleep Current: 10.37uA



CPU @ 4MHz (GCLK DIVSEL = 4)

Avg Active Current: 36.6uA



# SAML10 Low Power 2D demo

Hardware: SAML10 XPRO and QT8

Running: 2D Touchpad demo w/ low power enabled

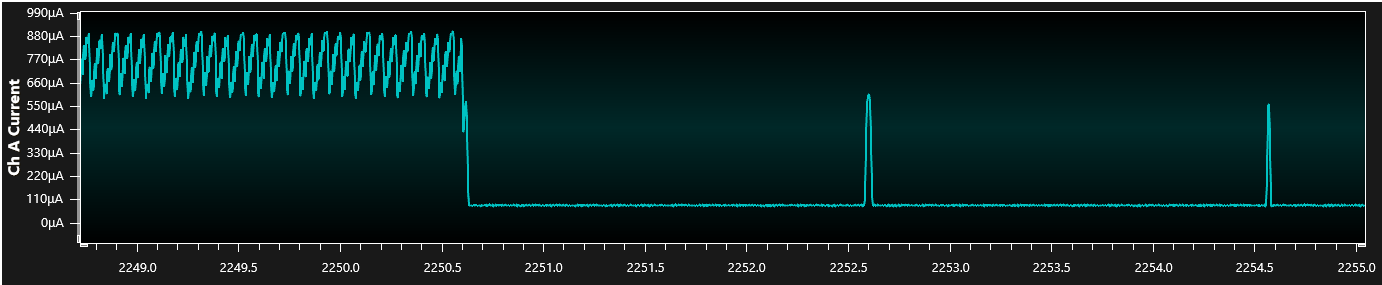
Git: <https://bitbucket.microchip.com/scm/~c13999/saml10_qt8_lowpower.git>

Sensor: 5x5 diamond pattern sensor array

## Power Modes

Active mode – Continuous scanning, decoding, and reference calibration.

Sleep Mode – After period of inactivity, enters sleep mode. Sleep mode auto scans all sensor nodes for touch while sleeping. Will periodically wake up CPU to update reference calibration for all nodes to compensate for environmental changes. Lump mode not currently implemented.



**QTM\_AUTOSCAN\_TRIGGER\_PERIOD** – defines auto scan trigger period, auto scan rate while in sleep

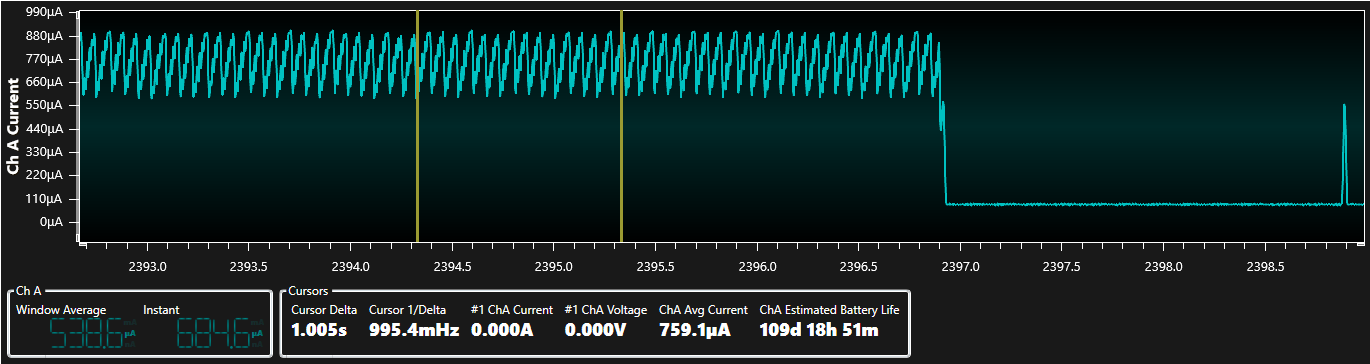
**DEF\_TOUCH\_DRIFT\_PERIOD\_MS** – defines drift measurement period, frequency to wake and recalibrate reference values

## Active Mode Performance @ 3.3Vdc

16MHz Internal OSC, 32.768kHz LPINTOSC

No serial debug enabled

Avg Current: 759.1uA



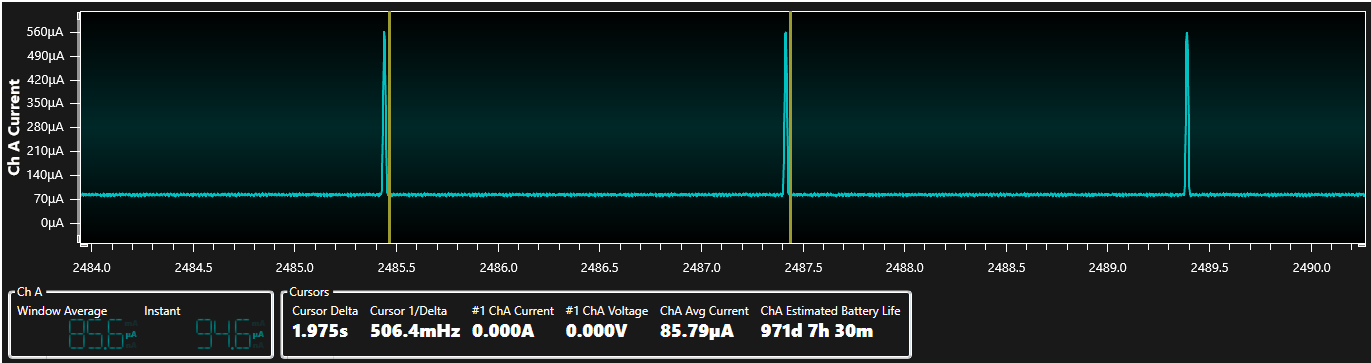
## Low Power Performance

Drift calibration set at 2 seconds

Comms disabled

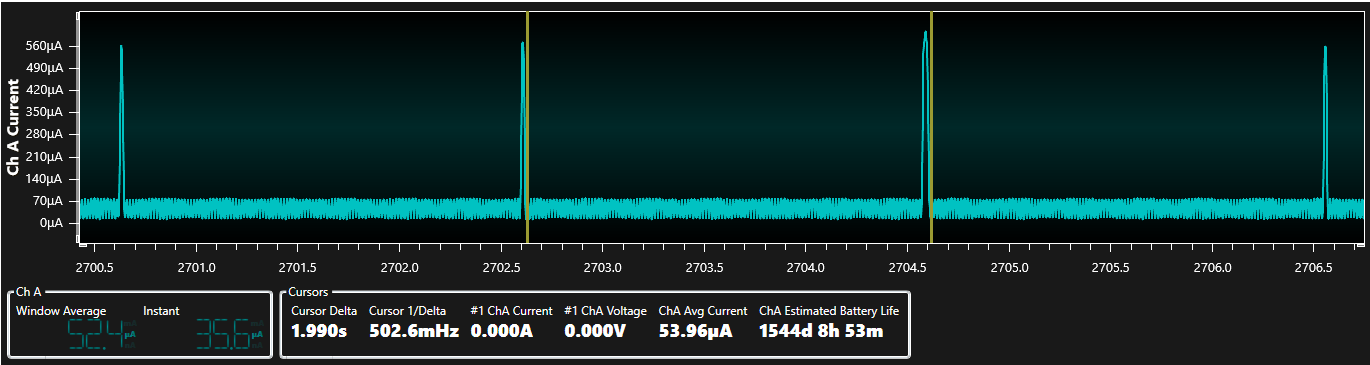
#define QTM\_AUTOSCAN\_TRIGGER\_PERIOD NODE\_SCAN\_8MS

Avg current: 86uA



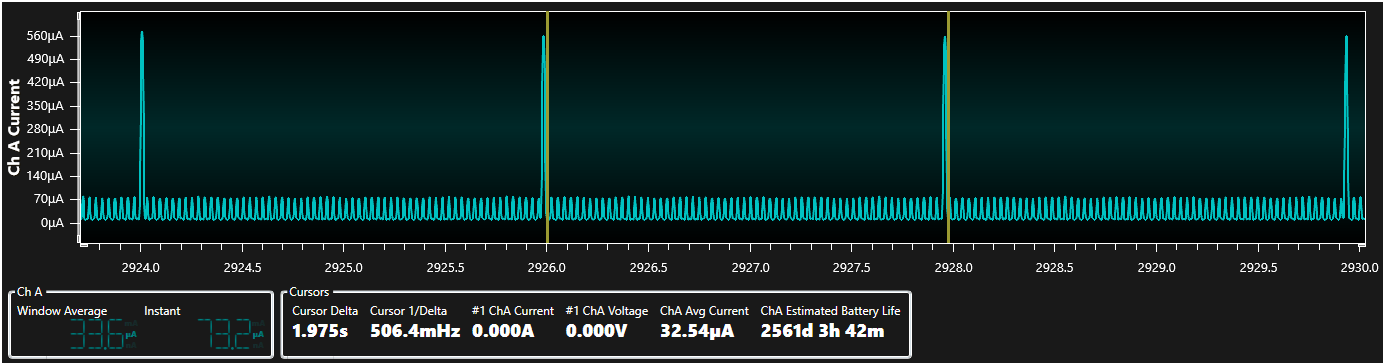
#define QTM\_AUTOSCAN\_TRIGGER\_PERIOD NODE\_SCAN\_16MS

Avg current: ~54uA



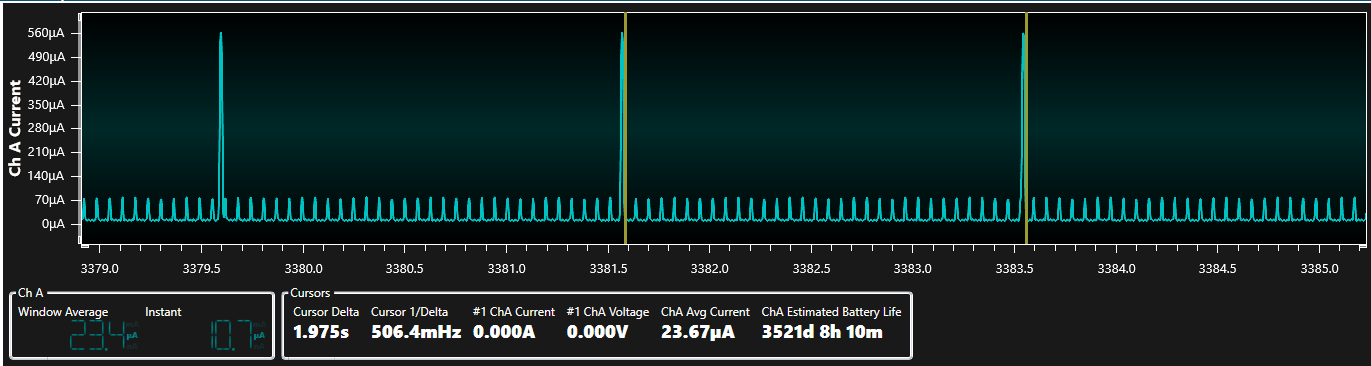
#define QTM\_AUTOSCAN\_TRIGGER\_PERIOD NODE\_SCAN\_32MS

Avg current: ~32.5uA



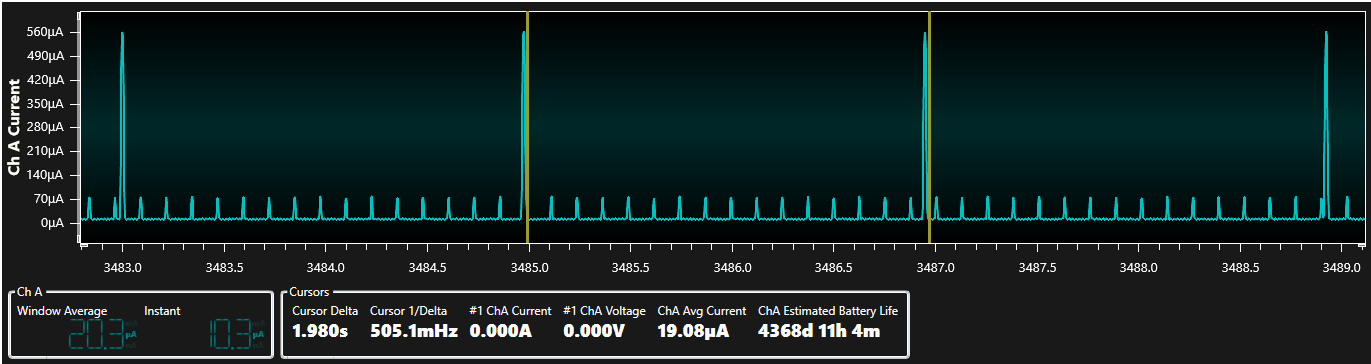
#define QTM\_AUTOSCAN\_TRIGGER\_PERIOD NODE\_SCAN\_64MS

Avg current: ~23.7uA



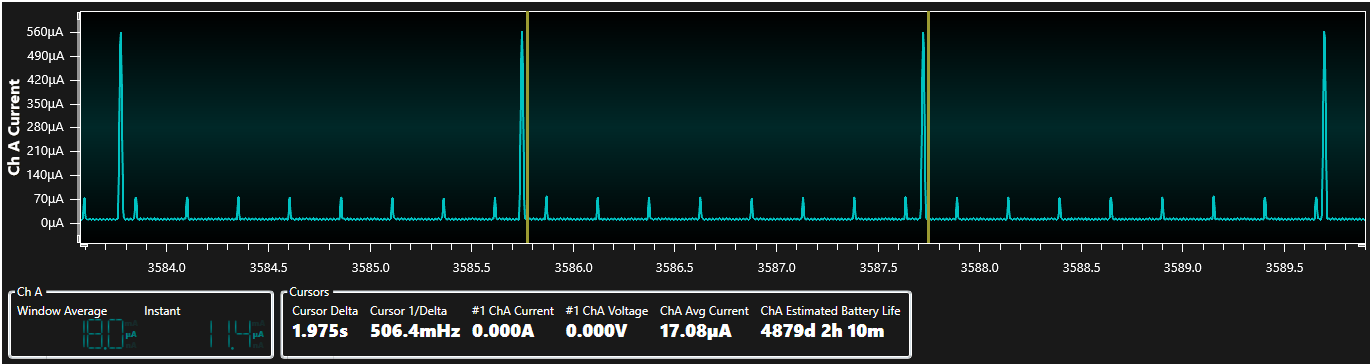
#define QTM\_AUTOSCAN\_TRIGGER\_PERIOD NODE\_SCAN\_128MS

Avg current: ~19uA



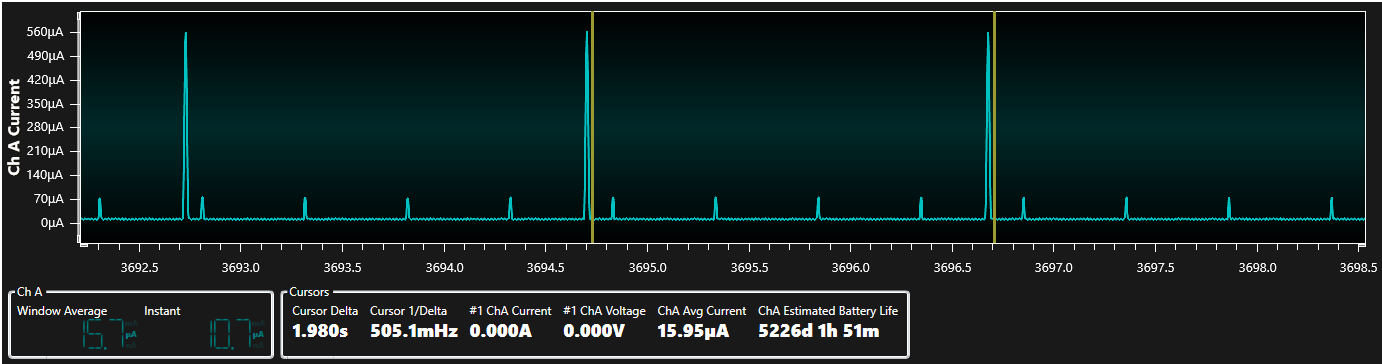
#define QTM\_AUTOSCAN\_TRIGGER\_PERIOD NODE\_SCAN\_256MS

Avg current: ~17uA



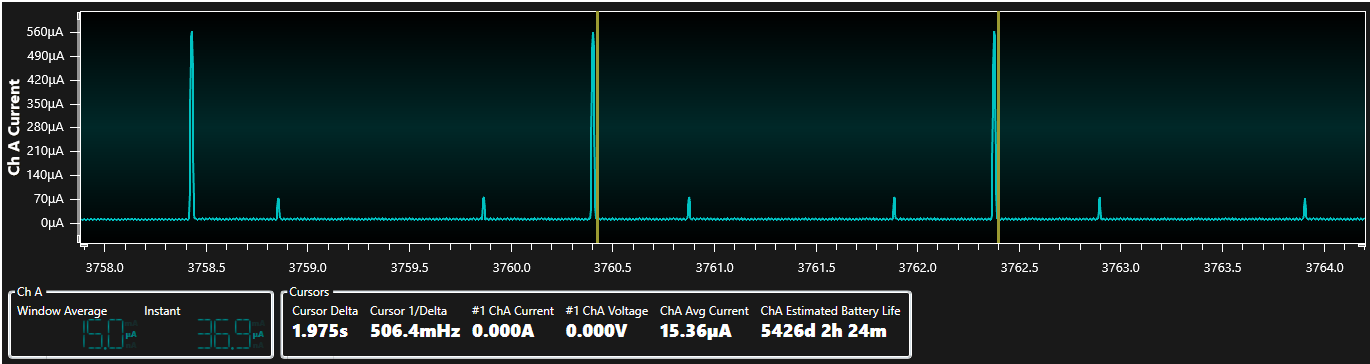
#define QTM\_AUTOSCAN\_TRIGGER\_PERIOD NODE\_SCAN\_512MS

Avg current: ~16uA



#define QTM\_AUTOSCAN\_TRIGGER\_PERIOD NODE\_SCAN\_1024MS

Avg current: ~15.3uA



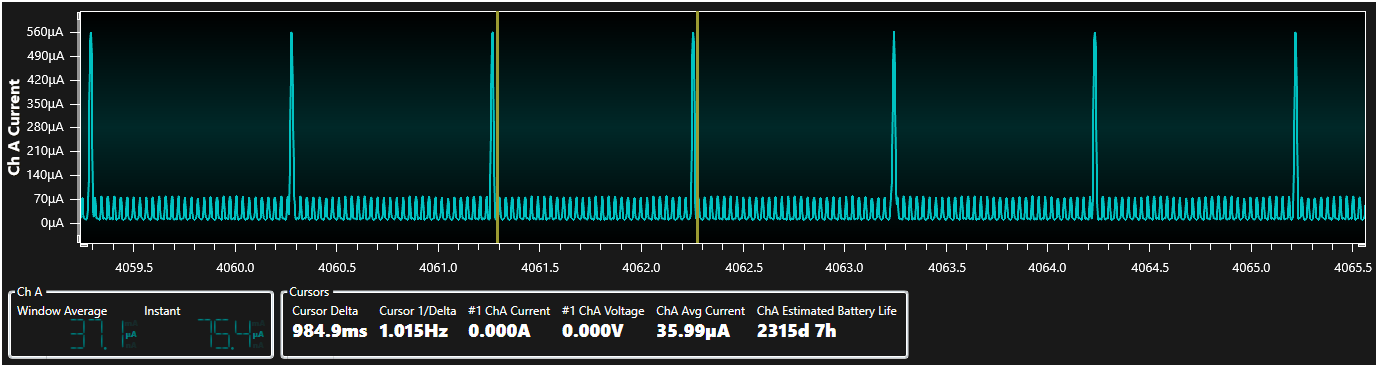
## Lower Power by increasing drift calibration time

All charts taken using:

#define QTM\_AUTOSCAN\_TRIGGER\_PERIOD NODE\_SCAN\_32MS

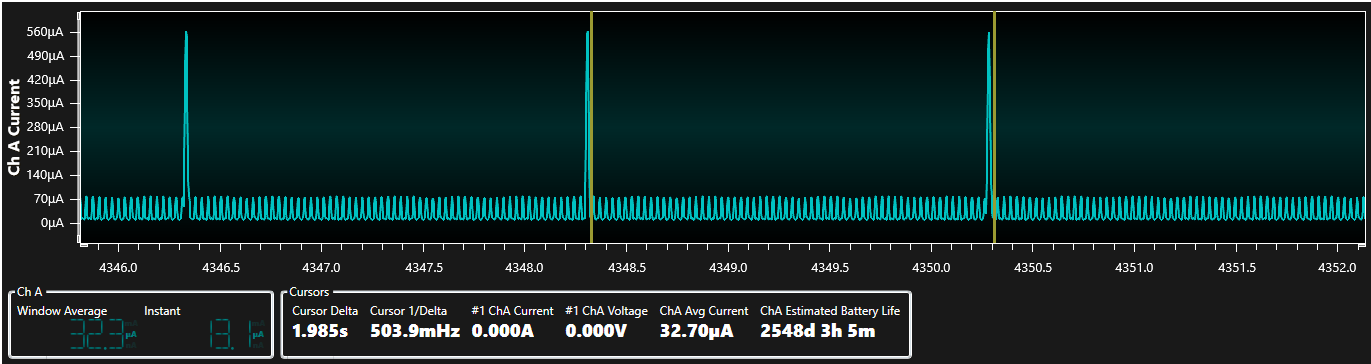
#define DEF\_TOUCH\_DRIFT\_PERIOD\_MS 1000

Avg current: ~36uA



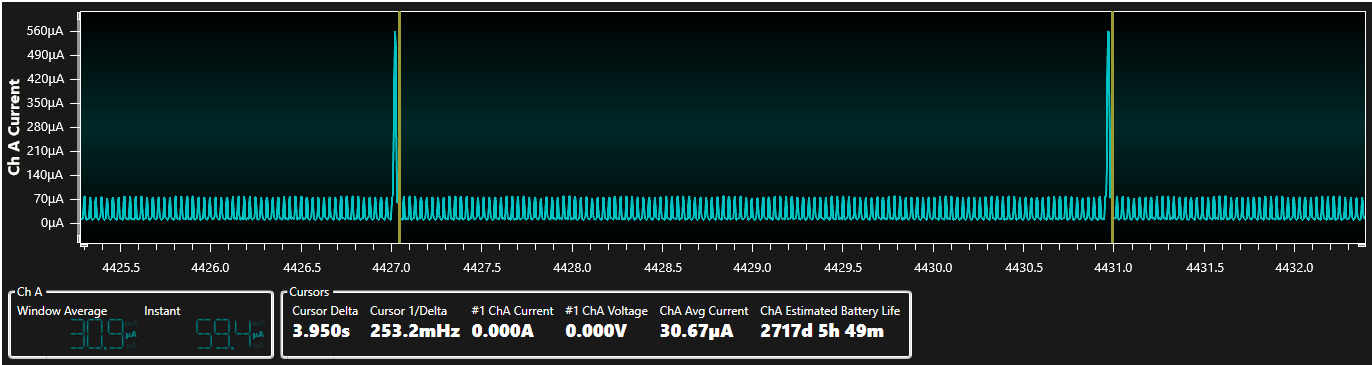
#define DEF\_TOUCH\_DRIFT\_PERIOD\_MS 2000

Avg current: ~32.7uA



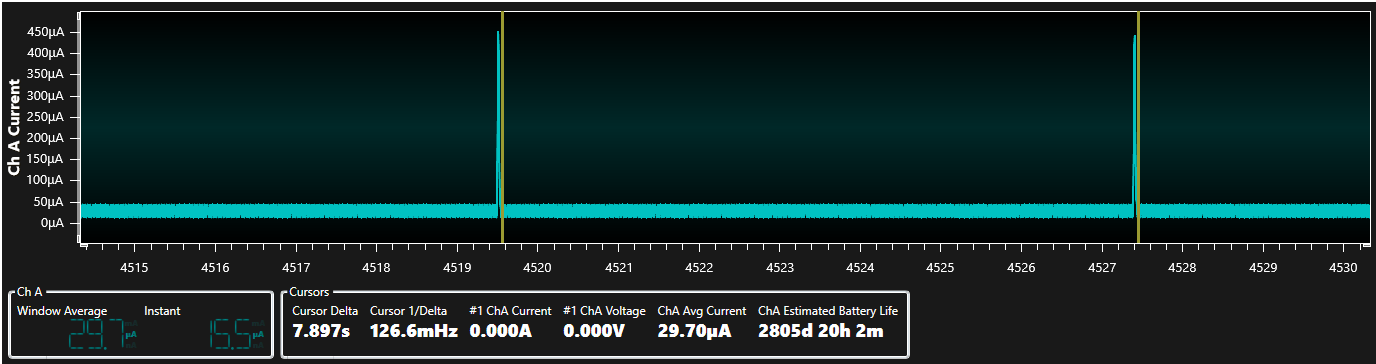
#define DEF\_TOUCH\_DRIFT\_PERIOD\_MS 4000

Avg current: ~30.7uA



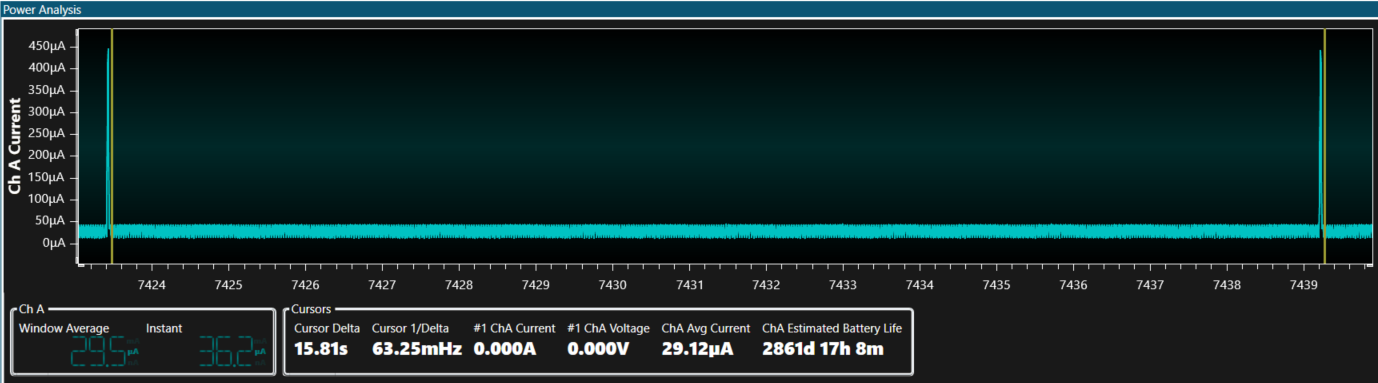
#define DEF\_TOUCH\_DRIFT\_PERIOD\_MS 8000

Avg current: ~29.7uA



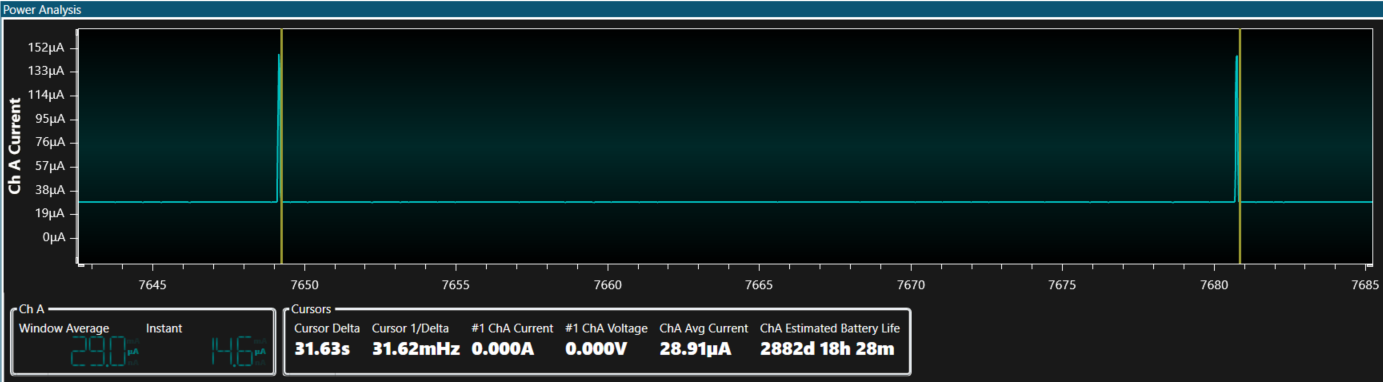
#define DEF\_TOUCH\_DRIFT\_PERIOD\_MS 16000

Avg current: ~29.12uA



#define DEF\_TOUCH\_DRIFT\_PERIOD\_MS 32000

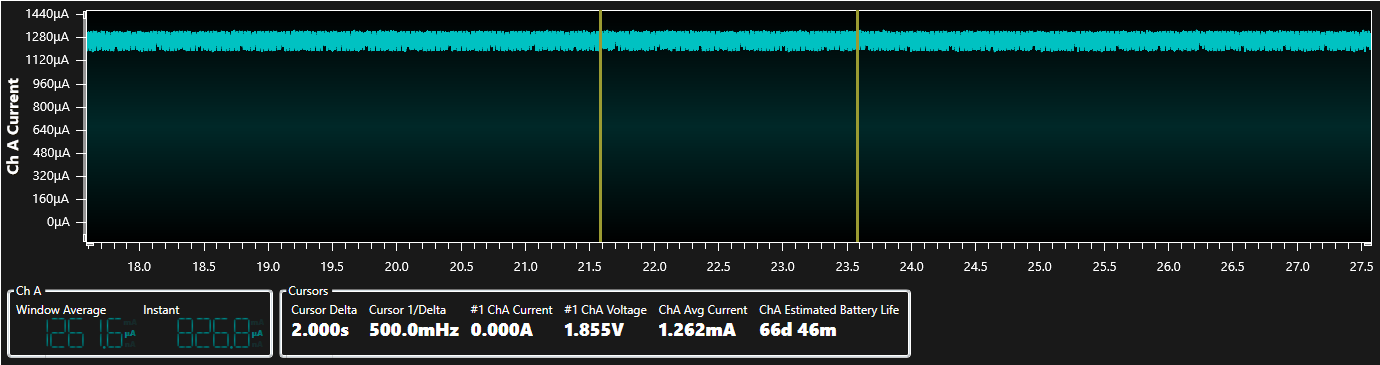
Avg current: ~28.91uA



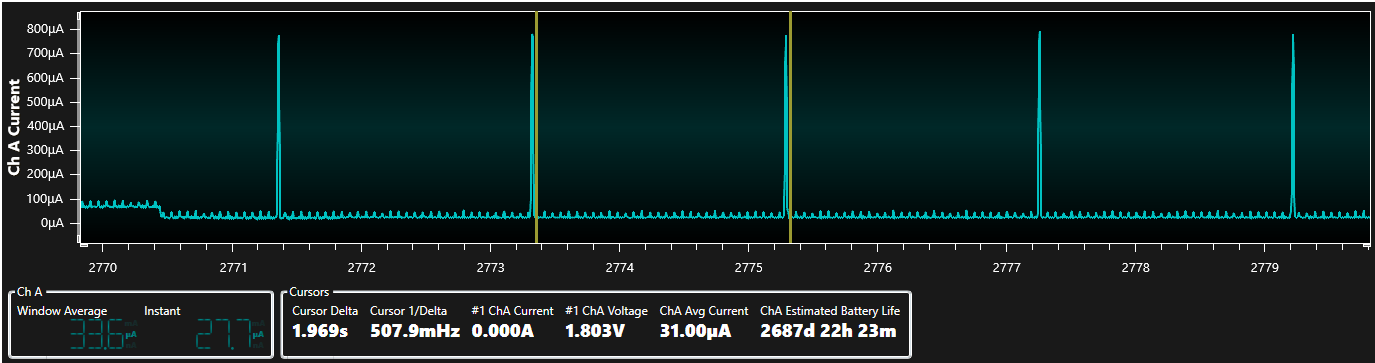
# SAML10 + QT8 1D Sensors w/ low power

Buttons FW – can use START code generator to change clocks

1.8Vdc

16MHz, no sleep

16MHz, sleep, 64mS auto scan



# SAM L10 Family Features

* Operating Conditions: 1.62V to 3.63V, -40ºC to +125ºC, DC to 32 MHz
* Core: 32 MHz (2.64 CoreMark/MHz and up to 31 DMIPS) Arm® Cortex®-M23 with:
  + Single-cycle hardware multiplier
  + Hardware divider
  + Nested Vector Interrupt Controller (NVIC)
  + Memory Protection Unit (MPU)
  + Stack Limit Checking
  + TrustZone® for ARMv8-M (optional)
* System
  + Power-on Reset (POR) and programmable Brown-out Detection (BOD)
  + 8-channel Direct Memory Access Controller (DMAC)
  + 8-channel event system for Inter-peripheral Core-independent Operation
  + CRC-32 generator
* Memory
  + 64/32/16 KB Flash
  + 16/8/4 KB SRAM
  + 2 KB Data Flash Write-While-Read (WWR) section for non-volatile data storage
  + 256 bytes TrustRAM with physical protection features
* Clock Management
  + Flexible clock distribution optimized for low power
  + 32.768 kHz crystal oscillator
  + 32.768 kHz ultra low-power internal RC oscillator
  + 0.4 to 32 MHz crystal oscillator
  + 16/12/8/4 MHz low-power internal RC oscillator
  + Ultra low-power digital Frequency-Locked Loop (DFLLULP)
  + 32-96 MHz fractional digital Phase-Locked Loop (FDPLL96M)
  + One frequency meter
* Low-Power and Power Management
  + Active, Idle, Standby with partial or full SRAM retention and off sleep modes:
    - Active mode (< 25 μA/MHz)
    - Idle mode (< 10 μA/MHz) with 1.5 μs wake-up time
    - Standby with Full SRAM Retention (0.5 μA) with 5.3 μs wake-up time
    - Off mode (< 100 nA)
  + Static and dynamic power gating architecture
  + Sleepwalking peripherals
  + Two performance levels
  + Embedded Buck/LDO regulator with on-the-fly selection
* Advanced Analog and Touch
  + One 12-bit 1 Msps Analog-to-Digital Converter (ADC) with up to 10 channels
  + Two Analog Comparators (AC) with window compare function
  + One 10-bit 350 kSPS Digital-to-Analog Converter (DAC) with external and internal outputs
  + Three Operational Amplifiers (OPAMP)
  + One enhanced Peripheral Touch Controller (PTC):
    - Up to 20 self-capacitance channels
    - Up to 100 (10 x 10) mutual-capacitance channels
    - Low-power, high-sensitivity, environmentally robust capacitive touch buttons, sliders, and wheels
    - Hardware noise filtering and noise signal desynchronization for high conducted immunity
    - Driven Shield Plus for better noise immunity and moisture tolerance
    - Parallel Acquisition through Polarity control
    - Supports wake-up on touch from Standby Sleep mode
* Packaging
  + 24-pin VQFN – 4x4mm, .85mm tall
  + 32-pin VQFN – 5x5mm, .85mm tall