# Computer Organization Lab 4 - Pipelined CPU

教授:蔡文錦

助教:劉益先、鄭吉呈、黃芷柔、林彧頎

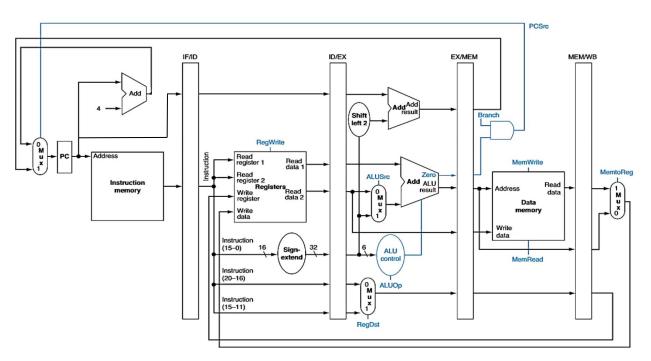
# **Objectives**

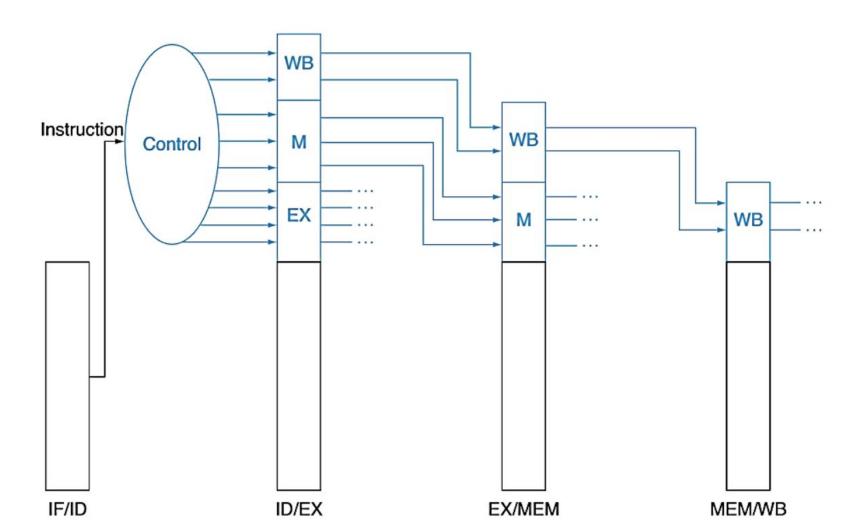
In this lab, you are going to implement a **Pipelined CPU** with memory unit, which can run **R-type** and **I-type** instructions.

- To realize how to set the control signal in different instruction type.
- To learn how to follow the datapath to form a pipelined CPU

### **Overview**

The following diagram is the datapath of pipelined CPU.





### **Attached Files**

#### TO DO

- Adder.v
- ALU\_Ctrl.v
- ALU.v
- Decoder.v
- MUX\_2to1.v
- o Pipe\_CPU.v
- Shift\_Left\_Two\_32.v
- Sign\_Extend.v

#### DO NOT modify

- Data\_Memory.v
- Instruction\_Memory.v
- Pipe\_Reg.v
- ProgramCounter.v
- Reg\_File.v

- For validation DO NOT modify
  - testbench.v
- Testcase YOU CAN modify the instructions in it.
  - \*.txt

### **Instruction Set**

You are going to implement these instructions:

- **R-type:** add, sub, AND, OR, NOR, slt
- I-type: lw, sw, beq, bne, addi

#### **Instruction Format:**

R-type:	ор	rs	rt	rd	shamt	funct
	6 bits	5 bits	5 bits	5 bits	5 bits	6 bits
I-type:	ор	rs	rt	constant or address		
	6 bits	5 bits	5 bits	16 bits		

## **Instruction Set**

R-type						
Function	Op Field	Function Field				
add	6'b000000	6'b100011				
sub	6'b000000	6'b100001				
AND	6'b000000	6'b100110				
OR	6'b000000	6'b100101				
NOR	6'b000000	6'b101011				
slt	6'b000000	6'b101000				

I-type				
Function	Op Field			
addi	6b'001001			
lw	6b'101100			
sw	6b'100100			
beq	6b'000110			
bne	6b'000101			

# Compile & Run

- Compile
  - \$ iverilog -o lab4 testbench.v

- Run
  - \$./lab4
  - (windows)\$ vvp lab4

#### Wrong results:

#### **Correct results:**

# **Grading Policy**

- There are 3 hidden cases with serial several instructions, and you will get
  33 points for each correct testcase, with an additional point for submitting, totally 100 points.
- Any assignment work by fraud will get a zero point!
- No late submission!

### **Submission**

- Please attach student IDs as comments at the top of each TO DO file.
- The files you should hand in include:
  - all \*.v files excluding testbench.v
- Compress all file \*.v into one zip file without any extra folder layer, and make sure do not add unnecessary files or folders (like .DS Store, MACOSX).
- Name your zip file as HW4\_{studentID}.zip
  - o e.g.
    - HW4\_123456789.zip
      - {\*.v}
- Wrong format will have 20% penalty!
- Deadline: 8/18 23:55