Computer Organization
# Lab 5 - Advanced Pipelined CPU

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Objectives

In this lab, you are going to modify your lab 4 **Pipelined CPU** design, and implement **hazard detection** and **data forwarding**.

- Your design needs to forward data if instructions have data dependency.
- Your design needs to stall pipelined CPU if it detects a load-use.

Overview

The next page's diagram is the datapath of advanced pipelined CPU.
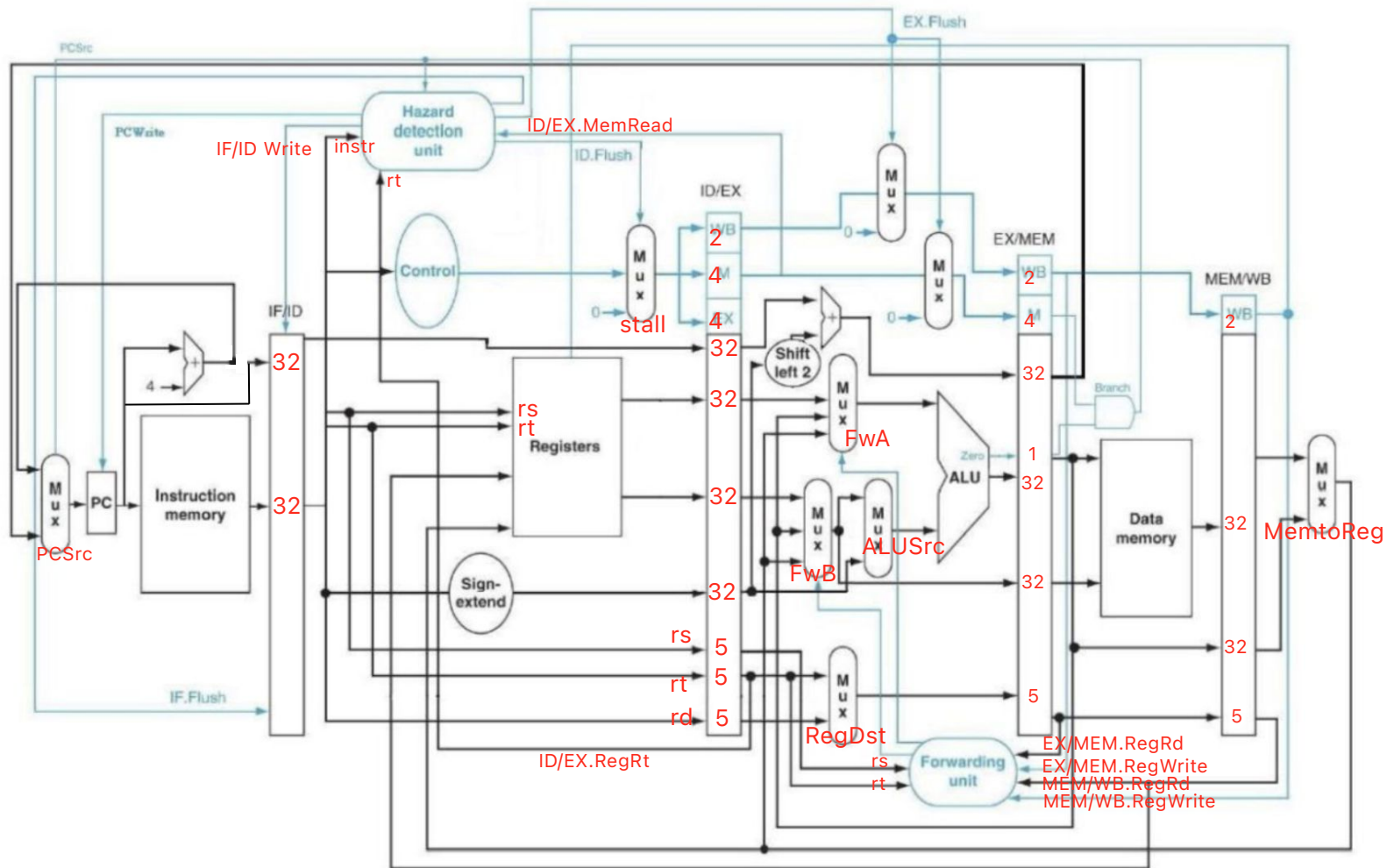
Attached Files

- **TO DO**
  - Adder.v
  - ALU_Ctrl.v
  - ALU.v
  - Decoder.v
  - MUX_2to1.v, MUX_3to1.v
  - Pipe_CPU_Pro.v
  - Shift_Left_Two_32.v
  - Sign_Extend.v
  - Forwarding_Unit.v
  - Hazard_Detection.v

- **DO NOT modify**
  - Data_Memory.v
  - Instruction_Memory.v
  - Pipe_Reg.v
  - ProgramCounter.v
  - Reg_File.v

- **For validation - DO NOT modify**
  - testbench.v

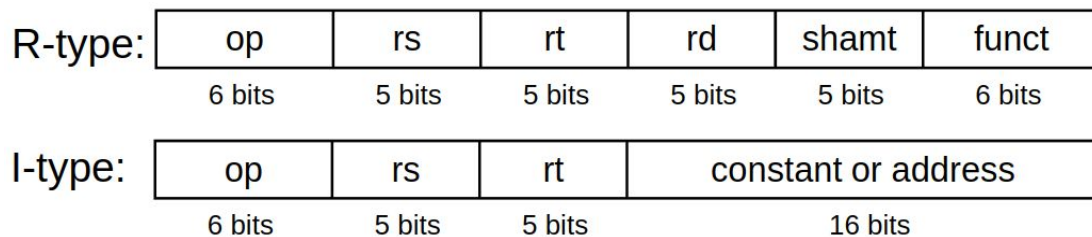- **Testcase** - **YOU CAN modify the instructions in it.**
  - *.txt

Instruction Set

You are going to implement these instructions :

- **R-type :** add, sub, AND, OR, NOR, slt
- **I-type :** lw, sw, beq, bne, addi

Instruction Format:

R-type:	op	rs	rt	rd	shamt	funct
	6 bits	5 bits	5 bits	5 bits	5 bits	6 bits

I-type:	op	rs	rt	constant or address
	6 bits	5 bits	5 bits	16 bits

Instruction Set

R-type		
Function	**Op Field**	**Function Field**
add	6'b000000	6'b100011
sub	6'b000000	6'b100001
AND	6'b000000	6'b100110
OR	6'b000000	6'b100101
NOR	6'b000000	6'b101011
slt	6'b000000	6'b101000

I-type	
Function	**Op Field**
addi	6b'001001
lw	6b'101100
sw	6b'100100
beq	6b'000110
bne	6b'000101

Compile & Run

- **Compile**
  - $ iverilog -o lab5 testbench.v

- **Run**
  - $ ./lab5
  - (windows)$ vvp lab5

Wrong results:

```
********************************************************
* Register Error! [Register 31]                        *
* Correct result: 00000050                             *
* Your result:    00000000                             *
********************************************************
********************************************************
*              You have 19 error !                     *
********************************************************
```

Correct results:

```
********************************************************
*              Congratulation. ALL PASS !              *
********************************************************
```

Grading Policy

- There are **3 little hidden cases with serial several instructions**, and you will get **33** points for each correct testcase, with a bonus point awarded this semester for your hard work, totally **100** points.

- **Any assignment work by fraud will get a zero point！**

- **No late submissiion！**

Submission

- **Please attach student IDs as comments at the top of each TO DO file.**
- The files you should hand in include:
  - **all *.v files excluding testbench.v**
- Compress all file ***.v** into one zip file **without any extra folder layer**, and **make sure do not add unnecessary files or folders** (like .DS_Store, __MACOSX).
- Name your zip file as **HW5_{studentID}.zip**
  - **e.g.**
    - **HW5_123456789.zip**
      - **{*.v}**
- **Wrong format will have 20% penalty！**
- **Deadline: 8/23 23:55**