2023-1 Computer Architecture Homework #4

Due: 6/22 (Thu) 11:59 p.m.

5.5 [60] For a direct-mapped cache design with a 32-bit address, the following
bits of the address are used to access the cache.

Tag	Index	Offset
31-10	9-5	4-0

5.5.1 [10] <§5.3> What is the cache block size (in words)?

5.5.2 [10] <§5.3> How many entries does the cache have?

Beginning from power on, the following byte-addressed cache references are recorded.

Address (decimal number)											
0	4	16	132	232	160	1024	30	140	3100	180	2180

5.5.3 [20] <§5.3> For each reference, list (1) its tag, index, and offset, (2) whether it is a hit or a miss, and (3) which bytes were replaced (if any).

5.5.4 [20] <§5.3> List the final state of the cache, with each valid entry represented as a record of <index, tag, data>.

5.10 [60] In this exercise, we will look at the different ways capacity affects overall performance. In general, cache access time is proportional to capacity. Assume that main memory accesses take 70 ns and that memory accesses are 36% of all instructions. The following table shows data for L1 caches attached to each of two processors, P1 and P2.

	L1 Size	L1 Miss Rate	L1 Hit Time
P1	2KB	8.0%	0.66ns
P2	4KB	6.0%	0.90ns

5.10.1 [10] <§5.4> Assuming that the L1 hit time determines the cycle times for P1 and P2, what are their respective clock rates?

5.10.2 [10] <§5.4> What is the Average Memory Access Time for P1 and P2?

5.10.3 [10] <§5.4> Assuming a base CPI of 1.0 without any memory stalls, what is the total CPI for P1 and P2? Which processor is faster? (When we say a "base CPI of 1.0", we mean that instructions complete in one cycle, unless either the instruction access or the data access causes a cache miss.)

For the next three problems, we will consider the addition of an L2 cache to P1 to presumably make up for its limited L1 cache capacity. Use the L1 cache capacities and hit times from the previous table when solving these problems. The L2 miss rate indicated is its local miss rate.

L2 Size	L2 Miss Rate	L2 Hit Time
1MB	95%	5.62ns

5.10.4 [10] <§5.4> What is the AMAT for P1 with the addition of an L2 cache? Is the AMAT better or worse with the L2 cache?

5.10.5 [10] <§5.4> Assuming a base CPI of 1.0 without any memory stalls, what is the total CPI for P1 with the addition of an L2 cache?

5.10.6 [10] <§5.4> What would the L2 miss rate need to be in order for P1 with an L2 cache to be faster than P1 without an L2 cache?