2018/12/10 유경호

5.5

tag : 22 bits index : 5 bits block offset : 5

5.5.1 Cache data size = $2^{10}$ byte $2^{10} / (\#\text{of blocks}) \cdot (4\text{bytes} = 1\text{word}) = 2^5 \cdot 2^2 = 2^3$ words 8 words

5.5.2 direct mapped ⇒ 1 entry for block(set) 32

5.5.3 addr 0 - 1. tag = 0 index = 0 offset = 0 상관x 표현함
2. miss (compulsory miss)
3. X

addr 4 - 1. tag = 0 index = 0 offset = 4
2. hit
3. X

addr 16 - 1. tag = 0 index = 0 offset = 16
2. hit
3. X

addr 132 - 1. tag = 0 index = 4 offset = 4
2. miss
3. X

$32 \overline{)132}$ 4, 128, 4

addr 232 - 1. tag = 0 index = 7 offset = 8
2. miss
3. X

$32 \overline{)232}$ 7, 224, 8

addr 160 - 1. tag = 0 index = 5 offset = 0
2. miss
3. X

addr 1024 - 1. tag = 1 index = 0 offset = 0
2. miss
3. replace bytes 0 ~ 31 in block 0

addr 30 - 1. tag = 0 index = 0 offset = 30
2. hit
3. X

addr 140 - 1. tag = 0 index = 4 offset = 12
2. hit
3. X

addr 3100 - 1. tag = 3 index = 0 offset = 6
2. miss
3. replace bytes 0~31 in block index 0

addr 160 - 1. tag = 0 index = 5 offset = 20
2. hit
3. X

addr 2160 - 1. tag = 2 index = 4 offset = 4
2. miss
3. replace bytes 128~159 in block index 4.
block size 32 byte.

5.5.4

procedure

| index | tag | data |
|---|---|---|
| 0 | 0 | mem[0-31] |
| 0 | 0 | hit |
| 0 | 0 | hit |
| 4 | 0 | mem[4·32 - 4·32+31] = mem[128-159] |
| 7 | 0 | mem[7·32 - 7·32+31] = mem[224-255] |
| 5 | 0 | mem[5·32 - 5·32+31] = mem[160-191] |
| 0 | 1 | mem[0-31] replace |
| 0 | 0 | hit |
| 4 | 0 | hit |
| 0 | 3 | mem[0-31] replace |
| 5 | 0 | hit |
| 4 | 2 | mem[128-159] replace |

| final state | index | tag | data |
|---|---|---|---|
| | 0 | 3 | mem[0-31] |
| | 4 | 2 | mem[128-159] |
| | 5 | 0 | mem[160-191] |
| | 7 | 0 | mem[224-255] |

5.10

| | L1 size | L1 miss rate | L1 hit time |
|---|---|---|---|
| P1 | 2Kb | 8.0% | 0.66ns |
| P2 | 4Kb | 6.0% | 0.90ns |

hit time determines cycle time
→ 0.66ns = 1 cycle

5.10.1 $1/0.66ns = \frac{100}{66ns}$ 66/198 / 34 P1 - 1.5 GHz

$1/0.90ns = \frac{10}{9ns}$ P2 - 1.1GHz

5.10.2 AMAT = hit time + miss rate × miss penalty (cycles)

cycle 소수점 올림

P1 - hit cycle 1 + 0.08 × $\lceil \frac{70}{0.66} \rceil$ (107) cycles = 9.56cycles per cycle 9.56×0.66ns = 6.31 ns

P2 - 1 + 0.06 × $\lceil \frac{70}{0.9} \rceil$ (78) cycles = 5.68cycles 5.68×0.9ns = 5.11 ns

5.10.3 total CPI : base CPI + I cache + D cache

P1 CPI = $1 + 0.08 \times \lceil \frac{70}{0.66} \rceil + 0.36 \times 0.08 \times \lceil \frac{70}{0.66} \rceil$ = 12.64 cycles

P2 CPI = $1 + 0.06 \times \lceil \frac{70}{0.9} \rceil + 0.36 \times 0.06 \times \lceil \frac{70}{0.9} \rceil$ = 7.36 cycles

P2 is faster

61,65

5.10.4 AMAT of P1 L1+L2

$\underbrace{1}_{\text{base cpi of L1}} + 0.08 \left( \underbrace{\lceil \frac{5.62}{0.66} \rceil}_{\text{L2 cpi}} + 0.95 \times \lceil \frac{70}{0.66} \rceil \right)$

$(\frac{0.66}{0.66})$ = 9.85ns

L1 → 0.08 → L2 → 0.95 → main memory

5.10.5 $9.85 \times 0.36 \times 0.08 \times \left(9 + \frac{95}{100} \times 107\right)$

= 31.38

5.10.6

P1 : 0.66 + 0.08 × 70 = 6.26ns

P1 with L2 : 0.66 + 0.08 (5.62 + M · 70) = 0.66 + 0.4496 + 5.6M

= 1.1096 + 5.6M

5.6M < 6.26 − 1.1096

M < 0.9

M < 9%