```
4.7 | Men / Dmen Regista Site Mux ALU
                                                                                                                                                                                                                 20181210 市安豆
                                                                                                                                                                       Adder
                                             25°PS 180PS 25PS 180PS 140PS
                                          Single grade Register Pand Rigister setup Sign extend Control
                                                                              3005
                                              5ps
                                                                                                                 30 ps
                                                                                                                                                      60ps
                                                             adder artiol (read)
                                                                                                                                                                                          sgate + mux
     4.7.1
                                      Register read + 1 mem + register file + mux + ALV + mux + reg setup
                                               30 250
                                                                                                                             150 25 180 25
                                     Lateray of R type: 690 ps
                                                                                        Control
                                                                                                                                                        sgate + mux
                                                                                            sign extend
    4.7.2
                                     Register read + I man + reg Sile + MUX + ALU + Dmom + mux + reg setup
                                               30 250 150 25 180 250 25 30
                                    Latercy of lw: 940 ps antol adder sign entor
                                                                                                sign extend
                                   Register read + / man + rig Sile + MUX + ALU + Dmem
   4.7.3
                                                        250 150 25 160 250
                                 Lating of sw : 885 ps
                                                                                                                                adder
                                                                                             Control
                                                                                                                      state + Mux
                                                                                            sign extend
 4.7.4
                                Ry road + I man + rey file + mux + ALU + 5 gite + mux + reg setup
                                        30 250 150 25 180 5 25 30
                               Latery of log: 695 ps
                            Adder sign ended sign ended to sign ended to
4.7.5
                           Lateray of state i type: 690 ps
1.7.6
```

Minimum clock period (critical path): 940 ps

```
4,6
              R type
                         1 type /w
                                           beg
               25%
                         27/. 25/ 11/. 12/.
   4.8.1
            lw + SW
                        3 6%
   4.8.2
                          100%
  4.6.3 Hype + (w+sw+ber 75%.
  4.8.4
           old CPU: 940 ps
           new CPU: 0.25×690 + 0.27×690 + 0.25×940 + 0.11×885 + 0.12×695 = 774,55ps
                        21 % faster
              10
          IF
                       EX
                                     WB
  4.16
                                MEM
          250 ps 350 ps 150 ps
                               400/8
                                      200 PS
          ALV/Logic Jump/Proveh
                               Lood
                                     Nore
           45%
                               25%
                     15%
                                     15%.
  4.16.1
          pipelined: 400ps non-pipelined: 1350ps
94,16.2
          piplined: 5×400=2000PS non-pipelined: 1350PS
4.16.3
          MEM stage max (IF, ID, EX, MEM, WB) = 350 ps
```

94.16.4

leg write = 1 when ramot, /w

45+25 = 70%

4.25.1

LOOP:

(w \$50, 0(\$53))

(w \$51, 4(\$53))

NOP

NOP

Add \$52, \$50, \$51

Sw \$52, 0(\$54))

addi \$53, \$53, -8

NOP

addi \$54 \$54, 4

bnez \$52, Loop

EX MEM - WB 10 MEM- WB IP ID EX 10 EX MEM WB 10 MEM 303 10 EX A IF 160 0 10 1F 50, 51 10 EX-MEM WB 0(\$54) EX 10 MEY WB EX MEY WB addi: IF 10 NOD IF addi

4.25.2

LOOP:

No \$50,0(\$13)

No \$51,4(\$53)

addi \$53,\$53,-6

addi \$52,\$50,\$51

addi \$52,\$50,\$51

addi \$54,\$54,4

NOP

Sw \$52,0(\$60)

bnez \$52, LOOP

lus IF ID EX MEM 图图 lw MB 10 EX MEM rews3 1F -1D addi EX MEM MB 60 MEM TUB oddi 17 10 ξX 52 addi 10 11 MEM 国图 now 54 odal 18 10 EX MEM . 0 0 to, 52 IF

EX MEM, WB IF 11 \$50,0(\$53) lw \$51, 4(\$53) 1w 18 10 MEM WB EX NOP 0 O0 0 0 \$52, \$50, \$51 add IF 41D EX MEM WB SW \$32, O(\$54) here IF > here MEM WB addi \$53, \$53, -8 EX 10 EX MEM WB addi \$54, \$54, 4 11) EX MEM WB IF bnez \$52 , LOOP IF 110 EX MEM WB /w \$50,0(\$53) IF 10 EX MEMI WB /w \$51, 4(\$,3) 1F 11) EX h MEM WB NOP \bigcirc \bigcirc add \$52,\$50,\$51 1F 41D EX MEM WB here Sw \$52, o(\$54) IF ID EX MEM WB addi \$53, \$53, -8 IF ID EX MEM WB addi \$54, \$54, 4 IF 10 EX MEIN WB bnez \$52, LOOP IF

10

EX

MEM WB