Començat el	diumenge, 17 d'octubre 2021, 11:50
Estat	Acabat
Completat el	diumenge, 17 d'octubre 2021, 11:53
Temps emprat	3 minuts 25 segons
Qualificació	**6,00** sobre 6,00 (**100**%)

Pregunta **1**

Correcte

Puntuació 1,00 sobre 1,00

Assuming a UMA system with two processors, sharing the access to 8 GB of main memory. Coherence is implemented with snooping write-invalidate MSI.

Assuming initially empty caches, let's consider the following sequence of memory accesses to the same memory address w0, r0, w0, r1, r0, w1, w0, r1 (being rx a read access by processor x and wx a write acces by processor x). In order to answer the following questions we suggest you do a table showing the CPU event (PrRd or PrWr), bus transaction (BusRd, BusRdX, BusUpgr or Flush) and cache line status (M, S or I) for each processor.

Is it true that all accesses to memory in the previous list always imply a bus transaction placed on the bus by the corresponding snoopy?

Trieu-ne una:

Respostes

- Vertader
- Fals ✔

Well done! there are three accesses by processor 0 (the two r0 accesses and second w0 access) that do no place any bus transaction.

Pregunta **2**

Correcte

Puntuació 5,00 sobre 5,00

Fil in the empty spaces in the following two sentences:

The previous sequence of memory accesses implies

2

✔ BusRd,

2

✔ BusRdX,

1

✔ BusUpgr, and

3

✔ Flush commands. In total

2

✔ cache line invalidations are performed.

◄ UMA coherence quizz (1)

Salta a...

Video lesson 5 (part 1): why directory-based coherence? ►