Començat el	diumenge, 17 d'octubre 2021, 11:41
Estat	Acabat
Completat el	diumenge, 17 d'octubre 2021, 11:49
Temps emprat	8 minuts 30 segons
Qualificació	**10,00** sobre 10,00 (**100**%)

Pregunta **1**

Correcte

Puntuació 1,00 sobre 1,00

In a UMA (Uniform Memory Access time) multiprocessor, there are two or more identical processors connected to a single shared main memory through an interconnection network; this network allows any processor to access any memory location.

Which of the following statements are true?

In a UMA system, processors access to shared memory using instructions that are different from those used to access local memory (i.e. cache).

Trieu-ne una:

Respostes

- Vertader
- Fals ✔

Well done!

Pregunta **2**

Correcte

Puntuació 1,00 sobre 1,00

In a UMA system with private (local) caches, the time to access main memory on a miss is independent of which processor is doing the access and which memory address is being accessed.

Trieu-ne una:

Respostes

- Vertader ✔
- Fals

Well done!

Pregunta **3**

Correcte

Puntuació 1,00 sobre 1,00

In a UMA system with private (local) caches, the coherence protocol guarantees that for each line in main memory there can only exist a single copy of the line in one of the private cache memories of the system, independently of the number of processors available.

Trieu-ne una:

Respostes

- Vertader
- Fals ✔

Well done!

Pregunta **4**

Correcte

Puntuació 1,00 sobre 1,00

In a UMA system with private (local) caches, a write-update coherence policy ensures that all copies in private caches of a memory line are updated.

Trieu-ne una:

Respostes

- Vertader ✔
- Fals

Well done! A write-update coherence policy updates all the copies of the line in private caches (and main memory too).

Pregunta **5**

Correcte

Puntuació 1,00 sobre 1,00

In a UMA system with private (local) caches and write-update coherence, the access to a memory address previously accessed by the same processor always results in a cache hit, unless the cache replacement algorithm decided to replace the line that contains that address.

Trieu-ne una:

Respostes

- Vertader ✔
- Fals

Well done!

Pregunta **6**

Correcte

Puntuació 1,00 sobre 1,00

In a UMA system with write-invalidate MSI, the BusRdX invalidation command is generated on the bus every time a processor performs PrWr on a valid line in its cache memory.

Trieu-ne una:

Respostes

- Vertader
- Fals ✔

Well done!

Pregunta **7**

Correcte

Puntuació 1,00 sobre 1,00

In a UMA system with write-invalidate MSI, when a processor performs a PrRd followed by a PrWr to an address residing in an uncached (or invalid) memory line, the associated snoopy needs to place two coherence commands on the bus, even when no other cores have accessed the memory location in between.

Trieu-ne una:

Respostes

- Vertader ✔
- Fals

Well done! This is one of the inefficiencies solved by the more advanced protocols (MESI).

Pregunta **8**

Correcte

Puntuació 1,00 sobre 1,00

In a UMA system with write-invalidate MSI, the BusRdX does not need to read the memory line that contains the address being accessed since the processor asks for the line with the purposes of modifying (writing to) it.

Trieu-ne una:

Respostes

- Vertader
- Fals ✔

Well done!

Pregunta **9**

Correcte

Puntuació 1,00 sobre 1,00

In a UMA system with the simplest write-invalidate MSI protocol explained in class, main memory is responsible for providing a memory line when one of the private caches asks for it unless the line is in M state in another private cache.

Trieu-ne una:

Respostes

- Vertader ✔
- Fals

Well done! This is one of the inefficiencies that is addressed by other more advanced protocols (look at MOSI or MSIF in the optional slides).

Pregunta **10**

Correcte

Puntuació 1,00 sobre 1,00

The implementation of the simplest write-invalidate MSI protocol explained in class requires two bits to track the state of each word in each cache line. Therefore, if the cache has capacity for N lines, each one storing M words, MSI requires N*M*2 bits to keep its contents coherent.

Trieu-ne una:

Respostes

- Vertader
- Fals ✔

Well done! Coherence is kept at cache line level, not at the individual word level. Therefore, N*2 bits are required by MSI to keep cache contents coherent.

◄ Slides for Unit 3: Introduction to parallel architectures

Salta a...

UMA coherence quizz (2) ►