2024 Analog IC Design Homework 2 ***due date: 2024/04/02***

Note: all the simulations are under TT 25°C

1. **Common Source (CS) (50%)**

   As shown in Fig. 1, we have a common source (CS) stage with $\mathbf{V_{DD}=1.8V}$.

   Try to design the size of M_1 and the resistance of R_D to achieve AC gain $|A_v| > 3$V/V and $V_{out,DC}$ = 0.9V (within 1% variation), under the constraint $\mathbf{V_{in,DC} = 0.9V}$. You need to make sure that **M_1 operates in saturation region**.

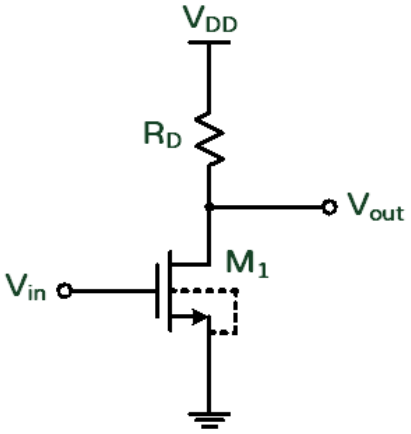

Fig. 1. A common source amplifier

(a) Design this circuit to achieve the requirements:

(1) M_1 operates in saturation region

(2) output DC voltage $V_{out,DC}$ = 0.9V±1%

(3) AC gain $|A_v| > 3$ (V/V)

(4) the resistance of $R_D < 50k\Omega$

Describe how you choose the size of M1 and the resistance of RD to achieve the requirements. (10%)

(b) Use ".op" command in Hspice and check the ".lis" file to show that M_1 operates in saturation region. Screenshot $V_{in,DC}$, $V_{out,DC}$ and drain current (I_D) of M_1. (5%)

Hint: use the following Hspice command in your .sp file

```
.op
```

After simulation, you will see $V_{in,DC}$ and $V_{out,DC}$ in .lis file:

```
****** operating point status is all       simulation time is     0.
   node    =voltage      node    =voltage      node    =voltage

+0:vdd     =   1.8000  0:vin     =  Vin,DC   0:vout    =  Vout,DC
```

and MOS characteristic parameters (including operation region, I_D, etc.) in .lis file:

```
**** mosfets


subckt
element  0:m1
model    0:n_18.1
region     MOS
 id        character-
 ibs       istic
 ibd       parameters
  ⋮
```

(c) Use ".tf" command in Hspice to print out:

(1) the small signal gain from V_{in} to V_{out} (2.5%)

(2) the output impedance (2.5%)

Hint: use the following Hspice command in your .sp file

```
.tf V(vout) Vin
```

After simulation, you will see small-signal parameters in .lis file:

```
****     small-signal transfer characteristics

     v(vout)/vin                                =   AC gain
     input resistance at             vin        =   Rin
     output resistance at v(vout)               =   Rout
```

(d) Calculate Vout,DC, AC gain and output impedance **by hand-calculation**. You can use the parameters in ".lis" file in (b). (10%)

Hint: you won't find "r_o" in .lis file. Instead, you can find the value of "gds" and use this relationship "$r_o=\frac{1}{gds}$."

(e) Compare AC gain and output impedance between those by simulation in (c) and those by hand-calculation in (d). Report the **error rate** ($=\frac{simulation-hand}{hand} \times 100\%$), and **describe** where the error comes from. (10%)

(f) Please fill in the following specification table. Make sure you achieve all the requirements. (10%)

	Specification	**simulation**	**hand-calculation**
V_{DD}	1.8V		
$V_{in,DC}$	0.9V		
M_1 (W/L, m)	–		
R_D	< 50kΩ		
$V_{out,DC}$	0.9V±1%		
gain $\|A_v\|$	> 3V/V		
output impedence	–		
I_D	–		–

Table 1. Specification table for CS

2. Common Gate (CG) (25%)

As shown in Fig. 2, we have a common gate (CG) stage with $\mathbf{V_{DD}=1.8V}$.

Try to design the size of M_2, the bias voltage V_b and the resistance of R_D to achieve AC gain $|A_v| > 9$V/V and $V_{out,DC} = 0.9$V (within 1% variation), under the constraint $\mathbf{V_{in,DC}}$ = **0.5V**. You need to make sure that $\mathbf{M_2}$ **operates in saturation region**.

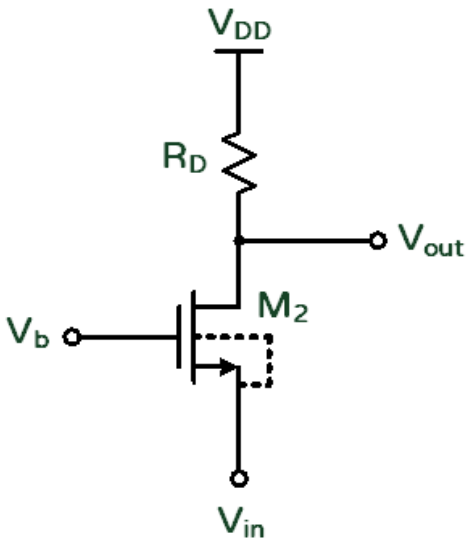

Fig. 2. A common gate amplifier

(a) Design this circuit to achieve the requirements:
   (1) M_2 operates in saturation region
   (2) output DC voltage $V_{out,DC} = 0.9V \pm 1\%$
   (3) AC gain $|A_v| > 9$ (V/V)
   (4) the resistance of $R_D < 100k\Omega$

   Describe how you choose the size of M2, the bias voltage Vb and the resistance of RD to achieve the requirements. (5%)

(b) Use ".op" command in Hspice and check the ".lis" file to show that M_2 operates in saturation region. Screenshot $V_{out,DC}$ and drain current (I_D) of M_2. (2%)

(c) Use ".tf" command in Hspice to print out:
   (1) the small signal gain from V_{in} to V_{out} (1%)
   (2) the input impedance (1%)
   (3) the output impedance (1%)

(d) Calculate Vout,DC, AC gain, input impedance and output impedance **by hand-calculation**. You can use the parameters in ".lis" file in (b). Compare AC gain, input impedance and output impedance with those by simulation in (c). Report the **error rate** ($=\frac{simulation-hand}{hand} \times 100\%$), and **describe** where the error comes from. (10%)

(e) Please fill in the following specification table. Make sure you achieve all the requirements. (5%)

	Specification	**simulation**	**hand-calculation**
V_{DD}	1.8V		
$V_{in,DC}$	0.5V		
M_2 (W/L, m)	–		
R_D	< 100kΩ		
$V_{out,DC}$	0.9V±1%		
gain $\|A_v\|$	> 9V/V		
input impedence	–		
output impedence	–		
I_D	–		–

Table 2. Specification table for CG

3. Common Drain (CD) (a.k.a. Source Follower, SF) (25%)

As shown in Fig. 3, we have a common drain (CD) stage with **V_{DD}=1.8V**.

Try to design the size of M_3 and the resistance of R_S to achieve AC gain $|A_v| > 0.75$V/V and $V_{out,DC}$ = 0.9V (within 1% variation), under the constraint **$V_{in,DC}$ = 1.5V**. You need to make sure that **M_3 operates in saturation region**.

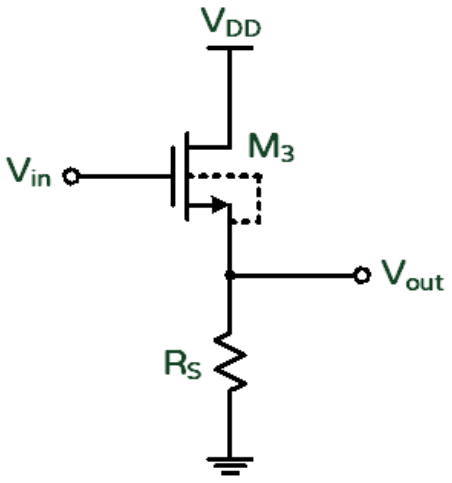

Fig. 3. A common drain amplifier

(a) Design this circuit to achieve the requirements:
   (1) M_3 operates in saturation region
   (2) output DC voltage $V_{out,DC}$ = 0.9V±1%
   (3) AC gain $|A_v| > 0.75$(V/V)
   (4) the resistance of $R_S < 80k\Omega$

   Describe how you choose the size of M3 and the resistance of Rs to achieve the requirements. (5%)

(b) Use ".op" command in Hspice and check the ".lis" file to show that M_3 operates in saturation region. Screenshot $V_{out,DC}$ and drain current (I_D) of M_3. (3%)

(c) Use ".tf" command in Hspice to print out:
   (1) the small signal gain from V_{in} to V_{out} (1%)
   (2) the output impedance (1%)

(d) Calculate Vout,DC, AC gain and output impedance **by hand-calculation**. You can use the parameters in ".lis" file in (b). Compare AC gain and output impedance with those by simulation in (c). Report the **error rate** ($=\frac{simulation-hand}{hand} \times 100\%$), and **describe** where the error comes from. (10%)

(e) Please fill in the following specification table. Make sure you achieve all the requirements. (5%)

	Specification	**simulation**	**hand-calculation**
V_{DD}	1.8V		
$V_{in,DC}$	1.5V		
M_3 (W/L, m)	–		
R_S	< 80kΩ		
$V_{out,DC}$	0.9V±1%		
gain $\|A_v\|$	> 0.75V/V		
output impedence	–		
I_D	–		–

Table 3. Specification table for CD