2024 Analog IC Design Homework 4 *due date: 2024/05/03*

Note: all the simulations are under TT 25°C

1. Use Composer and Hspice to simulate the differential amplifier as shown at Fig. 1 with **Vdd = 1.5V and output loading (CL) = 1pF**. Please design the bias voltage (Vb), input common mode voltage (Vin_CM), device size (W/L) of M1~M3 and resistor (Rd) to make differential gain $|A_{DM}| > 20$, $CMRR > 25$ dB, and $-3dB\ bandwidth > 1.5MHz$. **Please make sure all the MOSFETs operate in saturation region.** (75%)

   Hint: You can use the Hspice command showing below in your .sp file

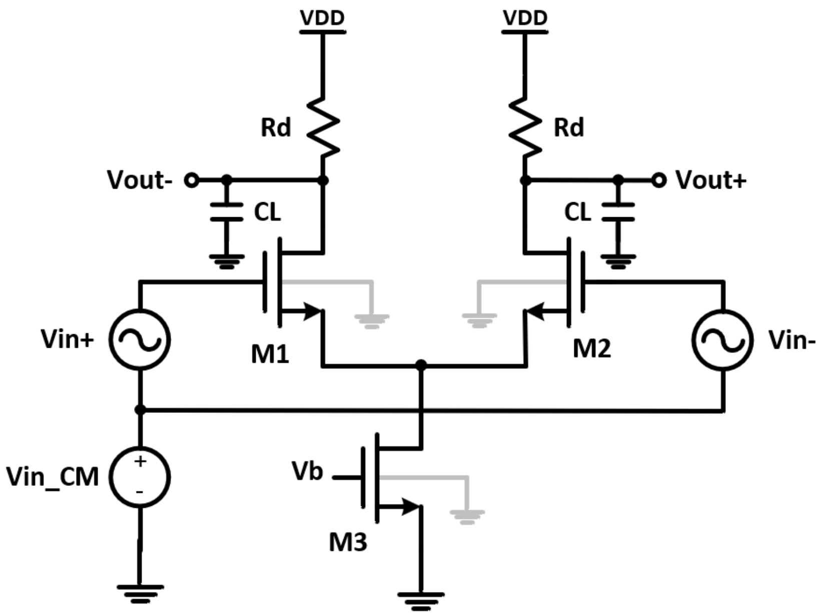

Fig. 1

(a) Describe your design consideration. (How you choose the size of M1~M3 、Rd, the bias voltage Vb , and Vin_CM) (10%)

(b) Please use ".op" command to print out the small signal parameters of active devices. Please make sure all the MOSFETs operate in saturation region. (5%)

(c) Please use ".tf" command to print out the small signal parameters. (5%)

(d) Use the parameters in (b) to calculate the $|A_{DM}|$, check your calculation with the simulation results. (5%)

(e) Please use ".ac" command to find **common mode gain** at 10kHz and use the A_{DM} from (c) to find $\boldsymbol{CMRR}$. (CMRR = $20\log\left(\frac{A_{DM}}{A_{CM-CM}}\right)$) (5%)

(f) Use the parameters in (b) to calculate the $\boldsymbol{CMRR}$, check your calculation with the simulation results. (5%)

(g) Please simulate and plot the frequency response of your design. Use ".pz" to simulate and mark the **dominant pole** on this curve. (5%)

(h) Use the parameters in (a) to calculate the **dominant pole**, and check your calculation with the simulation results. (5%)

(i) Please use the command below to find the input range which fits the requirement $|\boldsymbol{A_{DM}}| > \mathbf{5}$. Please print out the small signal parameters at the maximum and minimum to prove the mos is not in subthreshold region. (10%)
Hint: Input range should be continuous.

(j) Please discuss your design flow and calculate the figure of merit (FoM) value $\dfrac{\textbf{Total current (uA)}}{\textbf{Input range (mV)} \times \mathbf{-3dB\ bandwidth\ (MHz)}}$. Comment how to improve FoM of your design. (5%+15%)
Hint: Please use the Vdd current.
Example:

```
**** voltage sources

subckt
element  0:vip       0:vb       0:vdd      0:vin      0:vss
 volts    500.0000m  500.0000m    1.5000   500.0000m    0.
 current    0.         0.        -25.8755u    0.        25.8755u
 power      0.         0.         38.8132u    0.         0.

    total voltage source power dissipation=   38.8132u       watts
```

2. Design a 1:6 wide-swing cascade current source as shown in Fig. 2(a) with Vdd=1.8V. (25%)
   (a) With Iref = 20uA (Iout = 120uA), design the W/L sizes of M1~M4, and the dc bias Vb to get Rout > 700kΩ when Vout = 300mV. (10%)
   Hint: You can use the following Hspice command in your .sp file to find Rout.

```
.DC Vout 0 1.8 0.01
.meas dc deriv find deriv('I(M3)') at 300mV
.meas dc Rout PARAM='1/deriv'
```

   Example:

```
****** dc transfer curves tnom=  25.000 temp=  25.000 ******
deriv=   1.3196u
rout= 757.8167k
```

(b) Use the circuit structure as shown in Fig. 2(b) as a reference to design a bias generation circuit of Vb with Iin = 20uA (Iout = 120uA). State the M5's and M6's (Fig. 2. (b)) design strategy and show in hand calculation. And express Vin1, Vin2, and Vout in terms of Vov and Vth. (15%)

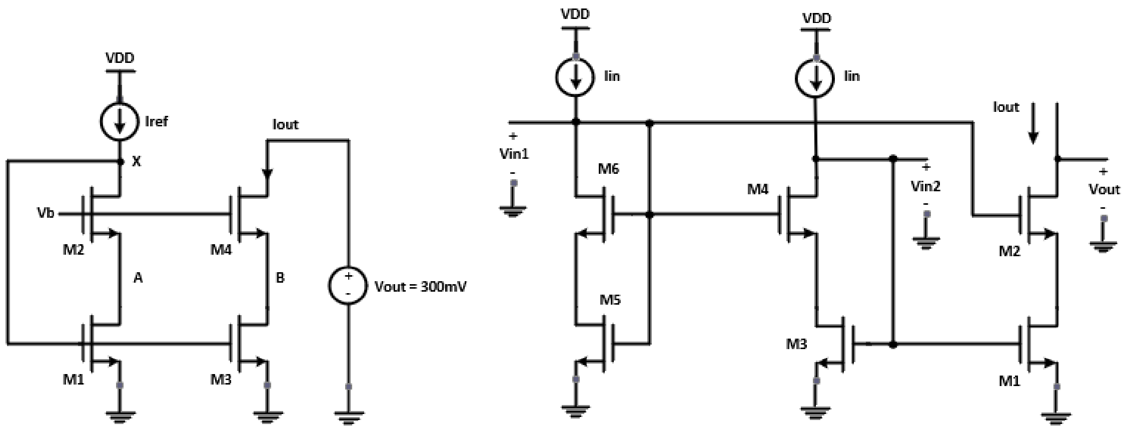

Fig. 2.(a) Fig. 2.(b)

Reference code

Differential mode:

Your input common mode

```
*Input
Vip vip 0 dc Vin_CM ac 0.5 0
Vin vin 0 dc Vin_CM ac 0.5 180

*Gain/Bandwidth
.op
.tf V(voutp, voutn) vip
.pz V(voutp, voutn) vip
.ac dec 10 1 100G
.print ac v(voutp) v(voutn) v(voutp, voutn)
.probe Vdb(voutp, voutn) Vp(voutp, voutn)
.meas ac dcgain_in_db max Vdb(voutp, voutn)
.meas ac BW when Vdb(voutp, voutn) = 'dcgain_in_db - 3'
```

Result examples:

Adm:

```
****     small-signal transfer characteristics

     v(voutp,voutn)/vip                          =   20.5256   |Adm|
     input resistance at               vip       =   1.000e+20
     output resistance at v(voutp,voutn)         =   153.2831k
```

Pole/Zero:

```
*********************************************************
 ******    pole/zero analysis

  input =  0:vip          output = v(voutp,voutn)

      poles (rad/sec)                   poles ( hertz) 注意單位
real              imag            real              imag
-8.51523x  第1個會因為pole和      -1.35524x         0.
-10.0208x                         -1.59485x         0.   dominant pole 請看第2個
-57.8283x  zero很近的關係相消      -9.20365x         0.

      zeros (rad/sec)                   zeros ( hertz)
real              imag            real              imag
-8.43947x         0.              -1.34318x         0.
-57.6666x         0.              -9.17793x         0.
5.46304g          0.              869.470x          0.

 ***** constant factor = 18.0480m
```

BW:

```
dcgain_in_db=  26.2459     at=   1.0000
                from=   1.0000     to= 100.0000g
bw=   1.5912x   -3dB bandwidth
```

Common mode:

```
*Input
Vip vip 0 dc Vin_CM ac 1 0
Vin vin 0 dc Vin_CM ac 1 0

*Gain
.op
.ac dec 10 1 100G
.meas ac acm_in_db find vdb(voutp) at=10k
```

Result example:

```
****** ac analysis tnom=  25.000 temp=  25.000 ******
acm_in_db= 641.0592m   Common mode gain in dB
```

$$\mathbf{CMRR = 20\log(20.5256) - 641.0592m = 25.605\ dB}$$

Input range test:

```
*Input
.param sweepv=Vin_CM
Vip vip 0 dc 'sweepv' ac 0.5 0
Vin vin 0 dc '2*Vin_CM-sweepv' ac 0.5 180

*Gain
.op
.dc sweepv 0 '2*Vin_CM' 1m
.tf V(voutp, voutn) vip
```

Result example:

Please find the input range around your Vin_CM (0.5V for example) which fits the requirement. (Make sure the range is **the continuous range**)

Please find the input range around your input common mode

For example, my input common mode is 0.5V

481.0000m	1.000e+20	28.1476k	[illegible]
482.0000m	1.000e+20	29.0007k	4.9662
483.0000m	1.000e+20	30.0169k	5.0859
484.0000m	1.000e+20	31.2398k	5.2313
485.0000m	1.000e+20	32.7294k	5.4098
486.0000m	1.000e+20	34.5706k	5.6321
487.0000m	1.000e+20	36.8869k	5.9134
488.0000m	1.000e+20	39.8615k	6.2767
489.0000m	1.000e+20	43.7735k	6.7568
490.0000m	1.000e+20	49.0494k	7.4073
491.0000m	1.000e+20	56.3372k	8.3096
492.0000m	1.000e+20	66.5372k	9.5773
493.0000m	1.000e+20	80.5628k	11.3276
494.0000m	1.000e+20	98.3243k	13.5540
[illegible]	1.000e+20	117.1996k	15.9332
[illegible]	1.000e+20	132.9484k	17.9329
[illegible]	1.000e+20	143.4520k	19.2787
[illegible]	1.000e+20	149.4481k	20.0525
499.0000m	1.000e+20	152.4020k	20.4301
500.0000m	1.000e+20	153.2831k	20.5256
501.0000m	1.000e+20	152.4020k	20.3679
502.0000m	1.000e+20	149.4481k	19.9018
503.0000m	1.000e+20	143.4520k	18.9785
504.0000m	1.000e+20	132.9484k	17.3796
505.0000m	1.000e+20	117.1996k	14.9995
506.0000m	1.000e+20	98.3243k	12.1603
507.0000m	1.000e+20	80.5628k	9.4964
508.0000m	1.000e+20	66.5372k	7.3959
509.0000m	1.000e+20	56.3372k	5.8684
510.0000m	1.000e+20	49.0494k	4.7757
511.0000m	1.000e+20	43.7735k	3.9824

Then print out the small signal parameters at Vip = 0.483V; Vin = 2*Vin_CM-0.483 and Vip = 0.509V; Vin = 2*Vin_CM-0.509 to prove the mos region.

For more detail, you can check Lecture 4, Page 12 !!!

天梯分數計算方式

1. 得到天梯分數資格為需要滿足 FoM < 1
2. 天梯分數級距

   1~2 名: 15 分

   3~5 名: 13 分

   6~10 名: 10 分

   11~20 名: 8 分

   21 名以後: 5 分
3. 天梯表格連結:

   https://docs.google.com/spreadsheets/d/1Cb1Ykvu3HXtgSUoKY7dYbgchWF2wmQXm/edit#gid=1062528342