2024 Analog IC Design Homework 6 ***due date: 2024/06/04***

Note: all the simulations are under TT 25°C

Please design a **single-ended operational amplifier** by using the folded-cascode circuit configuration with PMOS input stage as shown at Fig. 1. **Please make sure all the MOSFETs operate in saturation region.**

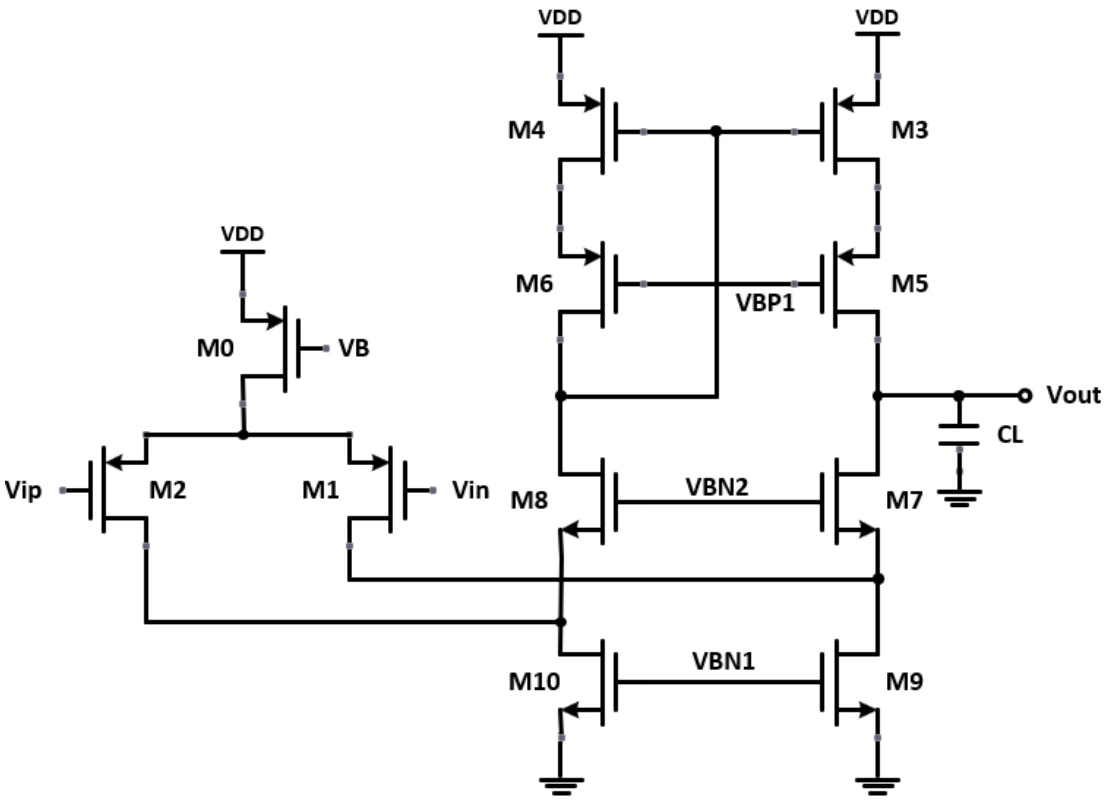


Fig. 1

This design is with output loading (CL) = 600fF, VDD = 1.8V, and input common mode voltage = 0.9V.

(a) You need to design the bias voltage (VB, VBN1, VBN2, VBP1) and device size (W/L) of M0~M10 to make DC gain larger than **65dB**, unity gain frequency larger than **15MHz,** and phase margin larger than **75°**. Please list all your device size, bias voltage and show your results. (10%)

(b) Please use .op command to print out the small signal parameters of active devices. Use the parameters to calculate the DC gain and check your calculation with the simulation results. (15%)

(c) Please simulate and plot the frequency response (magnitude and phase) of your design. Mark the DC gain, unity gain frequency, and phase margin on figure. (10%)

(d) Please simulate and plot the frequency response of your design. Use .pz to simulate and mark the first pole and second pole on this curve. (5%)

(e) Please input differential sinusoidal waveforms with 8mv linear range at 1MHz to estimate the harmonic distortion. Please use .four to simulate the THD performance. The THD has to be less than **0.85%** at 1MHz. (10%)

(f) Please calculate the figure of merit (FoM) value as

$$\text{"}\frac{Total\ current\ (uA)\times THD(\%)}{Gain\ (dB)\times Unity\ gain\ frequency\ (MHz)}\times 1000\text{"}$$

Try to find the best FoM of your design. (5%)

(g) Please fill the following table and discuss your design for best FoM. (15%+30%)

	Specification	This work
VDD	1.8V	
CL	600f	
Total current (uA)	Open for design	
DC gain (dB)	> 65	
Input common mode voltage	0.9V	
Output common mode voltage	Open for design	
Unity gain frequency (MHz)	> 15	
Phase margin (°)	> 75	
THD (%)	< 0.85	
FoM	As small as possible	

Result examples

```
dcgain_in_db=  70.1235   DC gain      1.0000
                from=    1.0000       to= 100.0000g
dcgain=    3.2076k       at=    1.0000
                from=    1.0000       to= 100.0000g
unity_frequency=  15.0299x   Unity gain frequency
phase=-104.9129
phase_margin=  75.0871   Phase margin
```

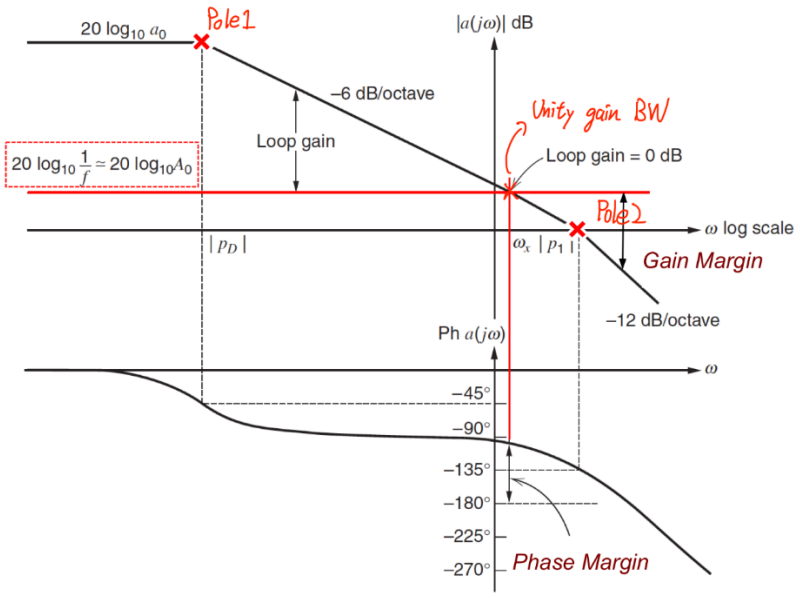
```
**** voltage sources

subckt
element  0:vb       0:vbn1     0:vbn2     0:vbp1     0:vdd      0:vin
 volts      1.2000   700.0000m  550.0000m    1.1000     1.8000   900.0000m
 current    0.         0.         0.         0.      -10.2326u     0.
 power      0.         0.         0.         0.       18.4187u     0.
                                                    Total current
```

```
fourier components of transient response v(vout)
dc component =    1.3487

harmonic frequency  fourier    normalized phase      normalized
no       (hz)       component  component  (deg)      phase (deg)
1           1.0000x  121.9137m    1.0000   179.7440     0.
2           2.0000x  456.6967u    3.7461m  -95.1398   -274.8838
3           3.0000x  309.8281u    2.5414m  -91.2001   -270.9441
4           4.0000x  231.3345u    1.8975m  -88.6446   -268.3886
5           5.0000x  184.2653u    1.5114m  -88.0292   -267.7732
6           6.0000x  154.3273u    1.2659m  -87.9019   -267.6460
7           7.0000x  131.5347u    1.0789m  -87.2187   -266.9628
8           8.0000x  115.6348u  948.4976u  -87.3587   -267.1027
9           9.0000x  102.6788u  842.2256u  -86.5859   -266.3300

total harmonic distortion =   0.554546   percent
```

THD

〈補充說明〉Phase margin

❑ Bode Diagram



The key point to make phase margin better is to push further the second pole from the unity gain frequency.

For more detail, you can check Lecture 10 !!!

天梯分數計算方式

1. 得到天梯分數資格需滿足 FoM < 6.5
2. 天梯分數級距

   1~2 名: 30 分

   3~5 名: 25 分

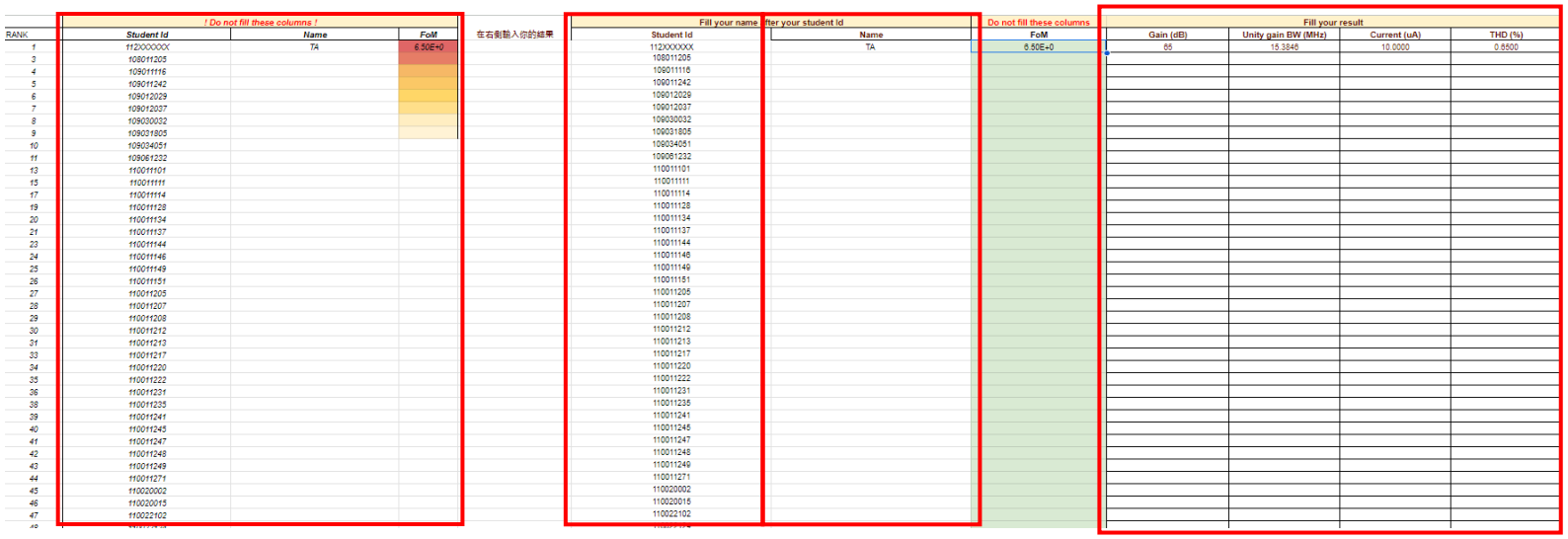
   6~10 名: 20 分

   11~20 名: 15 分

   21~30 名: 10 分

   31 名以後: 5 分
3. 天梯表格連結:

   https://docs.google.com/spreadsheets/d/1Ds97lnq0_m8mMIghyPJtGfywJy91g130/edit#gid=1062528342



排名會顯示左邊　學號　名字(可隨便取)　填入你的結果