2024 Analog IC Design Homework 5 ***due date:2024/5/17***

Note: all the simulations are under TT 25°C

1. **With Feedback**

   Use Hspice to simulate the circuit with **Vdd = 1.5V, C1 = 1pF, C2 = 1pF, RS1 = 50kΩ, RF = 1kΩ ,** as shown in Fig. 1. Please design the device size of M1~M2 and the input common mode current Iin1, to make **transimpedance DC gain |(Vout/Iin)| > 0.85kΩ** , its **bandwidth (-3dB point to DC gain) > 650MHz** and **output common mode voltage be 0.75V (± 1%).** (55%)

   Notice: the sign of transimpedance DC gain should be negative and all of the transistors must stay in saturation region.

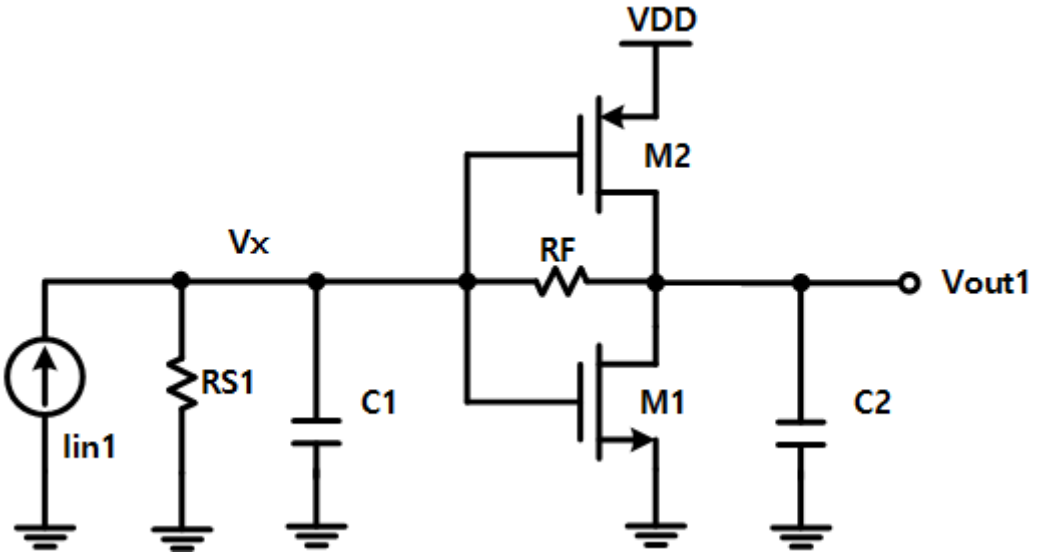

Fig. 1

a. Use ".op" command in Hspice and check the ".lis" file to show that M_1 and M_2 operate in **saturation** region. Screenshot $\mathbf{V_{dd}}$, $\mathbf{V_{out1,DC}}$, $\mathbf{V_{x,DC}}$ **and small signal parameters** of active devices. (5%)

b. Please use .tf command to print out the gain, input and output impedances. (5%)

c. Use .op's parameters to calculate the **transimpedance DC gain, input and output impedances**, and compare your calculation and the simulation results in b. (15%)

d. The small signal -3dB bandwidth has to be larger than 650MHz. Please simulate and plot the frequency response of this gain stage. Use .pz to simulate and mark the poles/zeros on this curve. (5%)

e. Use .op's parameters to calculate the **output pole and the zero** of Vout/Iin(s) frequency response. Check your calculation and the simulation results in d. (10%)

f. Please screenshot your total current, calculate the figure of merit (FoM) value , discuss your design consideration and **comment on how to improve FoM** of your design in detail. (15%)

$$\frac{total\ current(uA)}{transimpedance\ gain(k\Omega)\times -3dB\ bandwidth(MHz)}$$

Hint: Please use the Vdd current.

example:

```
**** voltage sources

subckt
element  0:vdd
 volts      1.5000
 current -662.6471u
 power    993.9707u
```

2. **Without Feedback**

Use Hspice to simulate the circuit as shown in Fig. 2 with **Vdd = 1.5V, C3 = 1pF, C4 = 1pF, RS2 = 50kΩ** . Remove the feedback resistance, use the same size of M1~M2 and the same input current in Fig. 1 to simulate the circuit in Fig. 2. (25%)

Notice: All of the transistors must stay in saturation region.

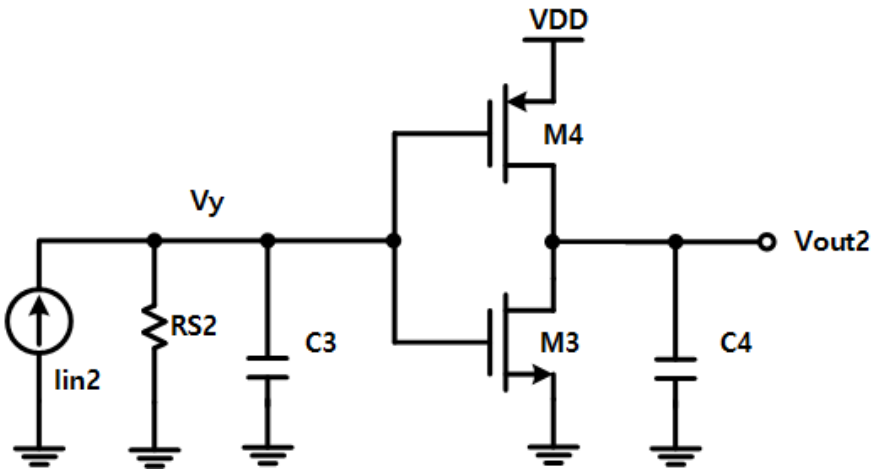

Fig. 2

a. Use ".op" command in Hspice and check the ".lis" file to show that M_3 and M_4 operate in **saturation** region. Screenshot $\mathbf{V_{dd}}$, $\mathbf{V_{out2,DC}}$, $\mathbf{V_{y,DC}}$ **and small signal parameters** of active devices. (5%)

b. Please use .tf command to print out the gain, input, and output impedances. (5%)

c. Use .op's parameters to calculate the **transimpedance DC gain and output impedances** and compare your calculation and the simulation results in a. (10%)

d. Please simulate and plot the frequency response of this gain stage. Use .pz to simulate and mark the poles/zeros on this curve. (5%)

e. Use .op's parameters to calculate the **output pole** of Vout/Iin(s) frequency response. Check your calculation and the simulation results in d. (5%)

3. **Discussion** (20%)

a. Discuss the difference of the circuit of fig. 1 and fig. 2. What are the advantages and drawbacks of the circuit of fig. 1? (15%)

b. Please fill the table. 1 and table. 2. (5%)

table. 1

Fig. 1			
Working item	Specification	Simulation	Calculation
Vdd (V)	1.5		
C1, C2 (F)	1p		
transimpedance DC gain (kΩ)	> 0.85		
bandwidth (MHz)	> 650		
Closed-loop poles/zeros (rad/s)			
Closed-loop input impedance (Ω)			
Closed-loop output impedance (Ω)			
Input common mode current (uA)			
Output common mode voltage (V)	0.75 (± 1%)		
M1 (W/L), m			
M2 (W/L), m			
FoM (uA/($k\Omega \times MHz$))			

table. 2

Fig. 2			
Working item	Specification	Simulation	Calculation
Vdd (V)	1.5		
C3, C4 (F)	1p		
transimpedance DC gain (kΩ)	-		
bandwidth (MHz)	-		
Closed-loop poles/zeros (rad/s)			
Closed-loop input impedance (Ω)			
Closed-loop output impedance (Ω)			
Input common mode current (uA)	same as Iin1		
Output common mode voltage (V)	-		
M3 (W/L), m	same as M1		
M4 (W/L), m	same as M2		

Reference Code

```
*** input
Iin1 gnd Vx Iin1_value ac 1 *** Iin1_value 為你的Iin1 DC value

*** gain_bandwidth
.op
.tf V(Vout1) Iin1
.ac DEC 10 1 100G
.probe vdb(Vout1) vp(Vout1)
.meas ac dcgain_in_db find Vdb(Vout1) at=10k
.meas ac BW when Vdb(Vout1)='dcgain_in_db-3'
.pz V(Vout1) Iin1
```