2024 Analog IC Design Homework 1 ***due date: 2024/ 3/ 19***

Note: all the simulations are under TT 25°C

1. Use Hspice to simulate the DC analysis of Fig.1 with Vdd=1.8V and Vgs from 0V to 1.8V with a step of 0.01V. Please keep the W/L ratio of NMOS and PMOS equal to 3, and sweep channel length of NMOS and PMOS from 0.5μm to 5μm with a step of 0.5μm.Please probe Id vs. Vgs with different channel lengths of NMOS and PMOS and discuss your observations.(10%)
   (Ref. code: .DC Vgs 0 1.8 0.01 sweep L 0.5u 5u 0.5u)

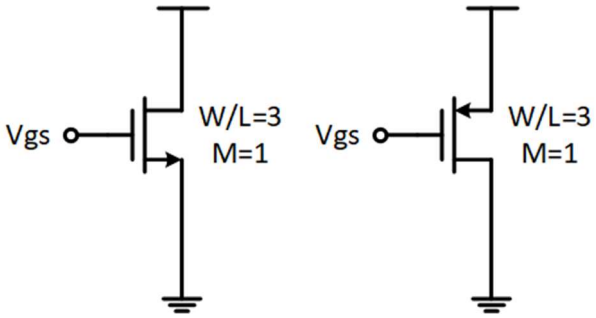

Fig. 1

2. Use Hspice to simulate the diode connected structure as shown at Fig.2 with Vdd=1.8V. Please keep the bias current constant and the W/L ratio of NMOS and PMOS equal to 3, and sweep channel length of NMOS and PMOS from 0.18μm to 10μm with a step of 0.01μm. Please probe the following parameters of NMOS and PMOS and discuss your observations.(40%)
   (a) V_{th} vs. L
   (b) g_{ds} vs. L
   (c) g_m vs. L
   (d) g_m/C_g vs. L

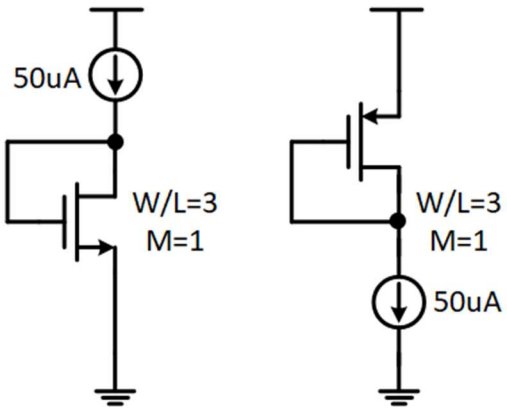

Fig. 2

3. Use Hspice to simulate the capacitance characteristic of NMOS as shown in Fig.3 with body connected to 0V. Please keep W/L=1.5μm/0.2μm and sweep V_G from -1.8V to 1.8V. Please probe the following parameters and discuss your observations.(40%)
   (a) C_{gs} vs. V_G
   (b) C_{gd} vs. V_G
   (c) C_{gb} vs. V_G
   (d) C_{g_total} vs. V_G

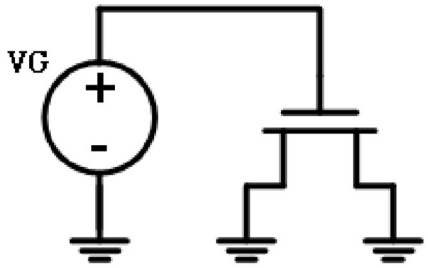

Fig. 3

4. **Body effect.** Use Hspice to simulate DC analysis of Fig.4 with Vdd=1.8V and V_b from 0V to 1.8V with a step of 0.01V. Please keep the bias current constant and the W/L ratio of NMOS and PMOS equal to 3, and sweep channel length of NMOS and PMOS from 0.5μm to 5μm with a step of 0.5μm. Please probe **V_{th} vs. V_b** of NMOS and PMOS and discuss your observations.(10%)

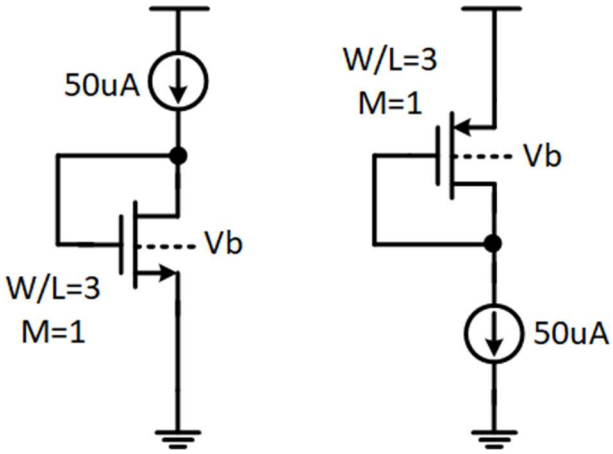

Fig. 4