**Analog IC Design Final Project**

系級：工科系25級

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1. **Schematic and Small Signal Parameters of Active Devices**

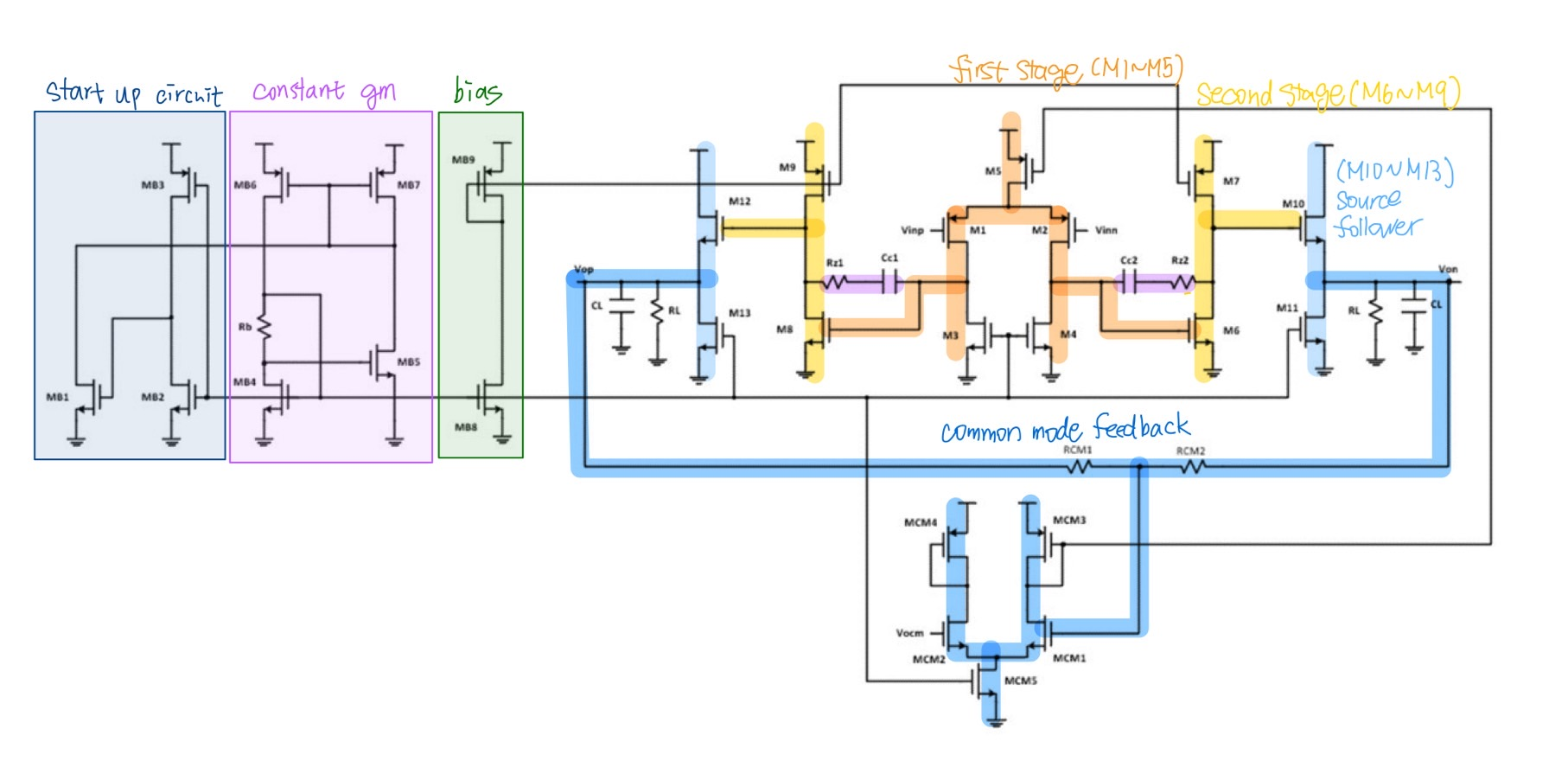


Fig1-1. Different Stages in the OPAMP

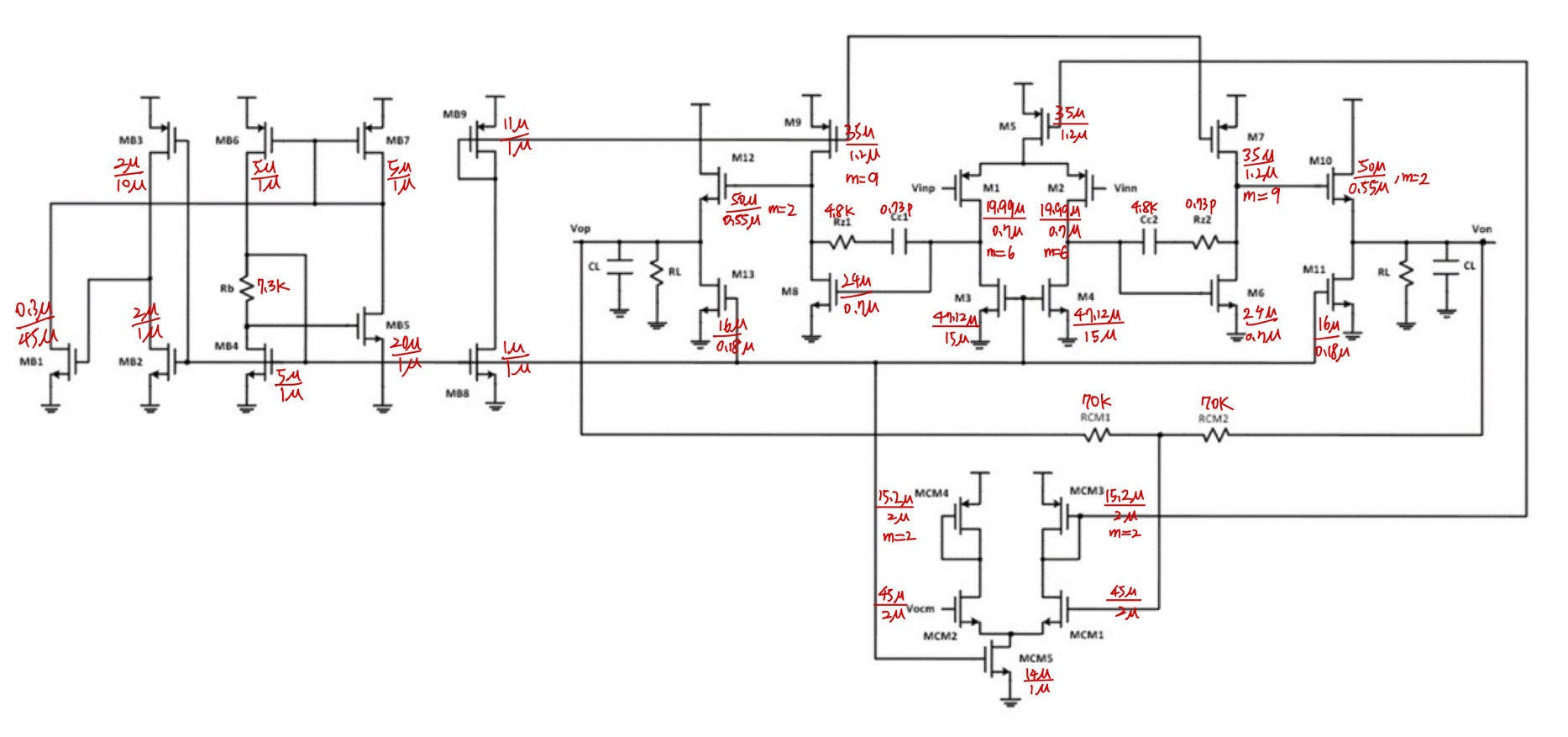


Fig1-2. My Designed Sizes of Transistors and compensation Resistors/Capacitors

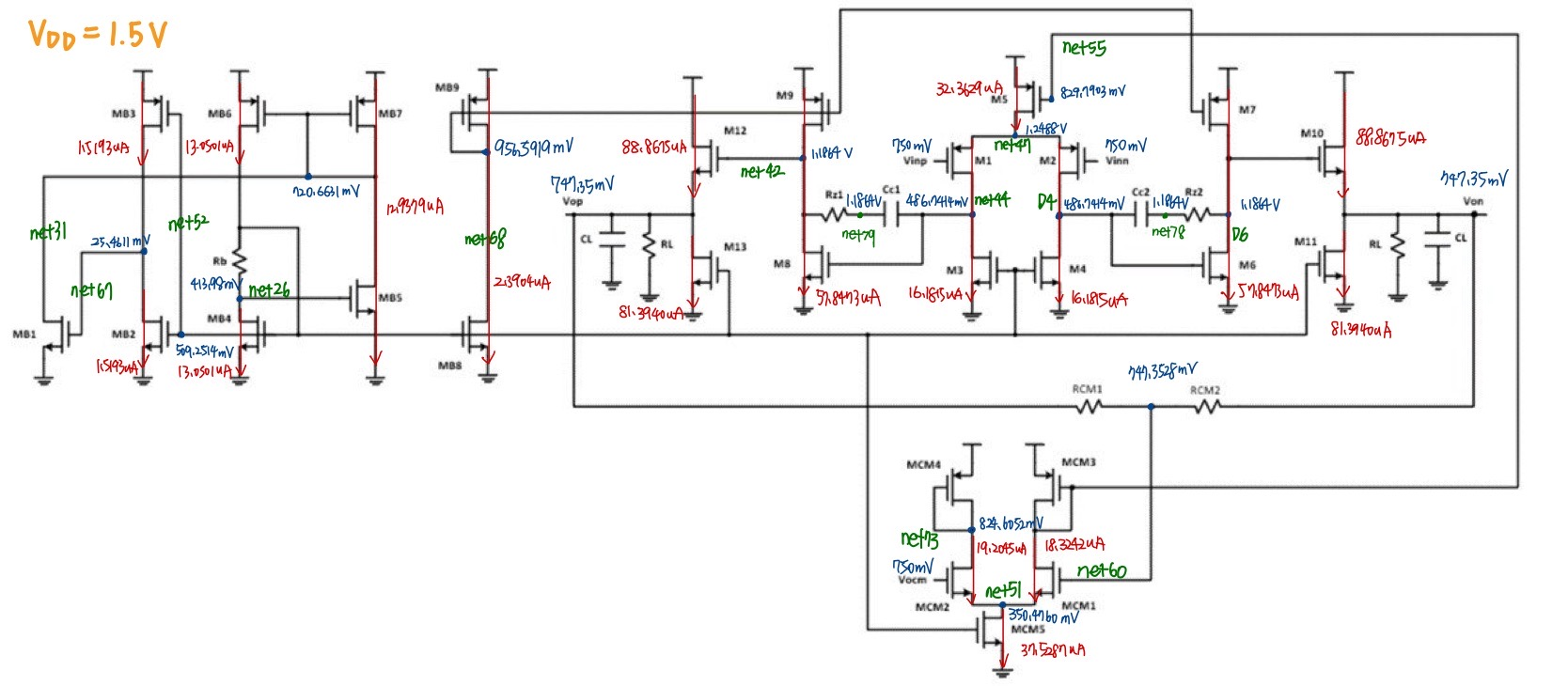


Fig1-3. Node Voltages, Branch Current and Nets

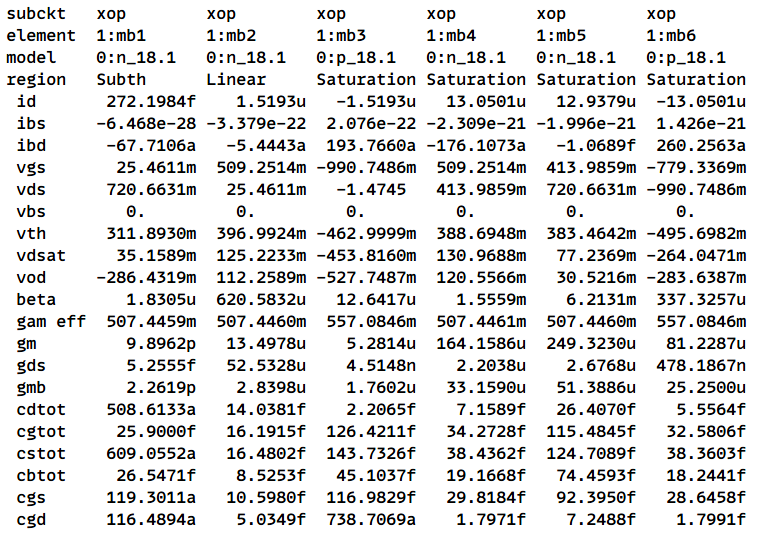
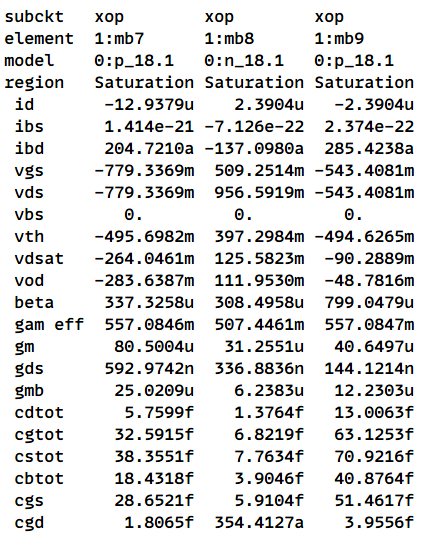
* **Transistor Parameters**

Fig1-4. Start-Up and Bias circuit (MB1~MB9)

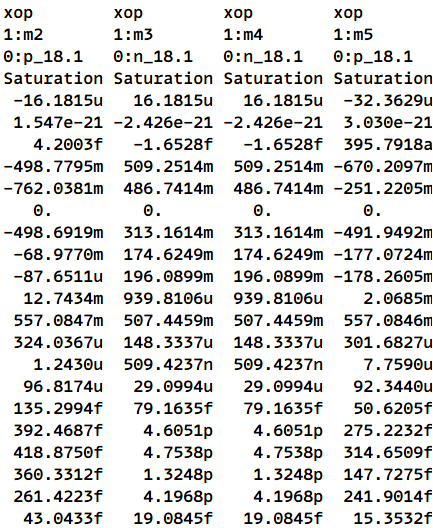
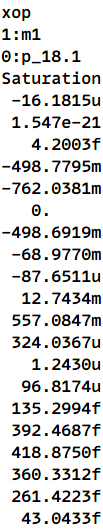
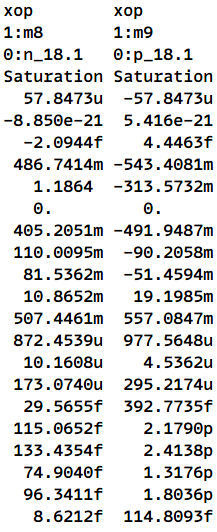


Fig1-5. First Stage Amplifier (M1~M5) Fig1-6. Second Stage Amplifier (M6~M9)

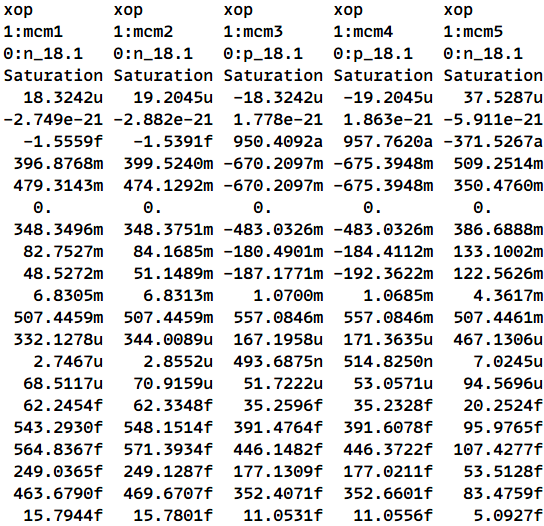
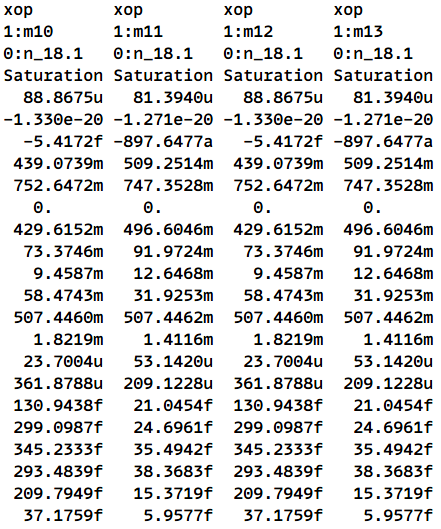
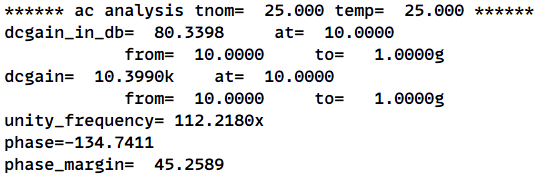


Fig1-7. Source Follower (M10~M13) Fig1-8. Common Mode Feedback (MCM1~MCM5)

* **All Constraints for Specification**

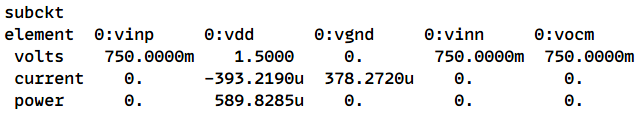
>80dB



>45°

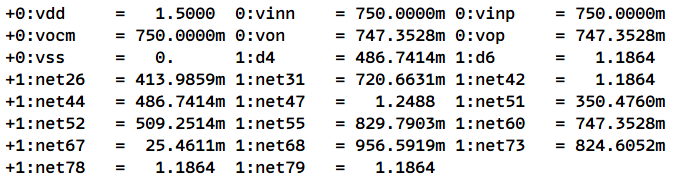
>100MHz

Fig1-9. Gain, Bandwidth, Phase Margin



<0.4mA

Fig1-10. Vdd Current



<750mV±1%

Fig1-11. Von, Vop in Vdd/2

* **Dis.1(a)**

Let , and from circuit design, we know that

(assume that all transistors operate in saturation region and no body effect)

Analyzing the circuit structure, we can establish

Substituting the equations derived above and (W/L)5 = 4\*(W/L)4, we can get

From the derivation of gmb4 under condition (W/L)5 = 4\*(W/L)4, we can infer that the gm of MB4 is affected by only Rb, means that it is insensitive to other variables, and not influenced by operating region, bias voltage and so on. Therefore, if we wish to pursue a specific constant gm current, it can be easily achieved by calculating the value Rb.

* **Dis.1(b)**

**(1) Why do we need a start-up circuit ?**

A start-up circuit is essential for proper initialization, preventing latch-up, and ensuring safe power-up in electronic systems. It ensures correct initial voltages and currents for components, avoids meta-stable states, and controls the power-up sequence to prevent oscillations and transient issues. By providing a controlled ramp-up of voltage and current, it protects components from spikes and ensures reliable operation.

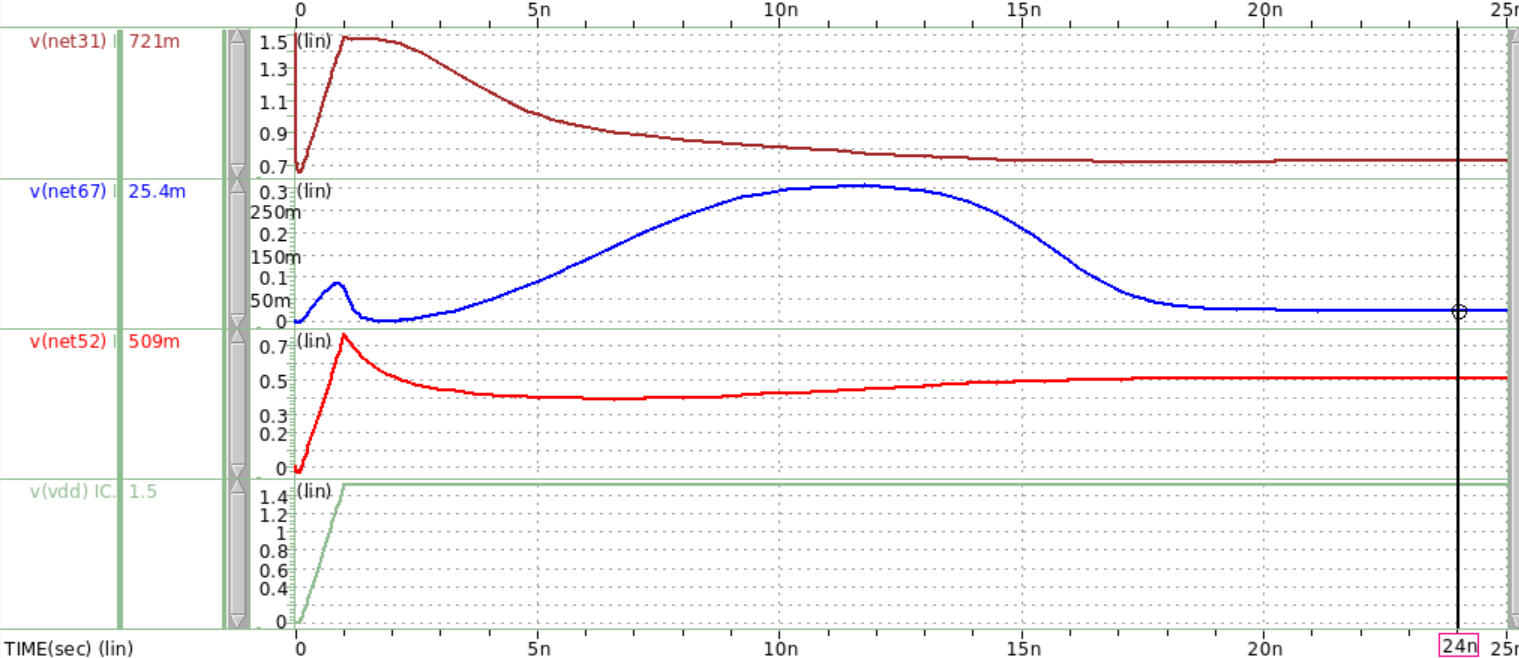
**(2) The functionality of start-up circuit**

The start-up circuit is designed to initialize the entire system when the power supply (Vdd) is first turned on. Initially, when Vdd is activated, MB3 receives a sufficiently large bias voltage and turns on, creating a conductive path between Vdd and the gate of MB1. As a result, the gate of MB1 starts charging and its voltage rises. Once the gate voltage of MB1 exceeds its threshold voltage (Vth), MB1 turns on, forming a path between MB6 and MB7. This connection causes the gates of MB6 and MB7, which are connected to MB1, to begin discharging. As the gate voltages of MB6 and MB7 drop, M12 and M13 are activated. This activation triggers the Constant gm Circuit. When the Constant gm Circuit starts operating, it causes the gates of MB4 and MB2 to begin charging. Once the gate voltage of MB2 exceeds its threshold voltage (Vth), MB2 turns on. This forms a path to ground, allowing the gate of MB1 to continue discharging. When the gate voltage of MB1 drops below its threshold voltage (Vth), MB1 turns off. This sequence of events ensures that the start-up circuit successfully initializes the main circuit, allowing it to reach a stable operating state.

**(3) How to design the size of the transistors to improve power efficiency after startup**

To enhance power efficiency and reduce power consumption in the start-up circuit, it is critical to minimize the current flowing through it. Given that MB1 will eventually turn off as the circuit stabilizes, we need to carefully consider the currents through MB2 and MB3. Since MB2 and MB3 remain active, their current values should be kept as low as possible to avoid unnecessary power dissipation. This can be accomplished by adjusting their (W/L) ratios. Specifically, the (W/L) ratios of MB2 and MB3 should not be excessively large, as larger ratios would lead to higher currents and increased power consumption. By optimizing these transistor sizes, we ensure that the start-up circuit performs its function effectively while maintaining low power usage, thereby improving the overall efficiency of the system.

**(4) Transient analysis**



**MB1 Drain/MB6,7 Gate**

**MB2 ,MB3 Gate**

**MB2 Drain, MB3 Source**

**MB1 Gate**

**Voltage (V)**

**Time (s)**

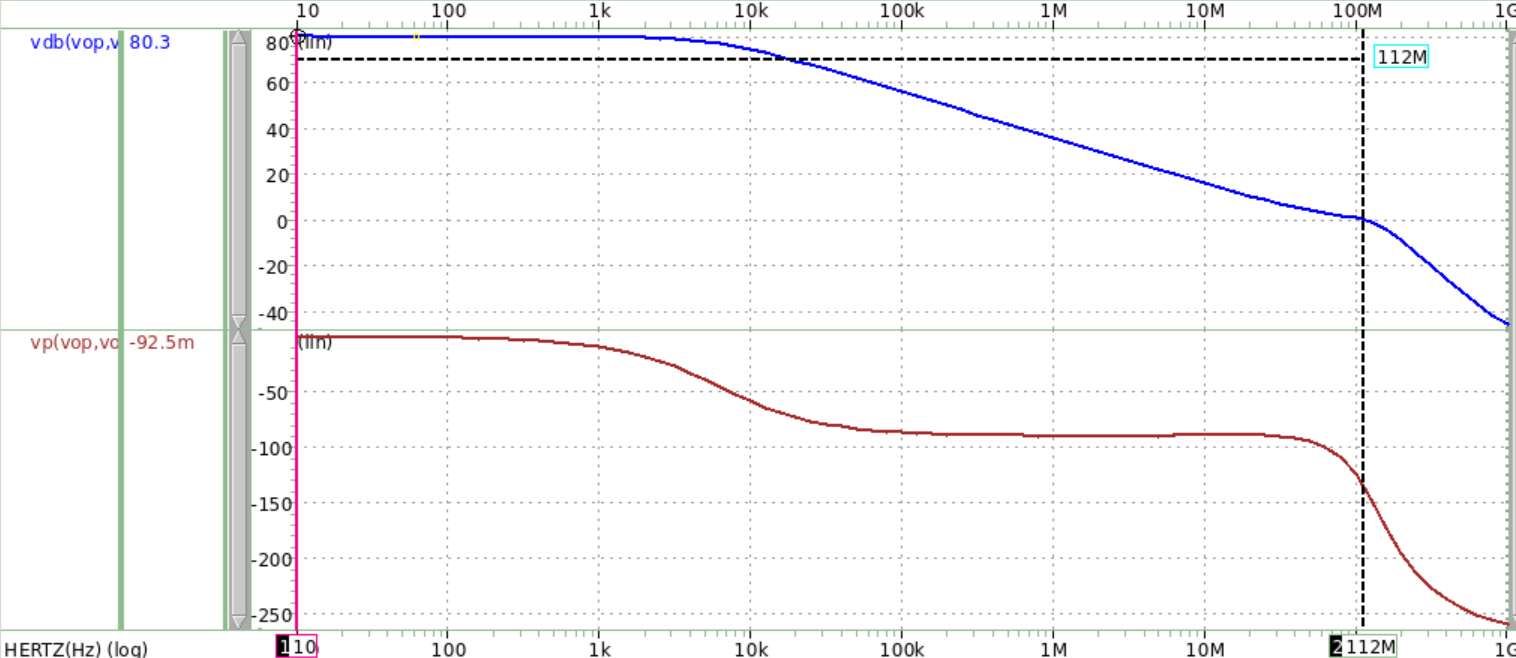
The startup circuit functionality explained in (2) is demonstrated on the waveview. Initially, Vdd turns on and provide large bias for MB3, so we can see that MB3 gate net52 charges up rapidly. Next, MB2 and MB3 turn on, providing current to charge MB1 gate net67, and during 2ns~10ns, MB1 turns on for a little time range, to activate the discharging of MB6,7, which is shown in net31. Finally, the circuit will be activated and operates in function as described in (2). After the circuit is stabilized, at the time roughly 20ns, we can observe that net67 is in a low voltage, that is, MB1 will turn off again and stay in subthreshold region; Secondly, net52 provides stable gate voltage that turns on MB2,3, but due to the gate voltage of net67, MB2 and MB3 will be in linear and saturation region respectively.

1. **Specification Table**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Design Items | Specifications | score | Simulation | Calculation |
| **Technology** | CIC pseudo 0.18um technology | | | |
| **Vicm, Vocm** |  | | | |
| **Supply voltage (V)** | Open for design  **1.8 / 1.5 / 1.3** | **2%** | 1.50 V |  |
| **4%** |
| **6%** |
| **Supply current (mA)**  **(including bias ckt)** | **< 3 / < 1 / < 0.4** | **2%** | 0.39 mA |  |
| **4%** |
| **6%** |
| **Loading** | 2 pF / 100 kΩ  (for each output) |  | 2 pF / 100 kΩ  (for each output) |  |
| **Compensation Rz, Cc** | Rz < 10 kΩ , Cc < 10 pF |  | Rz = 4.80 kΩ  Cc = 0.73 pF |  |
| **Open-loop simulation** | | | | |
| **DC gain (dB)** | **> 70 / > 75 / > 80** | **1%** | 80.34 dB | 80.34 dB |
| **3%** |
| **5%** |
| **G-BW (MHz)** | **> 50 / > 75 / > 90 / > 100** | **1%** | 112.22 MHz |  |
| **2%** |
| **3%** |
| **4%** |
| **P.M.** | > |  | 45.26 |  |
| **C.M.R.R. @10KHz** | > 90 dB |  | 112.18 dB | 112.21 dB |
| **P.S.R.R.+ @10KHz** | > 90 dB |  | 110.53 dB |  |
| **P.S.R.R.- @10KHz** | > 90 dB |  | 112.17 dB |  |
| **Closed-loop simulation** | | | | |
| Differential swing of 1.0 V (step or sinusoidal) | | | | |
| **Closed-loop gain** | > -0.1dB @ 10kHz |  | -0.00171 dB | -0.00167 dB |
| **S.R.+ (10% ~ 90%)** | > 15 V/us (single-ended output) |  | 19.55 V/us | 19.60 V/us |
| **S.R.- (90% ~ 10%)** | > 15 V/us (single-ended output) |  | 16.32 V/us | 16.28 V/us |
| **THD (1.0Vpp@100kHz Sin)** | < - 60 dB |  | -69.43 dB |  |
| **Settling+ (1.0Vstep to 0.5%)** | < 150 ns |  | 51.83 ns |  |
| **Settling- (1.0Vstep to 0.5%)** | < 150 ns |  | 57.97 ns |  |
| **(ns)** | **< 150 / < 90 / < 70 / < 55** | **1%** | 54.90 ns |  |
| **2%** |
| **3%** |
| **4%** |

1. **Simulation Results**

**3.1 Open-Loop Differential Mode AC Response**



**Phase Margin = (180-134.7411) = 45.2589**

**Frequency (Hz)**

**Phase ()**

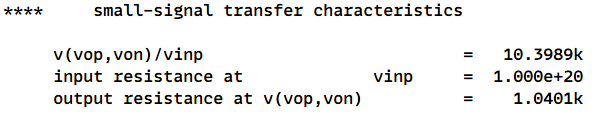
**Gain (dB)**

**Phase = -134.7411**

**DC Gain = 80.3398 dB**

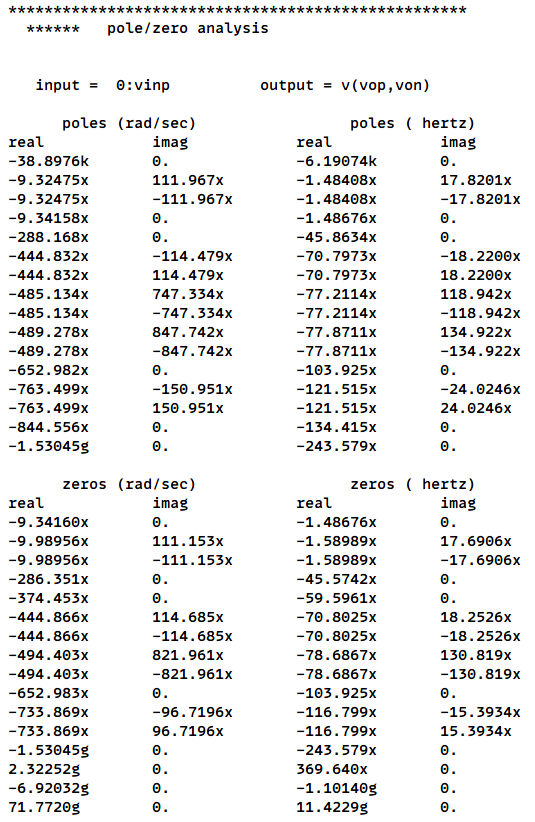
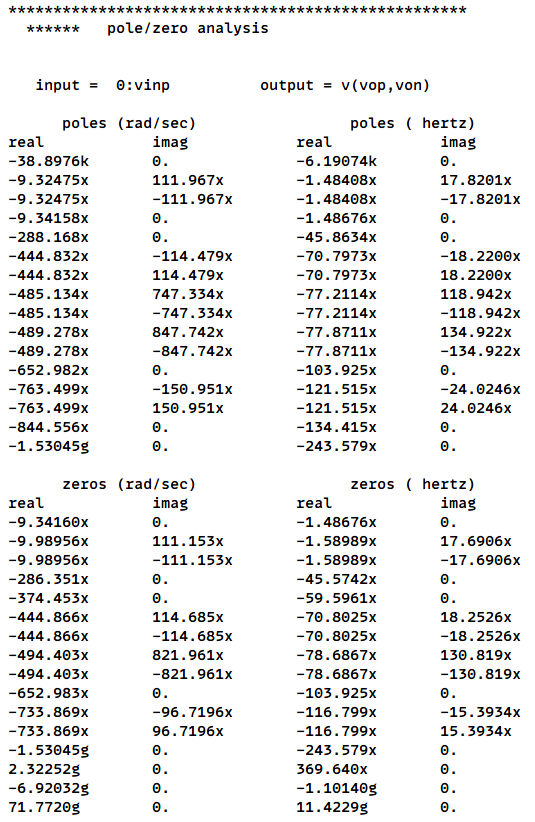
**Unity Gain Frequency = 112.2180 MHz**

Fig3.1(a)-1



Tab3.1(b)

* My DC gain is designed to be **80.3398 dB**
* My Gain Bandwidth is designed to be **112.2180 MHz**
* My Phase Margin is designed to be **45.2589**



**Pole3**

**Zero1**

**Pole1**

**Pole2**

Fig3.1(a)-2

* **Dis.3.1**

**1. Hand Calculation of Gain**

Using the half-circuit method, we can find the rough gain equation for the first stage, second stage and the source follower.

* The error of total gain compared to the simulation gain is 0.0046%, the value is absolutely small.

**2. Poles and Zeros**

**2.1 Pole 1 (Dominant Pole)**

The dominant pole is influenced by Miller effect, contributing a multiplying factor of A2 on the compensation capacitor Cc at the output of stage one.

* The error of dominant pole compared to the simulation first pole is 3.812%
* The first pole is dominant to the unity gain bandwidth, therefore to increase unity gain bandwidth, we must push pole 1 further from the original frequency. My strategy here is to decrease the compensation capacitor value and gm6 to get a relatively larger dominant pole.

**2.2 Pole 2 (Non-Dominant Pole)**

We can infer that the second pole is the output pole of the entire circuit because the loading capacitor isn’t on the output of the second stage. That is, from the example of the lecture slide, we can derive the equation below.

* The error of second pole compared to the simulation second pole is 7.33%
* Note that if we want a larger bandwidth we have to push pole 2 out of the unity gain frequency, if pole 2 is within the unity gain frequency, then the gain reduction will be dramatically faster than we expect, and the bandwidth might result to a small value, which is not a positive phenomenon for a stable and useful circuit.

**2.3 Pole 3 (Non-Dominant Pole)**

The third pole can be found as the output of the second stage, and moreover, it is affected by the frequency compensation mechanism.

* The error of third pole compared to the simulation third pole is 5.78%
* Pole 3 isn’t shown in the waveview, so we can roughly find it by observing the pz table shown in the lis file and dash out all the offset poles and zeros, then finally we can find pole 3.

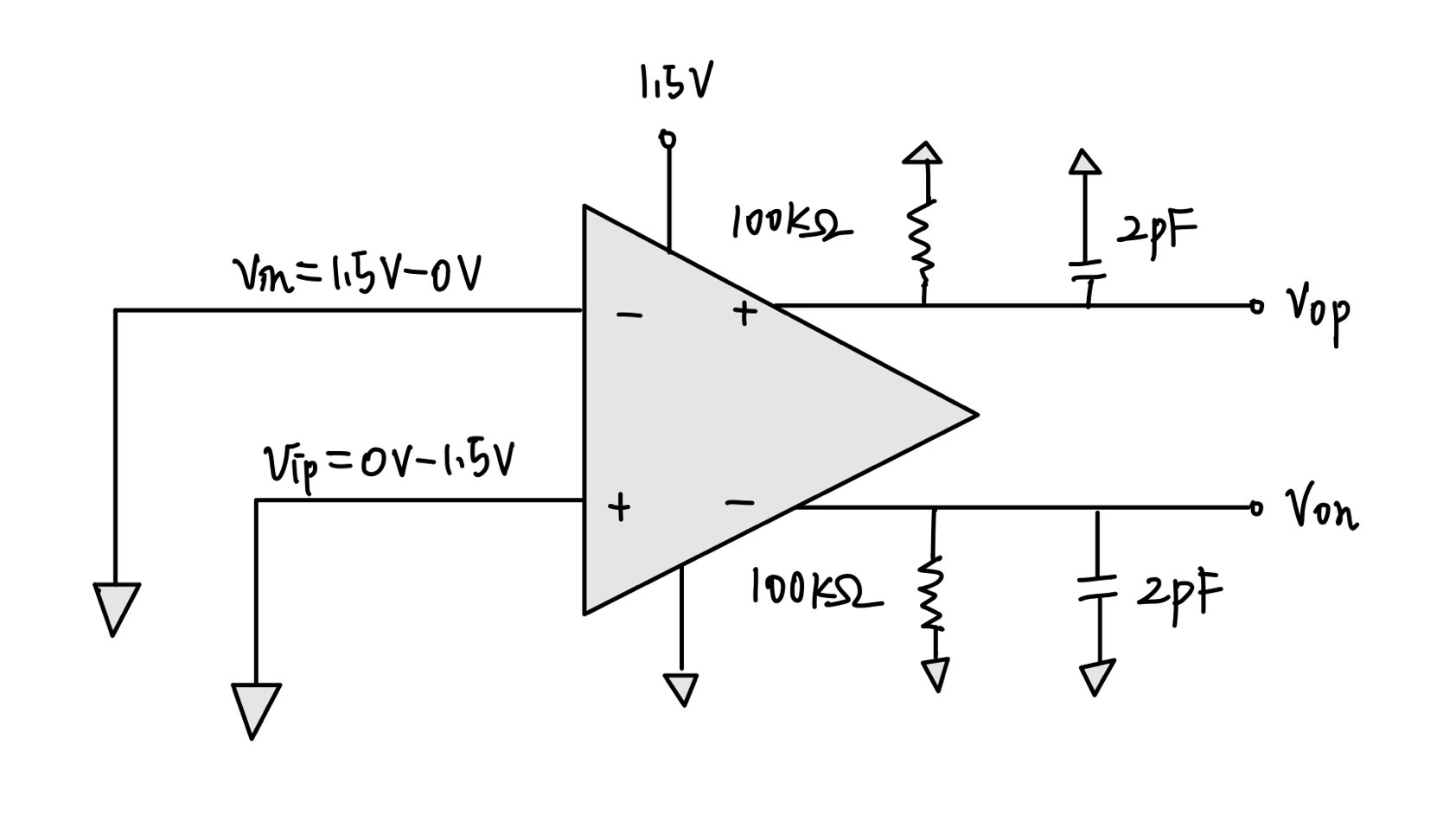
**2.4 Zero**

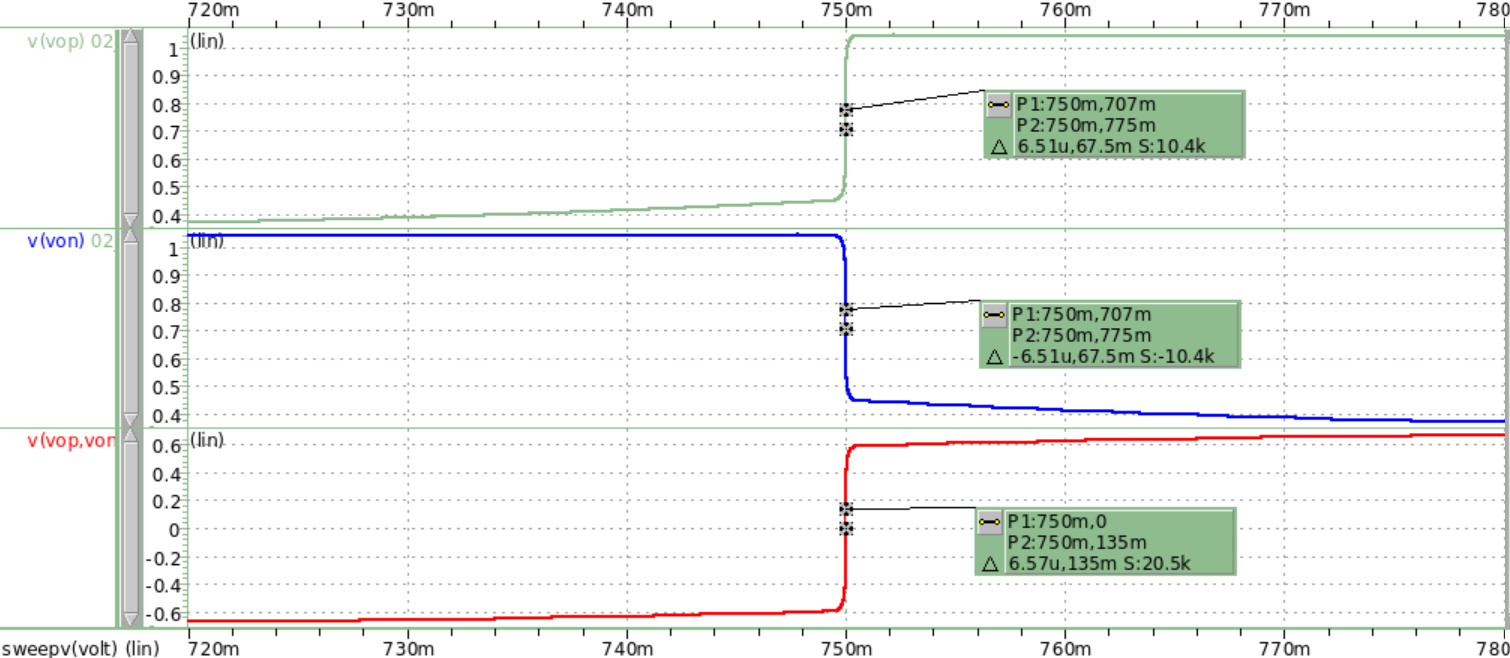
* The error of hand calc. zero compared to the simulation zero is 0.123%
* For design consideration, we aim to pull the zero back more before unity gain frequency to achieve a more larger bandwidth. When no miller compensation, it is a must to let the dominant pole lower in order to get sufficient phase margin, but it might sacrifice the bandwidth. To tackle the problem, adding compensation resistor Rz into the circuit in necessary. Rz can adjust the right half-plane zero to the left half-plane zero, avoiding phase to decline abruptly.

**3. Output Impedance**

The simulation value of Rout is 1.0401kΩ, the error 0.088% is very small, which proves to be correct.

**3.2 Open-Loop Differential Mode DC Sweep**





**Measured Gain**

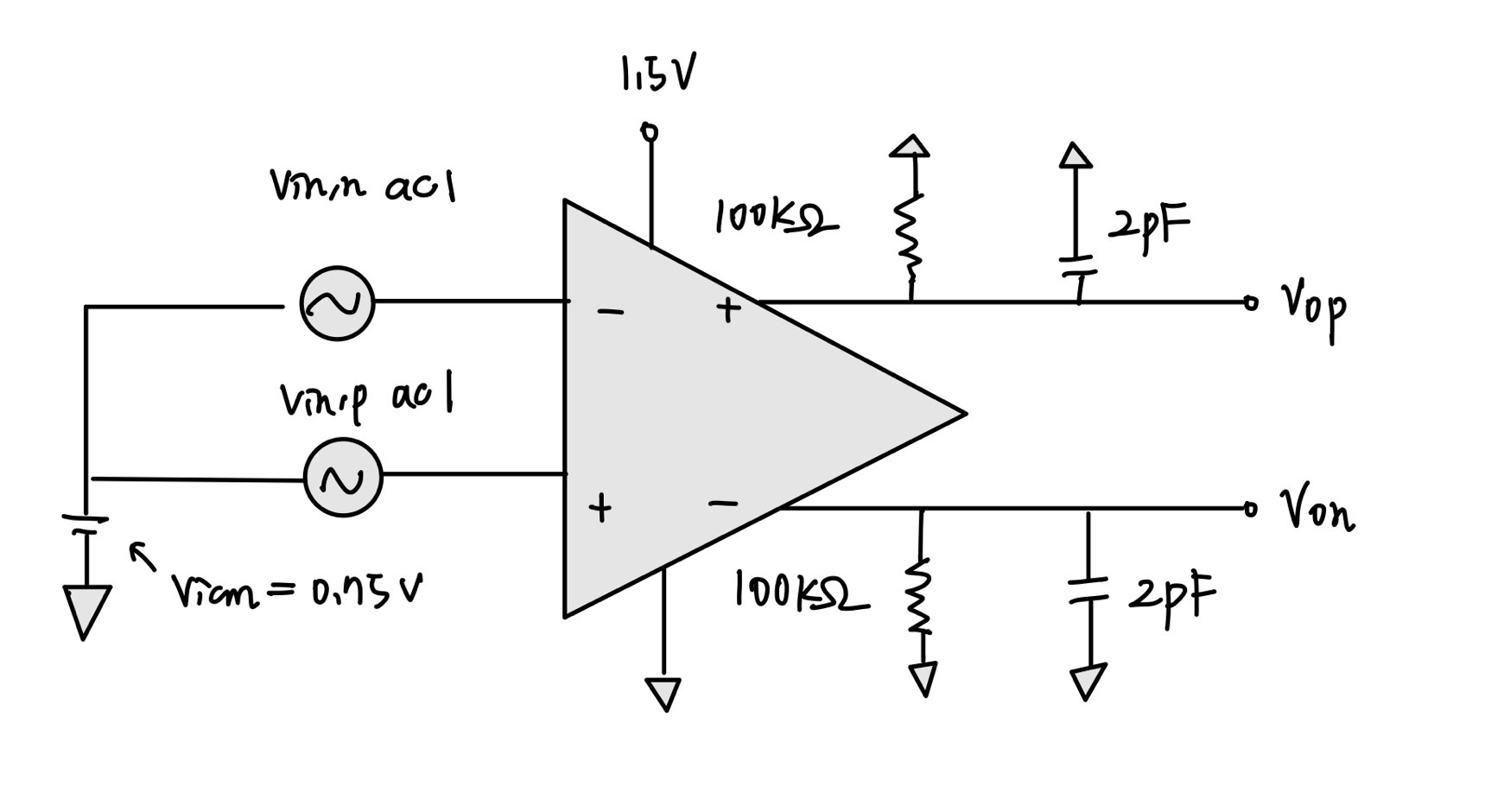
**Voltage (V)**

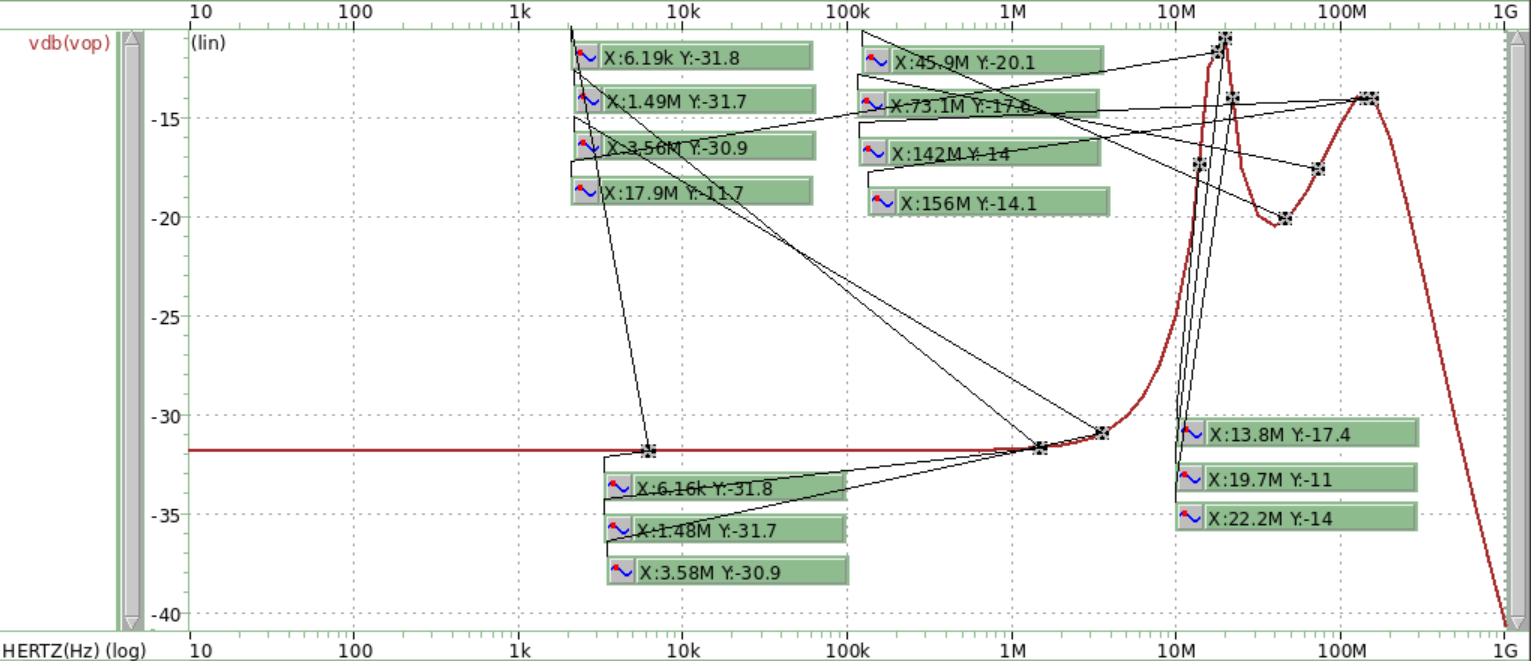
**Voltage (V)**

Fig3.2(a)

In the waveview above, I set the dc sweep range from 0.72V to 0.78V. From first and second panel, we can observe that the absolute value of slope in Vop and Von is 10.4k, which is a close value to the simulation value 10.3989k. The third panel demonstrates the differential gain, which is roughly two time larger than that in Vop and Von.

**3.3 Open-Loop Common Mode AC Response**





**Poles**

**Zeros**

**Frequency (Hz)**

**Gain (dB)**

Fig3.3(a)

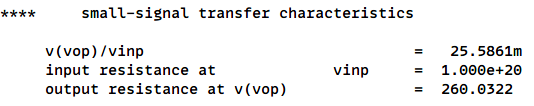




Fig3.3(b)

* The simulation CMRR = DC gain - acm\_in\_db = 80.34 + 31.84 = 112.18 dB > 90 dB



Fig3.3(c)

* **Dis.3.3**

**1. Hand Calculation of Gain**

The common mode feedback is designed to stabilize the output node Vocm.



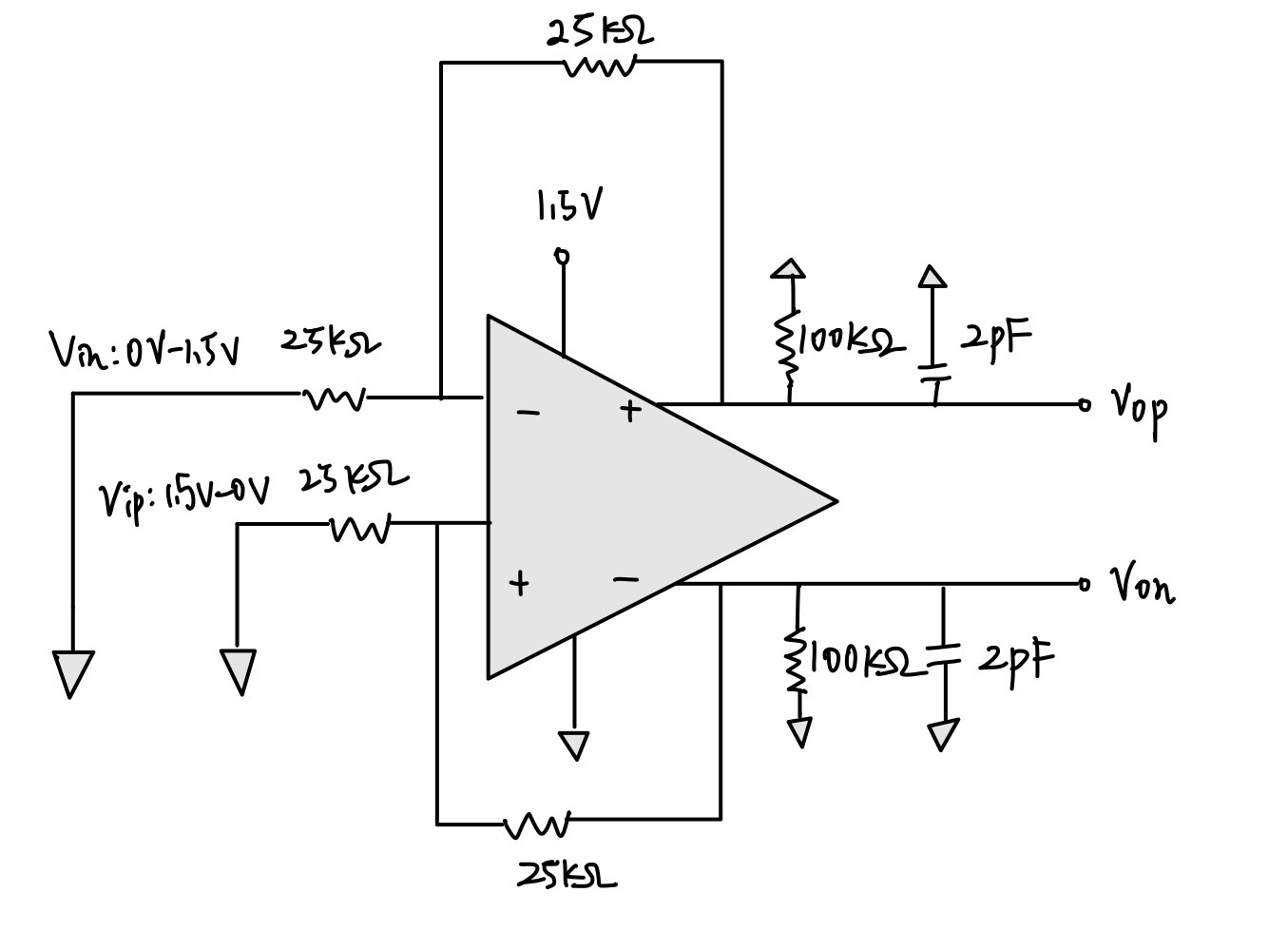
ACMC is the gain from the feedback node back to the OP, and ACMS is the gain from Von to the feedback node. Acm is composed of three stages, which are common mode, buffer and differential mode, the stages are solved by applying half-circuit method. The equation of derivation will be shown in the following.

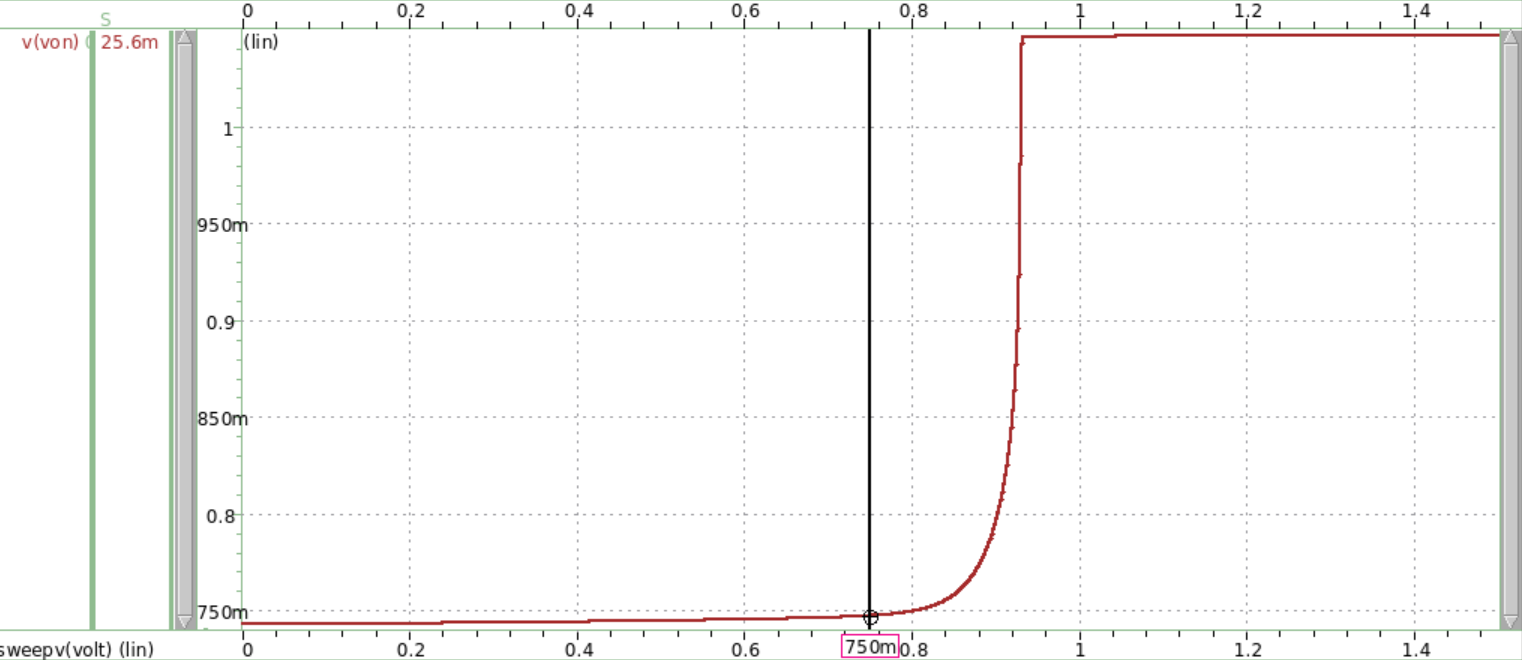
The error of common mode feedback gain compared to the simulation value is 0.344%, the error might come from the rough equation of ACMS, which neglects the resistances of transistors.

**2. Low Frequency Zero**

The calculated value of low frequency zero is close to the simulation result, error 0.093%

**3.4 Open-Loop Common Mode DC Sweep**





**Slope at VDD/2=25.6mV/V**

**Voltage (V)**

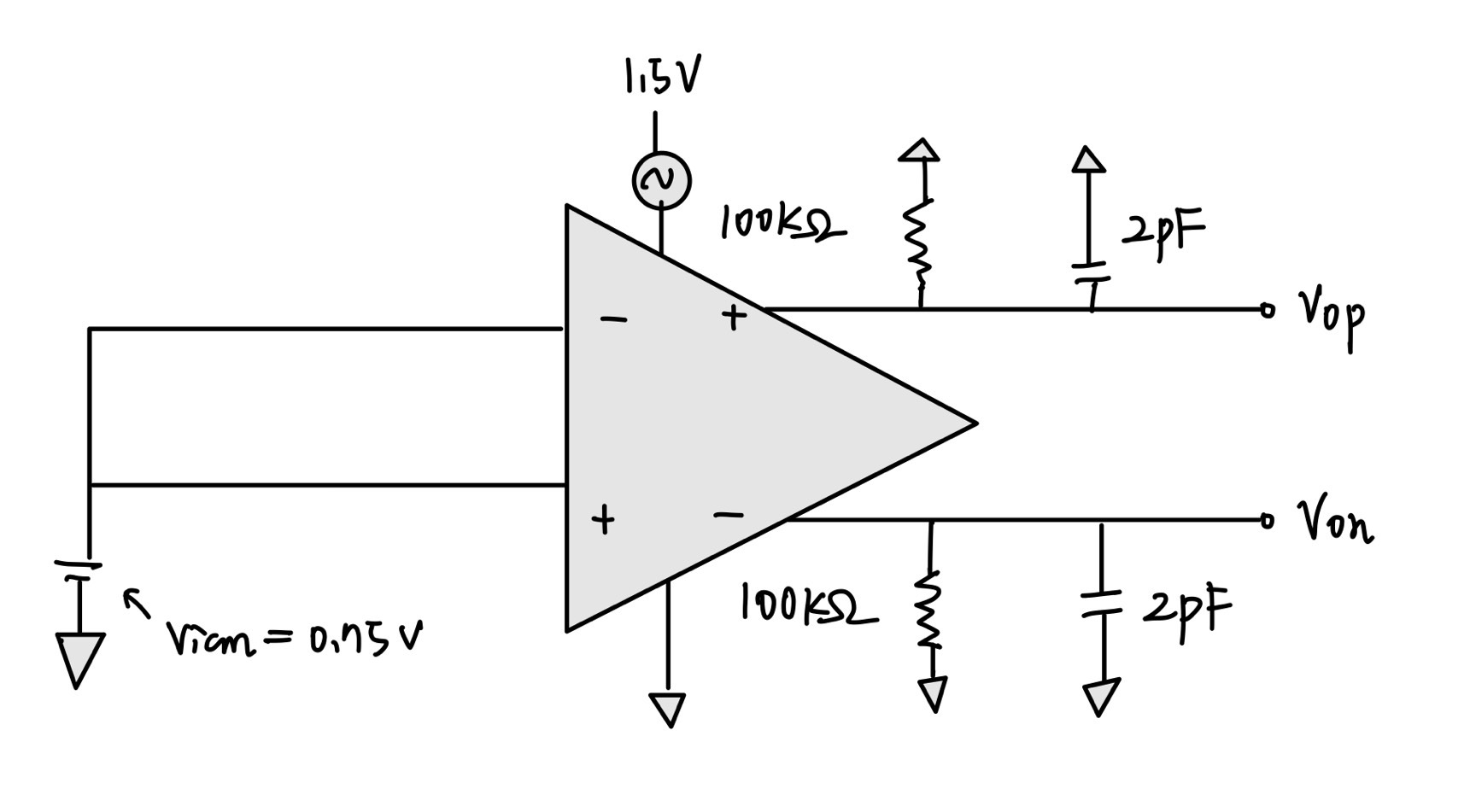
**Voltage (V)**

Fig3.4(a)

We can observe that the slope measured in the waveview is very close to the simulation value shown in below of 3.3(a) 25.5861mV/V.

**3.5 Open-Loop Power Supply AC Response**

**[ Positive Supply ]**



****

**Frequency (Hz)**

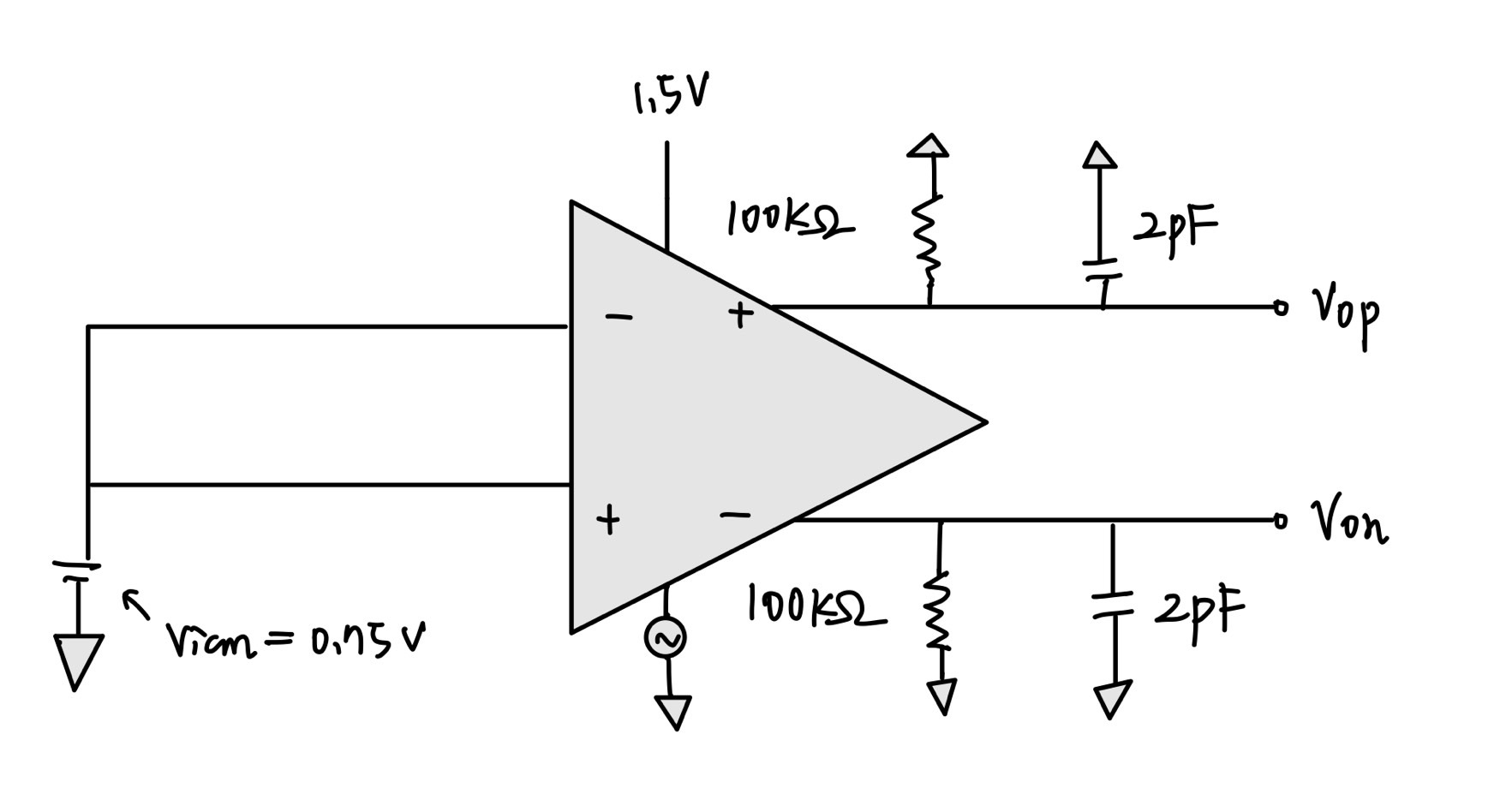
**Gain (dB)**

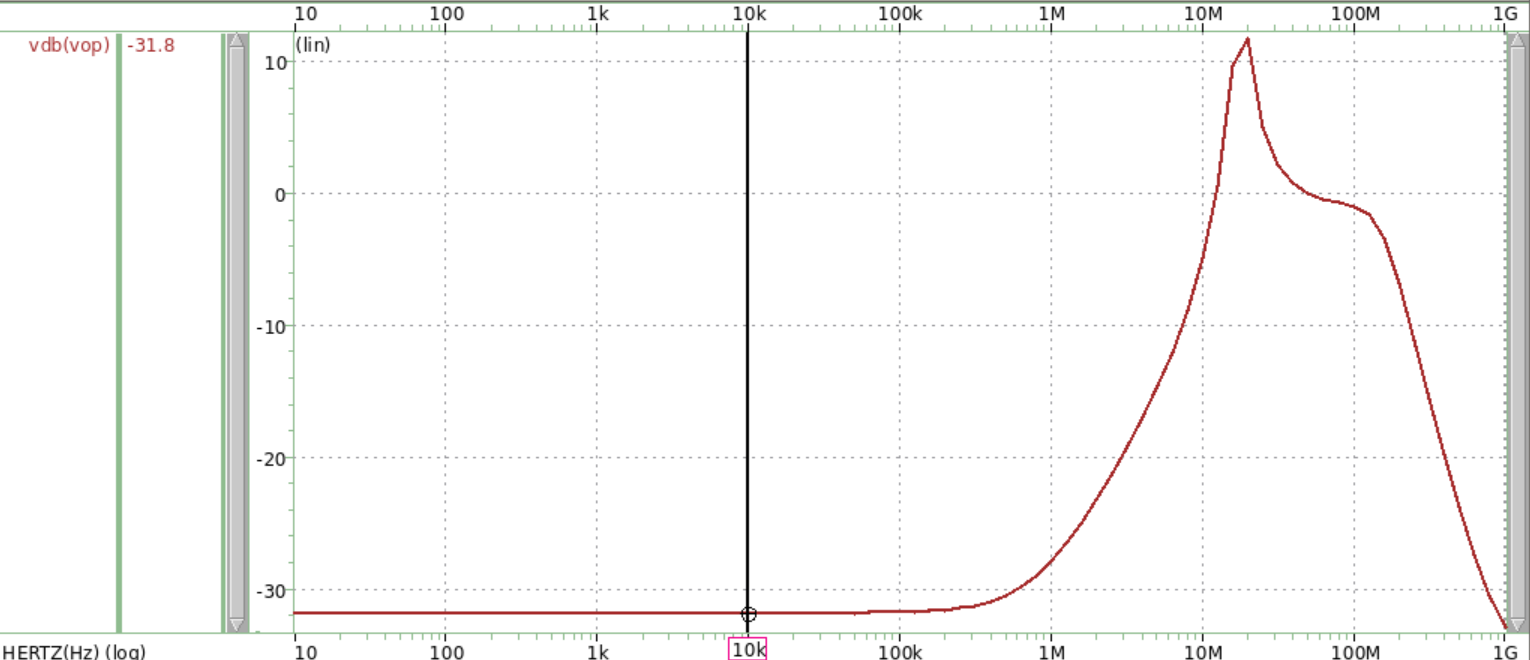
Fig3.5(a)



If we want a larger PSRR, a larger differential gain and a smaller supply small signal is required.

**[ Negative Supply ]**





**Frequency (Hz)**

**Gain (dB)**

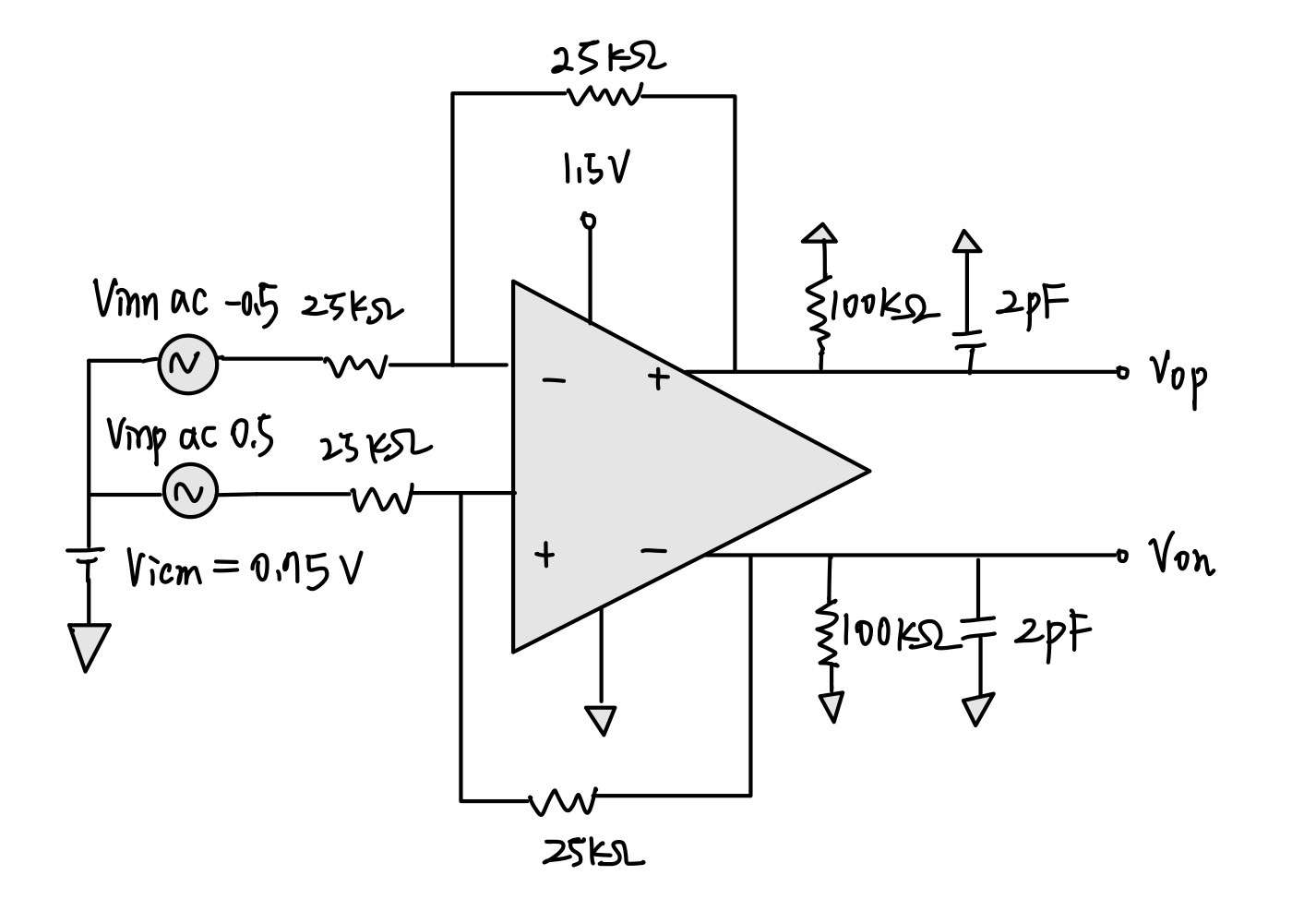
Fig3.5(b)

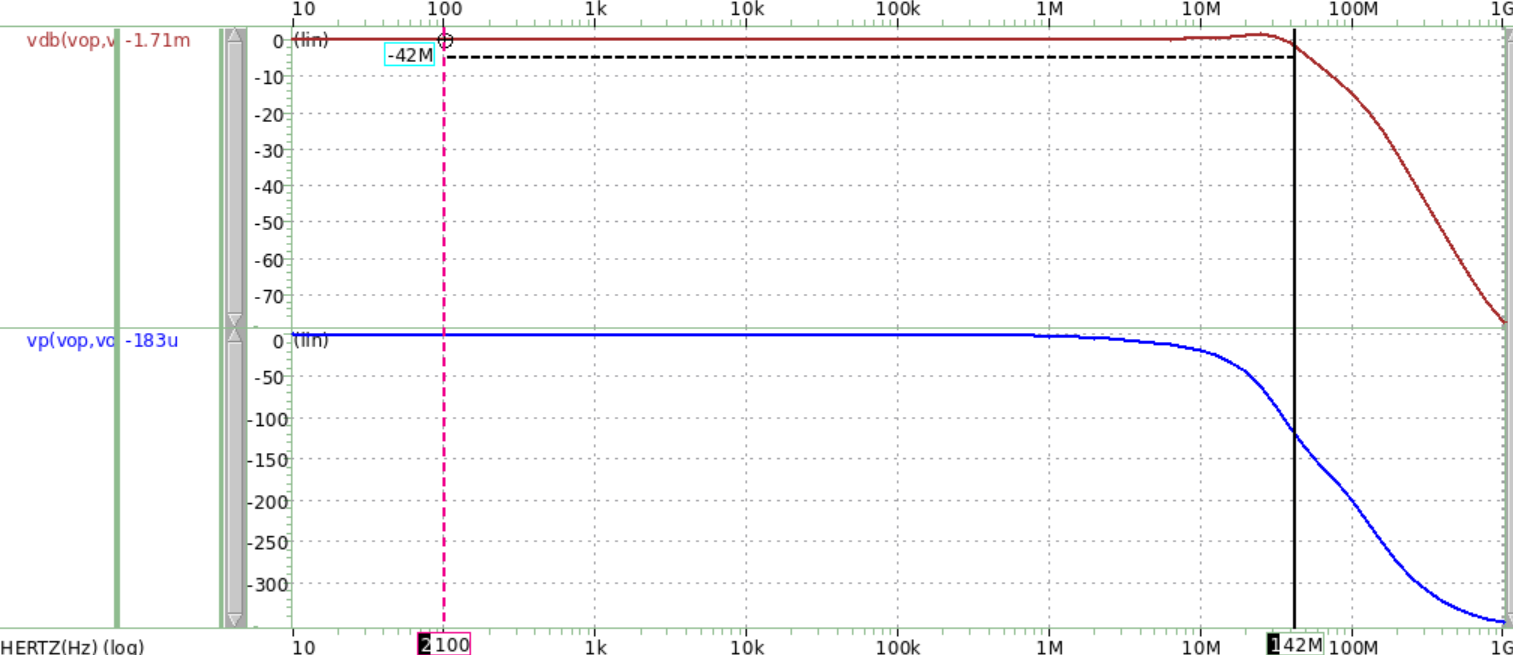


The testing signal is moved to the ground node compared to the positive supply question above.

If we want a larger PSRR, a larger differential gain and a smaller supply small signal is required.

**3.6 Closed Loop Differential Mode AC Response**





**-3 dB frequency = 42 MHz**

**Phase ()**

**Frequency (Hz)**

**Gain (dB)**

Fig3.6(a)



In the waveview above, I measured the -3dB frequency by finding the gain 1.4482 (max\_gain) - 3dB = -1.5518 dB and see what frequency value does it point to on the x-axis.

* **Dis.3.6(b)**

**1. Hand Calculation for Gain**

From the equation of the forward feedback amplifier taught in electronics I, we know that

The error of hand calculation compared to the simulation result is 0.0004%, we can assume that the equations are correct.

**2. -3dB Bandwidth**

From the hand calculation, the error is considerable, I consider that the error comes from the poles and zeros that aren’t considered. My open loop system might not be stable and ideal enough, so the equation might be more complicated than just a term.

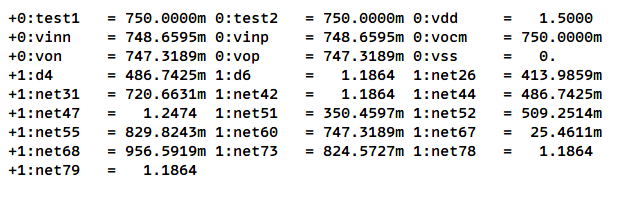


Fig3.6(c)

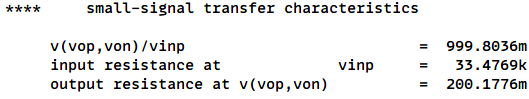
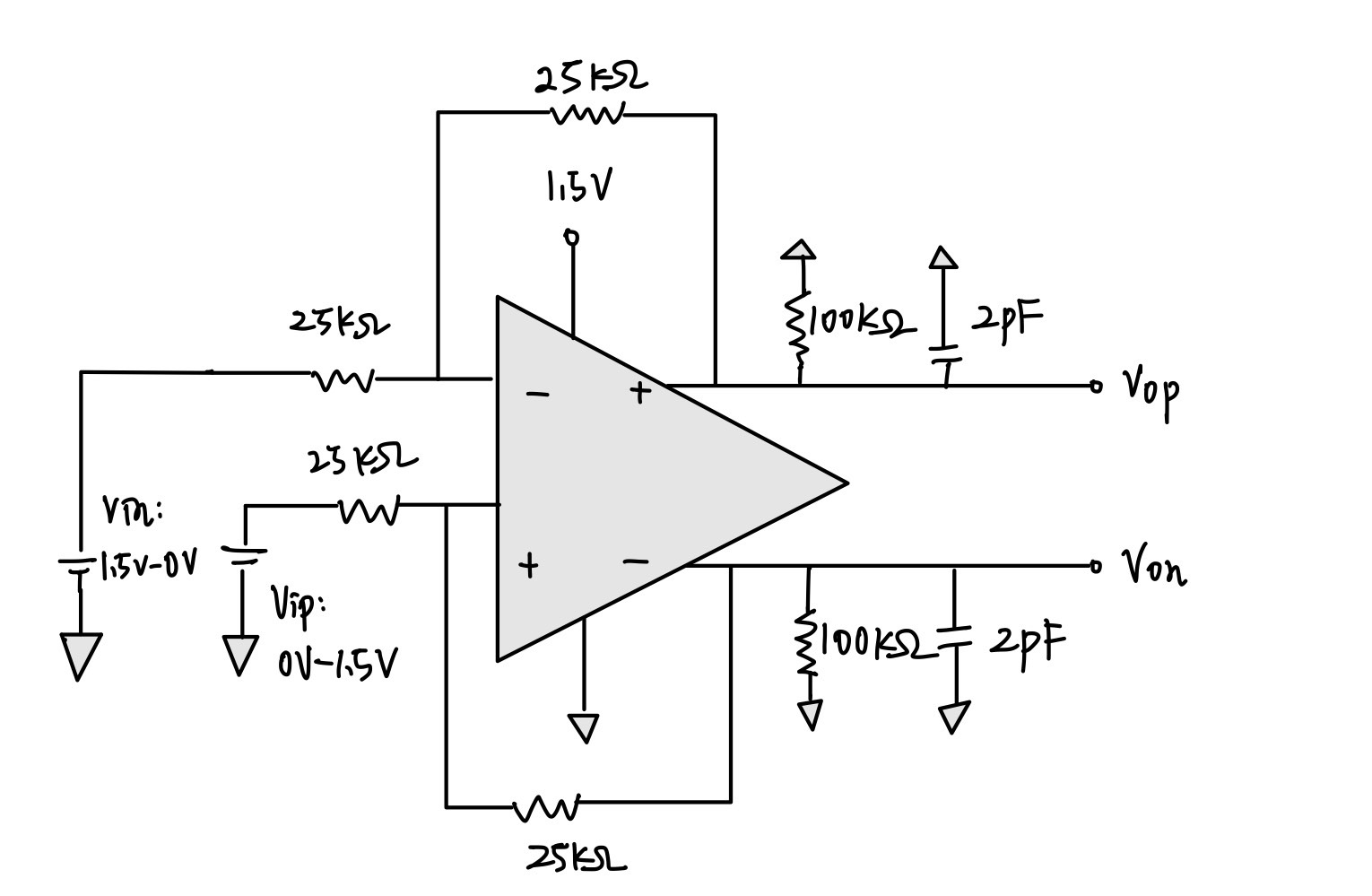
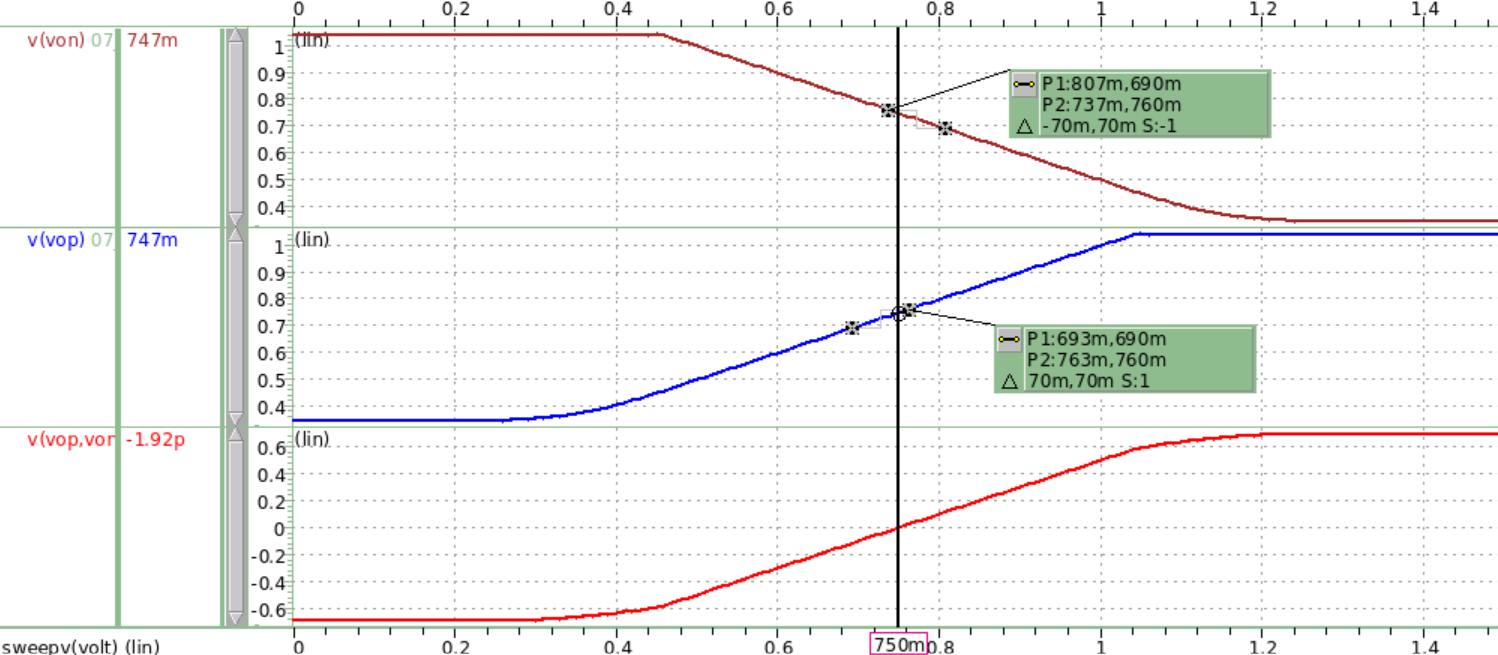


Fig3.6(d)

**3.7 Closed Loop Differential Mode DC Sweep**





**Vop-Von=0V**

**Vop=0.747V**

**Von=0.747V**

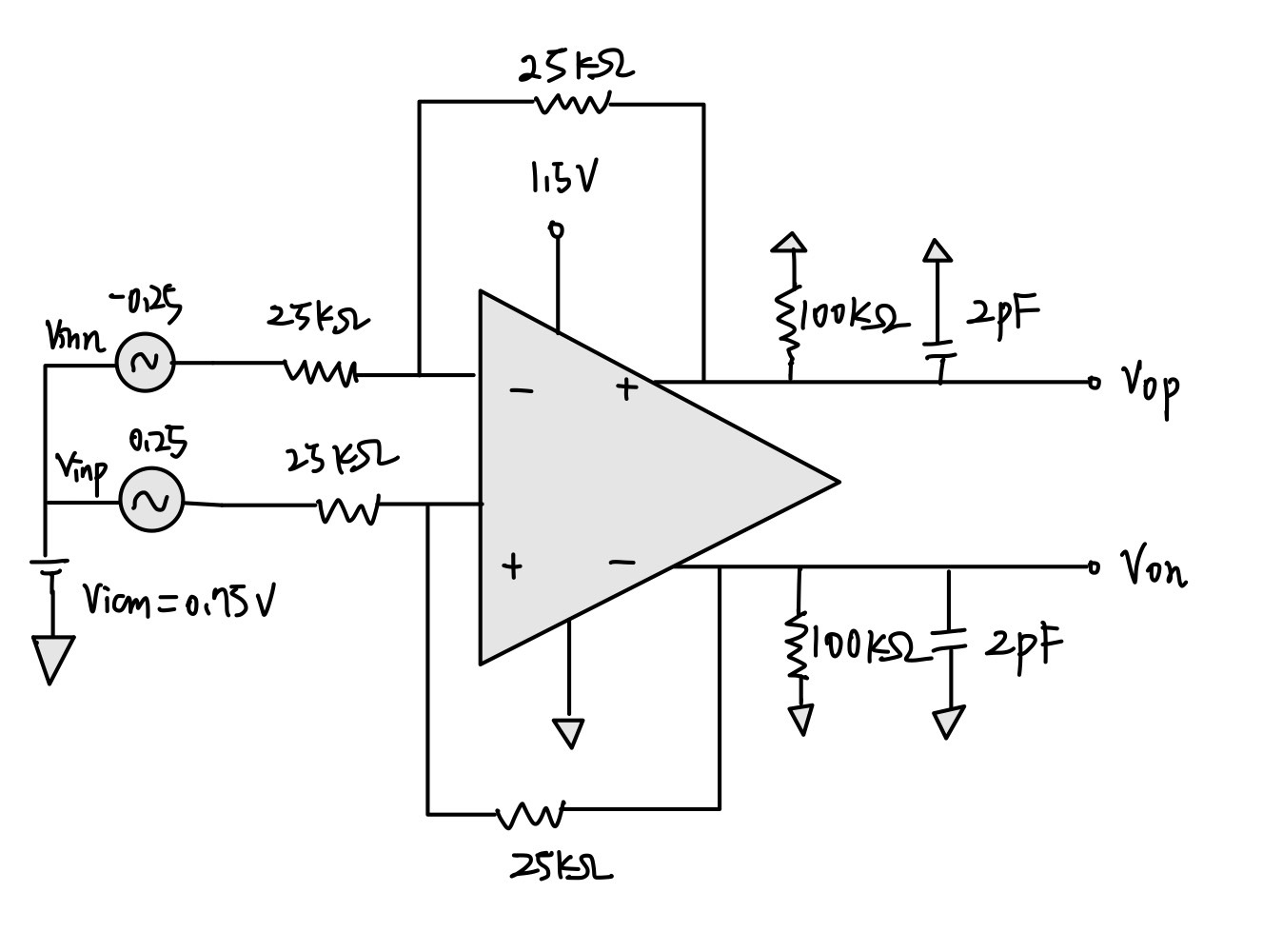
**Voltage (V)**

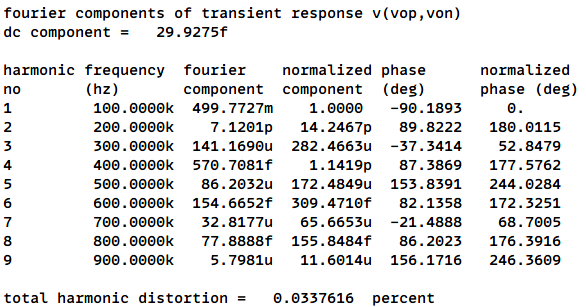
**Voltage (V)**

Fig3.7(a)

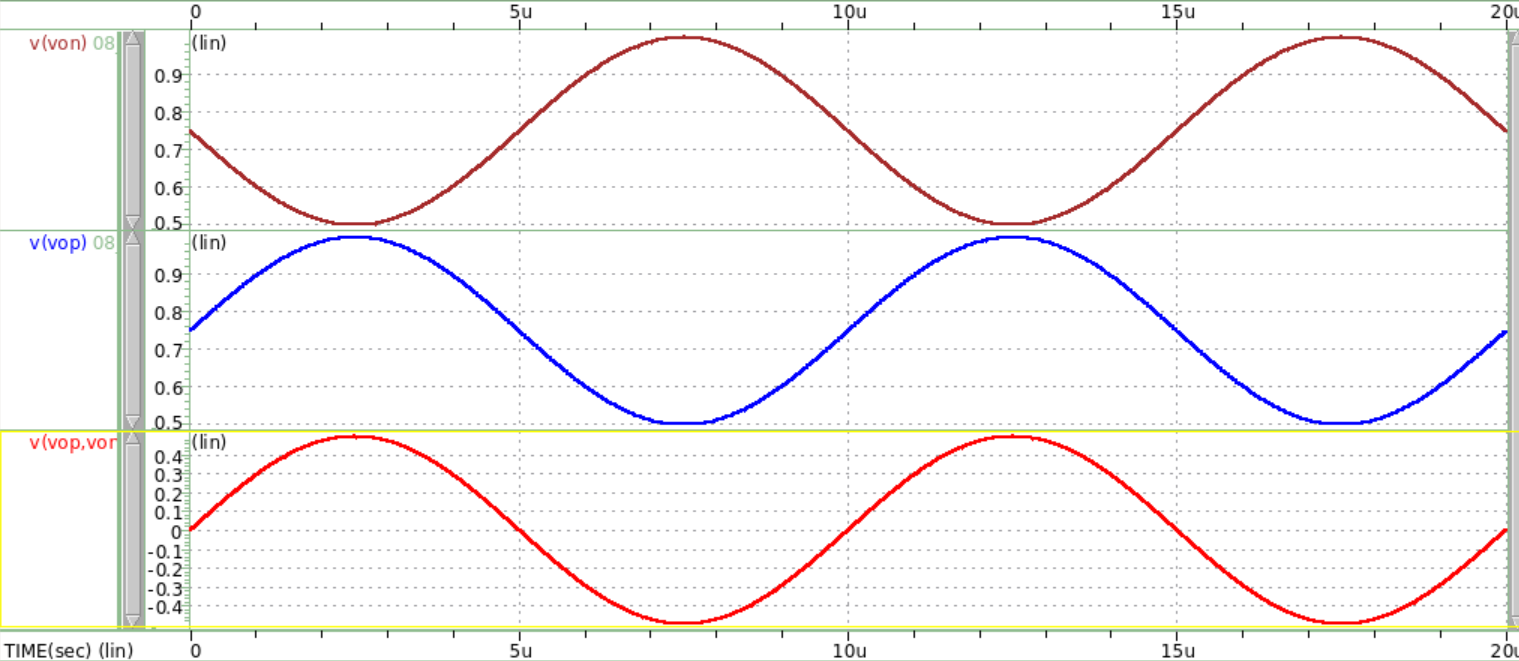
The waveview in Fig3.7(a) indicates that when the absolute value of Vin and Vip are 750mV, the corresponding Von and Vop are 0.747 according to the measurement. Moreover, when measuring the slope around input 750mV, we can observe the slope (differential ac gain) is 1(V/V), which is really close to our hand calculation .

**3.8 Closed Loop Distortion Simulation**





**THD < 0.1 percent**



**Time (s)**

**Voltage (V)**

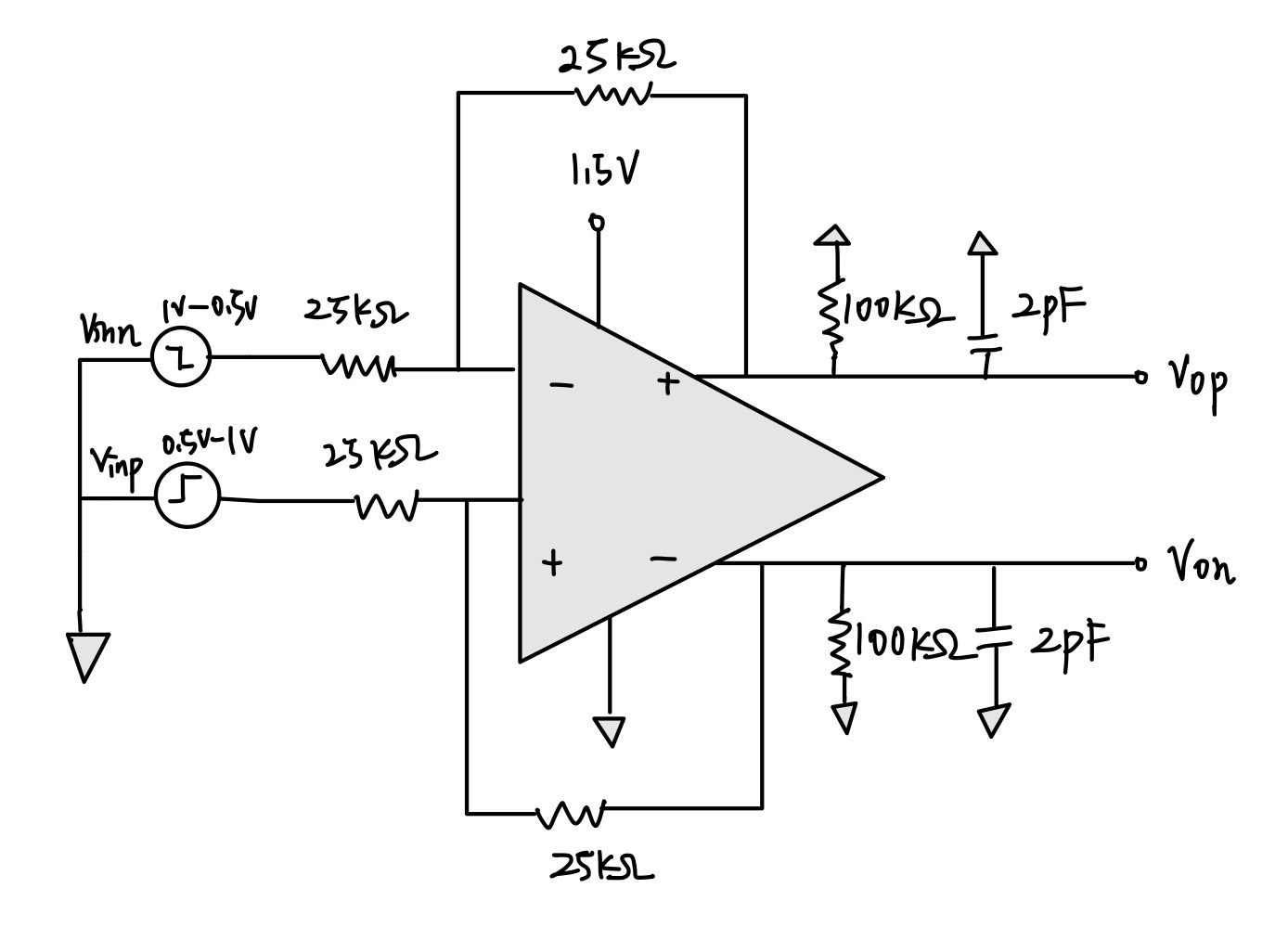
**Output Swing = 1V**

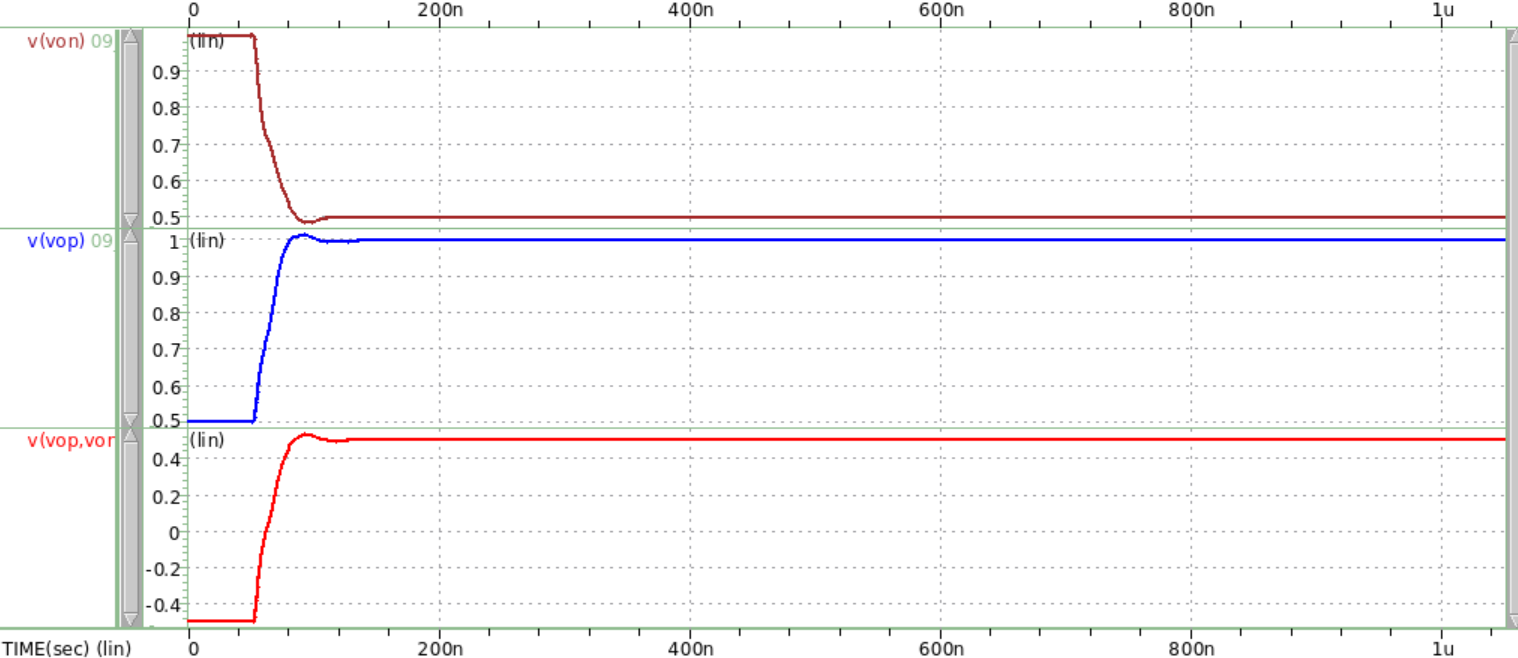
Fig3.8(a)

The Total Harmonic Distortion is calculated using the RMS values of the harmonic components as follows: where V1 is the RMS value of the fundamental frequency, and V2, V3,… are the RMS values of the second, third, fourth, etc., harmonics. The values of them are derived from complicated Fourier Transform. Observing the THD results simulated, I found that differential ouput THD is relatively smaller than the singled ended output THD, this is because differential mode might eliminate the components of even harmonics, therefore reducing the value of the numerator, leading to a smaller THD value.

My differential output THD value is .

**3.9 Closed Loop Step Response**





**Differential Vop-Von**

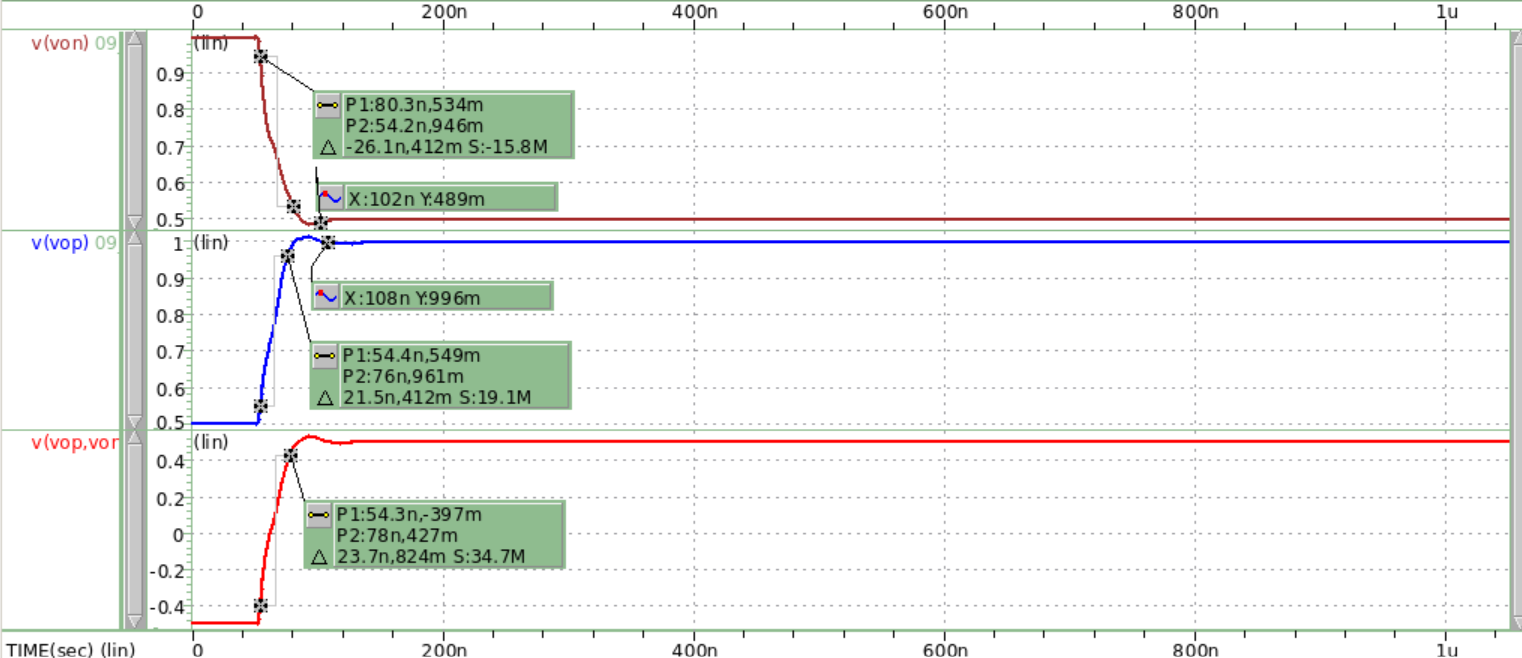
**Single-Ended Vop**

**Single-Ended Von**

**Voltage (V)**

**Time (s)**

Fig3.9(a)



**Measured 10%-90% SR-**

**Measured 10%-90% SR+**

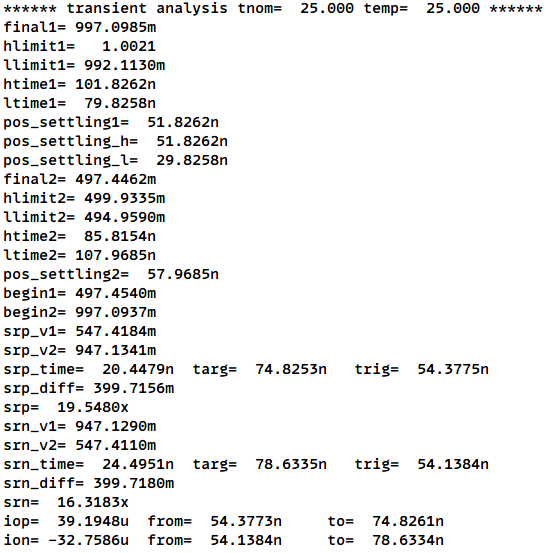
**Settling Time+ = 107.9685 ns-50 ns = 57.9685 ns**

**Settling Time- = 101.8262 ns-50 ns = 51.8262 ns**

**Voltage (V)**

**Time (s)**

Fig3.9(b)



The simulation results above indicate that the positive settling time is 51.8262 (ns), the negative settling time is 57.9685 (ns), the positive slew rate is 19.5480 (V/us), and the negative slew rate is 16.3183 (V/us). The values mentioned above all meet the requirements of the specification. For slew rate, it is generated by the external node of the circuit, the calculations are shown in the following, and the error might come from the preciseness of the mean discharging time.

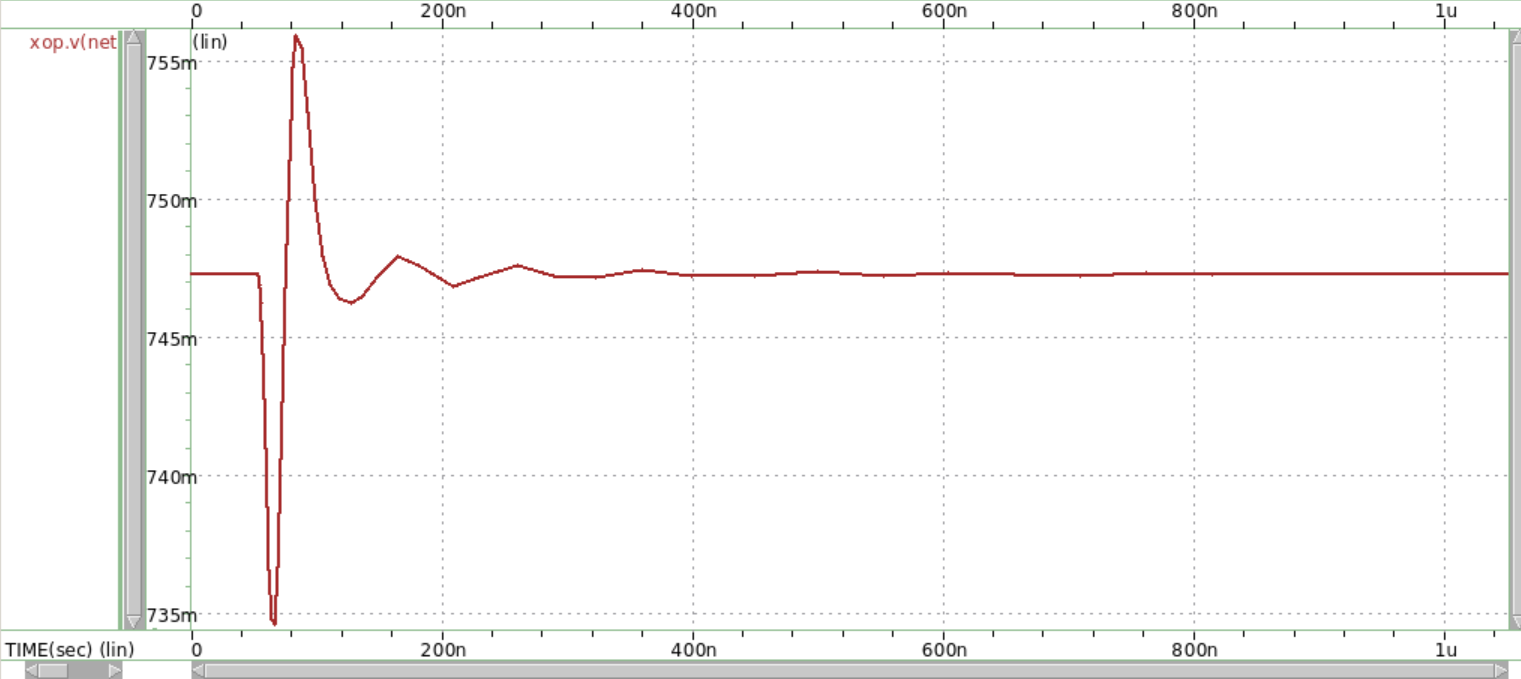


Fig3.9(c) common mode sensing node

* The common mode sensing node is located at the gate of MCM1
* **Dis.3.9(d)**

To enhance the common mode settling time and examine CMFB performance during step transients, I investigated different cases by modifying compensation elements to assess stability under normal and light load conditions. I found that reducing the damping ratio, which is closely linked to phase margin and bandwidth, is critical to decreasing settling time. Achieving an optimal phase margin and bandwidth results in a lower damping ratio, thus reducing settling time. The efficiency of the CMFB loop directly affects settling time; I discovered that optimizing Rz and Cc bolsters overall stability and shortens settling time. During step transients, the CMFB circuit mitigates deviations by averaging Von and Vop, comparing the result to the target common mode voltage, and making adjustments via the error amplifier. This feedback mechanism ensures the common mode voltage quickly returns to its intended value. By concentrating on these factors, I was able to design a system with reduced settling time and improved stability for various load conditions.

1. **Design Considerations**

**(a) Device Values and operation point selection**

**1. Startup circuit, Constant gm, Bias stage**

For the design of constant gm, I chose to let the bias gate voltage of MB3, MB4 to be at roughly 0.5V, to achieve this, I designed the startup circuit to operate in the mechanism described in Dis.1(b), where MB1 is forced to be in subthreshold region and MB2, MB3 is in linear region and saturation region respectively, and the operating region can be controlled by increasing the length of MB1 largely. By doing this, my start up circuit is able to activate the constant gm circuit. Because we know that the current of MB4 and MB5 are same, so by the derivation of Dis.1(a), I found that choosing size of MB5 four times of MB4 can make control on gm4 easier by just adjusting the value of Rb. Finally, the bias voltage at net52 can be stabilized to around 0.5V when value of Rb is chosen to be 7.3k. Moreover, in the bias stage, I want to design to send a roughly 0.95V bias to pmos transistors in the main circuit. In this stage, MB9 is diode connected, so if I want to create a higher node voltage at net68, larger size in MB9 is required compared to MB8, and finally a size of 10 times larger than MB8 is chosen for MB9.

**2. Design of Frequency and Time Domain**

From the experience of HW6, I know that if I want to get a larger unity gain bandwidth and a more stable system, non-dominant poles are required to push away from the unity gain frequency. The reason is that if number of poles is larger, the decreasing slope of gain will stack up and lead to a more rapid reduction in gain. Referred to the equation of the second pole, I consider to let the size M10 bigger to increase gm10 to get a larger pole 2; Besides, making gm12 larger is also an approach by increasing the current of source follower. Next, zero is also considered to be pulled before the unity gain frequency. This is because zero can alleviate the reduction of gain and phase. From the equation of zero, it is obvious that compensation resistors and capacitors are crucial for it. A larger Cc can lead to a smaller zero, but on the other hand, a larger Cc can cause worse settling time and slew rate, so for design consideration, I prefer to maintain Cc in a small value (0.73pF). Lastly, small Cc value leads to a larger dominant pole (mainly controlled by gm6), and trade-off is presented on phase margin when unity gain bandwidth increases. Therefore, It is important to make decisions on compensation devices and gm6, gm10 values to achieve better performance.

**3. Design of Gain**

Gain is composed of three stages mentioned in the previous section, the first stage and second stage are the main contributing stages. The buffer stage (source follower) is designed not for gain purpose, so I will neglect the discussion of buffer gain in this part. From equation of gain, Av=gm1(ro2 || ro4) for the first stage and Av=gm6(ro6 || ro7) for the second stage. It is simple at first to design larger gm1 and gm6, but later I found that there are some trade-offs between gain and the phase margin when choosing the value of gm6. Therefore, gm6 cannot be too large or too small, so I change my strategy to adjust the output resistances. By testing the trends, I found that increasing W/L of M1, M2 and M6, M8 pairs can increase gain. But one the other hand, a too large M6, M8 W/L might lead to an unbalanced dilemma between unity gain frequency and phase margin due to the effect of poles and zero. Besides, although multiplying a buffer gain will decrease the total gain, it plays an important role for reducing output impedance to minimize the loading effect when different stages are connected together, and thus preventing the gain to drop too much (loading effect shown in HW3 cascade).

**4. Design of THD**

I found that in the circuit, the source follower contributes to the THD most significantly (M10-13). The trend is to enlarge W/L of M10 and M12, while decreasing W/L of M11 and M13. Note that increasing M10 and M12 size will also bring up the current value, so I have to control the size not to be too large to suppress the current within 0.4mA. Moreover, I found that when Von and Vop are farther from Vdd/2, THD may be more stable and lower.

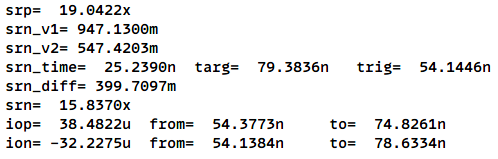
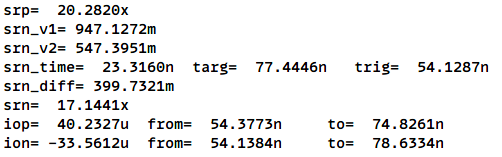
**5. Design of Common Mode FeedBack**

Because the circuit without common mode feedback will let Von and Vop change dramatically, and therefore run out of the value range of Vdd/2±1%, so a CMFB is required to correct and modify the Von and Vop value back into the range. In the CMFB block, the current is designed to be very low to reduce the total Vdd current, and it is controlled by the size of MCM5. To modify the values of Von and Vop, sizes of MCM3 and MCM4 can be adjusted to control them without changing the gain, phase margin, unity gain bandwidth and other specifications, which is the most advantageous point compared to circuit without CMFB.

**(b) Compensation**

Compensation design is mainly focused on the determination of Rz and Cc. Initially, I observed the trends with settling time, phase margin, bandwidth and slew rate. As mentioned previously, I designed Rz > 1/gm6 to let zero fall in the left half-sided plane. That is, Rz have to be large enough to meet the requirement, but on the other hand, the increasing of Rz will cause phase margin to reduce largely and unity frequency bandwidth to increase but not too much. Therefore, Rz should be adjusted by observing and assisting the Cc effect (main consideration).

Now considering Cc effect, it is the main influence for slew rate. When Cc decreases, slew rate increases, the trend is shown in the following graphs.



Cc=0.75pF

Cc=0.7pF

From simulation, I found that output node current is larger when Cc is smaller, indicates that the average current through the load capacitor increases. But there is a trade-off between phase and bandwidth, so Cc cannot be too small either. Finally, I seeked out a balance between small Cc and sufficient phase margin, unity gain bandwidth. (Rz = 4.8k, Cc = 0.73pF)

**(c) Supply Voltage**

Comparing different supply voltages, I tried to design 1.3V and 1.5V. Initially, I used 1.3V to design,

the first problem I encountered was the limitation when increasing gain, because the supply voltage was too small, the current flow in main circuit need to be large enough to compensate the lack of node bias voltages. Secondly, when performing closed loop ac response, transistors of my first stage and second stage amplifier could be easily falling into linear region, this was because my voltage distribution across all the current path is not well designed. Later, I decided to use 1.5V as my supply voltage. With a larger voltage swing, larger phase margin and unity gain frequency can be achieved using smaller current. Additionally, I found that higher supply voltages might contribute to a lower THD , and the output linearity is better than other lower supply voltages.

**(d) Optimizing Performance**

By integrating all the concepts above, to fulfill all the specifications, including gain bandwidth over 100 MHz, phase margin over 45 degree, gain over 80dB, current below 0.4mA, and all step transient specifications, I have to reduce the current of the CMFB and the startup, constant gm circuit to ensure that the current of first stage, second stage and buffer stage are enough. Next, improve my THD by adjusting sizes from M10 to M13. Then, a small Cc is set to get a larger slew rate as my fixed criterion and adjust gm6, gm10 and gm12 to firstly improve my unity gain frequency. Next, pick a suitable Rz to balance between phase margin and unity gain frequency. Finally, settling time can be controlled not only by small Cc, but also the CMFB (MCM3, MCM4), and next, check if my Von and Vop are around Vdd/2. My final design and optimization flow is completely described above.

* ***Trade-offs encountered when designing:***

***(the parameters in brackets are the influencing factor )***

1. Gain / Unity gain frequency (M6, M7)

2. Gain Bandwidth / Phase Margin (Rz)

3. Unity gain frequency / Phase Margin (Zero)

4. Slew rate / Settling Time (Cc)

5. Gain / Total Current (gm, M1, M2, M6, M7)

6. Slew rate / Total Current (Ion, Iop)

7. Gain / THD (Buffer current)

1. **Discussions**

(a) Experience and challenges encountered in the project

在做此次Final Project時，與之前作業不同的地方是將所有之前作業與上課所學的不同級電路與觀念都整合在一起，從最基礎的尺寸對Vth、電流等等相關參數的變化，到後來設計差動電路再到設計進階folded cascode電路，學到能應用在此project的很多觀念，例如diode connected電路該怎麼設計、pole與zero該怎麼分配phase margin與unity gain bandwidth等等觀念。在設計的時候，遇到的最大困難是對於補償頻率系統如何與phase margin、unity gain bandwidth互補提升performance，並且在調完上述的參數後，進行到step transient分析時，才發現Cc與Rz有一定的大小限制才能使系統穩定，否則settling time會變很大或者slew rate會變很小，因此後來重新設計時是固定補償電容Cc在較小值並調整主電路不同級的尺寸並配合Rz的修正來達到所有規格的方法。另外一點我一開始遇到的困難是還沒找到大致應該調整參數的順序，例如在前幾次我都是先依照檔案名稱的順序來一個一個看有無符合規格，但在達到phase margin那些pole / zero的規格後，發現THD非常大，但在嘗試幾次後發現THD主要由CMFB主導，因此我才知道先調THD (M10-M13)再調主放大器電路尺寸並不會影響frequency domain的規格太多。後來我發現settling time因為我的補償電容太大導致系統穩定時間太長，且slew rate也沒有達到標準，因此學到這些教訓之後我才慢慢有概念這個龐大電路運作設計的先後順序，最後使用1.5V的電壓源做到其他規格全滿，只有被扣除電壓源的分數2分。

(b) Summarizing key insights and lessons learned from the project and the course

我認為這次project最重要的地方是frequency與time domain的分析，好的系統要將pole 1、pole 2與主導的zero設計在對的位置才能最優化phase margin、unity gain frequency的值，再來，我認為其次重要的是電流分配的設計，因為我將電流設置0.4mA以下，因此在此情況下gain需要足夠的電流支持才能達到更大值。我認為此門課與電子學不同在於每次作業的hspice實作，除了了解每次電路的功能與設計之外，我也學到了許多助教範例的參數量測語法和一些FoM基本會看的參數指標，在以後若設計類比電路時也能有條理的去分析我所設計電路的好壞；另一方面，有時上課我發現老師的進度會越講越快，有時候會跟不上老師分析電路的速度，導致下半節課聽不太懂，希望未來老師授課時能將前面電子學基礎觀念加快講課速度，並在後面從頻率響應部分能舉更多範例練習來解釋觀念。這門課算是在這學期中花最多時間在做作業的科目，但也是相對來說我學習到最多的課，在最後的final project報告中我選擇使用英文撰寫，希望在這種大型專案報告中寫的正式一點，學習寫論文或是正式報告的精神。最後感謝助教每次出作業與批改時的用心，雖然很多同學不滿意天梯制度造成惡性鬥爭，但我認為這也是推動我們進步的一大動力，提醒我們任何設計沒有最好，只有更好。

1. **Reference**

1. HW1~HW6

2. Reference Circuit