Analog IC Design Final Project

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I. Schematic and Small Signal Parameters of Active Devices

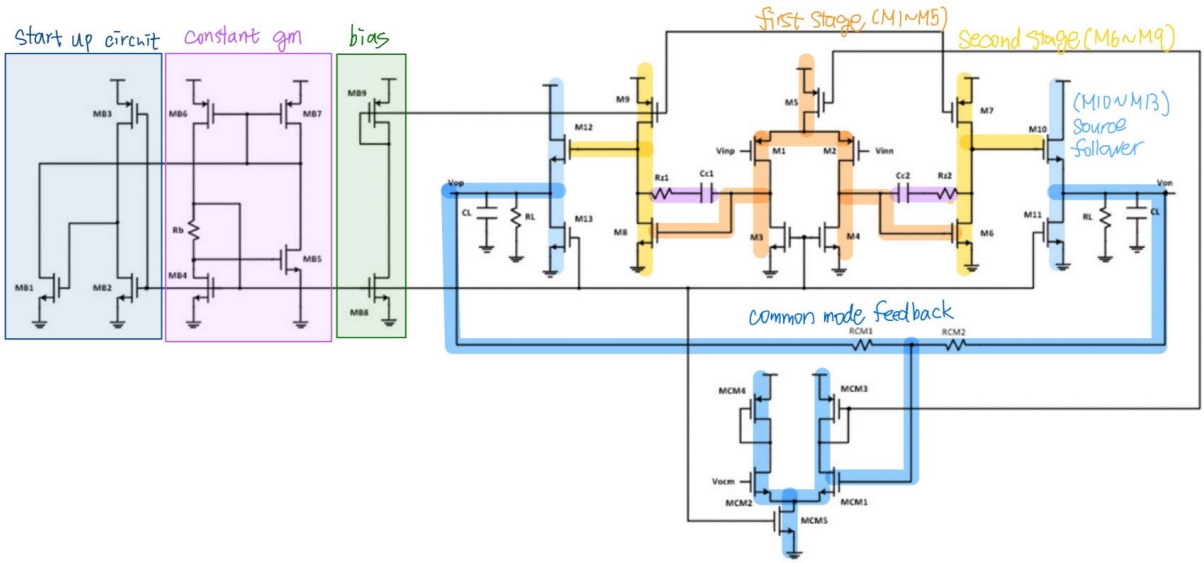


Fig1-1. Different Stages in the OPAMP

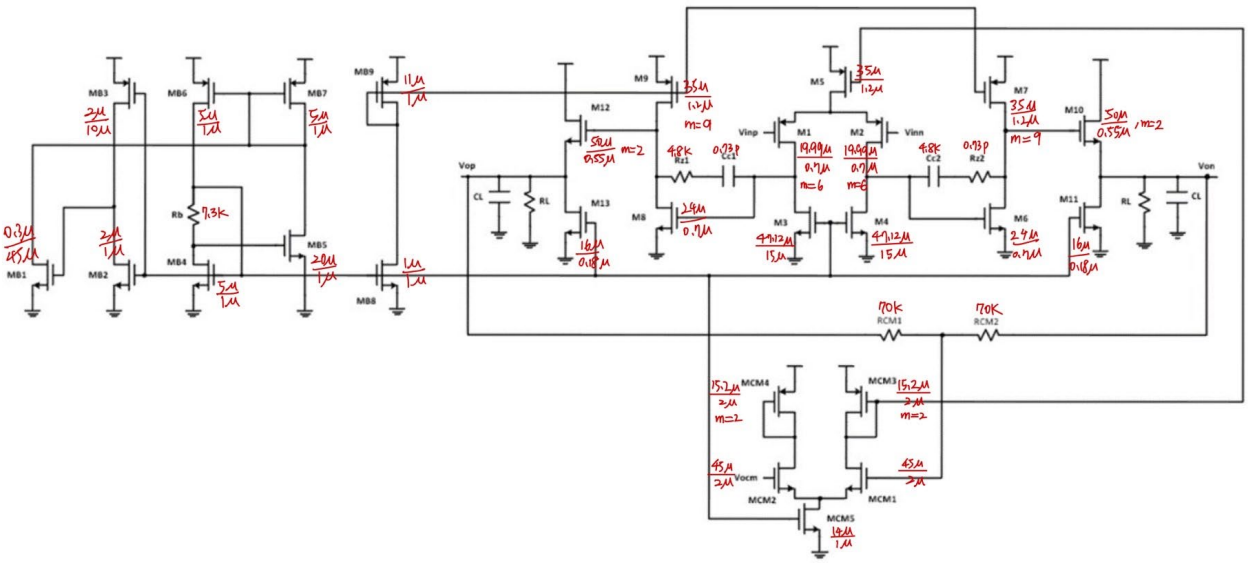


Fig1-2. My Designed Sizes of Transistors and compensation Resistors/Capacitors

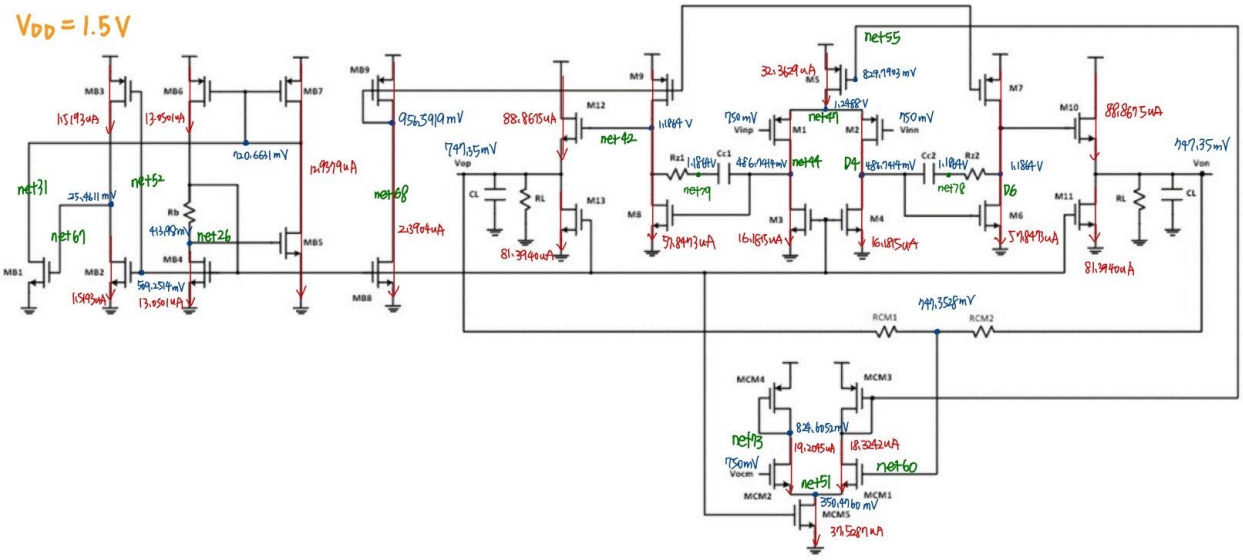


Fig1-3. Node Voltages, Branch Current and Nets

- **Transistor Parameters**

subckt	xop	xop	xop	xop	xop	xop	xop	xop	xop
element	1:mb1	1:mb2	1:mb3	1:mb4	1:mb5	1:mb6	1:mb7	1:mb8	1:mb9
model	0:n_18.1	0:n_18.1	0:p_18.1	0:n_18.1	0:n_18.1	0:p_18.1	0:p_18.1	0:n_18.1	0:p_18.1
region	Subth	Linear	Saturation	Saturation	Saturation	Saturation	Saturation	Saturation	Saturation
id	272.1984f	1.5193u	-1.5193u	13.0501u	12.9379u	-13.0501u	-12.9379u	2.3904u	-2.3904u
ibs	-6.468e-28	-3.379e-22	2.076e-22	-2.309e-21	-1.996e-21	1.426e-21	1.414e-21	-7.126e-22	2.374e-22
ibd	-67.7106a	-5.4443a	193.7660a	-176.1073a	-1.0689f	260.2563a	204.7210a	-137.0980a	285.4238a
vgs	25.4611m	509.2514m	-990.7486m	509.2514m	413.9859m	-779.3369m	-779.3369m	509.2514m	-543.4081m
vds	720.6631m	25.4611m	-1.4745	413.9859m	720.6631m	-990.7486m	-779.3369m	956.5919m	-543.4081m
vbs	0.	0.	0.	0.	0.	0.	0.	0.	0.
vth	311.8930m	396.9924m	-462.9999m	388.6948m	383.4642m	-495.6982m	-495.6982m	397.2984m	-494.6265m
vdsat	35.1589m	125.2233m	-453.8160m	130.9688m	77.2369m	-264.0471m	-264.0461m	125.5823m	-90.2889m
vod	-286.4319m	112.2589m	-527.7487m	120.5566m	30.5216m	-283.6387m	-283.6387m	111.9530m	-48.7816m
beta	1.8305u	620.5832u	12.6417u	1.5559m	6.2131m	337.3257u	337.3258u	308.4958u	799.0479u
gam eff	507.4459m	507.4460m	557.0846m	507.4461m	507.4460m	557.0846m	557.0846m	507.4461m	557.0847m
gm	9.8962p	13.4978u	5.2814u	164.1586u	249.3230u	81.2287u	80.5004u	31.2551u	40.6497u
gds	5.2555f	52.5328u	4.5148n	2.2038u	2.6768u	478.1867n	592.9742n	336.8836n	144.1214n
gmb	2.2619p	2.8398u	1.7602u	33.1590u	51.3886u	25.2500u	25.0209u	6.2383u	12.2303u
cdtot	508.6133a	14.0381f	2.2065f	7.1589f	26.4070f	5.5564f	5.7599f	1.3764f	13.0063f
cgtot	25.9000f	16.1915f	126.4211f	34.2728f	115.4845f	32.5806f	32.5915f	6.8219f	63.1253f
cstot	609.0552a	16.4802f	143.7326f	38.4362f	124.7089f	38.3603f	38.3551f	7.7634f	70.9216f
cbtot	26.5471f	8.5253f	45.1037f	19.1668f	74.4593f	18.2441f	18.4318f	3.9046f	40.8764f
cgs	119.3011a	10.5980f	116.9829f	29.8184f	92.3950f	28.6458f	28.6521f	5.9104f	51.4617f
cgd	116.4894a	5.0349f	738.7069a	1.7971f	7.2488f	1.7991f	1.8065f	354.4127a	3.9556f

Fig1-4. Start-Up and Bias circuit (MB1~MB9)

xop 1:m1 0:p_18.1	xop 1:m2 0:p_18.1	xop 1:m3 0:n_18.1	xop 1:m4 0:n_18.1	xop 1:m5 0:p_18.1
Saturation	Saturation	Saturation	Saturation	Saturation
-16.1815u	-16.1815u	16.1815u	16.1815u	-32.3629u
1.547e-21	1.547e-21	-2.426e-21	-2.426e-21	3.030e-21
4.2003f	4.2003f	-1.6528f	-1.6528f	395.7918a
-498.7795m	-498.7795m	509.2514m	509.2514m	-670.2097m
-762.0381m	-762.0381m	486.7414m	486.7414m	-251.2205m
0.	0.	0.	0.	0.
-498.6919m	-498.6919m	313.1614m	313.1614m	-491.9492m
-68.9770m	-68.9770m	174.6249m	174.6249m	-177.0724m
-87.6511u	-87.6511u	196.0899m	196.0899m	-178.2605m
12.7434m	12.7434m	939.8106u	939.8106u	2.0685m
557.0847m	557.0847m	507.4459m	507.4459m	557.0846m
324.0367u	324.0367u	148.3337u	148.3337u	301.6827u
1.2430u	1.2430u	509.4237n	509.4237n	7.7590u
96.8174u	96.8174u	29.0994u	29.0994u	92.3440u
135.2994f	135.2994f	79.1635f	79.1635f	50.6205f
392.4687f	392.4687f	4.6051p	4.6051p	275.2232f
418.8750f	418.8750f	4.7538p	4.7538p	314.6509f
360.3312f	360.3312f	1.3248p	1.3248p	147.7275f
261.4223f	261.4223f	4.1968p	4.1968p	241.9014f
43.0433f	43.0433f	19.0845f	19.0845f	15.3532f

Fig1-5. First Stage Amplifier (M1~M5)

xop 1:m6 0:n_18.1	xop 1:m7 0:p_18.1	xop 1:m8 0:n_18.1	xop 1:m9 0:p_18.1
Saturation	Saturation	Saturation	Saturation
57.8473u	-57.8473u	57.8473u	-57.8473u
-8.850e-21	5.416e-21	-8.850e-21	5.416e-21
-2.0944f	4.4463f	-2.0944f	4.4463f
486.7414m	-543.4081m	486.7414m	-543.4081m
1.1864	-313.5732m	1.1864	-313.5732m
0.	0.	0.	0.
405.2051m	-491.9487m	405.2051m	-491.9487m
110.0095m	-90.2058m	110.0095m	-90.2058m
81.5362m	-51.4594m	81.5362m	-51.4594m
10.8652m	19.1985m	10.8652m	19.1985m
507.4461m	557.0847m	507.4461m	557.0847m
872.4539u	977.5648u	872.4539u	977.5648u
10.1608u	4.5362u	10.1608u	4.5362u
173.0740u	295.2174u	173.0740u	295.2174u
29.5655f	392.7735f	29.5655f	392.7735f
115.0652f	2.1790p	115.0652f	2.1790p
133.4354f	2.4138p	133.4354f	2.4138p
74.9040f	1.3176p	74.9040f	1.3176p
96.3411f	1.8036p	96.3411f	1.8036p
8.6212f	114.8093f	8.6212f	114.8093f

Fig1-6. Second Stage Amplifier (M6~M9)

xop 1:m10 0:n_18.1	xop 1:m11 0:n_18.1	xop 1:m12 0:n_18.1	xop 1:m13 0:n_18.1
Saturation	Saturation	Saturation	Saturation
88.8675u	81.3940u	88.8675u	81.3940u
-1.330e-20	-1.271e-20	-1.330e-20	-1.271e-20
-5.4172f	-897.6477a	-5.4172f	-897.6477a
439.0739m	509.2514m	439.0739m	509.2514m
752.6472m	747.3528m	752.6472m	747.3528m
0.	0.	0.	0.
429.6152m	496.6046m	429.6152m	496.6046m
73.3746m	91.9724m	73.3746m	91.9724m
9.4587m	12.6468m	9.4587m	12.6468m
58.4743m	31.9253m	58.4743m	31.9253m
507.4460m	507.4462m	507.4460m	507.4462m
1.8219m	1.4116m	1.8219m	1.4116m
23.7004u	53.1420u	23.7004u	53.1420u
361.8788u	209.1228u	361.8788u	209.1228u
130.9438f	21.0454f	130.9438f	21.0454f
299.0987f	24.6961f	299.0987f	24.6961f
345.2333f	35.4942f	345.2333f	35.4942f
293.4839f	38.3683f	293.4839f	38.3683f
209.7949f	15.3719f	209.7949f	15.3719f
37.1759f	5.9577f	37.1759f	5.9577f

Fig1-7. Source Follower (M10~M13)

xop 1:mcm1 0:n_18.1	xop 1:mcm2 0:n_18.1	xop 1:mcm3 0:p_18.1	xop 1:mcm4 0:p_18.1	xop 1:mcm5 0:n_18.1
Saturation	Saturation	Saturation	Saturation	Saturation
18.3242u	19.2045u	-18.3242u	-19.2045u	37.5287u
-2.749e-21	-2.882e-21	1.778e-21	1.863e-21	-5.911e-21
-1.5559f	-1.5391f	950.4092a	957.7620a	-371.5267a
396.8768m	399.5240m	-670.2097m	-675.3948m	509.2514m
479.3143m	474.1292m	-670.2097m	-675.3948m	350.4760m
0.	0.	0.	0.	0.
348.3496m	348.3751m	-483.0326m	-483.0326m	386.6888m
82.7527m	84.1685m	-180.4901m	-184.4112m	133.1002m
48.5272m	51.1489m	-187.1771m	-192.3622m	122.5626m
6.8305m	6.8313m	1.0700m	1.0685m	4.3617m
507.4459m	507.4459m	557.0846m	557.0846m	507.4461m
332.1278u	344.0089u	167.1958u	171.3635u	467.1306u
2.7467u	2.8552u	493.6875n	514.8250n	7.0245u
68.5117u	70.9159u	51.7222u	53.0571u	94.5696u
62.2454f	62.3348f	35.2596f	35.2328f	20.2524f
543.2930f	548.1514f	391.4764f	391.6078f	95.9765f
564.8367f	571.3934f	446.1482f	446.3722f	107.4277f
249.0365f	249.1287f	177.1309f	177.0211f	53.5128f
463.6790f	469.6707f	352.4071f	352.6601f	83.4759f
15.7944f	15.7801f	11.0531f	11.0556f	5.0927f

Fig1-8. Common Mode Feedback (MCM1~MCM5)

- **All Constraints for Specification**

>80dB

```
****** ac analysis tnom=  25.000 temp=  25.000 ******
dcgain_in_db=  80.3398      at=  10.0000
               from=  10.0000      to=   1.0000g
dcgain=  10.3990k     at=  10.0000
               from=  10.0000      to=   1.0000g
unity_frequency= 112.2180x  >100MHz
phase=-134.7411
phase_margin=  45.2589  >45°
```

Fig1-9. Gain, Bandwidth, Phase Margin

```
subckt
element  0:vinp      0:vdd       0:vgnd      0:vinn      0:vocm
 volts    750.0000m    1.5000      0.          750.0000m   750.0000m
current     0.       -393.2190u  378.2720u      0.          0.
 power      0.        589.8285u     0.          0.          0.
```

<0.4mA

Fig1-10. Vdd Current

```
+0:vdd     =   1.5000  0:vinn    = 750.0000m 0:vinp    = 750.0000m
+0:vocm    = 750.0000m 0:von     = 747.3528m 0:vop     = 747.3528m  <750mV±1%
+0:vss     =   0.      1:d4      = 486.7414m 1:d6      =   1.1864
+1:net26   = 413.9859m 1:net31   = 720.6631m 1:net42   =   1.1864
+1:net44   = 486.7414m 1:net47   =   1.2488  1:net51   = 350.4760m
+1:net52   = 509.2514m 1:net55   = 829.7903m 1:net60   = 747.3528m
+1:net67   =  25.4611m 1:net68   = 956.5919m 1:net73   = 824.6052m
+1:net78   =   1.1864  1:net79   =   1.1864
```

Fig1-11. Von, Vop in Vdd/2±1%

- **Dis.1(a)**

Let $V_{thb5} = V_{thb4} = V_{th}$, and from circuit design, we know that $I_{D,b5} = I_{D,B4}$ (assume that all transistors operate in saturation region and no body effect)

$$\begin{cases} I_{D,b4} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_{b4}\left(V_{GS,b4} - V_{th}\right)^2 \\ I_{D,b5} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_{b5}\left(V_{GS,b5} - V_{th}\right)^2 \end{cases}$$

$$\Rightarrow V_{GS,b4} = \sqrt{\frac{I_{D,b4}}{\frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_{b4}}} + V_{th} \qquad V_{GS,b5} = \sqrt{\frac{I_{D,b5}}{\frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_{b5}}} + V_{th}$$

Analyzing the circuit structure, we can establish $V_{GS,b4} - V_{GS,b5} = I_{D,b4} * R_b$

Substituting the equations derived above and $(W/L)_5 = 4*(W/L)_4$, we can get

$$\left(\sqrt{\frac{I_{D,b4}}{\frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_{b4}}} + V_{th}\right) - \left(\sqrt{\frac{I_{D,b5}}{\frac{1}{2}\mu_n C_{ox} 4\left(\frac{W}{L}\right)_{b4}}} + V_{th}\right) I_{D,b4} * R_b$$

$$\Rightarrow \frac{1}{2}\sqrt{\frac{I_{D,b4}}{\frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_{b4}}} = I_{D,b4} * R_b$$

$$\Rightarrow \frac{I_{D,b4}}{\frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_{b4}} = 4\left(I_{D,b4} * R_b\right)^2$$

$$\Rightarrow I_{D,b4} = \frac{1}{2R_b^2\mu_n C_{ox}\left(\frac{W}{L}\right)_{b4}}$$

$$\because g_{m,b4} = \sqrt{2\mu_n C_{ox}\left(\frac{W}{L}\right)_{b4} I_{D,b4}}$$

$$\therefore g_{m,b4} = \sqrt{2\mu_n C_{ox}\left(\frac{W}{L}\right)_{b4} * \frac{1}{2R_b^2\mu_n C_{ox}\left(\frac{W}{L}\right)_{b4}}} = \frac{1}{R_b} \Rightarrow I_{D,b4} = \frac{V_{ov,b4}}{2R_b}$$

From the derivation of gmb4 under condition $(W/L)_5 = 4*(W/L)_4$, we can infer that the gm of MB4 is affected by only Rb, means that it is insensitive to other variables, and not influenced by operating region, bias voltage and so on. Therefore, if we wish to pursue a specific constant gm current, it can be easily achieved by calculating the value Rb.

- **Dis.1(b)**

(1) Why do we need a start-up circuit ?

A start-up circuit is essential for proper initialization, preventing latch-up, and ensuring safe power-up in electronic systems. It ensures correct initial voltages and currents for components, avoids meta-stable states, and controls the power-up sequence to prevent oscillations and transient issues. By providing a controlled ramp-up of voltage and current, it protects components from spikes and ensures reliable operation.

(2) The functionality of start-up circuit

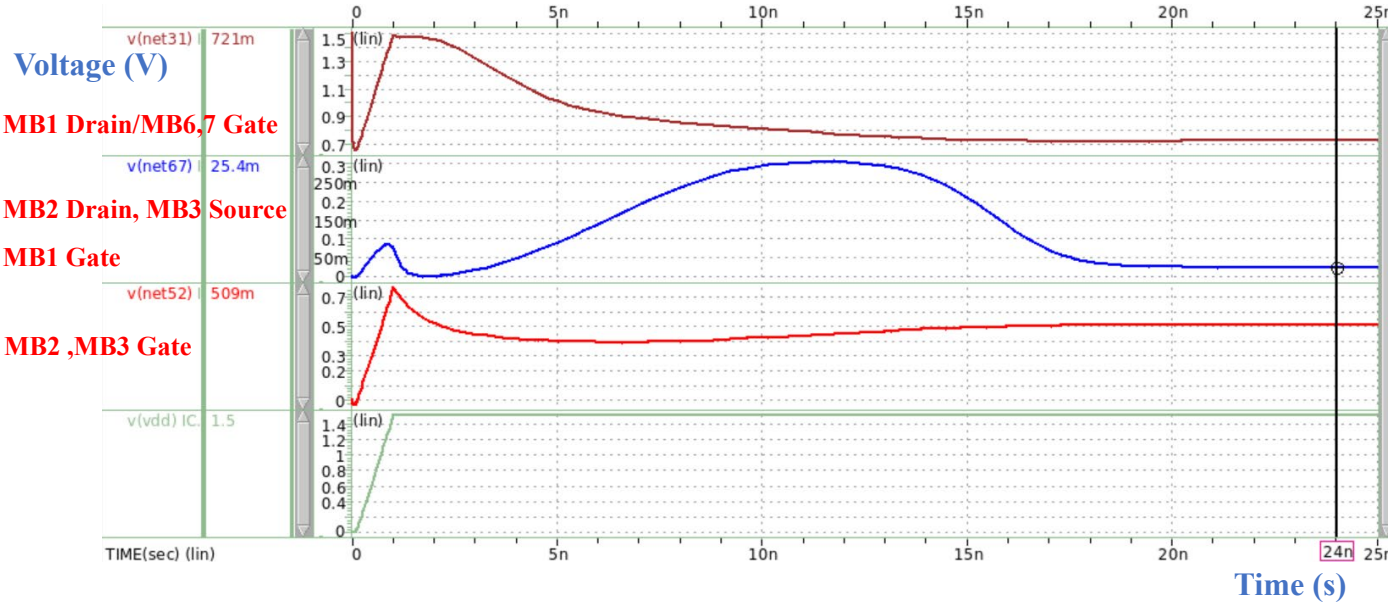
The start-up circuit is designed to initialize the entire system when the power supply (Vdd) is first turned on. Initially, when Vdd is activated, MB3 receives a sufficiently large bias voltage and turns on, creating a conductive path between Vdd and the gate of MB1. As a result, the gate of MB1 starts charging and its voltage rises. Once the gate voltage of MB1 exceeds its threshold voltage (Vth), MB1 turns on, forming a path between MB6 and MB7. This connection causes the gates of MB6 and MB7, which are connected to MB1, to begin discharging. As the gate voltages of MB6 and MB7 drop, M12 and M13 are activated. This activation triggers the Constant gm Circuit. When the Constant gm

Circuit starts operating, it causes the gates of MB4 and MB2 to begin charging. Once the gate voltage of MB2 exceeds its threshold voltage (Vth), MB2 turns on. This forms a path to ground, allowing the gate of MB1 to continue discharging. When the gate voltage of MB1 drops below its threshold voltage (Vth), MB1 turns off. This sequence of events ensures that the start-up circuit successfully initializes the main circuit, allowing it to reach a stable operating state.

(3) How to design the size of the transistors to improve power efficiency after startup

To enhance power efficiency and reduce power consumption in the start-up circuit, it is critical to minimize the current flowing through it. Given that MB1 will eventually turn off as the circuit stabilizes, we need to carefully consider the currents through MB2 and MB3. Since MB2 and MB3 remain active, their current values should be kept as low as possible to avoid unnecessary power dissipation. This can be accomplished by adjusting their (W/L) ratios. Specifically, the (W/L) ratios of MB2 and MB3 should not be excessively large, as larger ratios would lead to higher currents and increased power consumption. By optimizing these transistor sizes, we ensure that the start-up circuit performs its function effectively while maintaining low power usage, thereby improving the overall efficiency of the system.

(4) Transient analysis



The startup circuit functionality explained in (2) is demonstrated on the waveview. Initially, Vdd turns on and provide large bias for MB3, so we can see that MB3 gate net52 charges up rapidly. Next, MB2 and MB3 turn on, providing current to charge MB1 gate net67, and during 2ns~10ns, MB1 turns on for a little time range, to activate the discharging of MB6,7, which is shown in net31. Finally, the circuit will be activated and operates in function as described in (2). After the circuit is stabilized, at the time roughly 20ns, we can observe that net67 is in a low voltage, that is, MB1 will turn off again and stay in subthreshold region; Secondly, net52 provides stable gate voltage that turns on MB2,3, but due to the gate voltage of net67, MB2 and MB3 will be in linear and saturation region respectively.

II. Specification Table

Design Items	Specifications	score	Simulation	Calculation
Technology	CIC pseudo 0.18um technology			
Vicm, Vocm	$V_{DD}/2$			
Supply voltage (V)	Open for design ≤1.8 / ≤1.5 / ≤1.3	2% 4% 6%	1.50 V	
Supply current (mA) (including bias ckt)	< 3 / < 1 / < 0.4	2% 4% 6%	0.39 mA	
Loading	2 pF / 100 kΩ (for each output)		2 pF / 100 kΩ (for each output)	
Compensation Rz, Cc	Rz < 10 kΩ , Cc < 10 pF		Rz = 4.80 kΩ Cc = 0.73 pF	
Open-loop simulation				
DC gain (dB)	> 70 / > 75 / > 80	1% 3% 5%	80.34 dB	80.34 dB
G-BW (MHz)	> 50 / > 75 / > 90 / > 100	1% 2% 3% 4%	112.22 MHz	
P.M.	> 45°		45.26°	
C.M.R.R. @10KHz	> 90 dB		112.18 dB	112.21 dB
P.S.R.R.+ @10KHz	> 90 dB		110.53 dB	
P.S.R.R.- @10KHz	> 90 dB		112.17 dB	
Closed-loop simulation				
Differential swing of 1.0 V (step or sinusoidal)				
Closed-loop gain	> -0.1dB @ 10kHz		-0.00171 dB	-0.00167 dB
S.R.+ (10% ~ 90%)	> 15 V/us (single-ended output)		19.55 V/us	19.60 V/us
S.R.- (90% ~ 10%)	> 15 V/us (single-ended output)		16.32 V/us	16.28 V/us
THD (1.0Vpp@100kHz Sin)	< - 60 dB		-69.43 dB	
Settling+ (1.0Vstep to 0.5%)	< 150 ns		51.83 ns	
Settling- (1.0Vstep to 0.5%)	< 150 ns		57.97 ns	
$\frac{Settling+ + Settling-}{2}$(ns)	< 150 / < 90 / < 70 / < 55	1% 2% 3% 4%	54.90 ns	

III. Simulation Results

3.1 Open-Loop Differential Mode AC Response

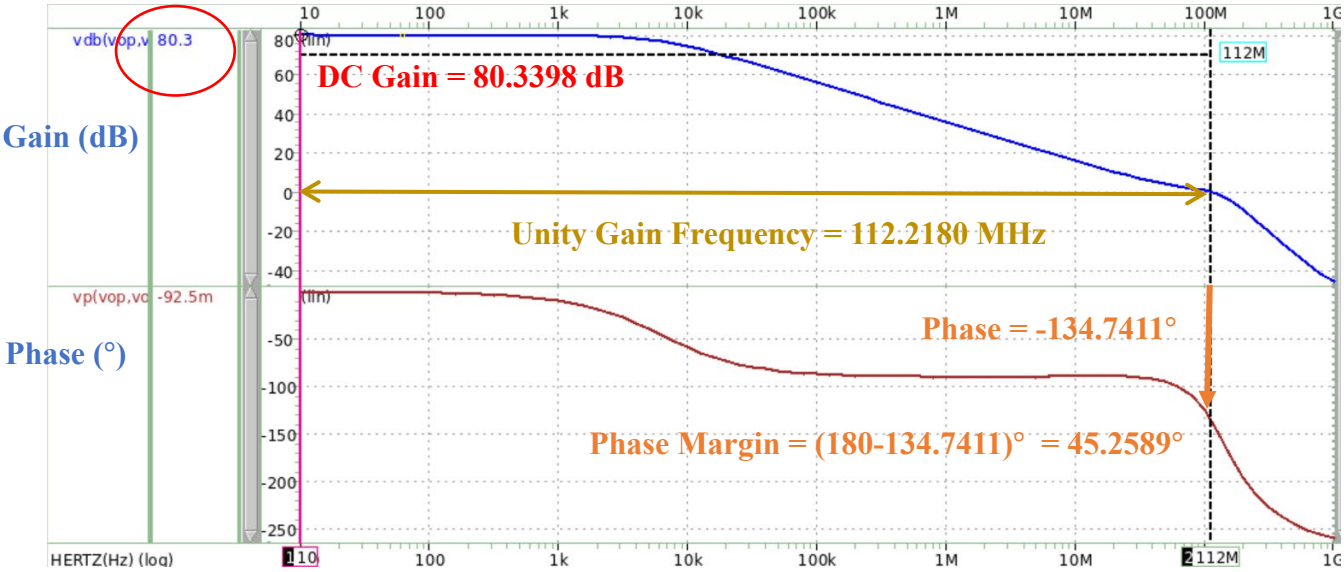


Fig3.1(a)-1

```
****     small-signal transfer characteristics

    v(vop,von)/vinp                          =   10.3989k
    input resistance at             vinp     =  1.000e+20
    output resistance at v(vop,von)          =    1.0401k
```

Tab3.1(b)

- My DC gain is designed to be **80.3398 dB**
- My Gain Bandwidth is designed to be **112.2180 MHz**
- My Phase Margin is designed to be **45.2589°**

poles (rad/sec)		poles (hertz)		
real	imag	real	imag	
-38.8976k	0.	-6.19074k	0.	Pole1
-9.32475x	111.967x	-1.48408x	17.8201x	
-9.32475x	-111.967x	-1.48408x	-17.8201x	
-9.34158x	0.	-1.48676x	0.	
-288.168x	0.	-45.8634x	0.	
-444.832x	-114.479x	-70.7973x	-18.2200x	
-444.832x	114.479x	-70.7973x	18.2200x	
-485.134x	747.334x	-77.2114x	118.942x	Pole2
-485.134x	-747.334x	-77.2114x	-118.942x	
-489.278x	847.742x	-77.8711x	134.922x	Pole3
-489.278x	-847.742x	-77.8711x	-134.922x	
-652.982x	0.	-103.925x	0.	
-763.499x	-150.951x	-121.515x	-24.0246x	
-763.499x	150.951x	-121.515x	24.0246x	
-844.556x	0.	-134.415x	0.	
-1.53045g	0.	-243.579x	0.	

zeros (rad/sec)		zeros (hertz)		
real	imag	real	imag	
-9.34160x	0.	-1.48676x	0.	
-9.98956x	111.153x	-1.58989x	17.6906x	
-9.98956x	-111.153x	-1.58989x	-17.6906x	
-286.351x	0.	-45.5742x	0.	
-374.453x	0.	-59.5961x	0.	Zero1
-444.866x	114.685x	-70.8025x	18.2526x	
-444.866x	-114.685x	-70.8025x	-18.2526x	
-494.403x	821.961x	-78.6867x	130.819x	
-494.403x	-821.961x	-78.6867x	-130.819x	
-652.983x	0.	-103.925x	0.	
-733.869x	-96.7196x	-116.799x	-15.3934x	
-733.869x	96.7196x	-116.799x	15.3934x	
-1.53045g	0.	-243.579x	0.	
2.32252g	0.	369.640x	0.	
-6.92032g	0.	-1.10140g	0.	
71.7720g	0.	11.4229g	0.	

Fig3.1(a)-2

- **Dis.3.1**

1. Hand Calculation of Gain

Using the half-circuit method, we can find the rough gain equation for the first stage, second stage and the source follower.

$$A_1 = -g_{m1}(r_{o2} \parallel r_{o4}) = -184.9077366\ V/V$$

$$A_2 = -g_{m6}(r_{o6} \parallel r_{o7}) = -59.36272028\ V/V$$

$$A_{buffer} = \frac{r_{o10} \parallel r_{o11} \parallel R_L \parallel R_{CM}}{g_{m10}^{-1} + (r_{o10} \parallel r_{o11} \parallel R_L \parallel R_{CM})} = 0.947410952\ V/V$$

$$\begin{cases} \text{Total Gain} = A_1 * A_2 * A_{buffer} = 10399.37593\ V/V = 80.3401\ V/V \\ Simulation\ Gain = \ 10398.9\ V/V \end{cases}$$

✓ The error of total gain compared to the simulation gain is 0.0046%, the value is absolutely small.

2. Poles and Zeros

2.1 Pole 1 (Dominant Pole)

The dominant pole is influenced by Miller effect, contributing a multiplying factor of A_2 on the compensation capacitor Cc at the output of stage one.

$$|f_{dominant}| = \left| -\frac{1}{g_{m6} * (r_{o2} \parallel r_{o4}) * (r_{o6} \parallel r_{o7}) * C_c} \right| = 6436.097215\ \text{Hz}$$

$$f_{simulation} = 6190.74\ Hz$$

✓ The error of dominant pole compared to the simulation first pole is 3.812%

✓ The first pole is dominant to the unity gain bandwidth, therefore to increase unity gain bandwidth, we must push pole 1 further from the original frequency. My strategy here is to decrease the compensation capacitor value and gm6 to get a relatively larger dominant pole.

2.2 Pole 2 (Non-Dominant Pole)

We can infer that the second pole is the output pole of the entire circuit because the loading capacitor isn't on the output of the second stage. That is, from the example of the lecture slide, we can derive the equation below.

$$|f_{pole2}| = | -\frac{1}{C_L \times ([R_L \parallel (r_{o10} \parallel r_{o11}) \parallel R_{CM}] \parallel g_{m10}^{-1})} | = 153.029\ \text{MHz}$$

$$f_{simulation} = 141.8054994\ MHz$$

✓ The error of second pole compared to the simulation second pole is 7.33%

✓ Note that if we want a larger bandwidth we have to push pole 2 out of the unity gain frequency, if pole 2 is within the unity gain frequency, then the gain reduction will be dramatically faster

than we expect, and the bandwidth might result to a small value, which is not a positive phenomenon for a stable and useful circuit.

2.3 Pole 3 (Non-Dominant Pole)

The third pole can be found as the output of the second stage, and moreover, it is affected by the frequency compensation mechanism.

$$|f_{pole3}| = \left| -\frac{g_{m8}}{\left(C_{dtot,M2} + C_{dtot,M4} + C_{gs,M6}\right) + \left(C_{dtot,M6} + C_{dtot,M7} + C_{gs,M10}\right)} \right| = 147.258\ MHz$$

$$f_{simulation} = 155.781\ MHz$$

- ✓ The error of third pole compared to the simulation third pole is 5.78%
- ✓ Pole 3 isn't shown in the waveview, so we can roughly find it by observing the pz table shown in the lis file and dash out all the offset poles and zeros, then finally we can find pole 3.

2.4 Zero

$$|f_{zero}| = \frac{1}{C_C\left(\frac{1}{g_{m6}} - R_z\right)} = 59.669\ MHz$$

$$f_{simulation} = 59.5961\ MHz$$

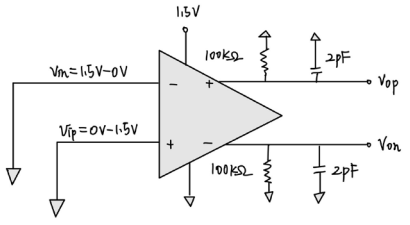
- ✓ The error of hand calc. zero compared to the simulation zero is 0.123%
- ✓ For design consideration, we aim to pull the zero back more before unity gain frequency to achieve a more larger bandwidth. When no miller compensation, it is a must to let the dominant pole lower in order to get sufficient phase margin, but it might sacrifice the bandwidth. To tackle the problem, adding compensation resistor Rz into the circuit in necessary. Rz can adjust the right half-plane zero to the left half-plane zero, avoiding phase to decline abruptly.

3. Output Impedance

$Rout = 2(R_{CM} \parallel g_{m10}^{-1} \parallel r_{o11} \parallel r_{o10} \parallel R_L) = 2 * 519.59 = 1039.18\ \Omega = 1.03918\ k\Omega$

The simulation value of Rout is 1.0401kΩ, the error 0.088% is very small, which proves to be correct.

3.2 Open-Loop Differential Mode DC Sweep



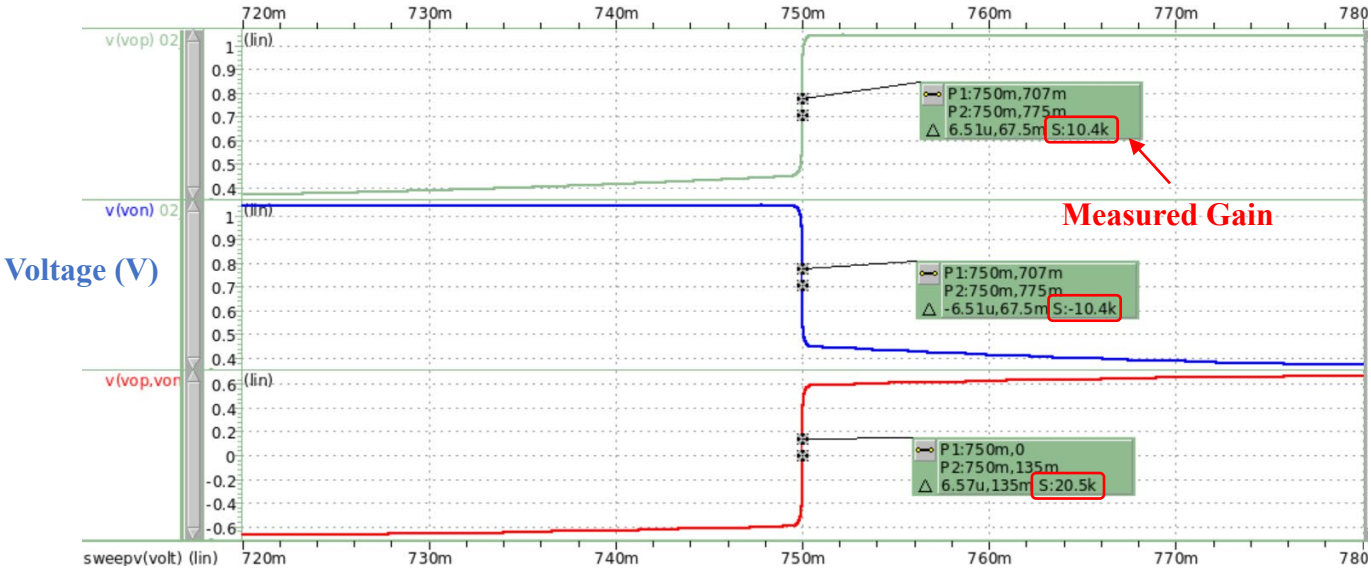
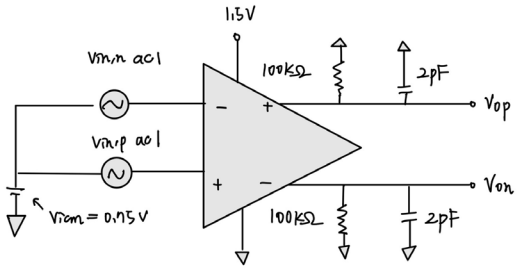


Fig3.2(a)

In the waveview above, I set the dc sweep range from 0.72V to 0.78V. From first and second panel, we can observe that the absolute value of slope in Vop and Von is 10.4k, which is a close value to the simulation value 10.3989k. The third panel demonstrates the differential gain, which is roughly two time larger than that in Vop and Von.

3.3 Open-Loop Common Mode AC Response



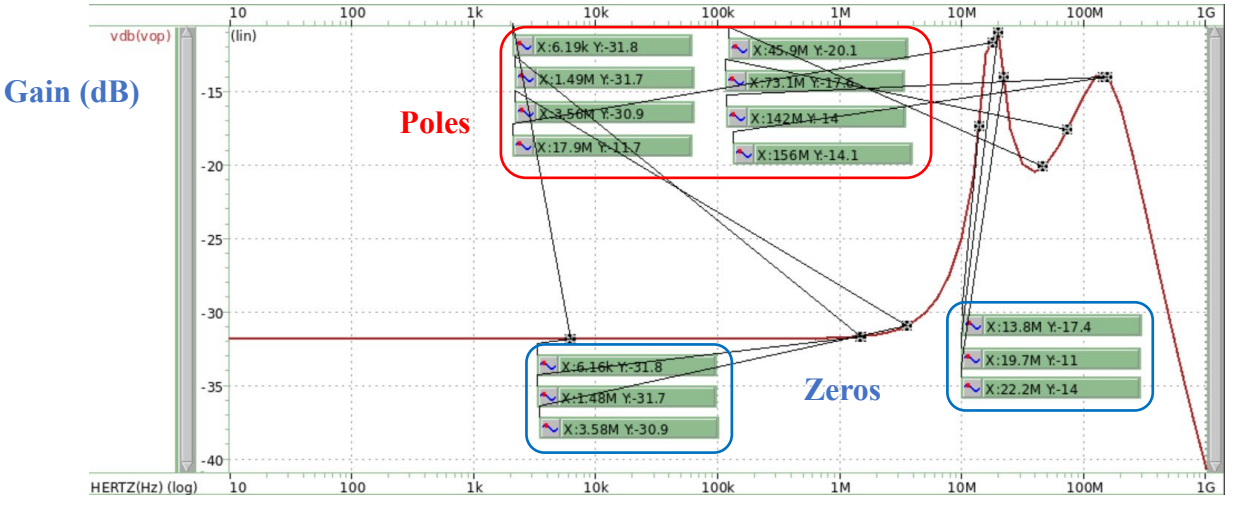


Fig3.3(a)

```
****     small-signal transfer characteristics

     v(vop)/vinp                               =   25.5861m
     input resistance at             vinp      =  1.000e+20
     output resistance at v(vop)               =  260.0322

 ****** ac analysis tnom=  25.000 temp=  25.000 ******
 acm_in_db= -31.8399
```

Fig3.3(b)

➢ The simulation CMRR = DC gain - acm_in_db = 80.34 + 31.84 = 112.18 dB > 90 dB

poles (rad/sec)		poles (hertz)	
real	imag	real	imag
-38.8976k	0.	-6.19074k	0.
-9.32475x	-111.967x	-1.48408x	-17.8201x
-9.32475x	111.967x	-1.48408x	17.8201x
-9.34158x	0.	-1.48676x	0.
-22.3879x	0.	-3.56315x	0.
-288.168x	0.	-45.8634x	0.
-444.832x	114.479x	-70.7973x	18.2200x
-444.832x	-114.479x	-70.7973x	-18.2200x
-485.134x	-747.334x	-77.2114x	-118.942x
-485.134x	747.334x	-77.2114x	118.942x
-489.278x	-847.742x	-77.8711x	-134.922x
-489.278x	847.742x	-77.8711x	134.922x
-652.982x	0.	-103.925x	0.
-763.499x	-150.951x	-121.515x	-24.0246x
-763.499x	150.951x	-121.515x	24.0246x

Output first 15 Zeros, (total 30)
Use .option pz_num = NUM to control output number, (default:10)

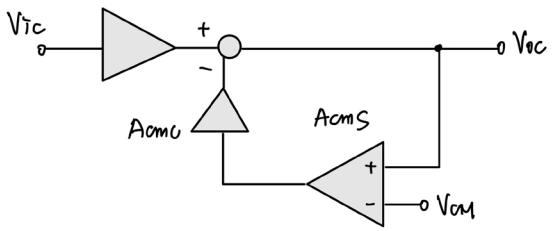
zeros (rad/sec)		zeros (hertz)	
real	imag	real	imag
-38.7184k	650.060m	-6.16222k	103.460m
-38.7184k	-650.060m	-6.16222k	-103.460m
-9.31204x	314.454	-1.48206x	50.0469
-9.31204x	-314.454	-1.48206x	-50.0469
-22.5149x	124.016k	-3.58336x	19.7377k
-22.5149x	-124.016k	-3.58336x	-19.7377k
-86.8533x	-2.88241k	-13.8231x	-458.749
-86.8533x	2.88241k	-13.8231x	458.749
124.018x	-1.42383k	19.7381x	-226.610
124.018x	1.42383k	19.7381x	226.610
-139.317x	-8.62630k	-22.1730x	-1.37292k
-139.317x	8.62630k	-22.1730x	1.37292k
-362.980x	0.	-57.7700x	0.
-374.565x	0.	-59.6139x	0.
-442.675x	114.279x	-70.4539x	18.1880x

Fig3.3(c)

- **Dis.3.3**

1. Hand Calculation of Gain

The common mode feedback is designed to stabilize the output node Vocm.



$$A_{CMFB} = \frac{V_{oc}}{V_{ic}} = \frac{A_{CM}}{1 + A_{CMC} * A_{CMS}}$$

A_{CMC} is the gain from the feedback node back to the OP, and A_{CMS} is the gain from Von to the feedback node. Acm is composed of three stages, which are common mode, buffer and differential mode, the stages are solved by applying half-circuit method. The equation of derivation will be shown in the following.

$$|\mathrm{A}_1| = \frac{g_{m2} r_{o2} r_{o4}}{r_{o2} + r_{o4} + (1 + g_{m2} r_{o2})(2r_{o5})} = 7.287381434\ (V/V)$$

$$|\mathrm{A}_2| = g_{m6}(r_{o6} \parallel r_{o7}) = 59.3627\ (V/V)$$

$$|\mathrm{A}_3| = \frac{r_{010} \parallel r_{o11} \parallel R_L \parallel R_{CM}}{(r_{010} \parallel r_{o11} \parallel R_L \parallel R_{CM}) + g_{m10}^{-1}} = 0.94741\ (V/V)$$

$$\boldsymbol{A_{cm}} = A_1 A_2 A_3 = 409.8482755\ (V/V)$$

$$|\mathrm{A}_4| = \frac{1}{2} g_{m5}\left(r_{o4} \parallel (r_{o2} + (1 + g_{m2} r_{o2}) * 2r_{o5})\right) = 287.7287\ (V/V)$$

$$|\mathrm{A}_5| = |A_2| = 59.3627\ (V/V)$$

$$|\mathrm{A}_6| = |\mathrm{A}_3| = 0.94741\ (V/V)$$

$$\boldsymbol{A_{CMC}} = A_4 A_5 A_6 = 16182.09676\ (V/V)$$

$$\boldsymbol{A_{CMS}} = \frac{g_{mMCM1}}{2 g_{mMCM3}} = 0.993230093\ (V/V)$$

$$\begin{cases} \boldsymbol{A_{CMFB}} = \dfrac{\mathrm{A_{CM}}}{1 + A_{CMC} * A_{CMS}} = 0.025498312 \approx 25.4983\ \left(\dfrac{mV}{V}\right) \\ A_{simulation} = 25.5861\ \left(\dfrac{mV}{V}\right) \end{cases}$$

The error of common mode feedback gain compared to the simulation value is 0.344%, the error might come from the rough equation of A_{CMS}, which neglects the resistances of transistors.

$$\mathrm{CMRR_{calc}} = 80.34 - 20log0.025498312 = 112.2097714\ (dB)$$

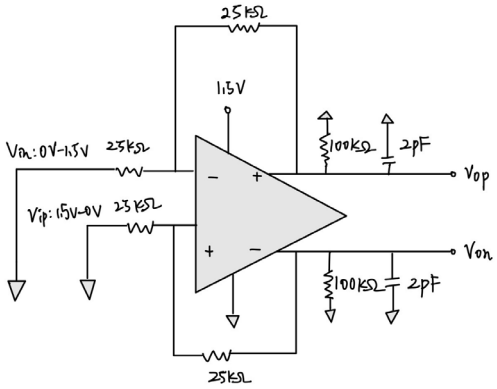
2. Low Frequency Zero

$$f_{low-freq-zero} = \frac{1}{(g_{m6}^{-1} - R_Z) C_C} = 59.66938926\ \mathrm{MHz}$$

$$f_{simulation} = 59.6139\ MHz$$

The calculated value of low frequency zero is close to the simulation result, error 0.093%

3.4 Open-Loop Common Mode DC Sweep



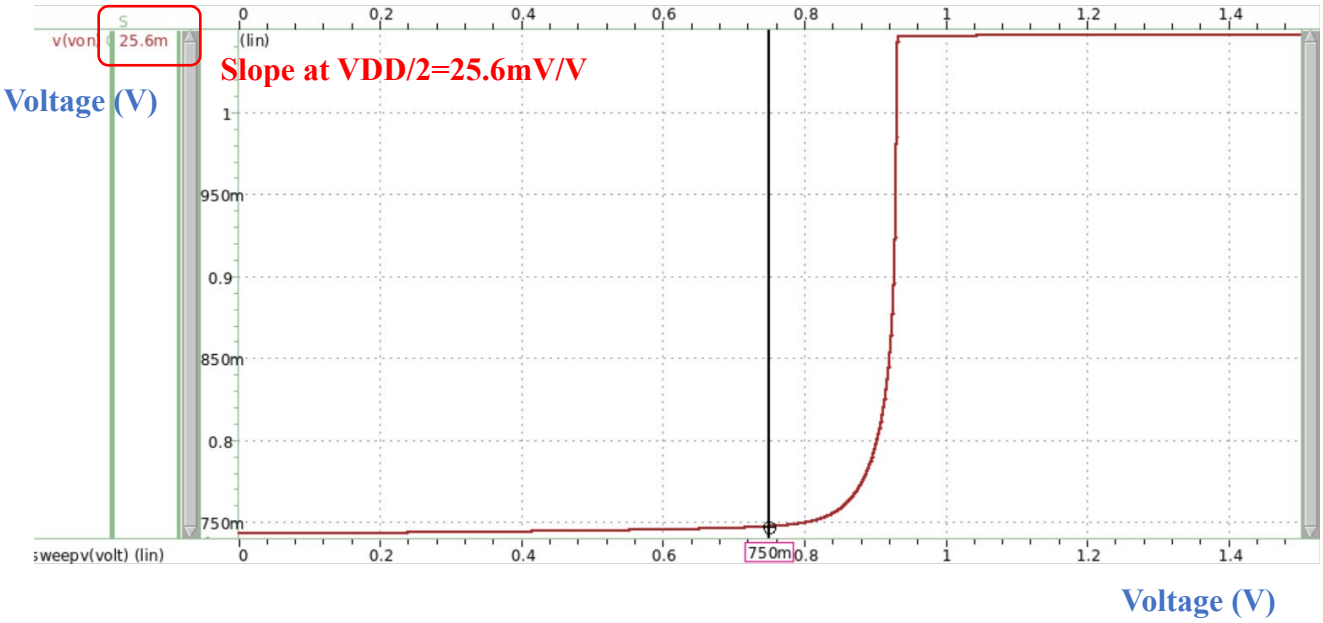
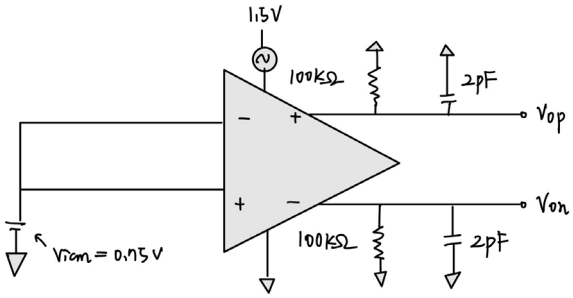


Fig3.4(a)

We can observe that the slope measured in the waveview is very close to the simulation value shown in below of 3.3(a) 25.5861mV/V.

3.5 Open-Loop Power Supply AC Response

[Positive Supply]



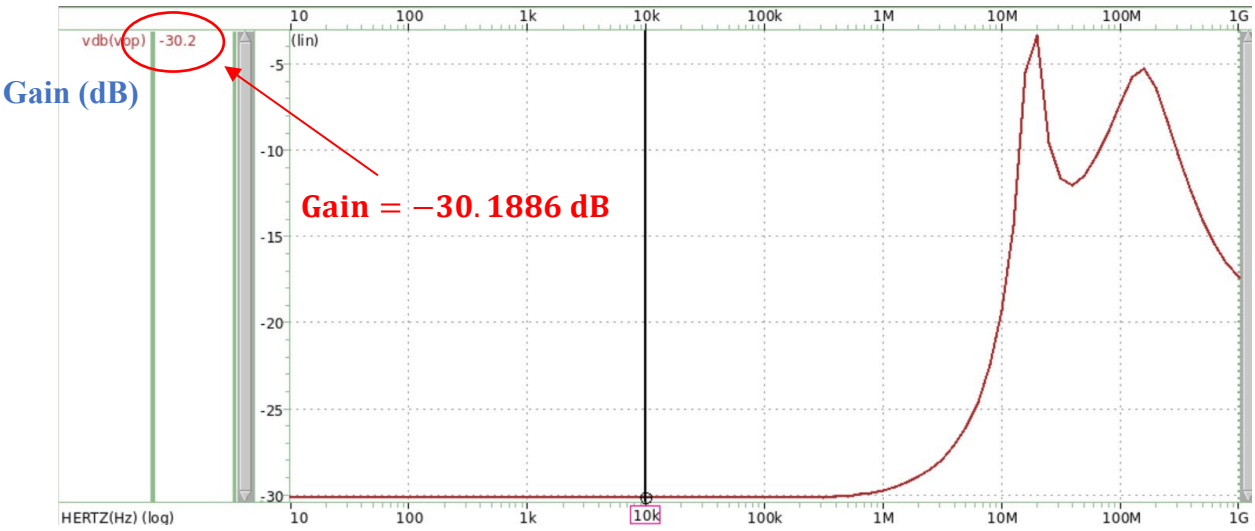


Fig3.5(a)

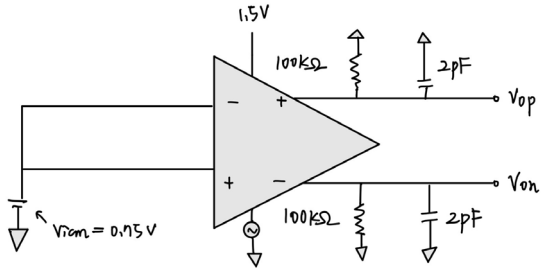
Frequency (Hz)

```
****** ac analysis tnom=  25.000 temp=  25.000 ******
psp_in_db= -30.1886
```

$$PSRR_{+} = 20\log\left(\frac{A_{DM}}{A_{VDD}}\right) = 20\log(\mathrm{A_{DM}}) - 20\log(\mathrm{A_{VDD}}) = 80.34 + 30.19 = 110.53 > 90\ \mathrm{dB}$$

If we want a larger PSRR, a larger differential gain and a smaller supply small signal is required.

[Negative Supply]



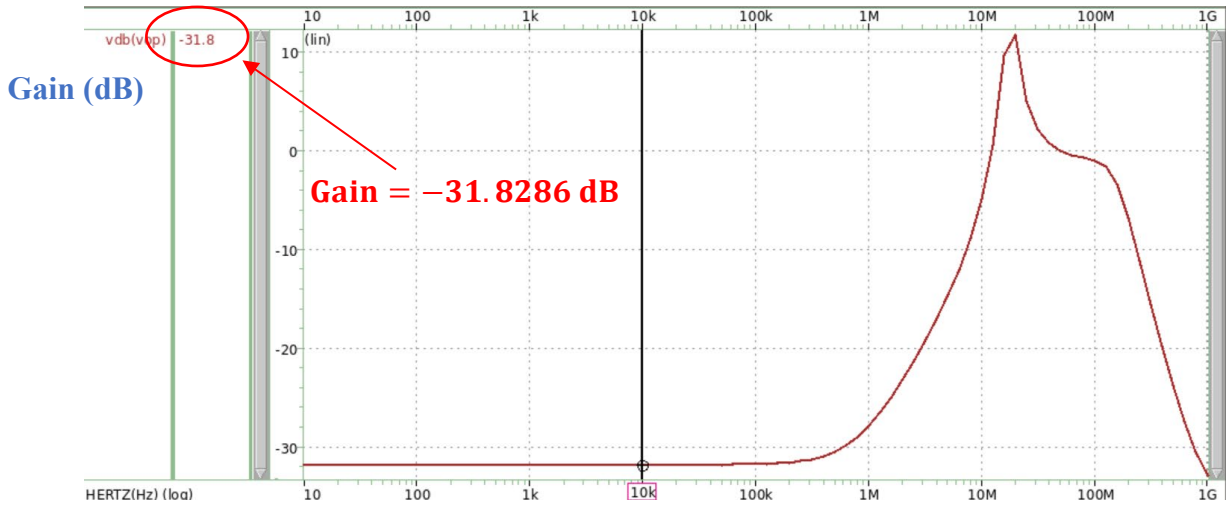


Fig3.5(b)

Frequency (Hz)

```
****** ac analysis tnom=  25.000 temp=  25.000 ******
psn_in_db= -31.8286
```

The testing signal is moved to the ground node compared to the positive supply question above.

$$PSRR\_ = 20\log\left(\frac{A_{DM}}{A_{VSS}}\right) = 20\log(\mathrm{A_{DM}}) - 20\log(\mathrm{A_{VSS}}) = 80.34 + 31.83 = 112.17 > 90\ \mathrm{dB}$$

If we want a larger PSRR, a larger differential gain and a smaller supply small signal is required.

3.6 Closed Loop Differential Mode AC Response

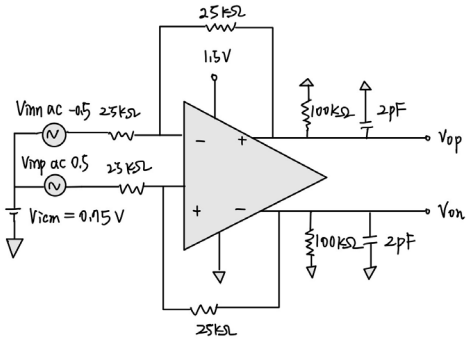


Fig3.6(a)

```
****** ac analysis tnom=  25.000 temp=  25.000 ******
dcgain_in_db=  -1.7054m
maxgain_in_db=   1.4482     at=  25.1189x
```

In the waveview above, I measured the -3dB frequency by finding the gain 1.4482 (max_gain) - 3dB = -1.5518 dB and see what frequency value does it point to on the x-axis.

- **Dis.3.6(b)**

1. Hand Calculation for Gain

From the equation of the forward feedback amplifier taught in electronics I, we know that

$$\begin{cases} \dfrac{V_1 - Vi}{R_1} = \dfrac{Vo - V_1}{R_2} \\ Vo = AV_1 \end{cases} , where\ V_1\ is\ the\ node\ between\ two\ 25k\Omega$$

$$\Rightarrow \frac{\mathrm{Vo}}{\mathrm{Vi}} = \frac{\frac{\mathrm{R_2}}{R_1}}{1 + \frac{\frac{R_2}{R_1}}{A}}$$

$$A = \frac{\mathrm{Vo}}{\mathrm{Vi}} = \frac{1}{1 + \frac{2}{10.3989\mathrm{k}}} = 0.99980771\ \frac{\mathrm{V}}{\mathrm{V}}$$

$$\mathrm{A_{simulation}} = 999.8036\mathrm{m} = 0.9998036\ \frac{\mathrm{V}}{\mathrm{V}}$$

The error of hand calculation compared to the simulation result is 0.0004%, we can assume that the equations are correct.

2. -3dB Bandwidth

$$\omega_{p1,close} = \left(1 + A_{v,open}\beta\right)\omega_{p1,open} = (1 + 10.3989k) * 6190.74 = 68.098\ MHz$$
$$\omega_{simulation} = 42\ MHz$$
$$Error(-3\ dB\ BW) = 38.3\%$$

From the hand calculation, the error is considerable, I consider that the error comes from the poles and zeros that aren't considered. My open loop system might not be stable and ideal enough, so the equation might be more complicated than just a $1 + A_{v,open}\beta$ term.

```
+0:test1    = 750.0000m 0:test2    = 750.0000m 0:vdd     =   1.5000
+0:vinn     = 748.6595m 0:vinp     = 748.6595m 0:vocm    = 750.0000m
+0:von      = 747.3189m 0:vop      = 747.3189m 0:vss     =   0.
+1:d4       = 486.7425m 1:d6       =   1.1864  1:net26   = 413.9859m
+1:net31    = 720.6631m 1:net42    =   1.1864  1:net44   = 486.7425m
+1:net47    =   1.2474  1:net51    = 350.4597m 1:net52   = 509.2514m
+1:net55    = 829.8243m 1:net60    = 747.3189m 1:net67   =  25.4611m
+1:net68    = 956.5919m 1:net73    = 824.5727m 1:net78   =   1.1864
+1:net79    =   1.1864
```

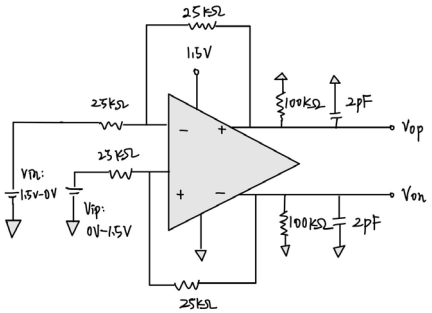
Fig3.6(c)

```
****     small-signal transfer characteristics

v(vop,von)/vinp                          =  999.8036m
input resistance at              vinp    =   33.4769k
output resistance at v(vop,von)          =  200.1776m
```

Fig3.6(d)

3.7 Closed Loop Differential Mode DC Sweep



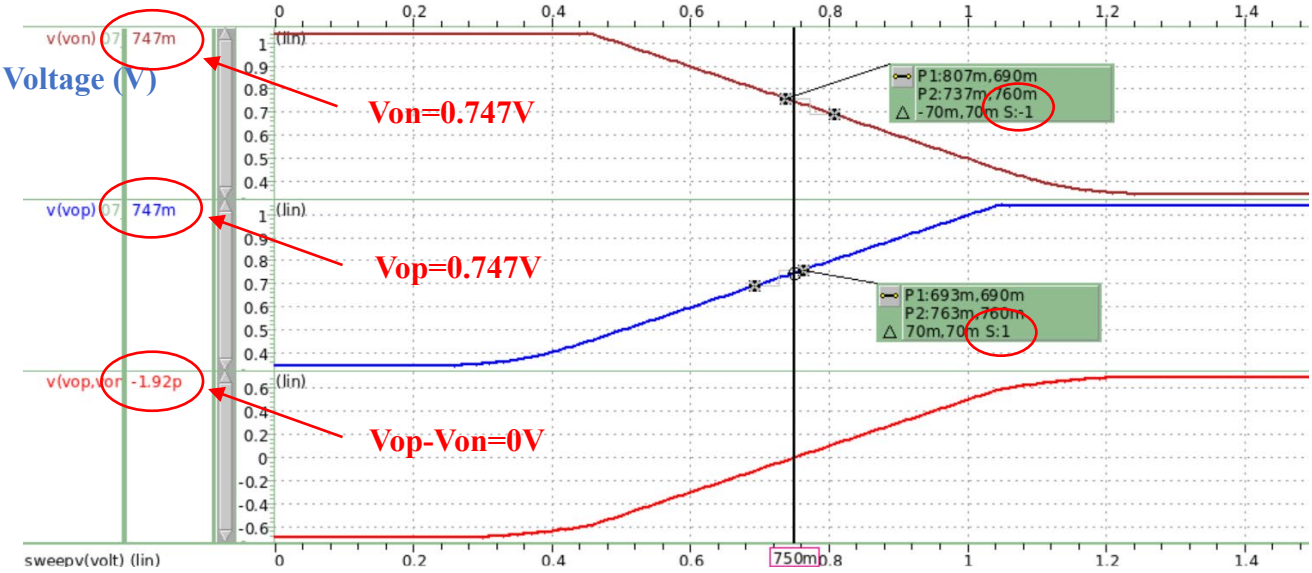
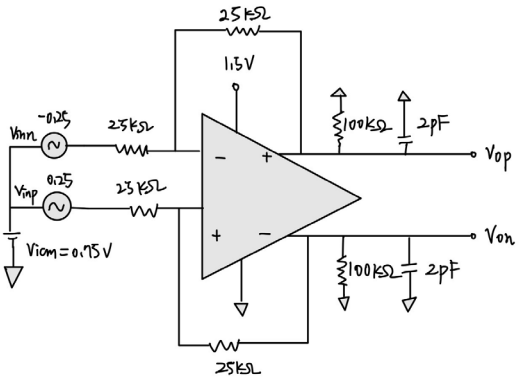


Fig3.7(a)

The waveview in Fig3.7(a) indicates that when the absolute value of Vin and Vip are 750mV, the corresponding Von and Vop are 0.747 according to the measurement. Moreover, when measuring the slope around input 750mV, we can observe the slope (differential ac gain) is 1(V/V), which is really close to our hand calculation $0.99990385\ \frac{V}{V}$.

3.8 Closed Loop Distortion Simulation



```
fourier components of transient response v(vop,von)
dc component =   29.9275f

harmonic frequency  fourier    normalized phase      normalized
no       (hz)       component  component  (deg)      phase (deg)
1         100.0000k  499.7727m    1.0000   -90.1893     0.
2         200.0000k    7.1201p   14.2467p   89.8222   180.0115
3         300.0000k  141.1690u  282.4663u  -37.3414    52.8479
4         400.0000k  570.7081f    1.1419p   87.3869   177.5762
5         500.0000k   86.2032u  172.4849u  153.8391   244.0284
6         600.0000k  154.6652f  309.4710f   82.1358   172.3251
7         700.0000k   32.8177u   65.6653u  -21.4888    68.7005
8         800.0000k   77.8888f  155.8484f   86.2023   176.3916
9         900.0000k    5.7981u   11.6014u  156.1716   246.3609

total harmonic distortion =  0.0337616  percent
```

THD < 0.1 percent

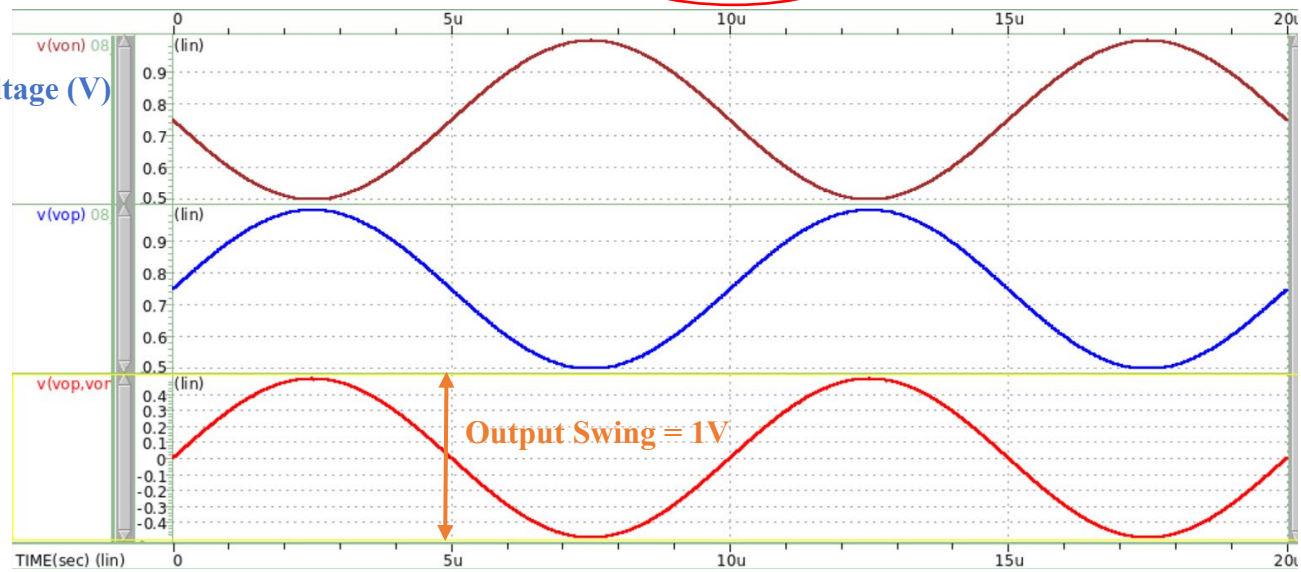
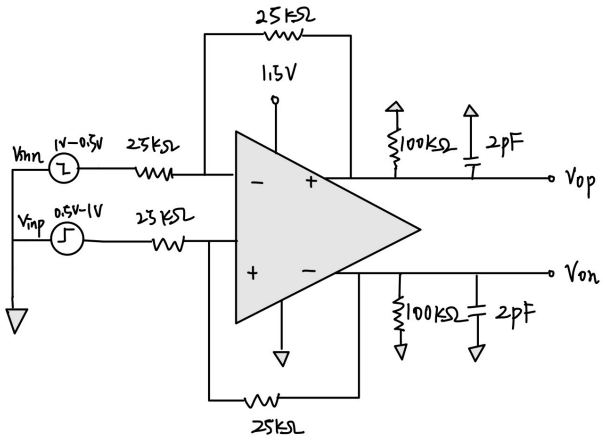


Fig3.8(a)

The Total Harmonic Distortion is calculated using the RMS values of the harmonic components as follows: $\text{THD} = \frac{\sqrt{V_2^2+V_3^2+\cdots}}{V_1}$, where V1 is the RMS value of the fundamental frequency, and V2, V3,… are the RMS values of the second, third, fourth, etc., harmonics. The values of them are derived from complicated Fourier Transform. Observing the THD results simulated, I found that differential ouput THD is relatively smaller than the singled ended output THD, this is because differential mode might eliminate the components of even harmonics, therefore reducing the value of the numerator, leading to a smaller THD value.

My differential output THD value is $20\log\left(\frac{0.0337616}{100}\right) = -69.4315\ (\text{dB}) < -60\ (dB)$.

3.9 Closed Loop Step Response



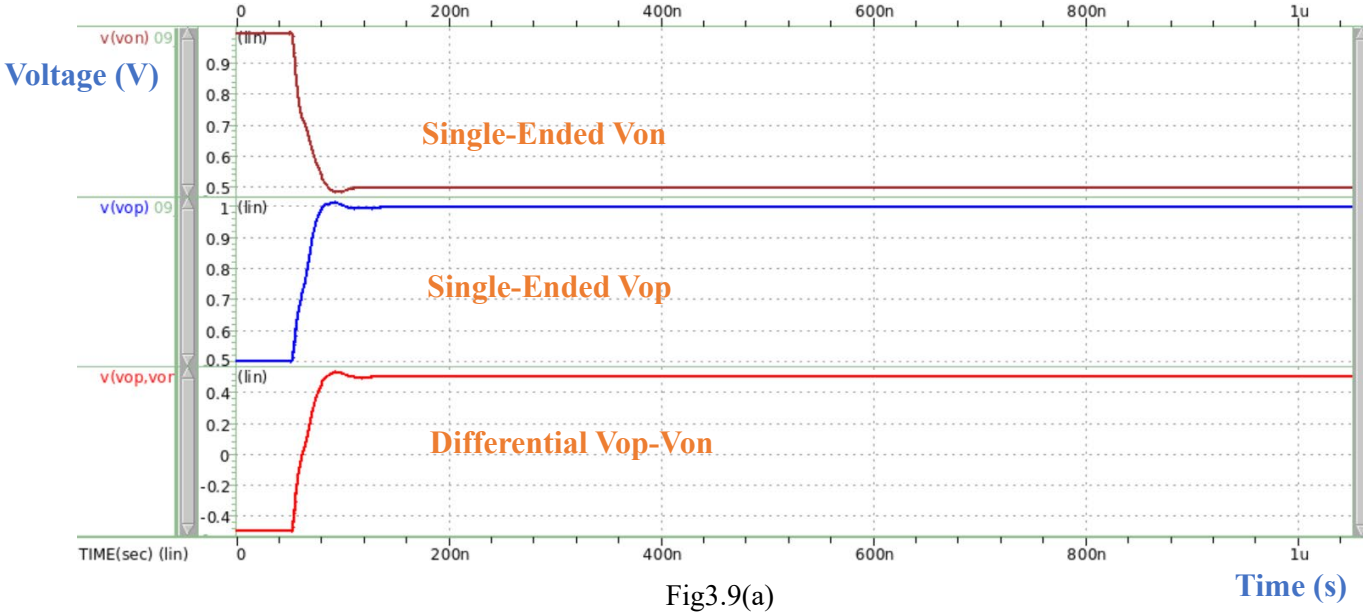


Fig3.9(a)

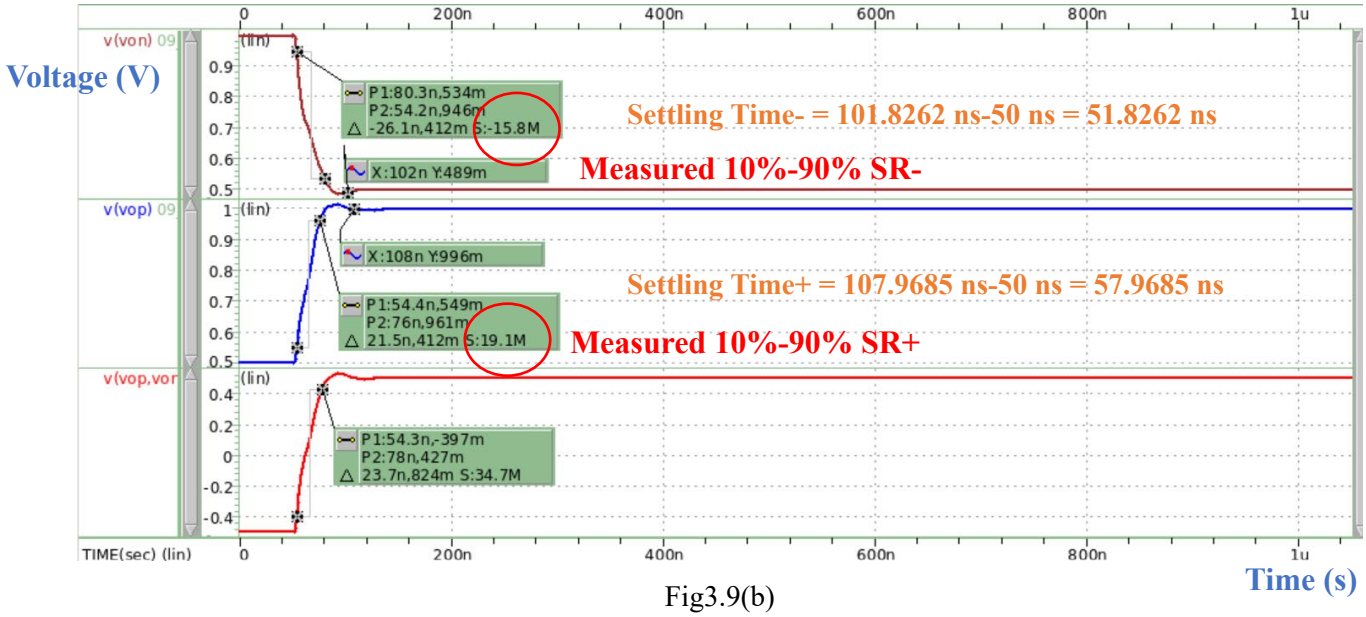


Fig3.9(b)

```
****** transient analysis tnom=  25.000 temp=  25.000 ******
final1= 997.0985m
hlimit1=   1.0021
llimit1= 992.1130m
htime1= 101.8262n
ltime1=  79.8258n
pos_settling1=  51.8262n
pos_settling_h=  51.8262n
pos_settling_l=  29.8258n
final2= 497.4462m
hlimit2= 499.9335m
llimit2= 494.9590m
htime2=  85.8154n
ltime2= 107.9685n
pos_settling2=  57.9685n
begin1= 497.4540m
begin2= 997.0937m
srp_v1= 547.4184m
srp_v2= 947.1341m
srp_time=  20.4479n  targ=  74.8253n   trig=  54.3775n
srp_diff= 399.7156m
srp=  19.5480x
srn_v1= 947.1290m
srn_v2= 547.4110m
srn_time=  24.4951n  targ=  78.6335n   trig=  54.1384n
srn_diff= 399.7180m
srn=  16.3183x
iop=  39.1948u  from=  54.3773n     to=  74.8261n
ion= -32.7586u  from=  54.1384n     to=  78.6334n
```

The simulation results above indicate that the positive settling time is 51.8262 (ns), the negative settling time is 57.9685 (ns), the positive slew rate is 19.5480 (V/us), and the negative slew rate is 16.3183 (V/us). The values mentioned above all meet the requirements of the specification. For slew rate, it is generated by the external node of the circuit, the calculations are shown in the following, and the error might come from the preciseness of the mean discharging time.

$$\mathrm{V_{op,SR}} = \frac{dVout}{dt}|_{max} = \frac{I_{op}}{C_L} = \frac{39.1948\mathrm{u}}{2\mathrm{p}} = 19.5974\ \mathrm{V/us}$$

$$\mathrm{V_{on,SR}} = \frac{dVout}{dt}|_{max} = \frac{I_{on}}{C_L} = \frac{32.7586\mathrm{u}}{2\mathrm{p}} = 16.3793\ \mathrm{V/us}$$

$$\begin{cases} Error(V_{op,SR}) = 0.252\% \\ Error(V_{on,SR}) = 0.372\% \end{cases}$$

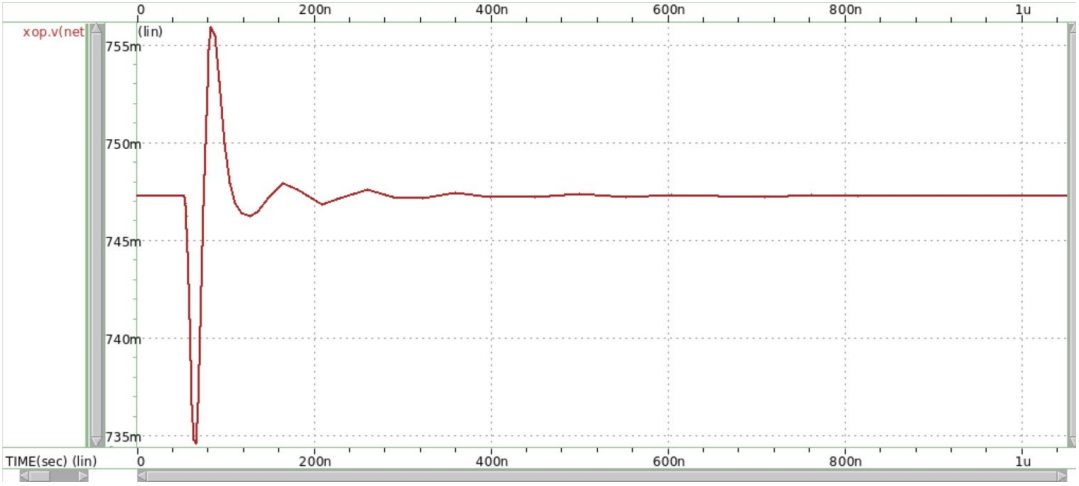


Fig3.9(c) common mode sensing node

- The common mode sensing node is located at the gate of MCM1

- **Dis.3.9(d)**

To enhance the common mode settling time and examine CMFB performance during step transients, I investigated different cases by modifying compensation elements to assess stability under normal and light load conditions. I found that reducing the damping ratio, which is closely linked to phase margin and bandwidth, is critical to decreasing settling time. Achieving an optimal phase margin and bandwidth results in a lower damping ratio, thus reducing settling time. The efficiency of the CMFB loop directly affects settling time; I discovered that optimizing Rz and Cc bolsters overall stability and shortens settling time. During step transients, the CMFB circuit mitigates deviations by averaging Von and Vop, comparing the result to the target common mode voltage, and making adjustments via the error amplifier. This feedback mechanism ensures the common mode voltage quickly returns to its intended value. By concentrating on these factors, I was able to design a system with reduced settling time and improved stability for various load conditions.

IV. Design Considerations

(a) Device Values and operation point selection

1. Startup circuit, Constant gm, Bias stage

For the design of constant gm, I chose to let the bias gate voltage of MB3, MB4 to be at roughly 0.5V, to achieve this, I designed the startup circuit to operate in the mechanism described in Dis.1(b), where MB1 is forced to be in subthreshold region and MB2, MB3 is in linear region and saturation region respectively, and the operating region can be controlled by increasing the length of MB1 largely. By doing this, my start up circuit is able to activate the constant gm circuit. Because we know that the current of MB4 and MB5 are same, so by the derivation of Dis.1(a), I found that choosing size of MB5 four times of MB4 can make control on gm4 easier by just adjusting the value of Rb. Finally, the bias voltage at net52 can be stabilized to around 0.5V when value of Rb is chosen to be 7.3k. Moreover, in the bias stage, I want to design to send a roughly 0.95V bias to pmos transistors in the main circuit. In this stage, MB9 is diode connected, so if I want to create a higher node voltage at net68, larger size in MB9 is required compared to MB8, and finally a size of 10 times larger than MB8 is chosen for MB9.

2. Design of Frequency and Time Domain

From the experience of HW6, I know that if I want to get a larger unity gain bandwidth and a more stable system, non-dominant poles are required to push away from the unity gain frequency. The reason is that if number of poles is larger, the decreasing slope of gain will stack up and lead to a more rapid reduction in gain. Referred to the equation of the second pole, I consider to let the size M10 bigger to increase gm10 to get a larger pole 2; Besides, making gm12 larger is also an approach by increasing the current of source follower. Next, zero is also considered to be pulled before the unity gain frequency. This is because zero can alleviate the reduction of gain and phase. From the equation of zero, it is obvious that compensation resistors and capacitors are crucial for it. A larger Cc can lead to a smaller zero, but on the other hand, a larger Cc can cause worse settling time and

slew rate, so for design consideration, I prefer to maintain Cc in a small value (0.73pF). Lastly, small Cc value leads to a larger dominant pole (mainly controlled by gm6), and trade-off is presented on phase margin when unity gain bandwidth increases. Therefore, It is important to make decisions on compensation devices and gm6, gm10 values to achieve better performance.

3. Design of Gain

Gain is composed of three stages mentioned in the previous section, the first stage and second stage are the main contributing stages. The buffer stage (source follower) is designed not for gain purpose, so I will neglect the discussion of buffer gain in this part. From equation of gain, $Av=g_{m1}(r_{o2} \parallel r_{o4})$ for the first stage and $Av=g_{m6}(r_{o6} \parallel r_{o7})$ for the second stage. It is simple at first to design larger gm1 and gm6, but later I found that there are some trade-offs between gain and the phase margin when choosing the value of gm6. Therefore, gm6 cannot be too large or too small, so I change my strategy to adjust the output resistances. By testing the trends, I found that increasing W/L of M1, M2 and M6, M8 pairs can increase gain. But one the other hand, a too large M6, M8 W/L might lead to an unbalanced dilemma between unity gain frequency and phase margin due to the effect of poles and zero. Besides, although multiplying a buffer gain will decrease the total gain, it plays an important role for reducing output impedance to minimize the loading effect when different stages are connected together, and thus preventing the gain to drop too much (loading effect shown in HW3 cascade).

4. Design of THD

I found that in the circuit, the source follower contributes to the THD most significantly (M10-13). The trend is to enlarge W/L of M10 and M12, while decreasing W/L of M11 and M13. Note that increasing M10 and M12 size will also bring up the current value, so I have to control the size not to be too large to suppress the current within 0.4mA. Moreover, I found that when Von and Vop are farther from Vdd/2, THD may be more stable and lower.

5. Design of Common Mode FeedBack

Because the circuit without common mode feedback will let Von and Vop change dramatically, and therefore run out of the value range of Vdd/2±1%, so a CMFB is required to correct and modify the Von and Vop value back into the range. In the CMFB block, the current is designed to be very low to reduce the total Vdd current, and it is controlled by the size of MCM5. To modify the values of Von and Vop, sizes of MCM3 and MCM4 can be adjusted to control them without changing the gain, phase margin, unity gain bandwidth and other specifications, which is the most advantageous point compared to circuit without CMFB.

(b) Compensation

Compensation design is mainly focused on the determination of Rz and Cc. Initially, I observed the trends with settling time, phase margin, bandwidth and slew rate. As mentioned previously, I designed Rz > 1/gm6 to let zero fall in the left half-sided plane. That is, Rz have to be large enough to meet the requirement, but on the other hand, the increasing of Rz will cause phase margin to reduce largely and unity frequency bandwidth to increase but not too much. Therefore, Rz should be adjusted by observing and assisting the Cc effect (main consideration).

Now considering Cc effect, it is the main influence for slew rate. When Cc decreases, slew rate increases, the trend is shown in the following graphs.

Cc=0.7pF

```
srp=  20.2820x
srn_v1= 947.1272m
srn_v2= 547.3951m
srn_time=  23.3160n  targ=  77.4446n   trig=  54.1287n
srn_diff= 399.7321m
srn=  17.1441x
iop=  40.2327u  from=  54.3773n     to=  74.8261n
ion= -33.5612u  from=  54.1384n     to=  78.6334n
```

Cc=0.75pF

```
srp=  19.0422x
srn_v1= 947.1300m
srn_v2= 547.4203m
srn_time=  25.2390n  targ=  79.3836n   trig=  54.1446n
srn_diff= 399.7097m
srn=  15.8370x
iop=  38.4822u  from=  54.3773n     to=  74.8261n
ion= -32.2275u  from=  54.1384n     to=  78.6334n
```

From simulation, I found that output node current is larger when Cc is smaller, indicates that the average current through the load capacitor increases. But there is a trade-off between phase and bandwidth, so Cc cannot be too small either. Finally, I seeked out a balance between small Cc and sufficient phase margin, unity gain bandwidth. (Rz = 4.8kΩ, Cc = 0.73pF)

(c) Supply Voltage

Comparing different supply voltages, I tried to design 1.3V and 1.5V. Initially, I used 1.3V to design, the first problem I encountered was the limitation when increasing gain, because the supply voltage was too small, the current flow in main circuit need to be large enough to compensate the lack of node bias voltages. Secondly, when performing closed loop ac response, transistors of my first stage and second stage amplifier could be easily falling into linear region, this was because my voltage distribution across all the current path is not well designed. Later, I decided to use 1.5V as my supply voltage. With a larger voltage swing, larger phase margin and unity gain frequency can be achieved using smaller current. Additionally, I found that higher supply voltages might contribute to a lower THD , and the output linearity is better than other lower supply voltages.

(d) Optimizing Performance

By integrating all the concepts above, to fulfill all the specifications, including gain bandwidth over 100 MHz, phase margin over 45 degree, gain over 80dB, current below 0.4mA, and all step transient specifications, I have to reduce the current of the CMFB and the startup, constant gm circuit to ensure that the current of first stage, second stage and buffer stage are enough. Next, improve my THD by adjusting sizes from M10 to M13. Then, a small Cc is set to get a larger slew rate as my fixed criterion and adjust gm6, gm10 and gm12 to firstly improve my unity gain frequency. Next, pick a suitable Rz to balance between phase margin and unity gain frequency. Finally, settling time can be controlled

not only by small Cc, but also the CMFB (MCM3, MCM4), and next, check if my Von and Vop are around Vdd/2. My final design and optimization flow is completely described above.

- ***Trade-offs encountered when designing:***

(the parameters in brackets are the influencing factor)

1. Gain / Unity gain frequency (M6, M7)
2. Gain Bandwidth / Phase Margin (Rz)
3. Unity gain frequency / Phase Margin (Zero)
4. Slew rate / Settling Time (Cc)
5. Gain / Total Current (gm, M1, M2, M6, M7)
6. Slew rate / Total Current (Ion, Iop)
7. Gain / THD (Buffer current)

V. Discussions

(a) Experience and challenges encountered in the project

在做此次 Final Project 時，與之前作業不同的地方是將所有之前作業與上課所學的不同級電路與觀念都整合在一起，從最基礎的尺寸對 Vth、電流等等相關參數的變化，到後來設計差動電路再到設計進階 folded cascode 電路，學到能應用在此 project 的很多觀念，例如 diode connected 電路該怎麼設計、pole 與 zero 該怎麼分配 phase margin 與 unity gain bandwidth 等等觀念。在設計的時候，遇到的最大困難是對於補償頻率系統如何與 phase margin、unity gain bandwidth 互補提升 performance，並且在調完上述的參數後，進行到 step transient 分析時，才發現 Cc 與 Rz 有一定的大小限制才能使系統穩定，否則 settling time 會變很大或者 slew rate 會變很小，因此後來重新設計時是固定補償電容 Cc 在較小值並調整主電路不同級的尺寸並配合 Rz 的修正來達到所有規格的方法。另外一點我一開始遇到的困難是還沒找到大致應該調整參數的順序，例如在前幾次我都是先依照檔案名稱的順序來一個一個看有無符合規格，但在達到 phase margin 那些 pole / zero 的規格後，發現 THD 非常大，但在嘗試幾次後發現 THD 主要由 CMFB 主導，因此我才知道先調 THD (M10-M13)再調主放大器電路尺寸並不會影響 frequency domain 的規格太多。後來我發現 settling time 因為我的補償電容太大導致系統穩定時間太長，且 slew rate 也沒有達到標準，因此學到這些教訓之後我才慢慢有概念這個龐大電路運作設計的先後順序，最後使用 1.5V 的電壓源做到其他規格全滿，只有被扣除電壓源的分數 2 分。

(b) Summarizing key insights and lessons learned from the project and the course

我認為這次 project 最重要的地方是 frequency 與 time domain 的分析，好的系統要將 pole 1、pole 2 與主導的 zero 設計在對的位置才能最優化 phase margin、unity gain frequency 的值，再來，我認為其次重要的是電流分配的設計，因為我將電流設置 0.4mA 以下，因此在此情況下 gain 需要足夠的電流支持才能達到更大值。我認為此門課與電子學不同在於每次作業的 hspice 實作，除了了解每次電路的功能與設計之外，我也學到了許多助教範例的參數量測語法和一

些 FoM 基本會看的參數指標，在以後若設計類比電路時也能有條理的去分析我所設計電路的好壞；另一方面，有時上課我發現老師的進度會越講越快，有時候會跟不上老師分析電路的速度，導致下半節課聽不太懂，希望未來老師授課時能將前面電子學基礎觀念加快講課速度，並在後面從頻率響應部分能舉更多範例練習來解釋觀念。這門課算是在這學期中花最多時間在做作業的科目，但也是相對來說我學習到最多的課，在最後的 final project 報告中我選擇使用英文撰寫，希望在這種大型專案報告中寫的正式一點，學習寫論文或是正式報告的精神。最後感謝助教每次出作業與批改時的用心，雖然很多同學不滿意天梯制度造成惡性鬥爭，但我認為這也是推動我們進步的一大動力，提醒我們任何設計沒有最好，只有更好。

VI. Reference

1. HW1~HW6
2. Reference Circuit