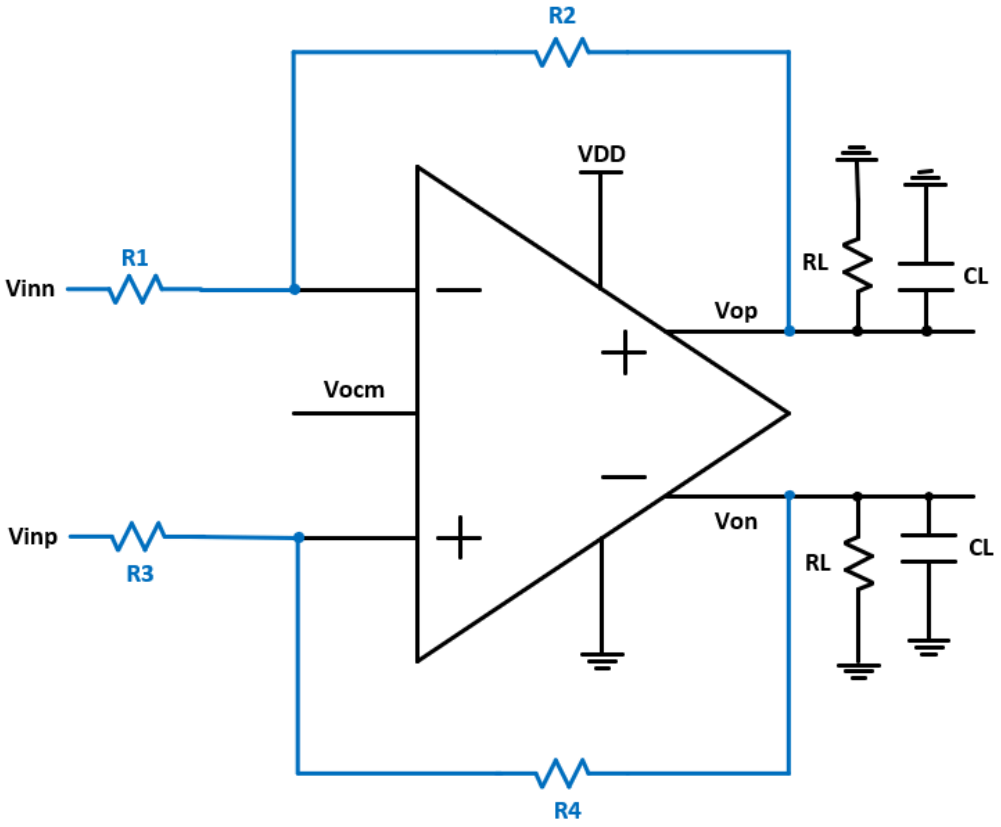
In the world of analog circuitry, operational amplifiers (OPAMPs) play a vital role in a wide range of applications. Among the various configurations, the **OPAMP-based unity-gain buffer** stands as a fundamental and versatile circuit. Its ability to provide unity gain while maintaining a high input impedance and low output impedance makes it an essential building block in analog circuit design.



In the final project, please design a **two stage differential-input, differential-output operational amplifier (OPAMP)** that operates as a unity-gain buffer of voltage gain $\frac{V_{op}-V_{on}}{V_{inp}-V_{inn}}$ > -0.1dB (at 10KHz) with a **capacitive load C_L=2pF and resistive load R_L=100kΩ**. **The values of resistors R_1~R_4 are set to be 25kΩ**. Please adhere to the instructions below to construct your circuit.

I. Implement the OPAMP as a sub-circuit with the following node definitions: "**.subckt op Vinp Vinn vdd gnd vop von vocm**". The circuit netlist file should be named "**op.spi**". **Do not include R_1~R_4, R_L and C_L in your sub-circuit**.

II. The OPAMP output should be capable of driving a loading resistor **R_L=100kΩ** and a capacitor **C_L=2pF**.

III. Only three ideal voltage sources for positive supply, negative supply and output common mode reference voltage can be used.

IV. Please use "**startup** circuit" + "**constant gm** circuit" as the biasing circuit.

V. Perform simulations using the TT corner at 25℃.

VI. The supply voltage for the OPAMP is flexible. However, **designing a supply voltage lower than 1.8 V will give you more points**. Additionally, the highest design accuracy for size can only reach $0.01\ \mu m$. Please note that the output common mode voltage **should be V_{DD}/2 ± 1% and the differential architecture should be symmetric.**

VII. The provided testbenches offered by TAs will be used for the specification table and ranking in part 2. Only the voltage of V_{DD} and V_{ocm} can be adjusted based on your design considerations. Please set V_{SS} = 0V (ground).

VIII. Please include your student ID and name on the first page of the report.

To ensure the correct format for the circuit netlist file (op.spi), please follow the format provided below:

```
.param supplyp=1.8 * Your positive supply voltage
.param supplyn=0 * Your negative supply voltage
.param comon=0.9 * Your output common mode voltage

.SUBCKT op Vinp Vinn vdd gnd vop von vocm
    Circuit Body (without voltage sources, R1~R4, RL and CL)
.ends
```

Please use this exact format for your circuit netlist file, and make sure to replace the comments with appropriate values for your design. Adhering to this format will ensure a correct testbench result.

In your report, please ensure to include the following items, and mark them clearly:

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1. Schematic and Small Signal Parameters of Active Devices (10%)

Please draw the schematic of your circuit. In the schematic, you should **label the size of each active device, the value of passive devices, DC node voltages, and branch current.** Additionally, you should use the ".op" command to print out the small signal parameters of all active devices.

Fig.1 Schematic of the Amplifier and Biasing Circuit

Lis.1 Small Signal Parameters of Active Devices (.op)

Dis.1(a) How the constant gm functions if we choose $(W/L)_{B5} = 4(W/L)_{B4}$? If a target gm is given, how do you decide the bias current of the constant gm?

Dis.1(b) Why do we need a start-up circuit? Please explain the functionality of the start-up circuit. How do you design the size of the transistors to improve the power efficiency after startup? Apply initial condition (.IC) and run the transient analysis with Hspice to verify the functionality of the start-up circuit.

2. Specification Table and Ranking (25%)

Please attach the specification table in your report. (所有數值取至小數點後第二位)

Please note that all the devices are assumed to be with **no body effect** and the current consumption includes all the circuits.

Tab.1 Specification Table

Design Items	Specifications	Score	Simulation	Calculation
Technology	CIC pseudo 0.18um technology			
Vicm, Vocm	$V_{DD}/2$			
Loading	2 pF / 100 kΩ (for each output)			
Supply voltage (V)	Open for design **≤1.8 / ≤1.5 / ≤1.3**	**2%** **4%** **6%**		
Supply current (mA) (including bias ckt)	**< 3 / < 1 / < 0.4**	**2%** **4%** **6%**		
Compensation Rz, Cc	Rz < 10 kΩ , Cc < 10 pF			
Open-loop simulation				
DC gain (dB)	**> 70 / > 75 / > 80**	**1%** **3%** **5%**		
G-BW (MHz)	**> 50 / > 75 / > 90 / > 100**	**1%** **2%** **3%** **4%**		
P.M.	> 45°			
C.M.R.R. @10KHz	> 90 dB			
P.S.R.R.+ @10KHz	> 90 dB			
P.S.R.R.- @10KHz	> 90 dB			
Closed-loop simulation				
Differential swing of 1.0 V (step or sinusoidal)				
Closed-loop gain	> -0.1dB @ 10kHz			
S.R.+ (10% ~ 90%)	> 15 V/us (single-ended output)			
S.R.- (90% ~ 10%)	> 15 V/us (single-ended output)			
THD (1.0Vpp@100kHz Sin)	< - 60 dB			
Settling+ (1.0Vstep to 0.5%)	< 150 ns			
Settling- (1.0Vstep to 0.5%)	< 150 ns			
$\frac{Settling+ + Settling-}{2}$ **(ns)**	**< 150 / < 90 / < 70 / < 55**	**1%** **2%** **3%** **4%**		

3. Simulations Results (45%)

Please use the testbenches provided from TAs for your operational amplifier simulation and compare the results with hand calculations.

3.1 Open-Loop Differential Mode AC Response

Fig 3.1(a)	Please plot the open-loop DM Magnitude and Phase Frequency Response. Mark the DC gain (dB), unity-gain frequency (Hz), and phase margin (degree) in this figure.
Tab 3.1(b)	Please print open-loop DM Gain and Impedance (.tf).
Tab 3.1(c)	Please print open-loop DM Poles and Zeros (.pz).
Dis 3.1	Please check the results with your hand calculations.

3.2 Open-Loop Differential Mode DC sweep

Fig 3.2(a)	Please plot the single-ended (Vop and Von separately) and differential (Vop-Von) outputs for inputs with differential signals. (zoom-in the operation range). Mark the slope to make sure the gain is like AC response.

3.3 Open-Loop Common Mode AC Response

Fig 3.3(a)	Open-Loop CM Magnitude Response. Mark the DC gain (dB) and poles and zeros in this figure.
Fig 3.3(b)	Open-Loop CM Gain and Impedance (.tf)
Fig 3.3(c)	Open-Loop CM Poles and Zeros (.pz)
Dis. 3.3	Please check the results with your hand calculations. (gain, and low frequency zero)

3.4 Open-loop common mode DC sweep

Fig. 3.4(a)	Please plot the single-ended (Vop or Von) Mark the slope to make sure the gain is like AC response.

3.5 Open-loop power supply AC response

Fig. 3.5(a) Please plot the magnitude response of power supply+ gain. Mark the DC gain (dB) in this figure.

Fig. 3.5(b) Please plot the magnitude response of power supply- gain. Mark the DC gain (dB) in this figure.

3.6 Closed-loop differential mode AC response

Fig. 3.6(a) Please plot the closed-loop magnitude and phase of DM gain frequency response. Mark the DC gain (dB) and -3dB bandwidth (Hz) in this figure.

Dis. 3.6(b) Compare DC gain and -3dB bandwidth with hand calculations.

Fig. 3.6(c) Please print the input and output node voltages from .op command.

Fig. 3.6(d) Please print the values of gain and impedances from .tf command.

Dis. 3.6(e) Please check the above .tf results with your hand calculations.

3.7 Closed-loop differential mode DC sweep

Fig. 3.7(a) Please plot the single-ended (Vop and Von separately) and differential (Vop-Von) outputs for inputs with differential signals. Mark the slope and compare it with gain in AC response.

3.8 Closed-loop distortion simulation

Fig. 3.8(a) Please plot the single-ended (Vop and Von separately) and differential (Vop-Von) outputs for 100KHz sinusoidal inputs with differential peak-to-peak signal of 1.0V. The THD must be less than -60dB.

3.9 Closed-loop step response

Fig. 3.9(a) Please plot the single-ended (Vop and Von separately) and differential (Vop-Von) outputs for 1.0V differential step inputs in one figure.

Fig. 3.9(b) Please mark the slew rate+ (10% to 90%), settling+ time (to 1% error), and slew rate- (90% to 10%), settling- time (to 1% error) in the figure. Check the slew rate results with your hand calculations

Fig. 3.9(c) Please plot the common mode sensing node waveform.

Fig. 3.9(d) Try to improve the common mode settling time. And discuss the CMFB operation during step transient.

4. Design Considerations (15%)

Please provide an explanation of your design considerations and optimizations regarding the following aspects:

(a) Device Values and operation point selection

Discuss how you determined the values of operation point, active and passive devices **in detail** of your design. Explain any considerations such as gain requirements, biasing conditions, and device matching.

(b) Compensation

Describe the compensation techniques employed in your design to ensure stability and prevent oscillations. Discuss how you determined the values of compensation components, such as capacitors and resistors.

(c) Supply Voltage

Explain your decision-making process and challenge for selecting the supply voltage for your operational amplifier.

(d) Optimizing **performance**

Describe how you achieve a better performance and the trade-offs you made.

5. Discussions (5%)

(a) Please provide a discussion of your experience with this project, including any challenges encountered during design.

(b) Conclude by summarizing the key insights and lessons learned from the project and provide suggestions for the improvement of this course.

6. References

State your reference following the same pattern as the example below:

[1] Chen, Lao-Da; Wang, Shuai-Qi; Chan, Bo-Shi; Tu, Bo-Shi. "A 10-Bit 2-GS/s Student-to-Scholar Converter with Shared Semi-Resting Switching Procedure" in 2023 IEEE International Solid-State Circuits Conference - (ISSCC), San Francisco, CA, USA, 2023, pp. 110-112, doi: 10.1109/ISSCC412.9889

7. Submission Guidelines

Please submit the following files following the same pattern as the example below:

- Final_1100XXXXX.pdf (PDF Report File)
- op.spi (HSPICE Circuit Netlist File)