2024 Analog IC Design Homework 3 ***due date: 2024/04/16***

Note: all the simulations are under TT 25°C

1. **Cascode amplifier (35%)**

   Design a common-source amplifier with cascode loading as shown in Fig. 1.
   With $\mathbf{V_{DD}=1.8V}$, design the size of M_1~M_4, the bias voltage V_{b1}~V_{b3}, and $V_{in,DC}$, to make $I_D < 5\mu A$, voltage gain $|A_v| \geq 45dB$, and output swing $\geq 1.2V$. You need to make sure that **all MOSFETs operate in saturation region**.

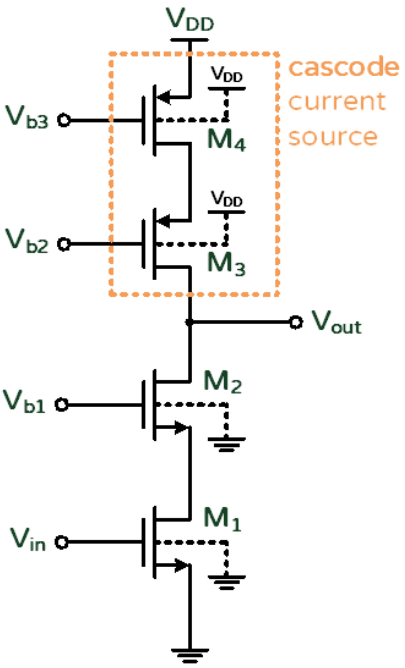


Fig. 1. Cascode structure

(a) Describe your design consideration. (How you choose the size of M_1~M_4, the bias voltage V_{b1}~V_{b3}, and $V_{in,DC}$, to achieve the target performance.) (10%)

(b) Use ".op" command in Hspice and check the ".lis" file to show that all MOSFETs operate in saturation region, and that $I_D < 5\mu A$. (3%)

(c) Use ".tf" command in Hspice to print out the small signal parameters (gain and output impedance). Confirm that $|A_v| \geq 45dB$. (2%)

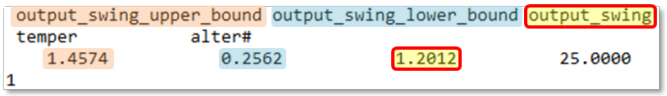
(d) Calculate Av and output impedance **by hand-calculation**. You can use the parameters in ".lis" from (b). Then compare your answer with the simulation results in (c). (5%)

(e) Use ".dc" command to sweep V_{in} from 0V to 1.8V (set **step=0.00001V=10μV**) in Hspice. Show that output swing $\geq$ 1.2V **under the condition $|A_v| \geq 45dB$ using WaveView**. (5%)

Hint: You can use the following Hspice command in your .sp file

```
.dc Vin_value 0 1.8 10u
.meas DC output_swing_upper_bound Find V(vout) WHEN deriv('V(vout)')='-10^(45/20)' cross=1
.meas DC output_swing_lower_bound Find V(vout) WHEN deriv('V(vout)')='-10^(45/20)' cross=2
.meas DC output_swing param='output_swing_upper_bound-output_swing_lower_bound'
```

After simulation, you will see the measured value of output_swing in .ms0 file:



However, this is just for quickly checking output swing for convenience. ***You should still show output swing ≥ 1.2V using cursor in WaveView !!***

Hint: You can use the following Hspice command in your .sp file

```
.dc Vin_value 0 1.8 10u
.probe gain=deriv('V(vout)')
```

which is because "$A_v=\frac{\partial Vout}{\partial Vin}$."

After simulation, you can see "gain (V/V) v.s. V_{in} (V)" waveform ***in WaveView****.*

(f) Calculate output swing **by hand-calculation**. You can use the parameters in ".lis" from (b). Then compare your answer with the simulation result in (e), and **describe** where the error comes from. (5%)

(g) Please fill in the following specification table. Make sure you achieve all the requirements. (5%)

	specification	**simulation**	**hand-calculation**
V_{DD}	1.8V		
M_1 (W/L, m)	–		
M_2 (W/L, m)	–		
M_3 (W/L, m)	–		
M_4 (W/L, m)	–		
$V_{in,DC}$	–		
V_{b1}	–		
V_{b2}	–		
V_{b3}	–		
I_D	< 5μA		–
gain $\|A_v\|$	≥ 45dB		
output impedence	–		
output swing	≥ 1.2V		

Table 1. Specification table for problem 1.

2. Cascade amplifier (55%)

Design a CS-CG cascade amplifier as in Fig. 3.

(a) As shown in Fig. 2.(a), with **V_{DD}=1.8V**, design the common source stage (with ideal current source load, static current=3μA) to make $V_{out1,DC}$=0.5V (within ±10mV variation) and voltage gain $|A_{v1}| \geq 100$V/V.

i. Describe your design consideration (How you choose the size of M_1 and $V_{in,DC}$). (5%)

ii. Use ".op" command in Hspice and check the ".lis" file to show that M_1 operates in saturation region, and that $V_{out1,DC}$=0.5V (within ±10mV variation) (3%)

iii. Use ".tf" command in Hspice to print out the small signal parameters (gain and output impedance). Confirm that $|A_{v1}| \geq 100$V/V. (2%)

iv. Calculate Av1 **by hand-calculation**. You can use the parameters in ".lis" in (ii.). Then compare your answer with the simulation results in (iii.). (5%)

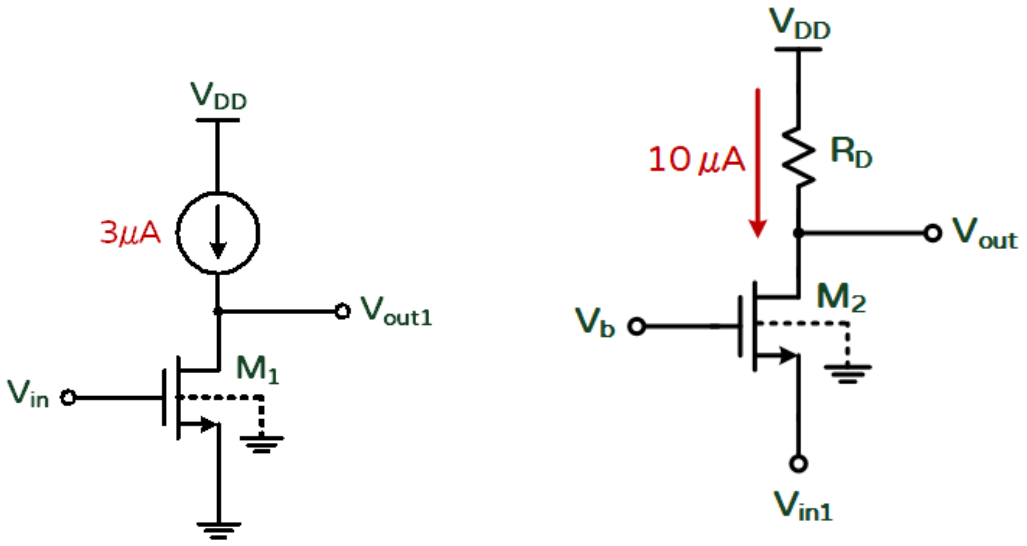
(b) As shown in Fig. 2.(b), with **V_{DD}=1.8V and $V_{in1,DC}$=0.5V**, design the common gate stage to make I_D=10μA (within 1% variation) and voltage gain $|A_{v2}| \geq 10$V/V.

i. Describe your design consideration (How you choose the size of M_2, the bias voltage V_b, and the resistance of R_D). (10%)

ii. Use ".op" command in Hspice and check the ".lis" file to show that M_2 operates in saturation region, and that I_D=10μA (within 1% variation). (3%)

iii. Use ".tf" command in Hspice to print out the small signal parameters (gain, input impedance, and output impedance). Confirm that $|A_{v2}| \geq 10$V/V. (2%)

iv. Calculate Av2, input impedance, and output impedance **by hand-calculation**. You can use the parameters in ".lis" in (ii.). Then compare your answer with the simulation results in (iii.). (5%)



(a) (b)

Fig. 2. Two stages in cascade structure. (a) stage 1; (b) stage 2

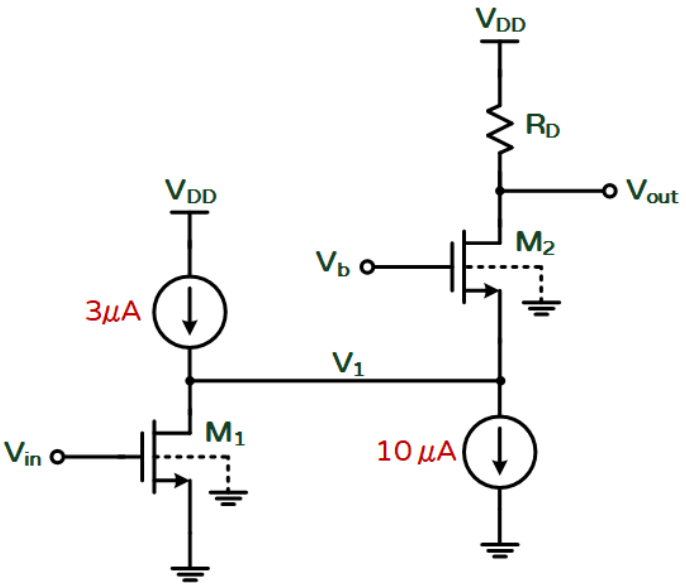


Fig. 3. Cascade structure

(c) Connect the above two stages and **add an additional 10μA current source** as shown in Fig. 3.

i. Use ".op" command in Hspice and check the ".lis" file: Is the DC bias (V_1) still **around 0.5V**? (5%)

ii. After simulation, whether the overall gain (from V_{in} to V_{out}) equals $A_{v1}\times A_{v2}$ or not? If not, why not? (5%)

iii. Please calculate the overall gain **by hand-calculation**, and compare your answer with the simulation results in (ii.). (5%)

(d) Please fill in the following specification table. Make sure you achieve all the requirements. (5%)

	specification	**simulation**	**hand-calculation**
Fig. 2.(a) Common-Source stage			
V_{DD}	1.8V		
current source load	3μA		
M_1 (W/L, m)	–		
$V_{in,DC}$	–		
$V_{out1,DC}$	0.5V±10mV		–
gain $\lvert A_{v1}\rvert$	≥ 100V/V		
output impedence	–		–

Fig. 2.(b) Common-Gate stage			
V_{DD}	1.8V		
$V_{in1,DC}$	0.5V		
M_2 (W/L, m)	–		
V_b	–		
R_D	–		
I_D	10μA±1%		–
gain $\lvert A_{v2}\rvert$	≥ 10V/V		
input impedence	–		
output impedence	–		
Fig. 3. Cascade CS-CG amplifier			
V_{DD}	1.8V		
DC bias (V_1)	–		–
overall gain $\lvert A_v\rvert$	–		

Table 2. Specification table for problem 2.

3. **Comparison between "cascode structure" & "cascade structure" (10%)**
   In this problem, let's discuss the differences between "cascode structure" and "cascade structure". What are the advantages and drawbacks of each of them? List from **two** points of view, for example, output swing and power. (5% for each)

1.	From _____ point of view, cascode / cascade structure is better than the other one because _____ .
2.	From _____ point of view, cascode / cascade structure is better than the other one because _____ .