#HW3 Cell Based Phased-Locked Loop Design report

◆ **Group member**

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◆ **Contribution**

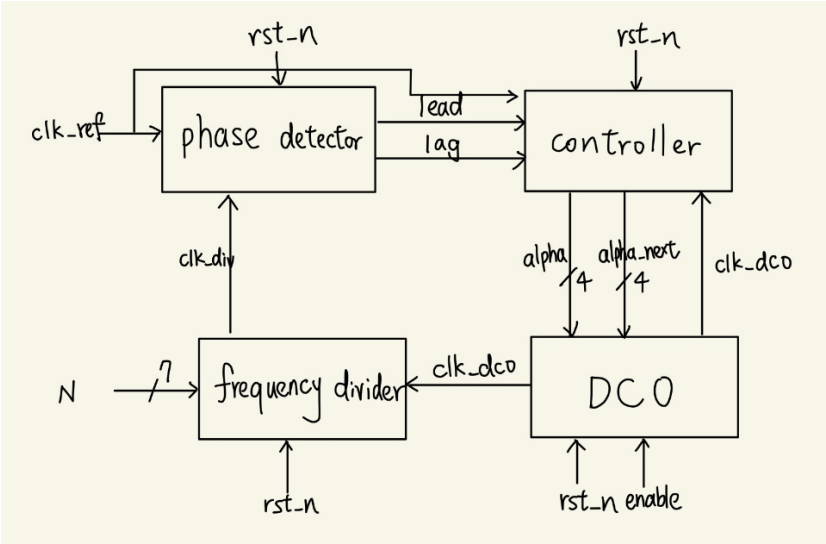
1. 林士登 - Verilog code, Testbench, Synthesis, Layout testing and Simulations, Final summary report
2. 陳立珩 - Verilog code, Testbench, Synthesis, Layout testing and Simulations

◆ **Outline**

1. PLL Architecture
2. PLL waveform and frequency comparison (pre-layout / post-layout)
3. Functional cells in PLL
4. Gate-level synthesis / Gate simulation report
5. Layout generation and analysis

◆ **Results and Analysis**

1. PLL Architecture

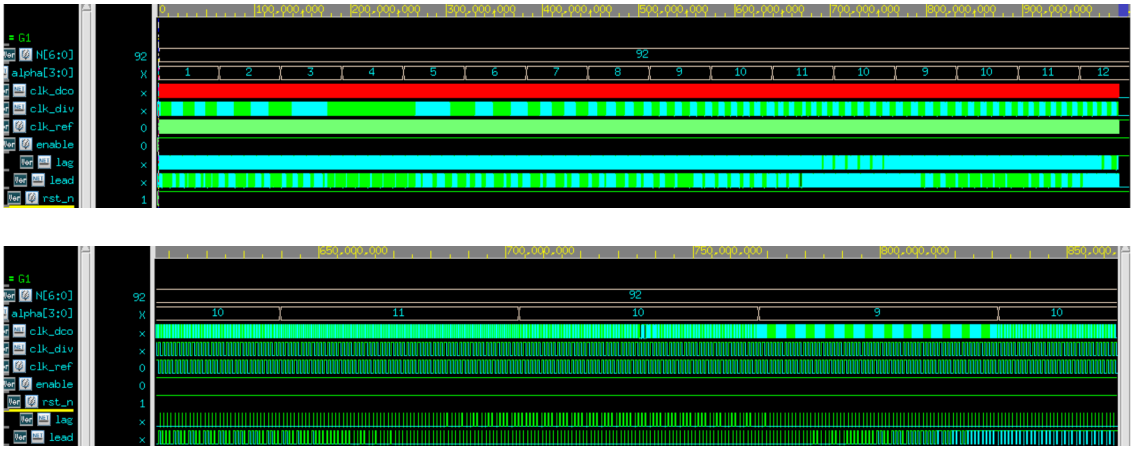


The graph indicated above represents our main PLL architecture. The main goal of the PLL is to achieve a 92MHz output clk signal with input reference clk of 1MHz. In addition to the general PLL design approach, we designed the controller and DCO more resilient to prevent the frequency divider from feeding in some glitch generated during the alpha code transition, the functional blocks and their corresponding function will be shown in the following part in our report (part 3.).

2. PLL waveform and frequency comparison

('PLL.v' and 'PLL_tb.v' code file is included in the submit area)

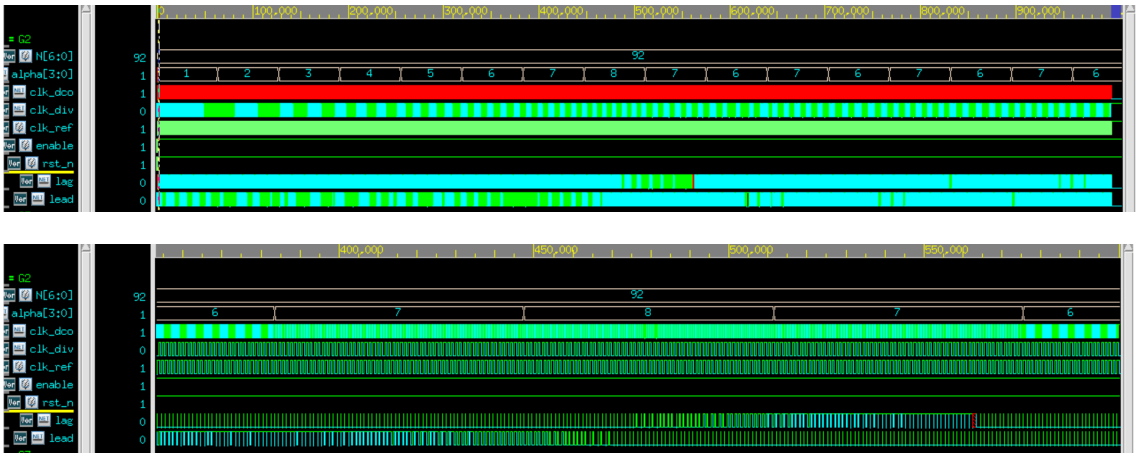
Pre-sim



(entire timeline vs. frequency acquisition)

- ✓ alpha = **10**, period = **10.848ns**, frequency = **92.183MHz**
- ✓ alpha = **11**, period = **10.976ns**, frequency = **91.108MHz**
- ✓ The average clock cycle times of clk_out observed over 10 clock cycles after the frequency acquisition is 10.848ns, the error compared to the ideal clock cycle time is | 10.848 - 10.87 | = **0.022ns**, which is **0.2%** in percentage .

Post-sim



(entire timeline vs. frequency acquisition)

- ✓ alpha = **6**, period = **10.807ns**, frequency = **92.533MHz**
- ✓ alpha = **7**, period = **10.941ns**, frequency = **91.399MHz**
- ✓ The average clock cycle times of clk_out observed over 10 clock cycles after the frequency acquisition is 10.807ns, the error compared to the ideal clock cycle time is | 10.807 - 10.87 | = **0.063ns**, which is **0.6%** in percentage .

Comparison of waveforms : The gate delays in post-layout is larger than those in pre-layout, which results in faster starting of frequency acquisition.

3. Functional cells in PLL

(phase_detector.v / frequency_divider.v / controller.v / DCO.v is included)

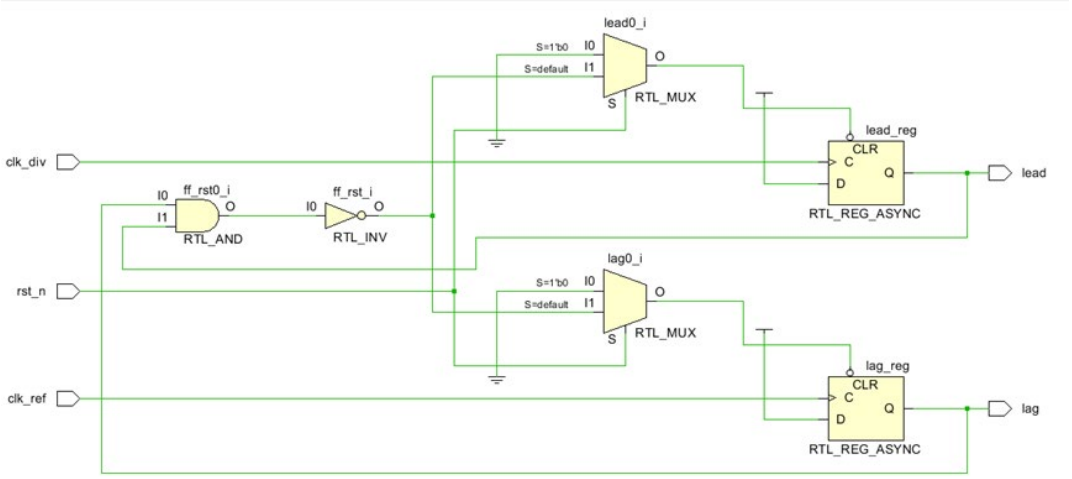
① Phase detector

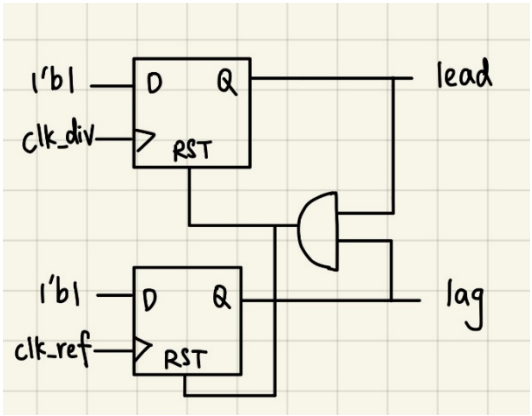
✓ ***IO:***

Input: clk_ref(clk), clk_div(clk_div), rst_n(rst_n)

Output: lead(lead), lag(lag)

✓ ***Logic diagram:***





✓ ***Operating mechanism:***

If clk_div lags clk_ref, then the phase detector produces a lag pulse. If clk_div is ahead of clk_ref, the phase detector produces a lead pulse. When both clk_div and clk_ref arrive, reset the lead and lag signals to 0.

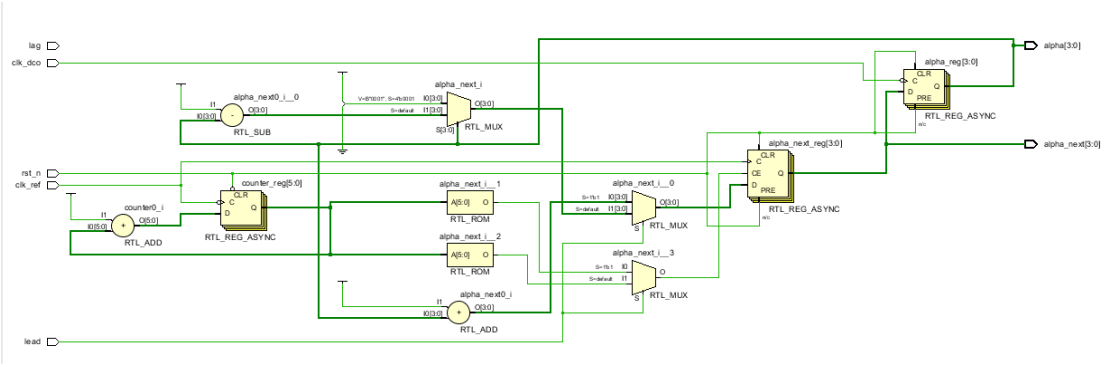
② Controller

✓ ***IO:***

Input: clk_dco(clk_dco), clk_ref(clk_ref), lead(lead), lag(lag), rst_n(rst_n)

Output: alpha(alpha), alpha _next(alpha_next)

✓ ***Logic diagram:***



✓ ***Operating mechanism:***

The controller is designed to detect the lead lag signal every 64 clk_ref cycles (counter = 64). If clk_div is ahead of clk_ref (lead), the alpha_next value will be incremented by 1. Otherwise, the alpha_next value will be decremented by 1. In addition, we designed to pass alpha_next to alpha when encountering clk_dco negative edge (because we found that switching code at negative edge clk_dco may eliminate glitches)

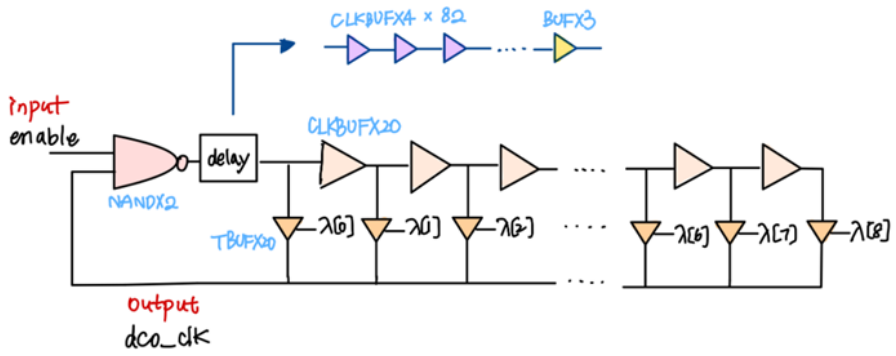
③ DCO

✓ ***IO:***

Input: enable(enable), rst_n(rst_n),alpha(alpha),alpha_next(alpha_next)

Output: clk_dco(clk_dco)

✓ ***Logic diagram:***



✓ ***Operating mechanism:***

The design is as same in HW2, but in order to eliminate glitches, we deliberately switch the lambda code when alpha == alpha_next.

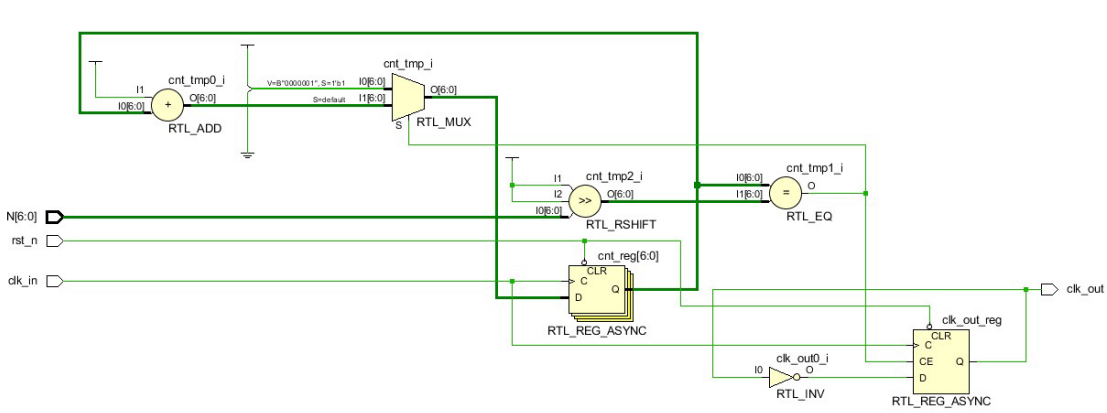
④ Frequency_divider

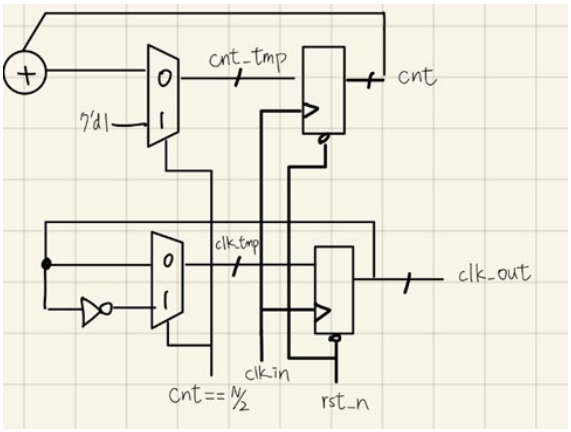
✓ ***IO:***

Input: clk_in(clk_dco), rst_n(rst_n), N(N)

Output: clk_out(clk_div)

✓ ***Logic diagram:***





✓ ***Operating mechanism:***

We designed a counter to calculate **N/2**, then declare a variable **cnt_tmp**. If the value of counter is equal to **N/2**, reset the counter and continue the loop. Next, we designed a flip-flop with an input **clk_tmp** and an output **clk_out**, which changes (~clk_tmp) every **N/2** times. Finally, a clock with frequency of **(clk_in)/N** can be generated.

4. Gate-level synthesis / Gate simulation report

Area Report

```
Combinational area:                913.046416
Buf/Inv area:                      491.803210
Noncombinational area:            1157.889605
Macro/Black Box area:               0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:                  2070.936021
Total area:                 undefined
```

① The total area shown in the 'PLL_syn.report' file is 2070.936021 um^2.

② The number of final gate count is 2070.936021 / 2.8224 = 733.75 .

Power Report

Power Group	Internal Power	Switching Power	Leakage Power	Total Power	(%)	Attrs
io_pad	0.0000	0.0000	0.0000	0.0000	(0.00%)	
memory	0.0000	0.0000	0.0000	0.0000	(0.00%)	
black_box	0.0000	0.0000	0.0000	0.0000	(0.00%)	
clock_network	0.0000	0.0000	0.0000	0.0000	(0.00%)	
register	1.5906e-02	2.1521e-04	5.9499e+05	1.6716e-02	(12.98%)	
sequential	2.6711e-02	6.3730e-05	2.3286e+06	2.9104e-02	(22.60%)	
combinational	5.1189e-02	2.4078e-02	7.6650e+06	8.2932e-02	(64.41%)	
Total	9.3806e-02 mW	2.4357e-02 mW	1.0589e+07 pW	0.1288 mW		

① Cell Internal Power = 93.806 uW (74%)

② Net Switching Power = 24.357 uW (26%)

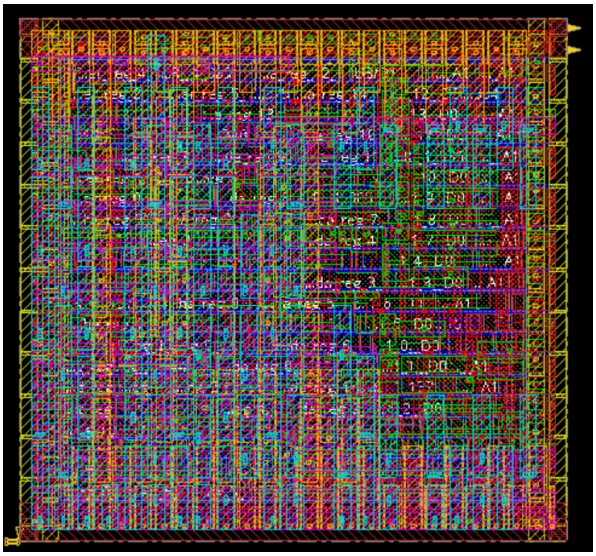
③ Total Dynamic Power = 93.806 + 24.357 = 118.163 uW (100%)

④ Cell Leakage Power = 10.589 uW

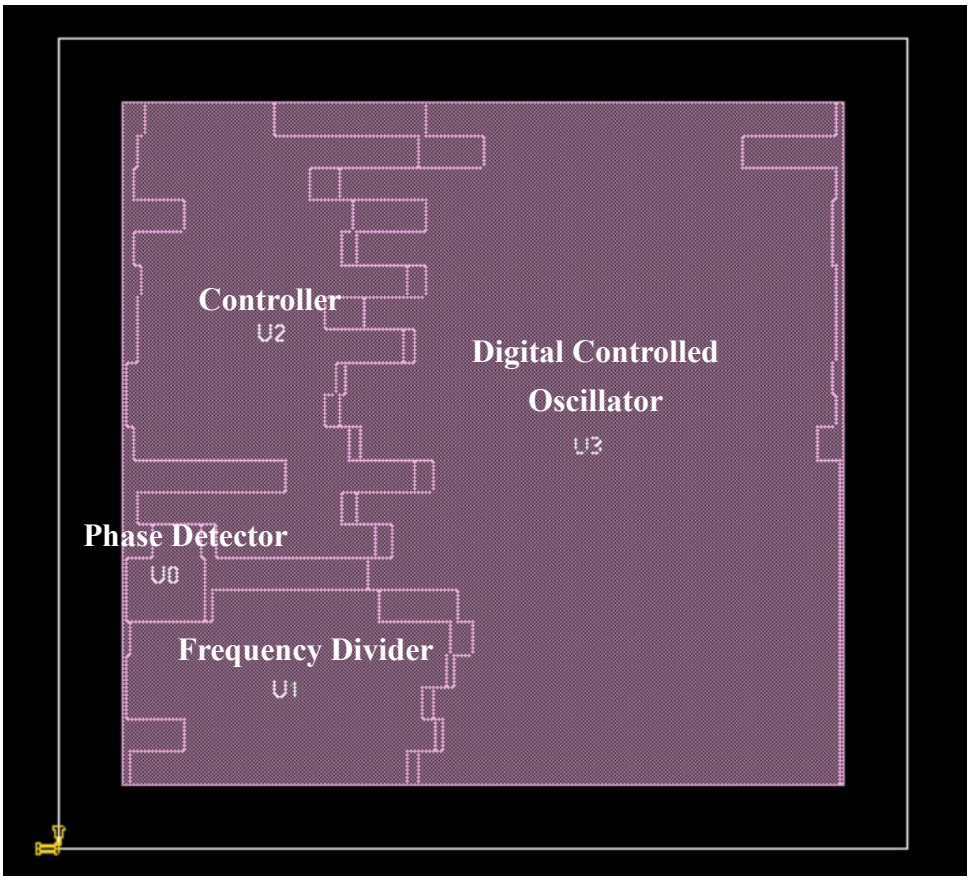
⑤ Total Power = 0.1288 mW

5. Layout generation and analysis

Physical view



Amoeba view



Area Report

Layout total area = 2075.170 um^2.

```
innovus 2> report_area
    Hinst Name       Module Name                                Inst Count          Total Area
-------------------------------------------------------------------------------------------
PLL                                                                    241            2075.170
 U0                  phase_detector                                      4              38.808
 U1                  frequency_divider                                  31             258.250
  U1/add_18_aco      frequency_divider_DW01_inc_0_DW01_inc_2             7              60.682
 U2                  controller                                         43             461.462
 U3                  DCO                                               163            1316.650
```

Power Report

```
Total Power
-------------------------------------------------------------------------------------------
Total Internal Power:        0.07820970            76.5267%
Total Switching Power:       0.01688925            16.5258%
Total Leakage Power:         0.00710033             6.9475%
Total Power:                 0.10219927
-------------------------------------------------------------------------------------------
```

1. Total Internal Power = 0.07820970 mW
2. Total Switching Power = 0.01688925 mW
3. Total Leakage Power = 0.00710033 mW
4. Total Power = 0.10219927 mW