A Fast-Locking All-Digital Fractional-Ratio Multiplying DLL

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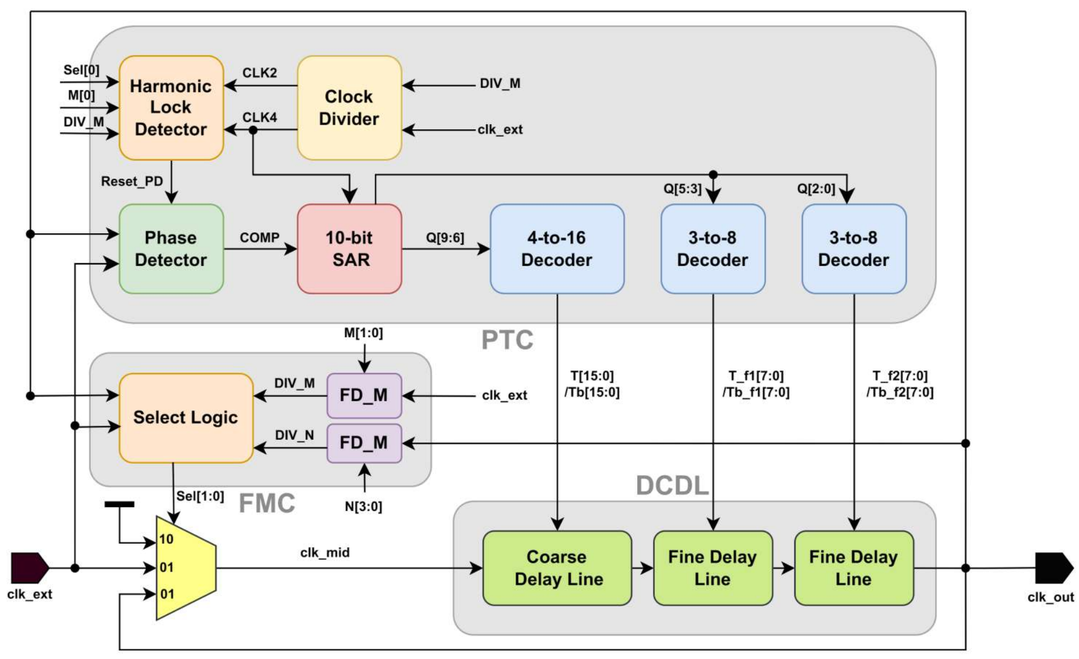
Abstract

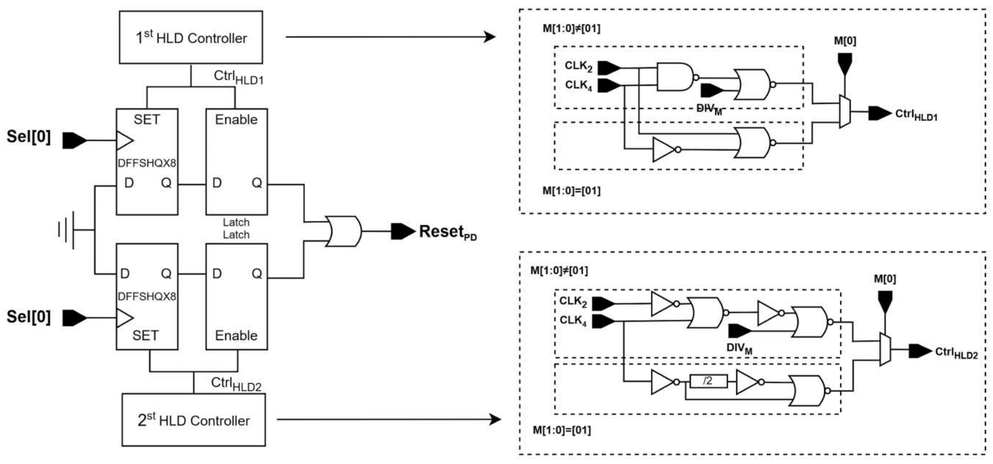
The project aims to develop a frequency-multiplying Delay-Locked Loop with fractional ratios (FMDLL). The new proposed circuit architecture adopts the Successive Approximation algorithm Register (SAR) and Harmonic Lock Detector (HLD) to achieve fast locking times and to ensure stable clock output even under complex frequency transition conditions. The project implementation is based on Cell-based Design Flow utilizing TSMC 90-nm process technology. The FMDLL provides a frequency multiplication ratio of N/M (N>M), with M={1, 2, 3} and N={1, 4, 5, 8, 10}, not only improving jitter control and locking times over traditional PLL and MDLL, but also opening new possibilities in meeting dynamic frequency scaling and precise frequency synthesis.

Implementation



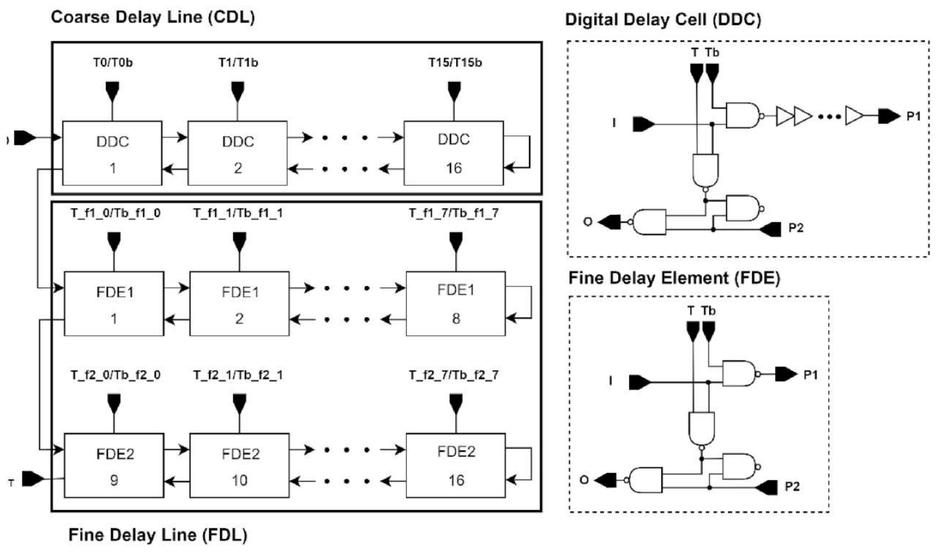
Proposed FMDLL Architecture

The FMDLL Architecture comprises four key components: the Phase Tracking Controller (**PTC**), the Frequency Multiplying Controller (**FMC**), a 3-to-1 Multiplexer, and a Digital Control Delay Line (**DCDL**). Within the PTC, the Successive Approximation Register (SAR) utilizes a binary search algorithm to achieve the desired delay, significantly reducing the locking time. In the FMC, an innovative Select Logic is integrated, offering three logical operating modes to enhance circuit stability.



Harmonic Lock Detector

A Harmonic Lock Detector (**HLD**) has been introduced in the PTC to rectify phase locking errors that may arise from substantial shifts in the delay control code Q[9:0].



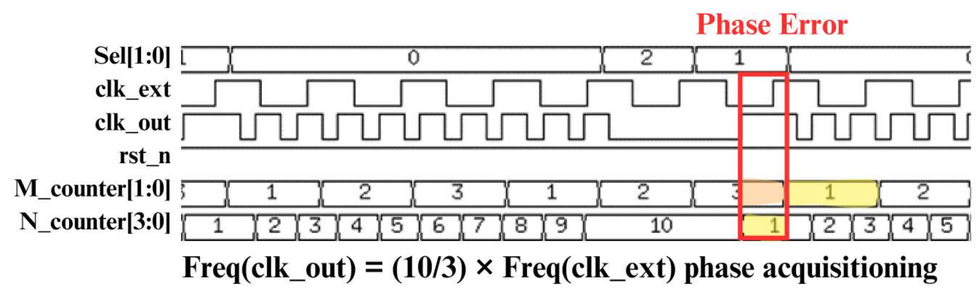
Digital Control Delay Line

The **DCDL** is segmented into three parts: a Coarse Delay Line and two Fine Delay Lines, each composed of multiple unit delay cells.

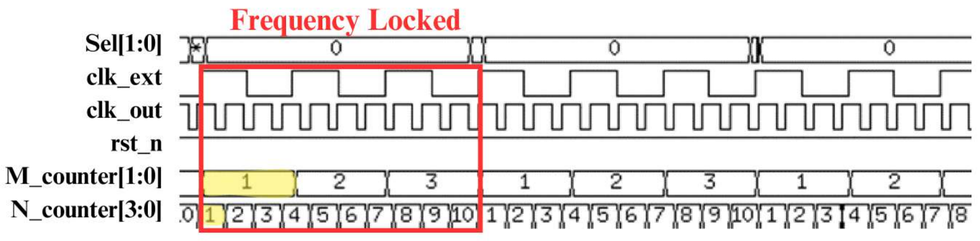
This architecture enables the FMDLL to achieve rapid locking in just **4×k×M** input clock periods (where 'k' represents the number of bits in Q), while also delivering a fractionally multiplied output frequency, defined as **freq(clk_out) = freq(clk_ext)×(N/M).**

Results

N/M=10/3, Tclk_ext = 30ns



Freq(clk_out) = (10/3) × Freq(clk_ext) phase acquisitioning

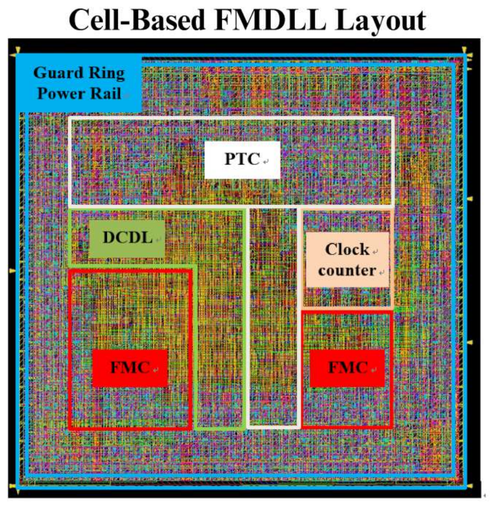


Freq(clk_out) = (10/3) × Freq(clk_ext) locked

FMDLL Performance Comparison In Paper Reference [1]

	[1] TCAS-1	Our Work
Architecture	All Digital	All Digital
Technology	TSMC 65nm	TSMC 90nm
Output Freq. (GHz)	0.7 - 2.0	0.004 - 0.114
Pk-to-Pk jitter (ps) @x-GHz	22 @2-GHz (1.1% UI)	250.60 @0.111-GHz (0.83% UI)
RMS jitter (ps) @x-GHz	2.859 @2-GHz (0.14% UI)	73.90 @0.111-GHz (0.25% UI)
Power (mW) @x-GHz	3.31 @1-GHz	0.20 @0.111-GHz
Chip Area (mm^2)	0.019	0.0360491

Cell-Based FMDLL Layout



Minimum & Maximum Freq. Range

Unit (MHz)	Input Frequency Range	Output Frequency Range
Pre-Layout	10.00-88.50	59.95-173.61
Post-Layout	1.00-50.00	4.00-114.32

UI : unit interval, one clock cycle time, **UI of [1]** : 2ns, **UI of our work** : 30ns /
The jitter types mentioned above are period jitter

Conclusion

In our analysis of the FMDLL we designed, the greater delay in our DCDL led to an output frequency range of only 4 - 114 MHz, which is considerably lower than the 0.7 - 2.0 GHz achieved in the paper [1]. Due to the larger clock signal period in our design, we observed relatively higher jitter. However, when we calculate the jitter relative to the input signal period, as in reference [2], the jitter-to-UI ratios of Peak -to-Peak and RMS jitter are similar to the values in paper [1]. Additionally, due to our lower maximum output frequency, the power consumption measured is lower compared with that of paper [1].

After completing our design process, the table above reveals that while the FMDLL circuit's basic functionality has been achieved, there is still considerable potential to improve the output frequency. Future optimizations should focus on improving the precision of the Delay Control Delay Line (DCDL) and its fine-tuning capabilities. With the aim of increasing the output frequency, we also hope to achieve tighter control over jitter.

Reference

[1] Jongsun Kim, and Sangwoo Han, “A Fast-Locking All-Digital Multiplying DLL for Fractional-Ratio Dynamic Frequency Scaling” IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: EXPRESS BRIEFS, VOL. 65, NO. 3, MARCH 2018

[2] Shi-Yu Huang, "Timing Circuit Design and Applications", Department of Electrical Engineering, National Tsing Hua University, Hsinchu, Taiwan, 2023.

[3] Shi-Yu Huang, "Cell-based IC Design and Implementation", Department of Electrical Engineering, National Tsing Hua University, Hsinchu, Taiwan, 2023.