Simulation and Analysis on the Electrical Characteristics of Scaled Superlattice GAA Lateral Nanowire Structures

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***Abstract*—This special topic aims to study the impact on the performance of lateral nanowire transistors by varying transistor structures, gate lengths, wire diameters, and wire pitches. The entire study is based on Sentaurus TCAD. A novel superlattice structure, consisting of alternating silicon and silicon-germanium layers, is introduced into the source and drain regions. The first project demonstrates that the superlattice LNW exhibits better electrical performance compared to the traditional all-silicon LNW. The second project simulates various wire diameters along with different channel lengths and pitches between each nanowire. The results indicate that reducing the gate length significantly degrades the electrostatic control of the device. However, this can be mitigated by decreasing the wire diameter. By understanding the trade-offs of device parameters, it is possible to achieve smaller nodes with enhanced device performance.**

***Keywords*—nanowire, Sentaurus TCAD, lateral gate-all-around (GAA) FET, scaling, superlattice**

I. Introduction

As technology scaling continues, the traditional FinFET structure is increasingly unable to provide sufficient gate control. Gate-all-around (GAA) or nanowire FETs (NWFETs) are promising candidates for CMOS scaling due to their excellent electrostatic integrity. For NWFETs, the channels can be oriented either vertically or horizontally, with more nanowire channels contributing to improved electrical properties such as subthreshold slope, DIBL, and so on. Additionally, the traditional all-silicon transistor structure is being replaced with superlattice Si and SiGe materials. By applying compressive or tensile strain between the Si and SiGe layers, carrier mobility is increased, thereby improving device speed and reducing short-channel effects.

From another perspective, reducing gate length exacerbates short-channel effects. Simulations are shown that reducing the nanowire diameter can improve electrostatic control at shorter gate lengths. The pitch distance between nanowires is also simulated, revealing that pitch values cannot be too small to avoid dramatical change in non-ideal effects.

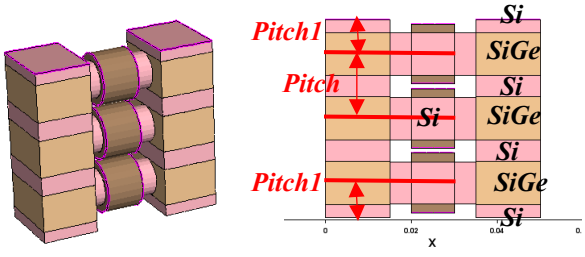

Fig.1. Lateral Nanowire transistor with superlattice structure (a) Three stacked LNW (b) cross-sectional view

II. Methodology

The gate-all-around LNW superlattice structure indicated in Fig.1.(a) is constructed with TCAD. It is stacked with three independent lateral nanowire channel. The cross-sectional view superlattice shown in Fig.1.(b) has seven layers in drain and source region. The SiGe layers are set to have mole fraction of $Si_{0.8}Ge_{0.2}$. The parameters of the structure is shown in the following table.

Table.1 Device Specifications

Parameters	***Project I***		
Channel Doping	10^17 cm^{-3}		
S/D Doping	8*10^19 cm^{-3}		
Wire radius	3nm	3.6nm	4.2nm
HfO2 Thickness	2nm		
Gate length	10nm		
Interlayer pitch	15nm		
Pitch1	8nm		
Channel Spacer	5nm		
$Si_{1-x}Ge_x$ (x)	0.2		
Work function	4.5eV		
Vg/Vd	1V/1V		

Parameters	***Project II***	
Channel Doping	10^17 cm^{-3}	
S/D Doping	8*10^19 cm^{-3}	
Wire radius	3nm	4nm
HfO2 Thickness	2nm	
Gate length	10~26nm, step=2nm	
Interlayer pitch	10~19nm, step=1nm	
Pitch1	8nm	
Channel Spacer	5nm	
$Si_{1-x}Ge_x$ (x)	0.2	
Work function	4.5eV	
Vg/Vd	0.7V/1V	

III. Results and Discussion

[***Project-I***]—*Comparison of electrical performance between traditional LNW and superlattice LNW*

I_{off}

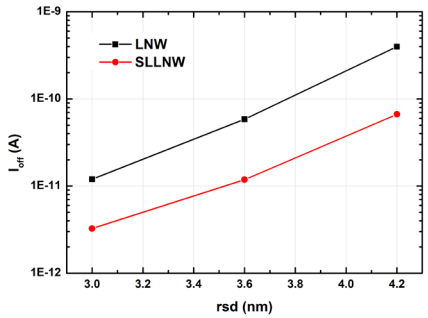

Fig.2. Off-current for different structures

SS

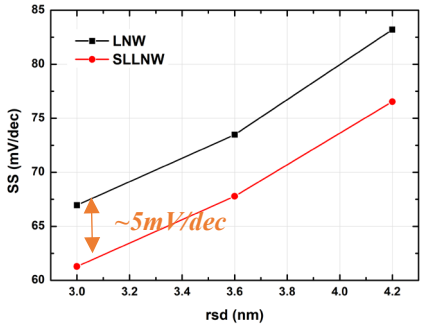

Fig.3. Subthreshold Slope for different structures

DIBL

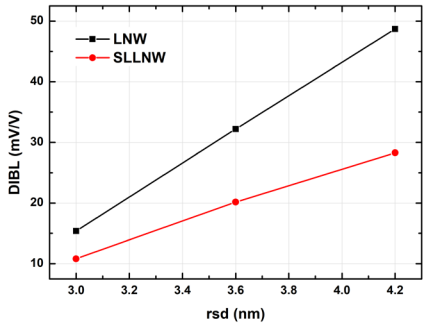

Fig.4. DIBL for different structures

V_{th}

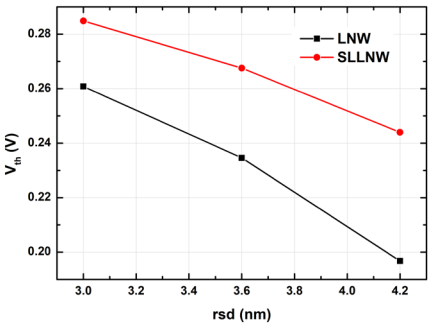

Fig.5. Threshold Voltage for different structures

V_{th} roll-off

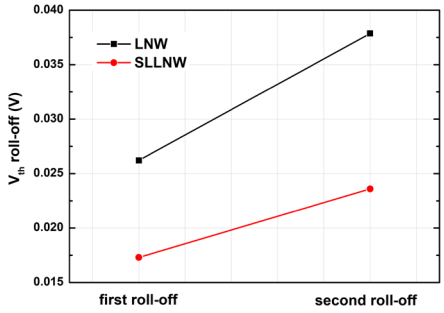

Fig.6. V_{th} roll-off for different structures

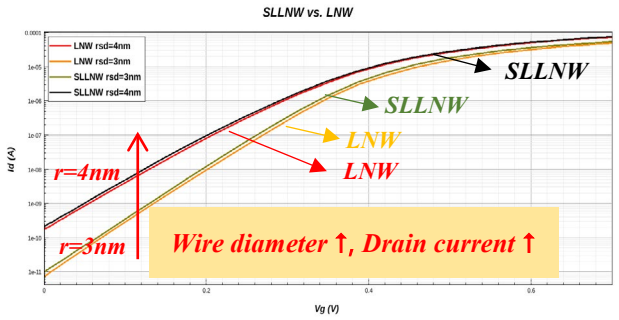

Fig.7. Id-Vg comparison

The first project compares the electrical properties of superlattice LNW (SLLNW) with general LNW (LNW). From the simulation results, the off-current (Fig. 2) and DIBL (Fig. 4) are lower for all wire diameters in the superlattice structure, indicating that the leakage current is better controlled. Additionally, observing the SS curves (Fig. 3), SLLNW also performs better than LNW, with the SLLNW curve being approximately 5mV/dec lower than the LNW curve for every node. This provides evidence that the SLLNW structure has better device switching capability.

Next, for the threshold voltage (Vth, Fig. 5), Vth of SLLNW is higher than that of LNW, which suggests that for the same node diameter, the superlattice structure requires a higher gate voltage to turn on the transistor. Moreover, Vth roll-off is calculated and presented in Fig. 6. Apparently, the roll-off from the first to the second node (first roll-off) and from the second to the third node (second roll-off) are both smaller in SLLNW. This indicates that the short-channel effect (SCE) is suppressed by the strain generated by the Si and SiGe layers in the source and drain areas. Finally, Id-Vg curve is presented in Fig.7. It is obvious that larger wire diameter provides larger current, and for each wire diameter, the current with superlattice structure increases slightly compared to the traditional nanowire structure.

In Project-I, the superlattice nanowire structure has been demonstrated to provide better electrical performance. It shows reduced leakage currents, improved switching capabilities, fewer short-channel effects, and enhanced on-currents compared to traditional nanowire structures. These improvements make the superlattice nanowire structure a promising candidate for future semiconductor applications.

[***Project-II***]—*Simulation of SLLNW with 3nm & 4nm wire radii, varying gate lengths, and channel pitches*

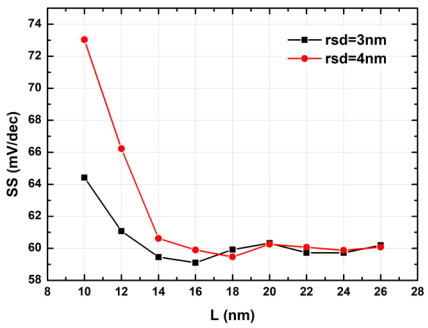

Fig.8. Subthreshold Slope with Variations in Gate Length

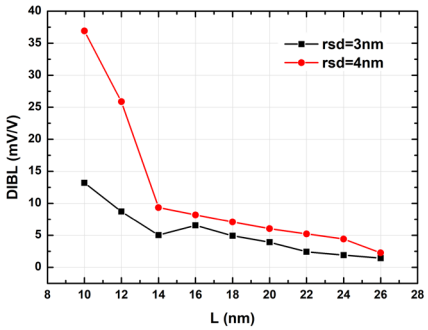

Fig.9. DIBL with Variations in Gate Length

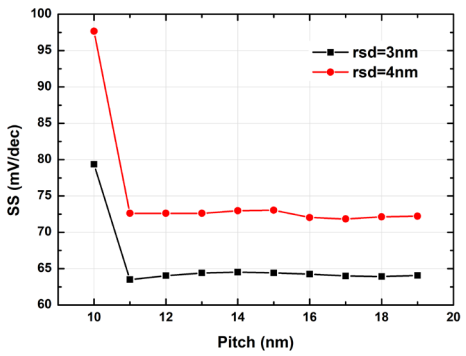

Fig.10. Subthreshold Slope with Variations in Gate Pitch

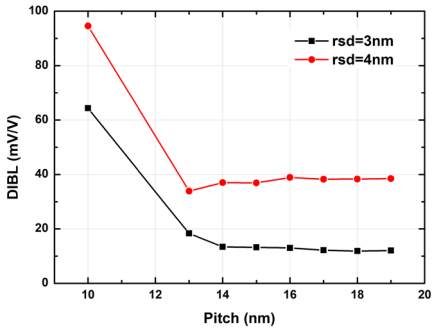

Fig.11. DIBL with Variations in Gate Pitch

In Project-II, superlattice nanowire structures with 3nm and 4nm radii are used to analyze the impact of gate length and channel pitch on electrical performance. Figures 8 and 9 compare the subthreshold slope (SS) and DIBL as functions of gate length. By reducing the gate length from 26nm to 10nm, both SS and DIBL rise significantly when the channel length is under 14nm. Notably, a smaller wire radius notably suppresses the increase in SS and DIBL.

Figures 10 and 11 show simulations of varying gate pitches. In Figure 10, SS remains quite similar when the gate pitch is larger than 11nm, but increases significantly when scaled down below 11nm. In Figure 11, DIBL remains similar when the gate pitch is larger than 13nm, but increases greatly when it is below 13nm.

From the analysis of gate lengths, pitches, and wire radii, we can conclude that while size downscaling is the future trend, channel length reduction is essential. However, to mitigate short-channel effects, smaller wire diameters can be used effectively. Additionally, gate pitches can be scaled down to reduce device size, but it is crucial that the values do not become too small, otherwise, device performance will degrade rapidly.

IV. Conclusion

A superlattice gate-all-around three-nanowire stacked FET structure has been developed and simulated using Sentaurus TCAD. The results show that its electrical performance (Ioff, DIBL, SS, Vth roll-off) surpasses that of traditional nanowire transistors. Additionally, when scaling down a superlattice nanowire transistor, the increased short-channel effects due to shorter gate lengths can be mitigated by reducing the wire diameter. Moreover, gate pitches can be slightly reduced to downsize the transistor without degrading device performance.

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