Macintosh SE Internal Monochrome Video Signal Analysis

1. Introduction

Purpose

This report provides a comprehensive technical analysis of the internal monochrome video signals generated by the Apple Macintosh SE logic board. The objective is to document the precise timing parameters, electrical characteristics, and architectural underpinnings of these signals, sufficient to enable replication or interfacing for hardware development, emulation, or repair purposes.

Scope

The analysis focuses exclusively on the digital video signals present at the J12 connector on the Macintosh SE main logic board. These signals include the Pixel Clock (Dot Clock), Horizontal Synchronization (HSync), Vertical Synchronization (VSync), and the monochrome Video Data signal. These signals are intended as inputs for the internal analog board, which drives the built-in Cathode Ray Tube (CRT) display. This report does not cover the signal processing performed by the analog board, the characteristics of the CRT itself, or the signals produced by external video cards that may have been installed in the SE's Processor Direct Slot (PDS).

It is crucial to distinguish the standard Macintosh SE, the subject of this report, from the later Macintosh SE/30. While sharing a similar form factor, the SE/30 possesses a significantly different architecture based on the Motorola 68030 processor and often utilizes different clock speeds and video memory arrangements.[1] Documentation and schematics for these models are frequently conflated or found together, requiring careful differentiation.[2] This report pertains specifically to the original Macintosh SE based on the Motorola 68000 processor.

Target Audience & Use Case

The intended audience comprises hardware engineers, experienced retrocomputing hobbyists, and technical enthusiasts engaged in projects requiring interaction with the Macintosh SE's native video output. This includes the design of display adapters, FPGA-based system recreations, diagnostic tools, or modifications requiring accurate video signal generation.

Sources

Information presented herein is derived from a combination of sources, including official Apple technical documentation (such as the "Guide to the Macintosh Family

Hardware" [12]), publicly available logic board schematics (both official Apple versions and reverse-engineered sets like those from Bomarc Services [22]), technical analyses published by the vintage computing community, and direct measurements reported in hardware modification projects. Some potentially relevant historical documents, such as specific service manuals, were inaccessible during research.[24] The reliance on reverse-engineered schematics necessitates careful cross-referencing and validation where possible.[20]

2. Video System Architecture

Overview

The Macintosh SE employs an integrated video system architecture characteristic of early compact Macintosh models. Unlike systems with dedicated video memory (VRAM) or separate graphics cards, the SE utilizes a portion of its main system Random Access Memory (RAM) as the video frame buffer.[12] The video generation logic resides primarily on the main logic board, which reads pixel data from this shared RAM buffer and generates the necessary synchronization and data signals. These digital signals are then transmitted via the internal J12 connector to the analog board, which contains the high-voltage circuitry required to drive the monochrome CRT.[12]

This shared memory architecture was a cost-saving measure but introduced contention for RAM access between the central processing unit (CPU) and the video circuitry.[1] Efficiently managing this contention was a key design challenge addressed by the SE's custom logic.

The Role of the BBU (Bob Bailey Unit) ASIC

Identification

Central to the Macintosh SE's logic board design is a custom Application-Specific Integrated Circuit (ASIC) known as the BBU, or Bob Bailey Unit.[12] This large 84-pin Plastic Leaded Chip Carrier (PLCC) component consolidated much of the discrete logic, particularly the Programmable Array Logic (PAL) chips used for timing and memory control in its predecessors like the Macintosh 128K, 512K, and Plus.[28] The BBU represents Apple's successful implementation of a single-chip solution for core logic functions that had been envisioned earlier but initially realized with PALs.[28] The BBU chip, specifically part number 344S0603-B for the SE, was also utilized in the later Macintosh Classic, indicating its production run from approximately 1986 through 1992.[28] Manufacturing was handled initially by VTi (later VLSI Technology) based on their ASIC designs, with IMP and Philips also serving as second sources.[28]

Functionality

The BBU serves as the primary glue logic for the Macintosh SE. Its responsibilities include address decoding for RAM, ROM, and peripherals, generation of various control signals, and, critically for video, managing Direct Memory Access (DMA) operations.[12] The BBU orchestrates the fetching of video data from the main RAM buffer and coordinates the sound data DMA, functions handled by multiple discrete components in earlier Macs.[12]

RAM Access Optimization

A significant advancement embodied by the BBU was its optimized handling of RAM access for video data. In the Macintosh Plus and earlier models, the video circuitry consumed 50% of the available RAM bandwidth during the active portion of each horizontal scan line, leaving the other 50% for the CPU.[28] The BBU improved this dramatically by implementing a more efficient DMA scheme. It fetches video data from RAM in bursts of two words (32 bits) at a time, effectively doubling the data transfer rate per access cycle compared to the older PAL-based system.[12]

This efficiency allows the video system to acquire the necessary pixel data while consuming only 25% of the RAM access time during active display periods.[28] This is achieved through a repeating 8-state memory access cycle: one state (or window) is allocated for video DMA, and the following three states are available for CPU access.[29] During the horizontal and vertical blanking intervals, when the CRT beam is not actively drawing, the BBU yields the video access time entirely to the CPU, further maximizing processor throughput.[28]

Performance Impact

The reduction in RAM contention achieved by the BBU translates directly into improved system performance. With the CPU having access to RAM 75% of the time during active display (compared to 50% on the Plus), the Macintosh SE exhibits a noticeable speed increase. Real-world benchmarks indicate a performance boost of approximately 10 to 20 percent compared to the Macintosh Plus, despite both machines using the same 7.8336 MHz Motorola 68000 CPU.[28]

Connection to Video Signals

The BBU, operating in concert with the main system clock oscillator, is the source of the fundamental timing for the video subsystem. It generates or derives the clock signals (including the pixel clock) and controls the timing logic that produces the HSync and VSync signals.[29] Furthermore, its DMA controller dictates precisely when

pixel data is read from RAM, which is then serialized and output as the VIDEO signal. Schematics, where available [6], would illustrate the BBU's output pins connected to the video generation and timing circuitry feeding the J12 connector.

The BBU's design represents a critical architectural element enabling the SE's balance of cost-effectiveness and performance. By using shared RAM but implementing a highly optimized DMA mechanism within the BBU, Apple mitigated the significant performance penalty typically associated with such architectures in earlier models. The specific 1-video-to-3-CPU access cycle [29] is a hardware-defined timing constraint fundamental to the SE's operation and directly influences the structure of the video signal timing.

3. Video Signal Timing Parameters

The precise timing of the video signals is dictated by the system's master clock and the requirements of displaying a 512x342 pixel image at approximately 60 Hz.

Master Clock Source

The Macintosh SE logic board utilizes a master clock frequency derived from a 15.6672 MHz oscillator.[29] This primary clock signal, often referred to as C16M in schematics, serves as the direct source for the video pixel clock. Derived clocks are generated from this master frequency, including the 7.8336 MHz clock (C8M) for the MC68000 CPU and a 3.9168 MHz clock (C4M), likely used for slower peripherals or timing references.[29] This clocking scheme ensures synchronization between the CPU, RAM access, and video generation.

Pixel Clock (Dot Clock)

- **Frequency:** The rate at which individual pixels are clocked out is precisely **15.6672 MHz**.[3] This frequency is fundamental to all other timing calculations.
- **Period:** The time duration of a single pixel clock cycle is 1 / 15.6672 MHz, which calculates to approximately **63.83 nanoseconds (ns)**.[8]
- **Significance:** This clock dictates the serialization rate of the pixel data onto the VIDEO line. It is exactly twice the CPU clock frequency (7.8336 MHz) [32] and is identical to the pixel clock used in the Macintosh Plus [33], reflecting the shared heritage and core timing constraints.

Horizontal Timing (HSync)

Horizontal timing defines the parameters for scanning a single line of pixels.

- **Frequency (Line Rate):** The rate at which horizontal lines are scanned is **22.25**

kHz.[8] Minor variations (e.g., 22.24 kHz [8]) are sometimes reported, likely due to measurement tolerances, but 22.25 kHz is the most consistently cited value.

- **Period (Total Line Time):** The total time allocated for scanning one line, including blanking, is the reciprocal of the line rate: 1 / 22.25 kHz ≈ **44.94 microseconds (µs)**. Direct measurements often report this as approximately 45 µs.[11]
- **Active Video:** The portion of the line during which pixel data is displayed consists of **512 pixels**.[1] The duration of the active video period is 512 pixels * 63.83 ns/pixel ≈ **32.68 µs**.[11]
- **Horizontal Blanking Interval (Total):** The time during which the electron beam retraces horizontally and is blanked is the total line time minus the active video time: 44.94 µs - 32.68 µs ≈ **12.26 µs**. This closely matches documentation stating the blanking interval corresponds to the time required for 192 pixel clocks (192 * 63.83 ns ≈ 12.25 µs).[8]
- **HSync Pulse Width (Low Period):** The duration for which the HSync signal is held in its active (low) state is consistently measured at **18.4 µs** [11] or **18.45 µs**.[35] This represents approximately 41% of the total line period (18.4 / 45 ≈ 0.409), contrasting with some anecdotal reports of a 50% duty cycle.[37] This pulse width is notably long compared to standards like VGA.[38]
- **Back Porch:** This is the interval between the start of the HSync pulse (falling edge) and the start of active video data. Measurements indicate that video data transmission begins **11.2 µs** after the HSync falling edge.[11]
- **Front Porch:** This is the interval between the end of active video data and the start of the next HSync pulse (falling edge). Based on the total line time (45 µs), HSync falling edge (t=0), video start (t=11.2 µs), and active video duration (32.7 µs), the video ends at t = 11.2 + 32.7 = 43.9 µs. The front porch is therefore 45 µs - 43.9 µs = **1.1 µs**.
- **Timing Overlap:** A critical and non-standard characteristic is the timing relationship between HSync and active video. The HSync pulse goes low at t=0 and stays low until t=18.4 µs. However, active video begins at t=11.2 µs. This means the HSync pulse is still active (low) during the first 7.2 µs (18.4 - 11.2) of the active video period. This overlap, sometimes referred to as a "negative back porch" [11], deviates significantly from typical video timing standards where sync, back porch, active video, and front porch are discrete, sequential intervals.

Vertical Timing (VSync)

Vertical timing defines the parameters for scanning a complete frame (image).

- **Frequency (Frame Rate):** The rate at which full frames are displayed is **60.15 Hz**.[8] This is very close to the common 60 Hz target for CRT displays to minimize

perceived flicker.

- **Period (Total Frame Time):** The total time for one frame is 1 / 60.15 Hz ≈ **16.626 milliseconds (ms)**.[8]
- **Active Video Lines:** The number of lines containing visible pixel data is **342**.[1]
- **Vertical Blanking Interval (Total):** The period during which the electron beam retraces from the bottom right to the top left of the screen. Documentation indicates this involves an additional **28 scan lines**.[8] Therefore, the total number of lines per frame is 342 (active) + 28 (blanking) = **370 lines**. The duration of the vertical blanking interval is 28 lines * 44.94 µs/line ≈ **1.26 ms**. (Checking consistency: Total frame time = 370 lines * 44.94 µs/line ≈ 16.628 ms, matching the calculated frame period).
- **VSync Pulse Width (Low Period):** The duration for which the VSync signal is held active (low) is **180 µs**.[11] This corresponds to the time taken for approximately 4 horizontal lines (180 µs / 45 µs/line ≈ 4 lines), matching calculations derived from some documentation.[8]
- **Back Porch:** The time from the VSync pulse falling edge to the start of the first active video line is measured at **1.26 ms**.[11] This duration (equivalent to 28 lines) encompasses the entire vertical blanking interval, including the VSync pulse itself.
- **Front Porch:** Since the back porch duration equals the total vertical blanking interval, it implies there is effectively **0 lines** of front porch (the time between the end of the last active line and the start of the VSync pulse). The VSync pulse appears to begin immediately following the 342nd active line.
- **Timing relative to HSync:** HSync pulses continue to be generated throughout the vertical blanking interval. The first HSync pulse during VBlank occurs approximately 8 µs after the VSync falling edge.[11]

The specific, non-standard 22.25 kHz HSync frequency of the Macintosh SE is not an arbitrary choice but a direct mathematical consequence of the system's core parameters. Given the fixed 512x342 pixel resolution [1], the target ~60 Hz refresh rate (measured at 60.15 Hz [8]), and the architecturally determined 15.6672 MHz pixel clock [29], the timing must accommodate both the active pixel data and the necessary blanking intervals for CRT retrace. Calculating the total lines required (342 active + 28 blanking = 370 lines [8]) and multiplying by the frame rate (370 lines * 60.15 Hz) yields the necessary horizontal line rate of 22,255 Hz, or 22.25 kHz.[8] All other horizontal timing parameters (period, blanking time) derive from this frequency and the pixel clock.

Furthermore, the horizontal timing details reveal characteristics optimized solely for the SE's internal analog board, rather than adherence to external standards. The

HSync pulse width of ~18.4 µs [11] is exceptionally long compared to VGA standards (e.g., 3.8 µs for 640x480@60Hz [38]). Most significantly, the overlap where the active video period commences *during* the HSync low pulse [11] is highly unconventional. Standard video timings maintain distinct, non-overlapping intervals for sync pulses and active video. This unique timing structure suggests a design tailored specifically to the input requirements of the SE's integrated analog display circuitry, without consideration for external monitor compatibility, which poses challenges for direct interfacing.[37]

Table 1: Macintosh SE Video Timing Summary

Parameter	Value	Unit	Source(s) / Calculation
Pixel Clock			
Frequency	15.6672	MHz	[29]
Period	~63.83	ns	Calculation from Freq. [8]
Horizontal Timing			
Frequency (Line Rate)	22.25	kHz	[8]
Period (Total Line)	~44.94 / ~45	µs	Calculation / [11]
Total Pixels per Line	704	Pixels	44.94 µs / 63.83 ns/pixel (Implied by [8])
Active Video	512	Pixels	[1]
Active Video Time	~32.68	µs	512 pixels * 63.83 ns/pixel
Blanking Interval (Total)	~12.26	µs	44.94 µs - 32.68 µs (Matches 192 pixels [8])

HSync Pulse Width (Low)	~18.4	µs	[11]
Back Porch (HSync Fall -> Video Start)	11.2	µs	[11]
Front Porch (Video End -> HSync Fall)	~1.1	µs	Calculation
Vertical Timing			
Frequency (Frame Rate)	60.15	Hz	[8]
Period (Total Frame)	~16.626	ms	Calculation / [8]
Total Lines per Frame	370	Lines	342 Active + 28 Blanking [8]
Active Video	342	Lines	[1]
Blanking Interval (Total)	28	Lines	[8]
Blanking Interval Time	~1.26	ms	28 lines * 44.94 µs/line
VSync Pulse Width (Low)	180	µs	[11] (Approx. 4 lines [8])
Back Porch (VSync Fall -> Video Start)	~1.26	ms	[11] (Equals Total Blanking Time / 28 Lines)
Front Porch (Video End -> VSync Fall)	0	Lines	Implied by Back Porch = Total Blanking

4. Video Signal Characteristics

Beyond timing, the electrical nature and encoding of the signals are crucial for

interfacing.

Pixel Data

- **Format:** The VIDEO signal (Pin 9 on J12) is a 1-bit digital signal representing monochrome pixel data.[1]
- **Encoding:** The logic level directly encodes the pixel state. Official documentation indicates that a logic '0' represents a white pixel, and a logic '1' represents a black pixel.[12] Therefore, assuming standard positive logic where Low < 0.8V and High > 2.0V, a **Logic Low corresponds to White**, and a **Logic High corresponds to Black**. This is consistent with observations that the signal level is high during blanking periods when no pixels are sent, corresponding to the screen border.[35]
- **Timing:** The data is transmitted serially, one bit per pixel clock cycle (at 15.6672 MHz), during the active horizontal video period.[31] Data transmission begins 11.2 µs after the falling edge of the HSync signal.[11]

Electrical Levels & Impedance

- **Voltage Levels:** The HSync, VSync, and Video Data signals generated by the SE logic board operate at standard 5V Transistor-Transistor Logic (TTL) levels.[40] Based on typical TTL specifications and related documentation for the SE/30 PDS slot [19], a Logic High is generally considered > 2.0V (up to +5V), and a Logic Low is < 0.8V. The circuitry is powered by the +5V DC supply available on the J12 connector.[11]
- **Signal Nature:** It is essential to understand that these signals are raw logic outputs from the BBU or associated buffer chips (potentially 74LS series logic [43]). They are intended to drive the high-impedance inputs of the nearby analog board circuitry. They are *not* standard, impedance-controlled video signals designed for transmission over cables.[36] The output impedance of these signals will be relatively low, characteristic of TTL drivers, not the 75 Ohms expected by standard video equipment.
- **Compatibility & Buffering:** Driving inputs of different logic families directly may cause issues; for instance, 74LS outputs may not reliably drive 74HC inputs due to slightly different voltage thresholds for logic low. 74HCT logic is typically recommended as a compatible replacement or interface buffer.[43] For interfacing with external devices, especially over any significant distance, buffering is highly recommended to provide adequate drive strength and signal integrity. Level shifting is also required to convert the 0/5V TTL swings to the lower analog voltage levels (e.g., 0-0.7V or 0-1V) expected by interfaces like VGA.[40]
- **Impedance:** The output impedance of the logic board signals is not 75 Ohms. Connecting these signals directly to standard 75 Ohm video inputs will result in a

severe impedance mismatch, causing signal reflections and degradation. Proper interfacing requires impedance matching, typically achieved by adding a series resistor at the source (e.g., a 100 Ohm series resistor feeding into three paralleled 75 Ohm RGB inputs results in an effective 25 Ohm load, forming a voltage divider [40]).

Signal Polarity

- **HSync/VSync:** Both synchronization signals are active-low square waves. The falling edge marks the beginning of the synchronization event.[11]
- **Video Data:** As established above, Logic Low represents White, and Logic High represents Black.[12]

J12 Connector Pinout

The J12 connector provides the power and signal interface between the logic board and the analog board.

Table 2: J12 Logic Board Video Connector Pinout

Pin	Signal Name	Description	Source(s)
1	GND	Ground	11
2	GND	Ground	11
3	GND	Ground	11
4	GND	Ground	11
5	GND	Ground	11
6	-5V DC	Negative 5 Volt Power	11
7	-12V DC	Negative 12 Volt Power	11
8	GND	Ground	11
9	VIDEO	Video Data (TTL, 1-bit)	11
10	/HSYNC	Horizontal Sync (TTL, Low)	11
11	/VSYNC	Vertical Sync (TTL, Low)	11
12	+5V DC	Positive 5 Volt Power	11
13	+5V DC	Positive 5 Volt Power	11
14	+12V DC	Positive 12 Volt Power	11

The electrical characteristics highlight that the signals at J12 are essentially raw logic outputs. While they use standard TTL voltage levels, they lack the impedance matching, controlled drive strength, and specific voltage ranges (like 0-0.7V for analog video) required by standard external video interfaces.[36] This is expected, given their purpose was solely to drive the adjacent, tightly coupled analog board. Consequently, direct connection to external monitors or capture devices without appropriate interface circuitry (buffering, level shifting, impedance matching) is

unlikely to function correctly and may even risk damaging components.

5. Implementation Considerations for Signal Generation/Interfacing

Successfully generating or interfacing with the Macintosh SE's video signals requires careful attention to its unique and non-standard characteristics.

Challenges Recap

The primary obstacles for interfacing with modern equipment stem from the SE's deviation from common video standards:

1. **Non-Standard HSync Frequency:** The 22.25 kHz line rate is incompatible with standard VGA monitors, which typically require 31.5 kHz or higher.[36] Composite video standards (NTSC/PAL) also use different frequencies.
2. **Non-Standard HSync Timing:** The exceptionally long HSync pulse width (~18.4 µs) and the overlap between the HSync pulse and the start of active video data are problematic for standard sync processing logic.[11]
3. **Raw TTL Logic Levels:** The 0V/5V TTL signals require conversion to the analog levels (e.g., 0-0.7V) and impedance matching (typically 75 Ohms) expected by most analog video inputs.[40]

Sync Signal Adaptation

When generating signals *to* mimic the SE, strict adherence to the timings in Table 1 is paramount. When adapting the SE's *output* for other displays:

- **Frequency Adaptation:** Bridging the 22.25 kHz HSync frequency gap to VGA's 31.5 kHz+ typically requires scan conversion hardware, which is beyond simple signal adaptation. Some multisync monitors *might* tolerate the lower frequency, but it's not guaranteed.[39]
- **Pulse Width / Overlap Correction:** The long HSync pulse often needs shortening for compatibility with external monitors. This can be achieved using monostable multivibrator ICs ("one-shots") triggered by the HSync falling edge to generate a shorter pulse [37], or by using a simple RC high-pass filter to differentiate the falling edge and create a narrower pulse.[39] Addressing the overlap might require more complex logic to delay the video data relative to a corrected HSync pulse.
- **Sync Combining/Separation:** If targeting a composite video input, the separate TTL HSync and VSync signals must be combined into a single composite sync signal with appropriate voltage levels and timing relationships.[37] Conversely, if

adapting a signal *with* composite sync (less relevant here, but common in other retro contexts) for a VGA monitor requiring separate H/V sync, a sync separator IC like the LM1881 can be used.[46]

Level Shifting and Buffering

Converting the SE's 5V TTL signals is necessary for most analog inputs:

- **Voltage Conversion:** Simple resistive voltage dividers can scale the 0/5V signal down to the 0-0.7V or 0-1V range suitable for VGA inputs.[40] Care must be taken to account for the input impedance of the target device (typically 75 Ohms).
- **Impedance Matching:** A series resistor between the TTL output (or buffer output) and the video input is needed to approximate the required source impedance and prevent reflections.[40]
- **Buffering:** Using buffer ICs (e.g., 74HCT series) is recommended to isolate the original SE logic, provide stronger signal drive, and ensure clean signal edges, especially if driving cables or multiple inputs.[43]

Modern Implementation Approaches

Modern programmable logic offers powerful and flexible solutions for both generating and adapting these signals:

- **FPGAs (Field-Programmable Gate Arrays):** FPGAs excel at precise timing generation and can easily replicate the 15.6672 MHz pixel clock and derived sync timings. They can also incorporate logic for sync pulse correction, level shifting (with appropriate external circuitry), and even scan conversion within a single device.[10]
- **Microcontrollers (MCUs):** Fast MCUs with flexible peripheral interfaces (like the Raspberry Pi Pico's PIO or the Parallax Propeller) can also be programmed to generate the required video timings through careful cycle counting or dedicated state machines ("bit banging").[11] Projects like the one documented at trmm.net demonstrate using a BeagleBone's Programmable Realtime Unit (PRU) for this purpose.[11] Attempts have also been made using devices like the GBS-Control scaler board, highlighting the community interest in adapting these signals.[34] Adaptation projects for similar Mac models (like the Plus) using platforms like RGB2HDMI further illustrate this approach.[33]

Ultimately, generating a video signal fully compatible with the Macintosh SE's internal expectations requires meticulous replication of the specific, non-standard timing parameters detailed in this report – particularly the 15.6672 MHz pixel clock driving a 512x342 display area within a 370-line frame refreshed at 60.15 Hz, resulting in the

22.25 kHz line rate and its associated unique horizontal timings. Interfacing the SE's native output with standard display equipment is equally challenging, demanding careful signal conditioning to address the HSync frequency disparity, the unusual HSync pulse characteristics, and the conversion from raw TTL logic levels to impedance-matched analog video signals.

6. Conclusion

Summary of Findings

The Macintosh SE's internal monochrome video system is characterized by its reliance on a shared main memory buffer managed by the custom BBU ASIC. This architecture, while cost-effective, imposes specific timing constraints. The key video signal specifications generated at the J12 logic board connector are:

- **Pixel Clock:** 15.6672 MHz
- **Resolution (Active):** 512 pixels x 342 lines
- **Horizontal Sync (HSync):** 22.25 kHz frequency, ~45 µs period, ~18.4 µs active-low pulse width. Active video starts 11.2 µs after HSync falling edge, overlapping the HSync pulse.
- **Vertical Sync (VSync):** 60.15 Hz frequency, ~16.63 ms period, 180 µs active-low pulse width. Total frame is 370 lines (including 28 blanking lines).
- **Signal Type:** Raw 5V TTL logic levels (HSync, VSync, Video Data), active-low sync, Video Low=White / High=Black.

Relevance to User Goal

The detailed timing parameters summarized in Table 1, the electrical characteristics, and the J12 connector pinout (Table 2) provide the essential technical data required to accurately generate compatible Macintosh SE video signals. This information serves as a foundational reference for hardware developers aiming to emulate the SE's display output, create custom display adapters, or interface with the logic board for diagnostic or modification purposes.

Final Caution

Users seeking to interface the SE's native video output with standard monitors or video equipment must be aware of its non-standard nature. The 22.25 kHz HSync frequency, the unusually long and overlapping HSync pulse, and the raw TTL signal levels necessitate appropriate signal conditioning circuitry (including buffering, level shifting, impedance matching, and potentially sync timing correction) for successful and reliable operation. Direct connection without such interfacing is highly likely to

fail.

7. References

- [24] ccadams.org/se/MacSEservice.pdf (Inaccessible)
- [12] Guide to the Macintosh Family Hardware, 2nd Edition (1990). VintageApple.org. URL: https://vintageapple.org/inside_o/pdf/Guide_to_Macintosh_Family_Hardware_2nd_Edition_1990.pdf
- [28] "Everything you wanted to know about the BBU but were afraid to ask". Tinkerdifferent Forum Thread. URL: https://tinkerdifferent.com/threads/everything-you-wanted-to-know-about-the-bbu-but-were-afraid-to-ask.880/
- [8] "Compact Mac Video Timings Needed for SuperVideo Input Parameters". 68kmla Forum Thread. URL: https://68kmla.org/bb/index.php?threads/compact-mac-video-timings-needed-for-supervideo-input-parameters.33342/
- [36] "Mac Plus external video mod TTL to VGA". 68kmla Forum Thread. URL: https://68kmla.org/bb/index.php?threads/mac-plus-external-video-mod-ttl-to-vga.7023/
- [11] "Macintosh SE Video interface". Trammell Hudson Blog Post. URL: https://trmm.net/Mac-SE_video/
- [22] "Bomarc Services reverse engineered 68K Macintosh Schematics...". Macintosh Repository. URL: https://www.macintoshrepository.org/25838-bomarc-services-reverse-engineered-68k-macintosh-schematics-m0001-plus-se-classic-ii-color-ii-iici-iicx-iifx-iisi-lc-ii-iii-quadra-840av-
- [25] Macintosh SE Schematics & Repair. Macintosh Garden. (Inaccessible)
- [30] "Mac SE Schematics". Macintosh Repository. URL: https://www.macintoshrepository.org/28274-mac-se-schematics
- [15] "Macintosh SE/30 Schematics and Repair". Macintosh Repository. URL: https://www.macintoshrepository.org/875-macintosh-se-30-schematics-and-repair
- [4] Apple Manual: Macintosh SE/30. Internet Archive. URL: https://archive.org/details/macse30
- [5] Macintosh SE/30 Original Schematic (Apple). MacDat.net. URL: https://www.macdat.net/files/pdf/apple/schematics/apple/se30_original.pdf
- [6] Bomarc SE/30 Schematics. Absurd Engineering. URL: http://absurdengineering.org/library/MASTER%20Schematics/Schematics%20-%2

0BOMARC/Macintosh%20SE30%20Schematic%20(BOMARC)/BOMARC%20SE30%20Schematics.pdf

- [7] Macintosh SE/30 Schematic (Apple). MacDat.net. URL: https://www.macdat.net/files/pdf/apple/schematics/apple/se30.pdf
- [1] "Compact Macintosh framebuffer/video out design". 68kmla Forum Thread. URL: https://68kmla.org/bb/index.php?threads/compact-macintosh-framebuffer-video-out-design.4449/
- [8] "Compact Mac Video Timings Needed for SuperVideo Input Parameters". 68kmla Forum Thread. URL: https://68kmla.org/bb/index.php?threads/compact-mac-video-timings-needed-for-supervideo-input-parameters.33342/
- [2] "Mac SE/30 processor question". 68kmla Forum Thread. URL: https://68kmla.org/bb/index.php?threads/mac-se-30-processor-question.5602/
- [36] "Mac Plus external video mod TTL to VGA". 68kmla Forum Thread. URL: https://68kmla.org/bb/index.php?threads/mac-plus-external-video-mod-ttl-to-vga.7023/
- [9] "Apple "mistake? video 512 x 342 vs. 512 x 384". 68kmla Forum Thread. URL: https://68kmla.org/bb/index.php?threads/apple-mistake-video-512-x-342-vs-512-x-384.36841/
- [27] "MacSE-RAM, a crazy Mac SE PDS RAM concept!". 68kmla Forum Thread. URL: https://68kmla.org/bb/index.php?threads/macse-ram-a-crazy-mac-se-pds-ram-concept.46129/
- [10] "se/30 and/or other classic Mac video output direct conversion". 68kmla Forum Thread. URL: https://68kmla.org/bb/index.php?threads/se-30-and-or-other-classic-mac-video-output-direct-conversion.37379/
- [11] "Macintosh SE Video interface". Trammell Hudson Blog Post. URL: https://trmm.net/Mac-SE_video/
- [37] "Macintosh SE Composite Video Signal". All About Circuits Forum Thread. URL: https://forum.allaboutcircuits.com/threads/macintosh-se-composite-video-signal.165550/
- [28] "Everything you wanted to know about the BBU but were afraid to ask". Tinkerdifferent Forum Thread. URL: https://tinkerdifferent.com/threads/everything-you-wanted-to-know-about-the-bbu-but-were-afraid-to-ask.880/
- [12] Guide to the Macintosh Family Hardware, 2nd Edition (1990). VintageApple.org. URL: https://vintageapple.org/inside_o/pdf/Guide_to_Macintosh_Family_Hardware_2nd_Edition_1990.pdf

- [13] "I get knocked down, but I get up again: The Sisyphean Macintosh SE/30 struggles". Vladovince Blog Post. URL: https://blog.vladovince.com/i-get-knocked-down-but-i-get-up-again-the-sisyphean-macintosh-se-30-struggles/
- [14] "Mac SE/30 Repair Log". 68kmla Forum Thread. URL: https://68kmla.org/bb/index.php?threads/mac-se-30-repair-log.45345/
- [15] "Macintosh SE/30 Schematics and Repair". Macintosh Repository. URL: https://www.macintoshrepository.org/875-macintosh-se-30-schematics-and-repair
- [16] macse30mlb GitHub Repository. URL: https://github.com/mishimasensei/macse30mlb
- [17] "SE/30 and Macintosh Portable Schematics". 68kmla Forum Thread. URL: https://68kmla.org/bb/index.php?threads/se-30-and-macintosh-portable-schematics.45418/
- [26] "Macintosh SE schematics". Applefritter Forum Thread. URL: https://www.applefritter.com/content/macintosh-se-schematics
- [5] Macintosh SE/30 Original Schematic (Apple). MacDat.net. URL: https://www.macdat.net/files/pdf/apple/schematics/apple/se30_original.pdf
- [7] Macintosh SE/30 Schematic (Apple). MacDat.net. URL: https://www.macdat.net/files/pdf/apple/schematics/apple/se30.pdf
- [6] Bomarc SE/30 Schematics. Absurd Engineering. URL: http://absurdengineering.org/library/MASTER%20Schematics/Schematics%20-%20BOMARC/Macintosh%20SE30%20Schematic%20(BOMARC)/BOMARC%20SE30%20Schematics.pdf
- [31] Macintosh Hardware: Video. mac.linux-m68k.org. URL: http://www.mac.linux-m68k.org/devel/plushw.php
- [32] "Why the unusual frequency?". 68kmla Forum Thread. URL: https://68kmla.org/bb/index.php?threads/why-the-unusual-frequency.18919/
- [29] "Reimplementing the Mac SE's BBU". Tinkerdifferent Forum Thread. URL: https://tinkerdifferent.com/threads/reimplementing-the-mac-ses-bbu.1139/
- [33] "RGB2HDMI brought to a Mac Plus". Tinkerdifferent Forum Thread. URL: https://tinkerdifferent.com/threads/rgb2hdmi-brought-to-a-mac-plus.868/
- [34] "Macintosh Classic / SE / Plus / 512k / 128k timings". GBS-Control GitHub Issue. URL: https://github.com/ramapcsx2/gbs-control/issues/238
- [2] "Mac SE/30 processor question". 68kmla Forum Thread. URL: https://68kmla.org/bb/index.php?threads/mac-se-30-processor-question.5602/
- [3] Macintosh SE/30 Developer Note (HW14). Apple Developer (Archived). URL: https://leopard-adc.pepas.com/technotes/hw/hw_14.html
- [11] "Macintosh SE Video interface". Trammell Hudson Blog Post. URL:

https://trmm.net/Mac-SE_video/

- [35] "Hacking the Macintosh Classic CRT Part 1". Nerdhut Blog Post. URL: https://nerdhut.de/2016/06/26/macintosh-classic-crt-1/
- [39] "WarpSE: 25 MHz 68HC000 based Accelerator for Mac SE". Tinkerdifferent Forum Thread. URL: https://tinkerdifferent.com/threads/warpse-25-mhz-68hc000-based-accelerator-for-mac-se.253/page-11
- [46] "Classic Macintosh Video Signals Demystified, Designing a Mac-to-VGA Adapter with LM1881". Big Mess o' Wires Blog Post. URL: https://www.bigmessowires.com/2023/10/04/classic-macintosh-video-signals-demystified-designing-a-mac-to-vga-adapter-with-lm1881/
- [38] VGA Timings. Martin Hinner Info Page. URL: http://martin.hinner.info/vga/timing.html
- [37] "Macintosh SE Composite Video Signal". All About Circuits Forum Thread. URL: https://forum.allaboutcircuits.com/threads/macintosh-se-composite-video-signal.165550/
- [47] "Mac-to-VGA Sync Splitter Prototype". Big Mess o' Wires Blog Post. URL: https://www.bigmessowires.com/2023/10/11/mac-to-vga-sync-splitter-prototype/
- [18] SE/30 Direct Slot. Applefritter PDF. URL: https://www.applefritter.com/files/221706.PDF
- [44] "TTL to Composite Video Interface". Abzman2k Blog Post. URL: https://abzman2k.wordpress.com/2024/02/17/ttl-to-composite-video-interface/
- [40] Compact Mac Video Adapter. Waveguide.se Article. URL: https://www.waveguide.se/?article=compact-mac-video-adapter
- [43] "Macintosh SE Video Issue". 68kmla Forum Thread. URL: https://68kmla.org/bb/index.php?threads/macintosh-se-video-issue.45429/
- [45] Understanding and Interpreting Standard-Logic Data Sheets. Texas Instruments Application Report (SCEA030). URL: https://www.ti.com/lit/SCEA030
- [41] "Can I rewire a compact Macintosh SE or other compact Mac to play RCA video?". Retrocomputing Stack Exchange Question. URL: https://retrocomputing.stackexchange.com/questions/15447/can-i-rewire-a-compact-macintosh-se-or-other-compact-mac-to-play-rca-video
- [42] "Information about a Radius FPD SE/30 Video Card". 68kmla Forum Thread. URL: https://68kmla.org/bb/index.php?threads/information-about-a-radius-fpd-se-30-video-card.38923/
- [19] Micron Technology Xceed SE/306-48 Manual (1989). VintageApple.org. URL: https://vintageapple.org/macbooks/pdf/Micron_Technology_Xceed_SE-306-48_1989.pdf

- [23] Apple Schematic Archive. MacDat.net. URL: https://www.macdat.net/repair/apple_schematics.html
- [22] "Bomarc Services reverse engineered 68K Macintosh Schematics...". Macintosh Repository. URL: https://www.macintoshrepository.org/25838-bomarc-services-reverse-engineered-68k-macintosh-schematics-m0001-plus-se-classic-ii-color-ii-iici-iicx-iifx-iisi-lc-ii-iii-quadra-840av-
- [4] Apple Manual: Macintosh SE/30. Internet Archive. URL: https://archive.org/details/macse30
- [20] "Macintosh SE/30 Schematics (modernization effort)". 68kmla Forum Thread. URL: https://68kmla.org/bb/index.php?threads/macintosh-se-30-schematics-modernization-effort.7235/page-2
- [6] Bomarc SE/30 Schematics. Absurd Engineering. URL: http://absurdengineering.org/library/MASTER%20Schematics/Schematics%20-%20BOMARC/Macintosh%20SE30%20Schematic%20(BOMARC)/BOMARC%20SE30%20Schematics.pdf
- [15] "Macintosh SE/30 Schematics and Repair". Macintosh Repository. URL: https://www.macintoshrepository.org/875-macintosh-se-30-schematics-and-repair
- [16] macse30mlb GitHub Repository. URL: https://github.com/mishimasensei/macse30mlb
- [30] "Mac SE Schematics". Macintosh Repository. URL: https://www.macintoshrepository.org/28274-mac-se-schematics
- [21] Macintosh SE/30 Recap Guide. Recap-a-Mac. URL: https://recapamac.com.au/macintosh-se-30/
- [7] Macintosh SE/30 Schematic (Apple). MacDat.net. URL: https://www.macdat.net/files/pdf/apple/schematics/apple/se30.pdf

Works cited

1. Compact Macintosh framebuffer/video out design? - 68kMLA, accessed April 13, 2025, https://68kmla.org/bb/index.php?threads/compact-macintosh-framebuffer-video-out-design.4449/
2. Mac SE/30 processor question. - 68kMLA, accessed April 13, 2025, https://68kmla.org/bb/index.php?threads/mac-se-30-processor-question.5602/
3. Technical Note HW14: Macintosh SE/30 Info, accessed April 13, 2025, https://leopard-adc.pepas.com/technotes/hw/hw_14.html
4. Macintosh SE/30 : Apple : Free Download, Borrow, and Streaming - Internet Archive, accessed April 13, 2025, https://archive.org/details/macse30

5. Logic Board (Apple, Original) - MacDat, accessed April 13, 2025, https://www.macdat.net/files/pdf/apple/schematics/apple/se30_original.pdf
6. BOMARC SE30 Schematics, accessed April 13, 2025, http://absurdengineering.org/library/MASTER%20Schematics/Schematics%20-%20BOMARC/Macintosh%20SE30%20Schematic%20(BOMARC)/BOMARC%20SE30%20Schematics.pdf
7. Macintosh SE/30 Schematic 01 of 09 CPU FPU - MacDat, accessed April 13, 2025, https://www.macdat.net/files/pdf/apple/schematics/apple/se30.pdf
8. Compact Mac Video Timings Needed for SuperVideo Input ..., accessed April 13, 2025, https://68kmla.org/bb/index.php?threads/compact-mac-video-timings-needed-for-supervideo-input-parameters.33342/
9. Apple "mistake? video 512 x 342 vs. 512 x 384 - 68kMLA, accessed April 13, 2025, https://68kmla.org/bb/index.php?threads/apple-mistake-video-512-x-342-vs-512-x-384.36841/
10. se/30 and/or other classic Mac video output direct conversion - 68kMLA, accessed April 13, 2025, https://68kmla.org/bb/index.php?threads/se-30-and-or-other-classic-mac-video-output-direct-conversion.37379/
11. Mac-SE/30 video interface - Trammell Hudson, accessed April 13, 2025, https://trmm.net/Mac-SE_video/
12. Guide to the Macintosh® Family Hardware Second ... - Vintage Apple, accessed April 13, 2025, https://vintageapple.org/inside_o/pdf/Guide_to_Macintosh_Family_Hardware_2nd_Edition_1990.pdf
13. I get knocked down, but I get up again: my Sisyphean Macintosh SE/30 struggles - Vlado Vince, accessed April 13, 2025, https://blog.vladovince.com/i-get-knocked-down-but-i-get-up-again-the-sisyphean-macintosh-se-30-struggles/
14. Mac SE/30 Repair Log - 68kMLA, accessed April 13, 2025, https://68kmla.org/bb/index.php?threads/mac-se-30-repair-log.45345/
15. Macintosh SE/30 Schematics and Repair - Macintosh Repository, accessed April 13, 2025, https://www.macintoshrepository.org/875-macintosh-se-30-schematics-and-repair
16. mishimasensei/macse30mlb: Macintosh SE/30 Main Logic Board Schematic Drawings - GitHub, accessed April 13, 2025, https://github.com/mishimasensei/macse30mlb
17. SE/30 and Macintosh Portable Schematics - 68kMLA, accessed April 13, 2025, https://68kmla.org/bb/index.php?threads/se-30-and-macintosh-portable-schematics.45418/
18. ICKY is a multiple resolution video card for the Macintosh II PDS computers. - Applefritter, accessed April 13, 2025, https://www.applefritter.com/files/221706.PDF
19. Micron Technology Memory Applications Group - Vintage Apple, accessed April

13, 2025, https://vintageapple.org/macbooks/pdf/Micron_Technology_Xceed_SE-306-48_1989.pdf
20. Macintosh SE/30 Schematics (modernization effort) | Page 2 - 68kMLA, accessed April 13, 2025, https://68kmla.org/bb/index.php?threads/macintosh-se-30-schematics-modernization-effort.7235/page-2
21. Macintosh SE/30 - Recap-a-Mac, accessed April 13, 2025, https://recapamac.com.au/macintosh-se-30/
22. Bomarc Services reverse engineered 68K Macintosh Schematics (M0001, Plus, SE, Classic/II/Color, II/IIci/IIcx/IIfx/IIsi, LC II/III, Quadra 840av), accessed April 13, 2025, https://www.macintoshrepository.org/25838-bomarc-services-reverse-engineered-68k-macintosh-schematics-m0001-plus-se-classic-ii-color-ii-iici-iicx-iifx-iisi-lc-ii-iii-quadra-840av-
23. Apple Schematic Archive - MacDat, accessed April 13, 2025, https://www.macdat.net/repair/apple_schematics.html
24. accessed December 31, 1969, http://www.ccadams.org/se/MacSEservice.pdf
25. accessed December 31, 1969, https://macintoshgarden.org/apps/macintosh-se-schematics-repair
26. Macintosh SE schematics | Applefritter, accessed April 13, 2025, https://www.applefritter.com/content/macintosh-se-schematics
27. MacSE-RAM, a crazy Mac SE PDS RAM concept! - 68kMLA, accessed April 13, 2025, https://68kmla.org/bb/index.php?threads/macse-ram-a-crazy-mac-se-pds-ram-concept.46129/
28. Everything you wanted to know about the BBU, but were afraid to ..., accessed April 13, 2025, https://tinkerdifferent.com/threads/everything-you-wanted-to-know-about-the-bbu-but-were-afraid-to-ask.880/
29. Reimplementing the Mac SE's BBU | TinkerDifferent, accessed April 13, 2025, https://tinkerdifferent.com/threads/reimplementing-the-mac-ses-bbu.1139/
30. Mac SE Schematics - Macintosh Repository, accessed April 13, 2025, https://www.macintoshrepository.org/28274-mac-se-schematics
31. Mac Plus hardware - Linux/m68k for Macintosh, accessed April 13, 2025, http://www.mac.linux-m68k.org/devel/plushw.php
32. Why the unusual frequency? - 68kMLA, accessed April 13, 2025, https://68kmla.org/bb/index.php?threads/why-the-unusual-frequency.18919/
33. RGB2HDMI brought to a Mac Plus | TinkerDifferent, accessed April 13, 2025, https://tinkerdifferent.com/threads/rgb2hdmi-brought-to-a-mac-plus.868/
34. Compact Macintosh video · Issue #238 · ramapcsx2/gbs-control - GitHub, accessed April 13, 2025, https://github.com/ramapcsx2/gbs-control/issues/238
35. Control a Macintosh Classic CRT with a BeagleBone Black – Part 1 - nerdhut, accessed April 13, 2025, https://nerdhut.de/2016/06/26/macintosh-classic-crt-1/
36. Mac Plus external Video Mod: TTL to VGA? | 68kMLA, accessed April 13, 2025,

https://68kmla.org/bb/index.php?threads/mac-plus-external-video-mod-ttl-to-vga.7023/
37. Macintosh SE Composite Video Signal | All About Circuits, accessed April 13, 2025, https://forum.allaboutcircuits.com/threads/macintosh-se-composite-video-signal.165550/
38. VGA Timings, accessed April 13, 2025, http://martin.hinner.info/vga/timing.html
39. WarpSE: 25 MHz 68HC000-based accelerator for Mac SE | Page 11 | TinkerDifferent, accessed April 13, 2025, https://tinkerdifferent.com/threads/warpse-25-mhz-68hc000-based-accelerator-for-mac-se.253/page-11
40. Compact Mac video adapter - waveguide.se, accessed April 13, 2025, https://www.waveguide.se/?article=compact-mac-video-adapter
41. Can I rewire a compact Macintosh SE or other compact Mac to play RCA Video?, accessed April 13, 2025, https://retrocomputing.stackexchange.com/questions/15447/can-i-rewire-a-compact-macintosh-se-or-other-compact-mac-to-play-rca-video
42. Information about a Radius FPD SE/30 video card - 68kMLA, accessed April 13, 2025, https://68kmla.org/bb/index.php?threads/information-about-a-radius-fpd-se-30-video-card.38923/
43. Macintosh se video issue - 68kMLA, accessed April 13, 2025, https://68kmla.org/bb/index.php?threads/macintosh-se-video-issue.45429/
44. TTL to composite video interface - Evan's Techie-Blog, accessed April 13, 2025, https://abzman2k.wordpress.com/2024/02/17/ttl-to-composite-video-interface/
45. Voltage Translation Between 3.3-V, 2.5-V, 1.8-V, and 1.5-V Logic Standards - Texas Instruments, accessed April 13, 2025, https://www.ti.com/lit/SCEA030
46. Classic Macintosh Video Signals Demystified, Designing a Mac-to-VGA Adapter with LM1881 | Big Mess o' Wires, accessed April 13, 2025, https://www.bigmessowires.com/2023/10/04/classic-macintosh-video-signals-demystified-designing-a-mac-to-vga-adapter-with-lm1881/
47. Mac-to-VGA Sync-Splitter Prototype | Big Mess o' Wires, accessed April 13, 2025, https://www.bigmessowires.com/2023/10/11/mac-to-vga-sync-splitter-prototype/