Lab 4: Shift Registers

Objective

- ✓ Review sequential circuits.
- ✓ Review shift registers.

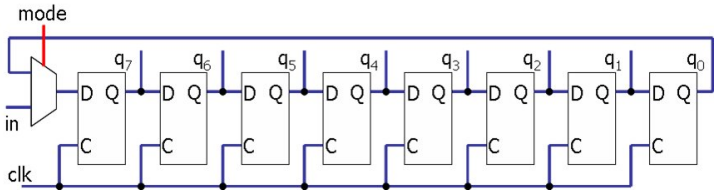
Prerequisite

- ✓ Fundamentals of logic gates.
- ✓ Clocking concepts
- ✓ Logic modeling in Verilog HDL.

Pre-labs

1 Cascade eight DFFs together as the figure shown below with the input bits D=(d), output Q=($q_7q_6q_5q_4q_3q_2q_1q_0$), and tie all their Cs together as clk (the divided clock). This is a serial shift register circuit. By adding a multiplexer before the first DFF, we can choose the input from outside or from q_0. As the clk changes 0,1,0,1,…, let the output of LEDs be (01010101), (10101010), (01010101), (10101010), ….

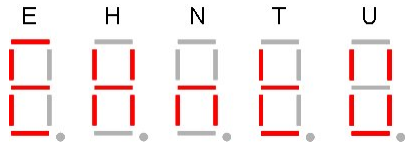
1.1 Construct the Verilog RTL representation for the logics with verification



Experiments

1 Implement pre-lab1 with the following pin assignments.

2 Use the idea from pre-lab1. We can do something on the seven-segment display. Assume we have the pattern of E, H, N, T, U for seven-segment display as shown below. Try to implement the scrolling pre-stored pattern NTHUEE with the four seven-segment displays.



3 (Bonus) Display 1010 in the seven-segment display. Use the DIP switch (one bit to indicate left/right shift, three bits with one hot to display the kind of shift operation) as the control input to implement the functional/arithmetic/barrel shifter. Use one push button to control the display of the number before/after the shift operation.

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