Lab 8: Electronic Clock II (Multi-functions)

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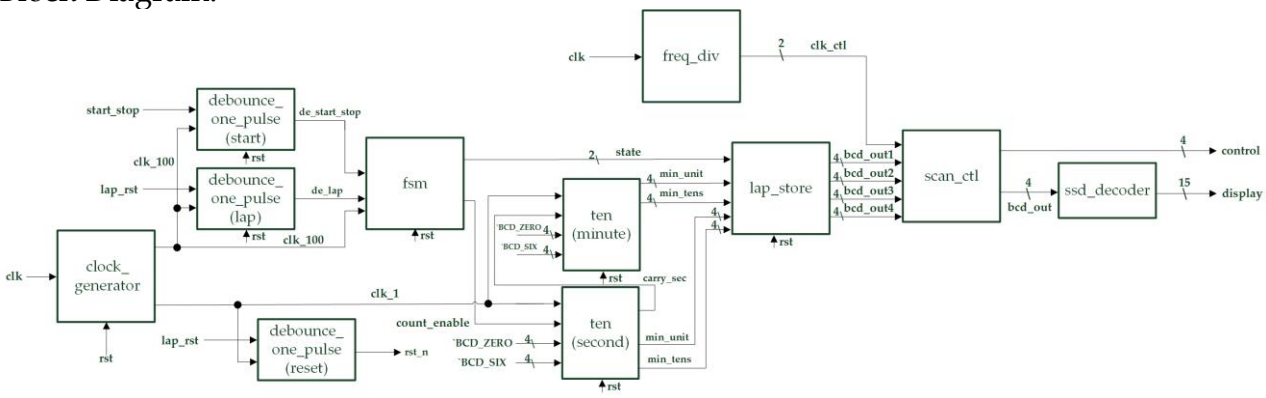
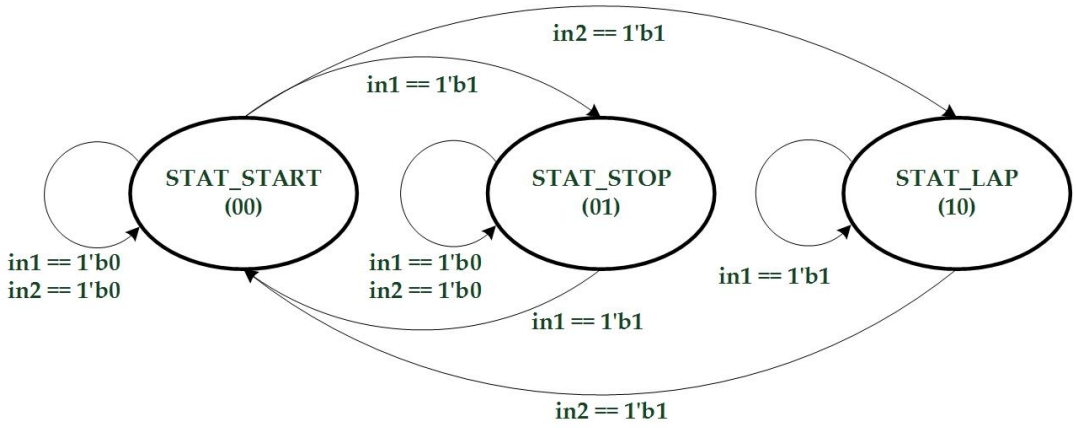
Design Specification

1. Stop Watch

- ✓ Experiment Goal:
  Construct an stop watch which can support lap(the display is frozen but the watch is still counting in the background) and start/stop function.
- ✓ Block Diagram:



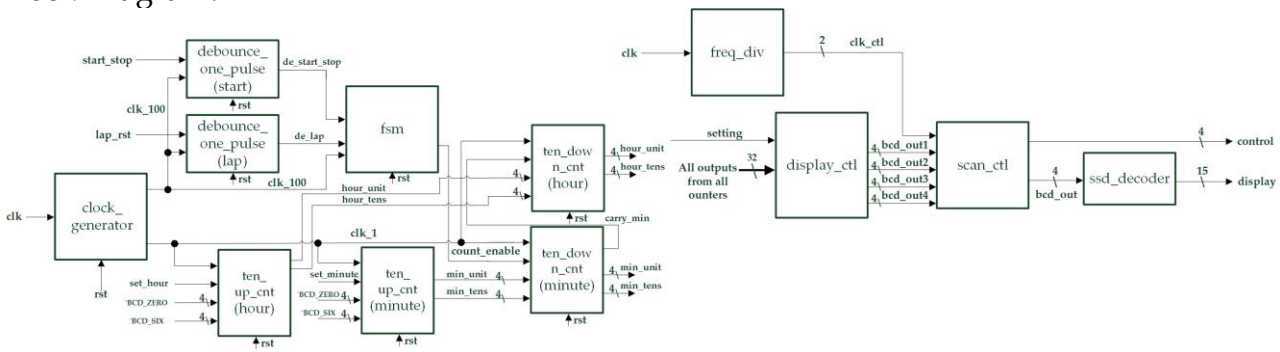
- ✓ State Diagram:



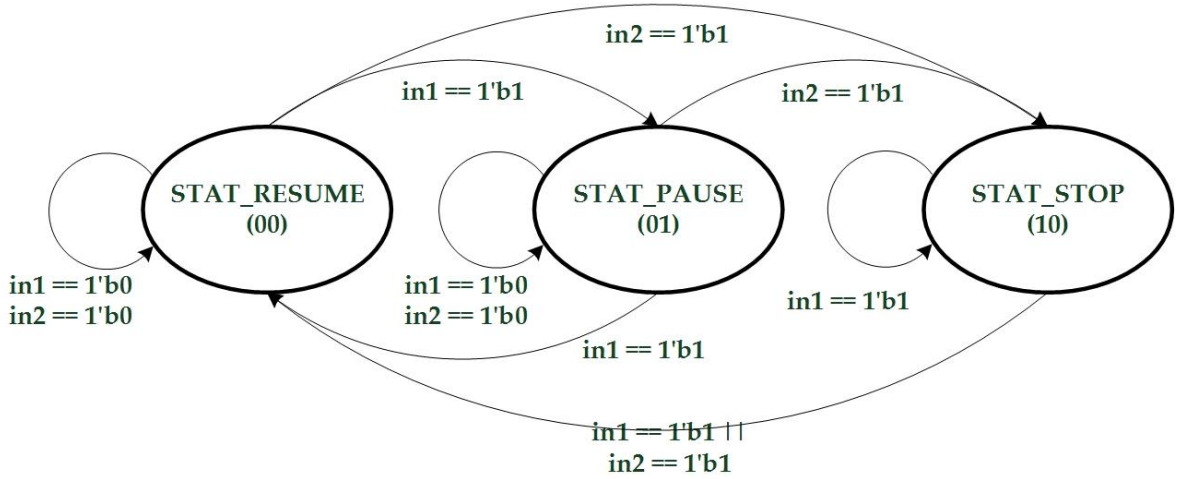
- ✓ I/Os:
  Inputs: clk, start_stop, lap_rst.
  Outputs: [3:0] control, [14:0] display.
- ✓ Details about some module:
  - ■ lap_store: Build with four flip-flops which will store the value from seconds and minutes. When in the start mode the flip-flops will refresh the value at every clock positive edge. When in the lap mode it will keep the value until back to start mode.

2. Timer

- ✓ Experiment Goal:
  Build a timer which we can set the initial start down counting value.
- ✓ Block Diagram:



- ✓ State Diagram:



- ✓ I/Os:
  Inputs: clk, setting, set_minute, set_hour, start_stop, pause_resume.
  Outputs: [3:0] control, [14:0] display, [15:0] led.
- ✓ Details about some module:
  - display_ctl: Determines what is going to show on the 14-degment display according from the 1-bit DIP input.

Design Implementation

1. Stop Watch

- ✓ First, use the up counter module in the previous lab to build second and minute counter. Second, the finite state machine has two button inputs which determine the next state, and the outputs will control whether counters should count or not. Third, a four-flip-flop module will store the value from counters to decide keep update the display or go to lap mode.

- ✓ I/O Pins Assignment:

Port Name	Assignment	Function
clk	R10	FPGA board oscillator input
start_stop	P4	Start & stop button
lap_rst	N3	Lap & reset button
control[0]~control[3]	V8, U8, V6, T6	14-SD control signal
display[0]~display[14]	U5, T7, R7, V7, V4, T4, T3, R5, N5, R3, U7, T5, V5, N4, P6	14-SD light control signal

2. Timer

- ✓ First, construct two up counter which represent minute and hour separately, and their increase enable input are from button "set_minute" & "set_hour" individually. Second, adjust the up counter into down counter which is the main timer module, and their initial value may input from the up counters. Third, the finite state machine has two button inputs which determine the next state, and the outputs will control whether down counters should count or not. Fourth, pass all the outputs from the counters to display controller which it will determine what is going to show on the 14-degment display.
- ✓ I/O Pins Assignment:

Port Name	Assignment	Function
clk	R10	FPGA board oscillator input
set_minute	N3	Set minute button
set_hour	P4	Set hour button
start_stop	L6	Start & stop button
pause_resume	P3	Lap & reset button
control[0]~control[3]	V8, U8, V6, T6	14-SD control signal
display[0]~display[14]	U5, T7, R7, V7, V4, T4, T3, R5, N5, R3, U7, T5, V5, N4, P6	14-SD light control signal
led[0]~led[15]	K4, K3, L5, K5, H4, H3, L7, K6, G3, G1, J7, J6, F2, F1, H6, H5	Led lights output

Discussion

- ✓ I did not encounter any big errors which are hard to debug. But I spent most of the thinking and designing the two experiment's framework. I think maybe I should do more code practicing to improve my coding skills and decrease the coding times

Conclusion

- ✓ Many electronic devices has little buttons, such as iPhone with only one home button, but it can done many kinds of things. So, this lab's main goal is to train us building many kinds of functions in limited buttons. Turning out to be more user friendly to control the board.

References

- ✓ Previous codes in Lab5 and Lab 7.