LCD Display (2)

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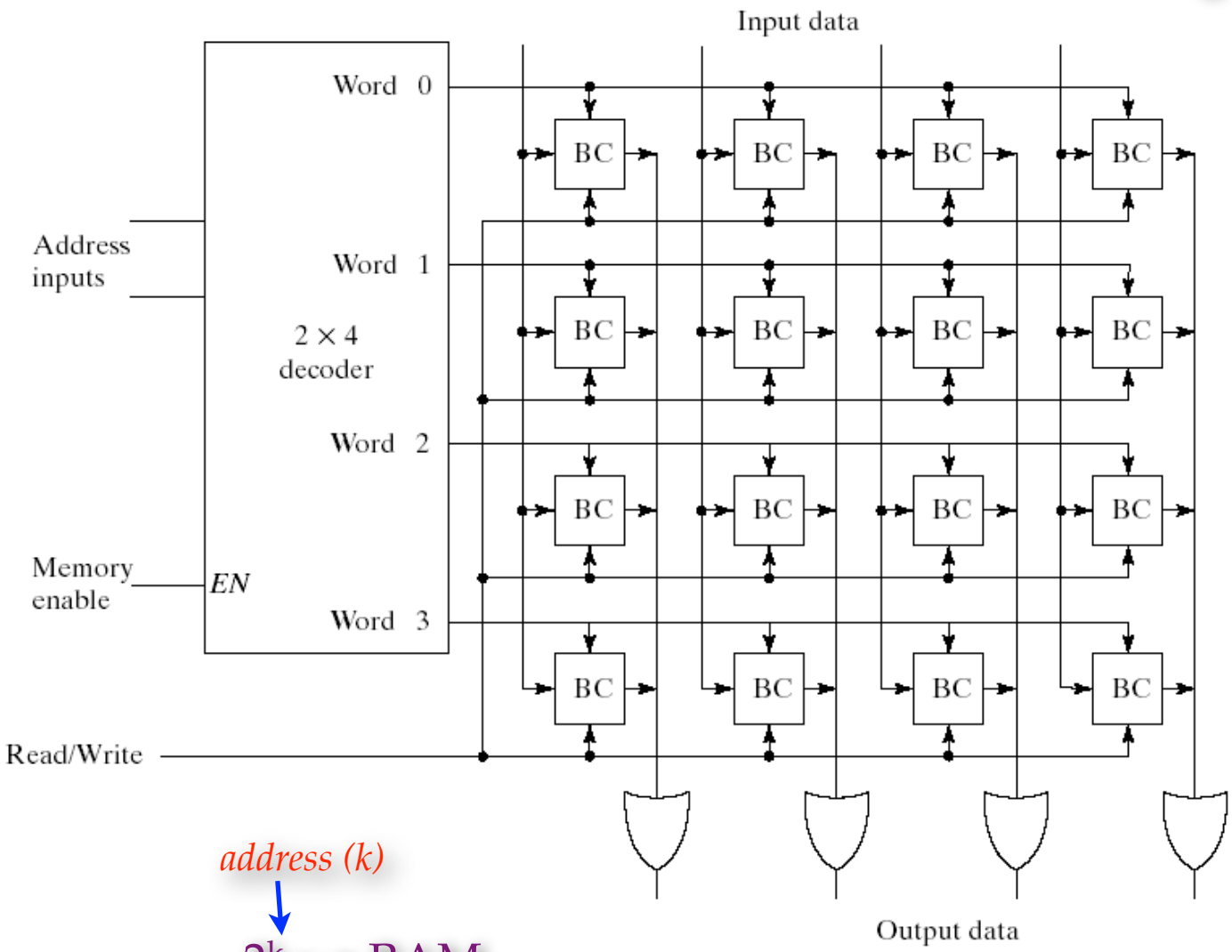
RAM Revisit

2^2 x 4 RAM



address (k)

2^k x n RAM

# of output bits (n)

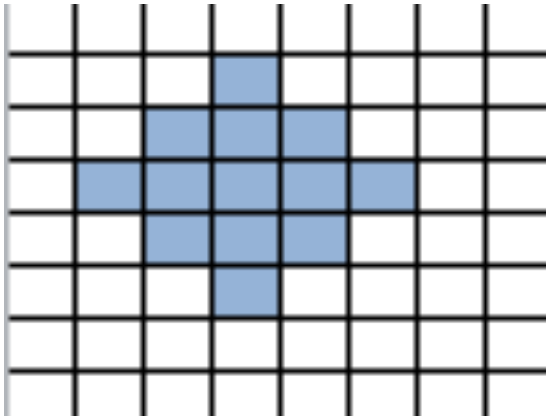
COE Format

- COE: memory coefficient file
- Two parameter:
  - **memory_initialization_radix**
    - Radix of the values in the *memory_initialization_vector*
    - Ex: 2, 10, or 16
  - **memory_initialization_vector:**
    - Memory content
    - Memory words are separated by whitespace
    - You can use comma (,) to help identify the boundary
    - Vector (entire memory) ended by semicolon

COE Example

```
; 8-bitwide by 8-deep RAM
memory_initialization_radix=2;
memory_initialization_vector=
00000000 ,
00010000 ,
00111000 ,
01111100 ,
00111000 ,
00010000 ,
00000000 ,
00000000 ;
```

whitespace



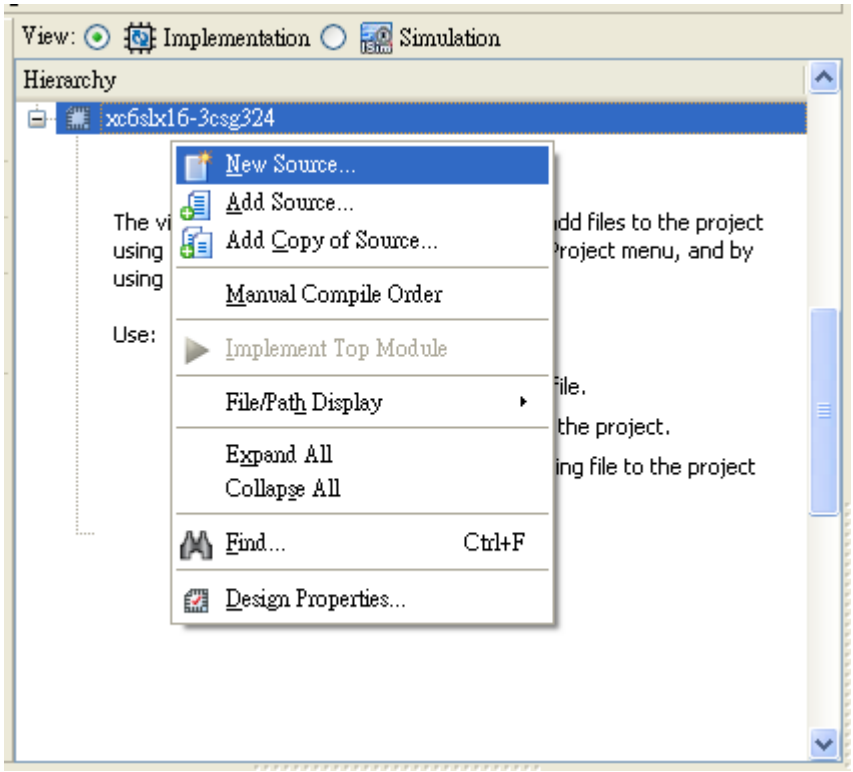
You can use ASCII art generator to generate the pictures or use drawing tool to export the figures for you.

Use RAM

- You can use RAM for changeable LCD display of your project
- Similar as ROM
  - The same in IP generator, except choose 'Single Port RAM'
  - Now have write
- Timing
  - Write control, address, data should be at the same clock cycle
  - Data read out from RAM is one clock cycle late than the address control

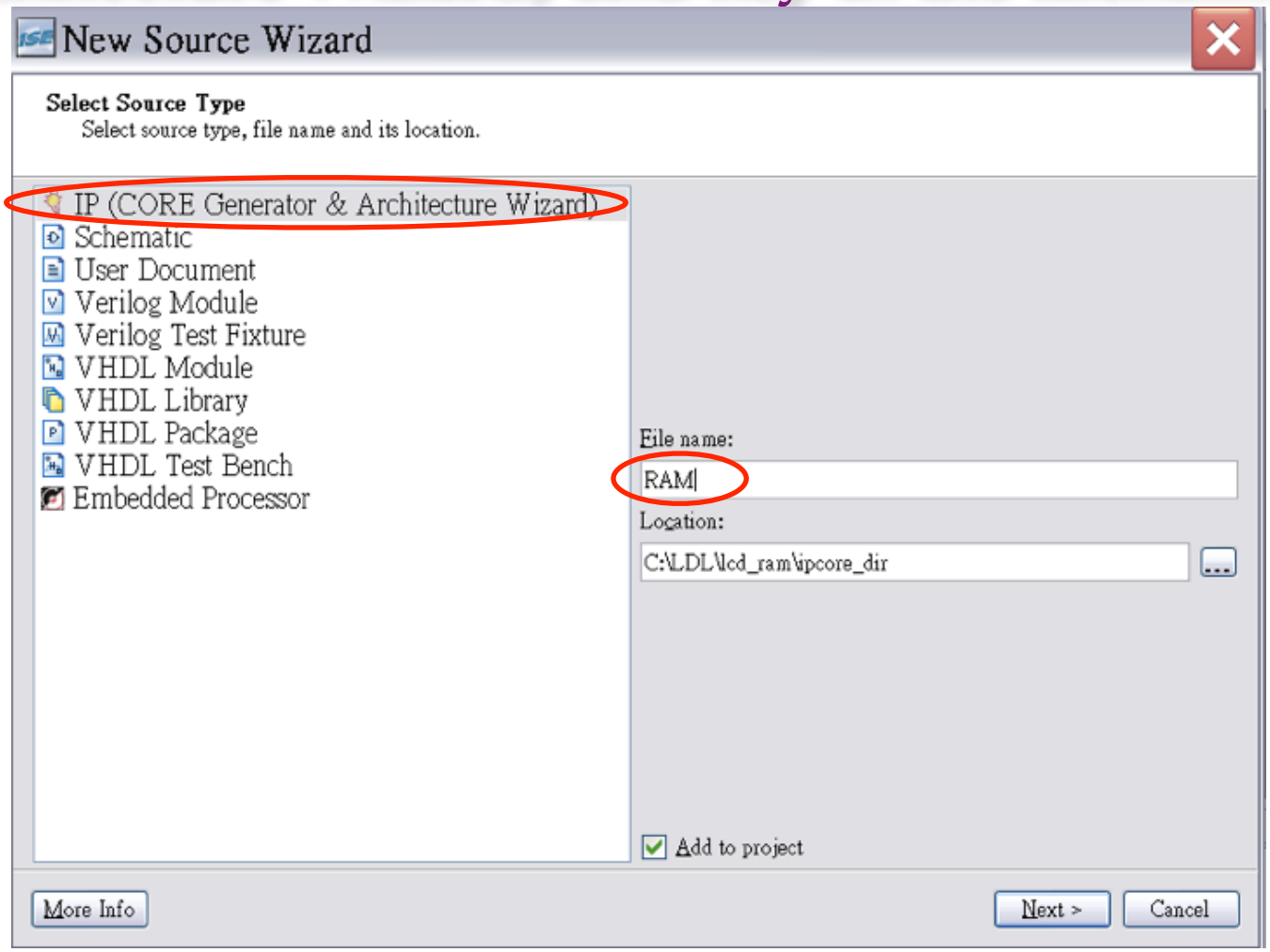
Generate RAM (1/6)

- New Source



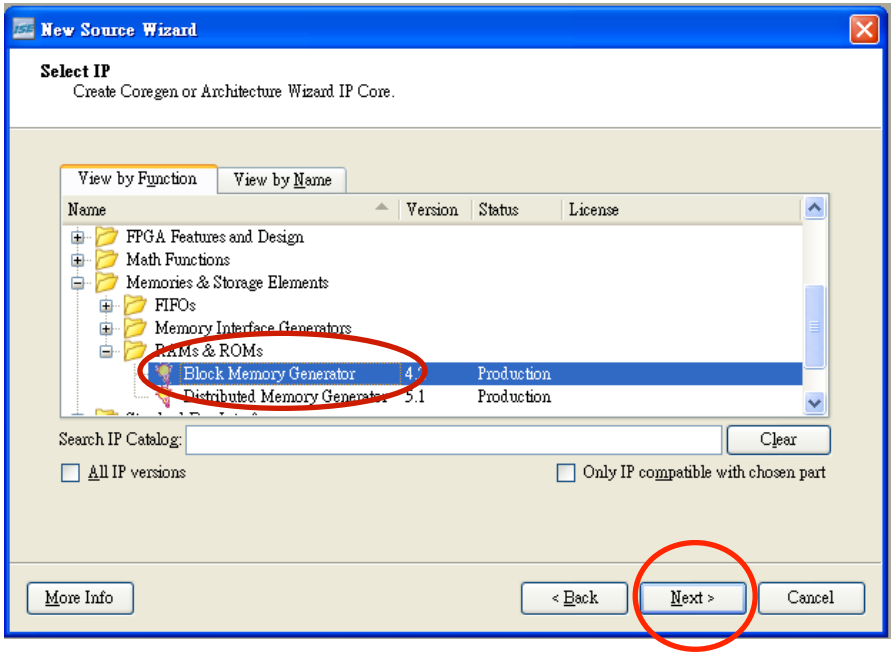
Generate RAM (2/6)

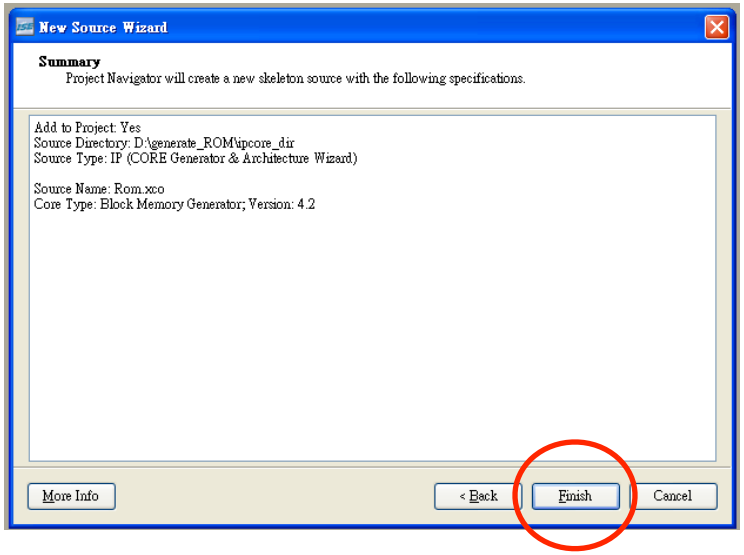
- Choose the source type: IP (CORE Generator & Architecture Wizard) and key in the filename



Generate RAM (3/6)

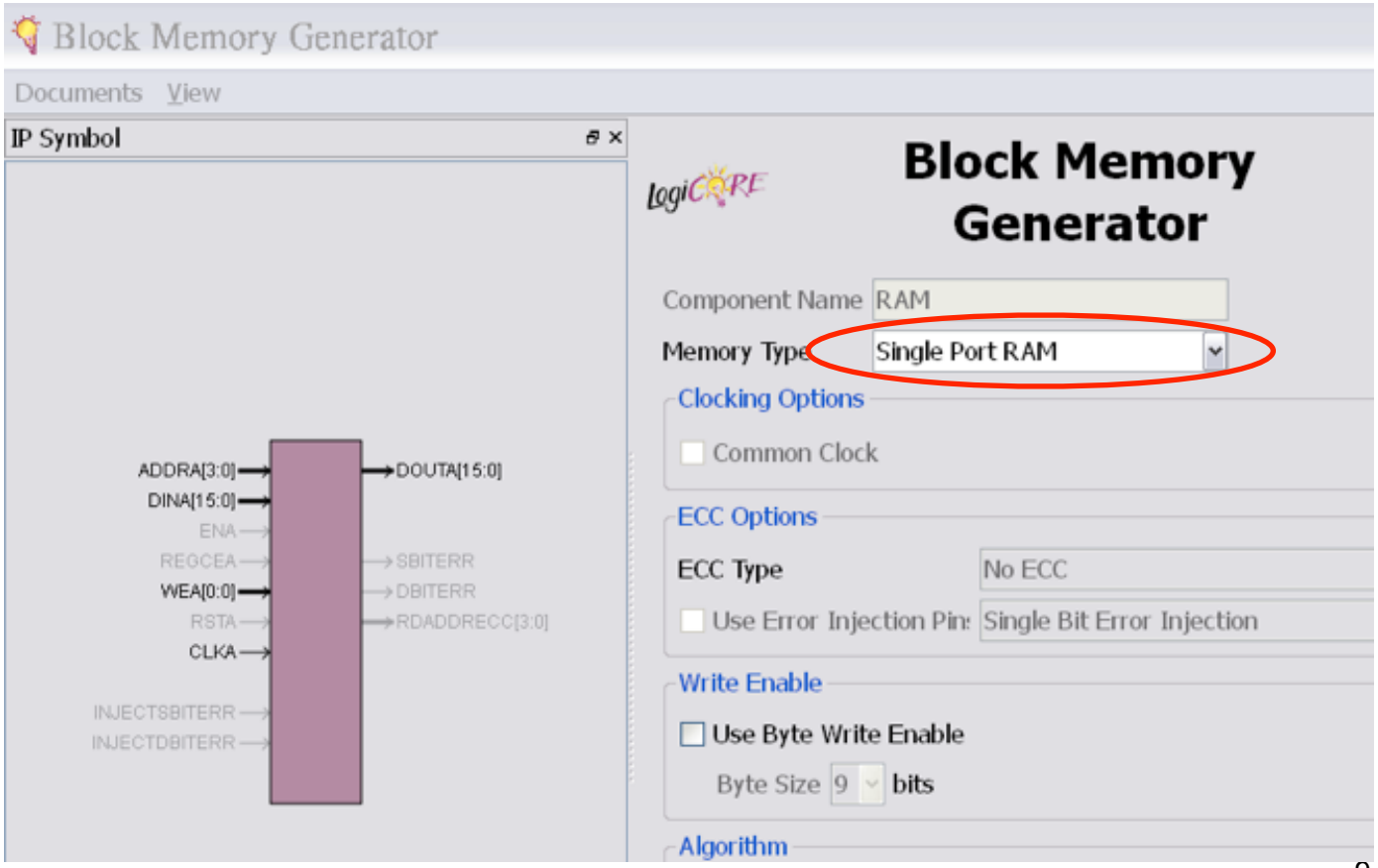
- Select:
  - Memories & Storage Elements -> RAMs/ROMs -> Block Memory Generator





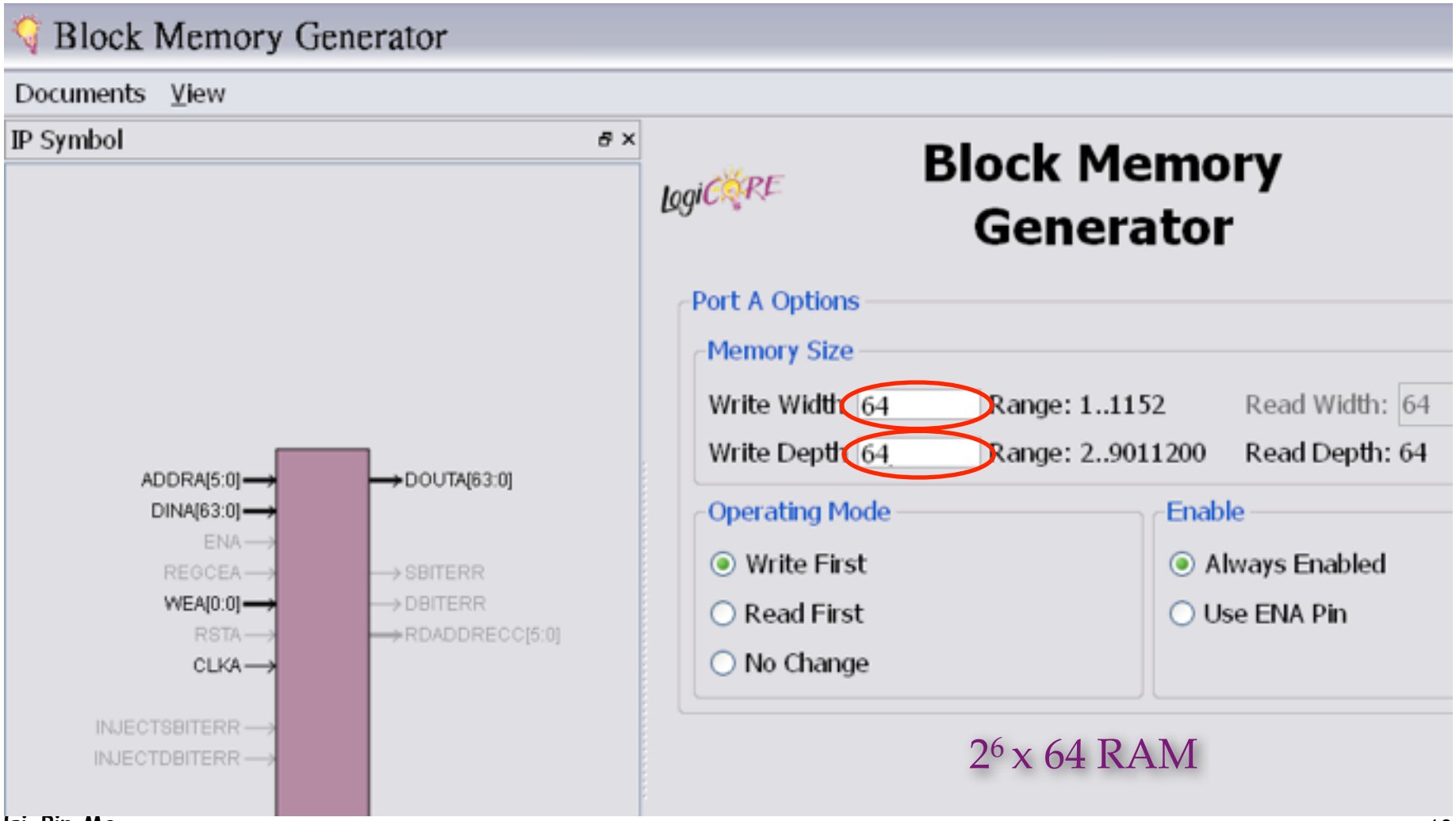
Generate RAM (4/6)

- Wait for a while
- Select Memory Type: Single Port RAM



Generate RAM (5/6)

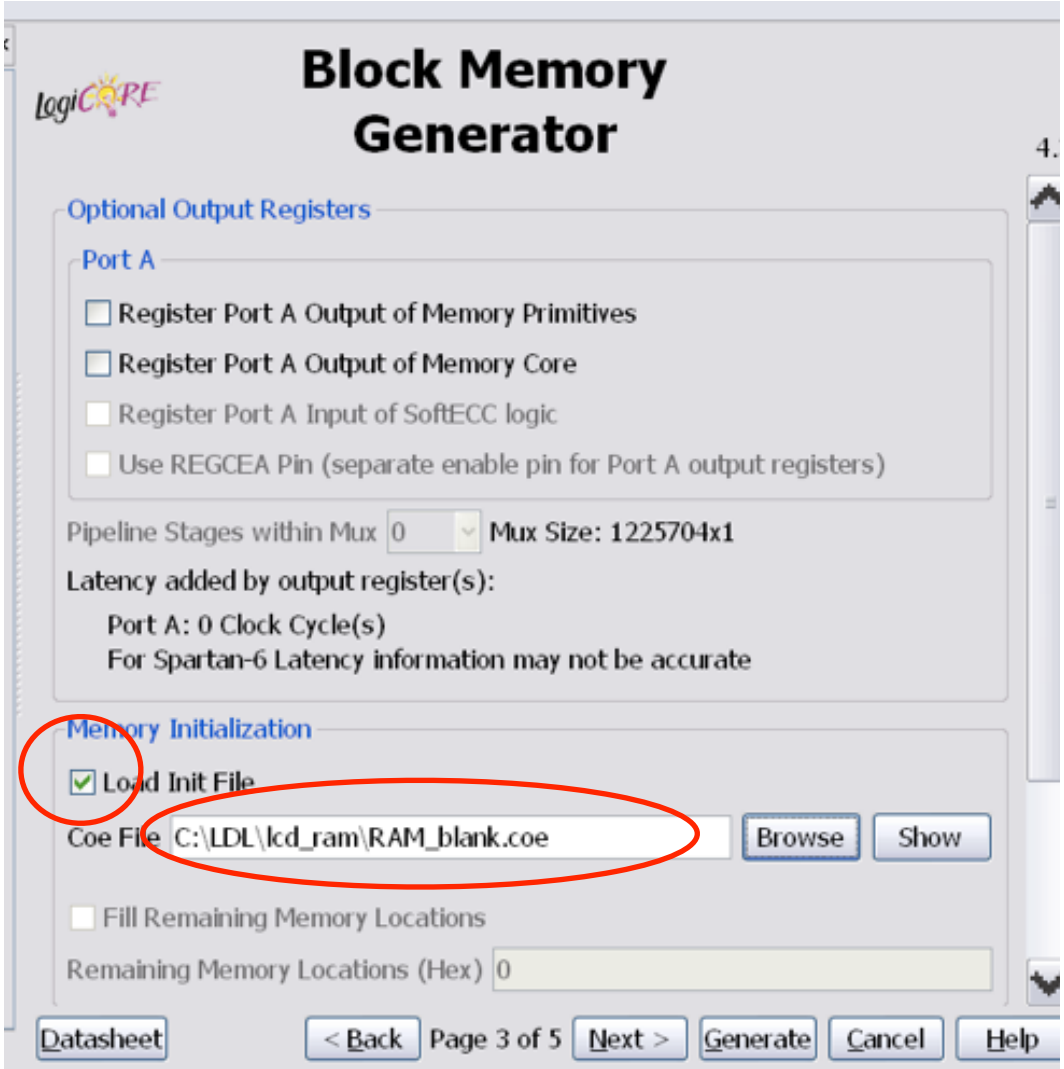
- Data width: 64 bits, address depth: 64 (1 frame)



2^6 x 64 RAM

Generate RAM (6/6)

- Check "Load Init File"
- Select "Browse" and load your COE file



How to Use RAM Module

- You can find the port names through the functional model

ISE Project Navigator (M.81d) - C:\LDL\lcd_ram\lcd_ram.xise - [RAM.veo]

File Edit View Project Source Process Tools Window Layout Help

Design

View: Implementation Simulation

Hierarchy

- lcd_ram
- xc6slx16-3csg324
  - RAM (RAM.xco)
  - lcd_display (lcd_display.v)
    - U_LCDctrl - lcd_ctrl (lcd_ctrl.v)
    - U_romctrl - rom_ctrl (rom_ctrl.v)
      - R1 - ROM ()

No Processes Running

Processes: RAM

- CORE Generator
  - Manage Cores
  - Regenerate Core
  - View HDL Functional Model
  - View HDL Instantiation Template

Start Design Files Libraries

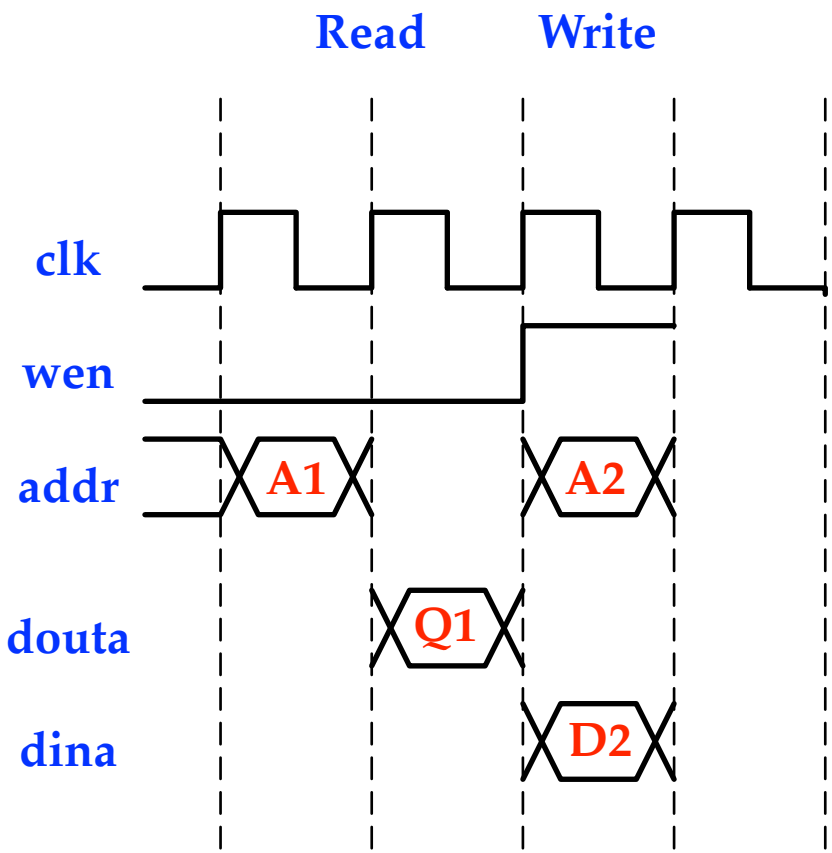
```
49  // core to be instantiated. Change the
50  // (in parentheses) to your own signal
51
52  //----------- Begin Cut here for INSTAN
53  RAM YourInstanceName (
54      .clka(clka),
55      .wea(wea), // Bus [0 : 0]
56      .addra(addra), // Bus [5 : 0]
57      .dina(dina), // Bus [63 : 0]
58      .douta(douta)); // Bus [63 : 0]
59
60  // INST_TAG_END ------ End INSTANTIATIO
61
62  // You must compile the wrapper file RA
63  // the core, RAM. When compiling the wr
64  // reference the XilinxCoreLib Verilog
65  // instructions, please refer to the "C
66
67
```

Design Summary rom_ctrl.v

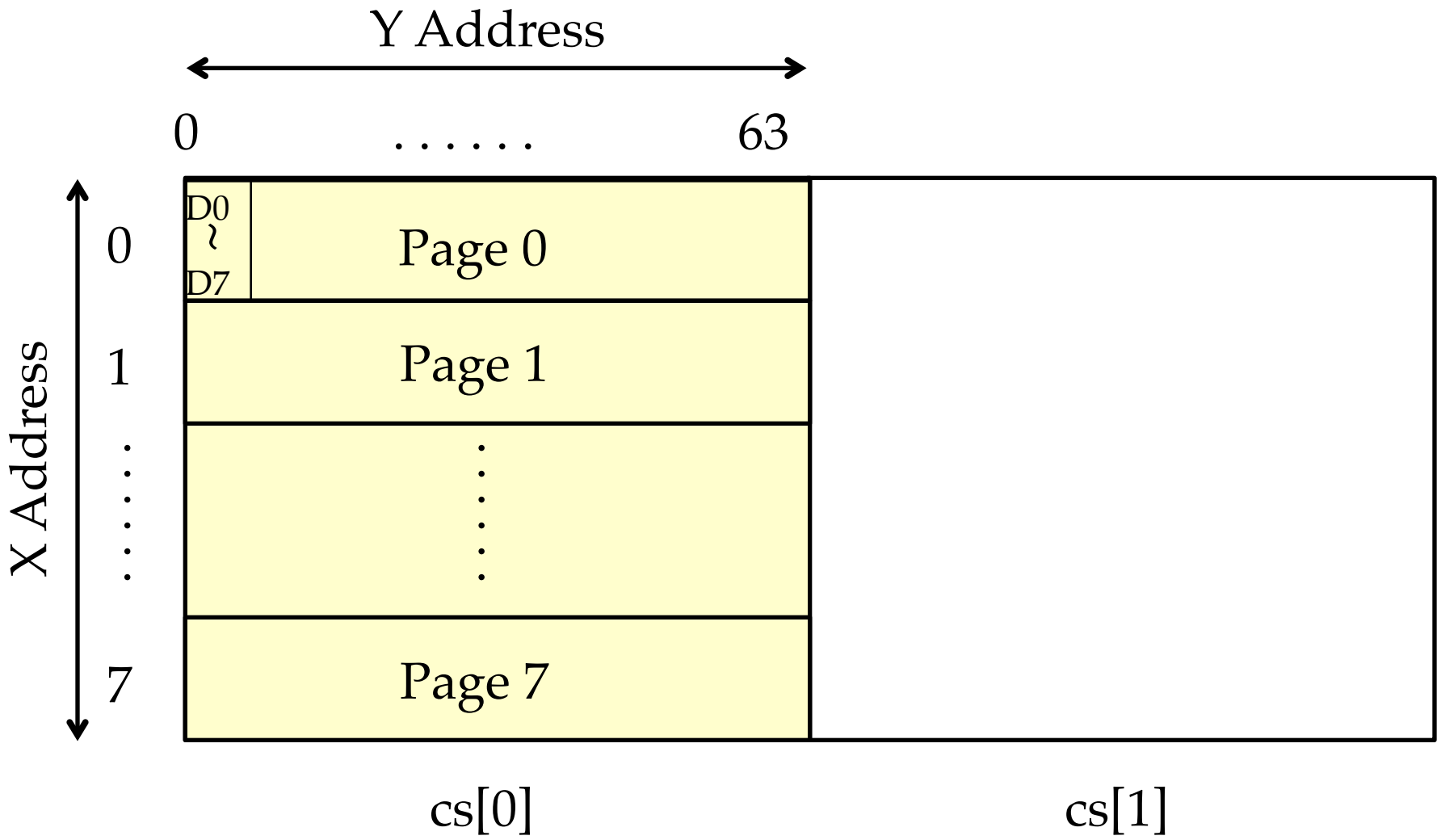
How to Use RAM Module

```
wire clk;
wire wen;
wire [63:0] data_in;
wire [63:0] out_64;
wire [5:0] addr;

RAM R1(
  .clka(clk),
  .wea(wen),
  .addra(addr),
  .dina(data_in),
  .douta(out_64)
);
```

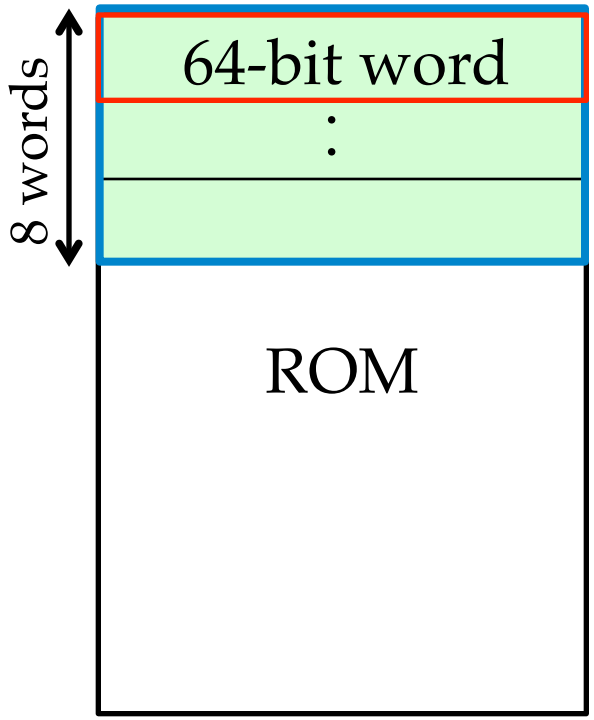


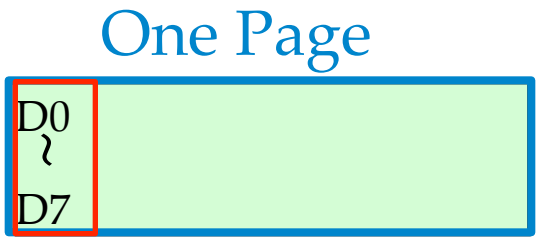
LCD Display (128x64)

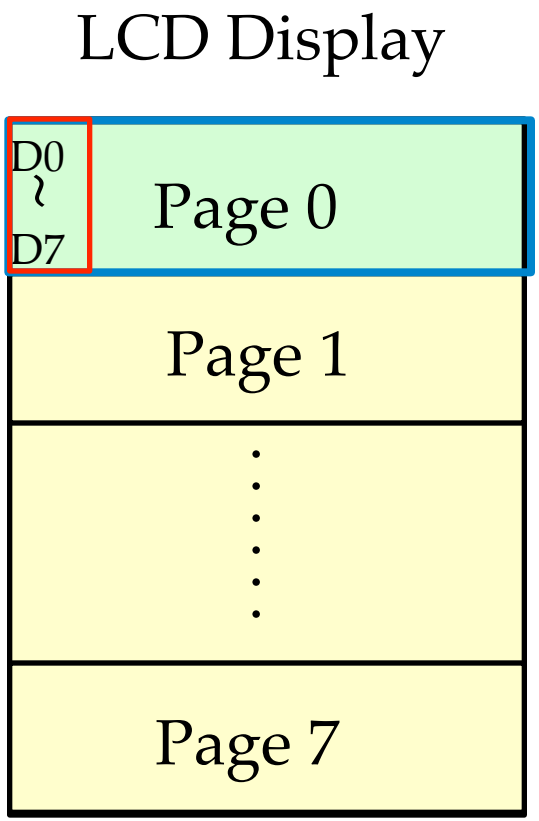


Concept of a ROM Controller

- Fetch a page one time
- Data rearrangement (words to bytes)
  - 8x64-bit (8 ***words***) to 64x8-bit (64 ***bytes***)

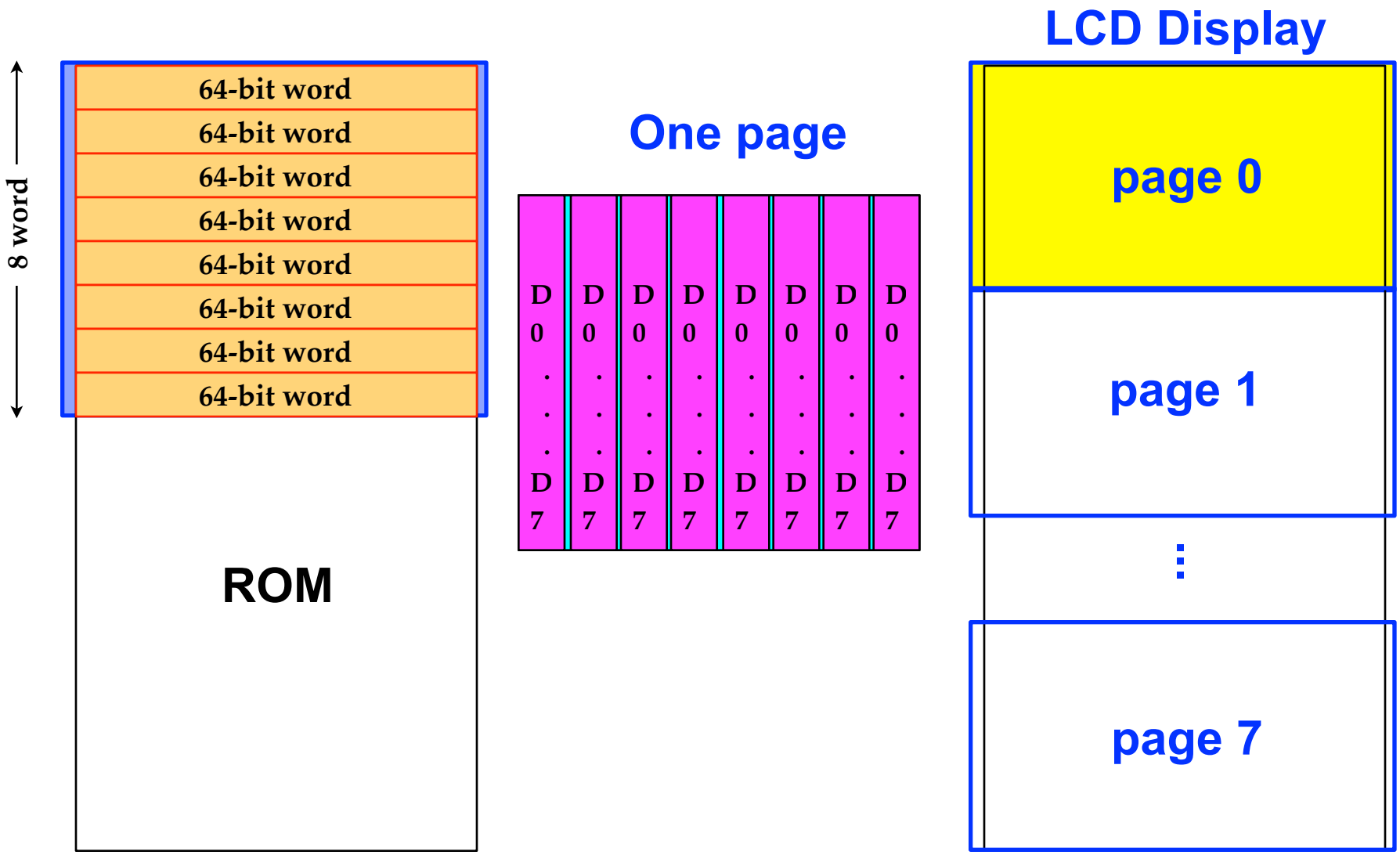




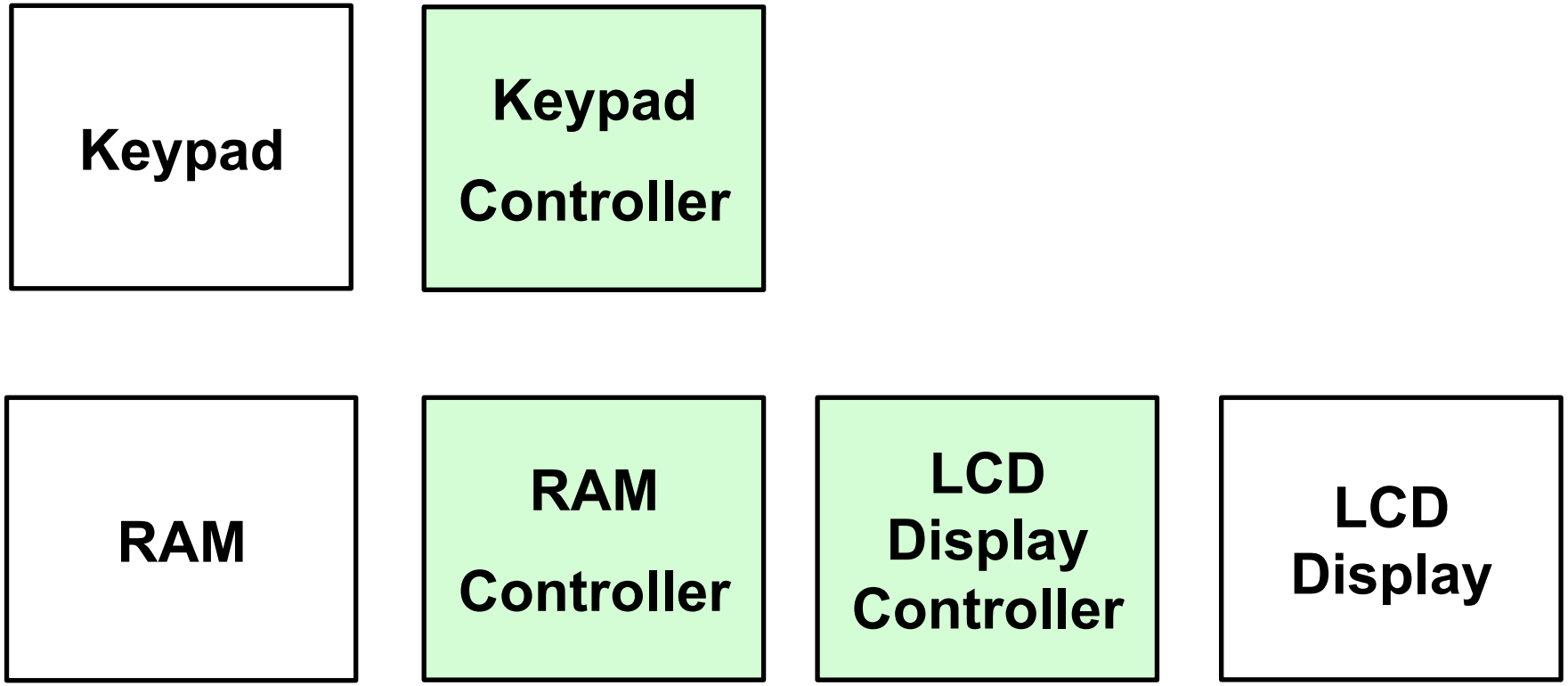


[cthuang]

Concept of a ROM Controller

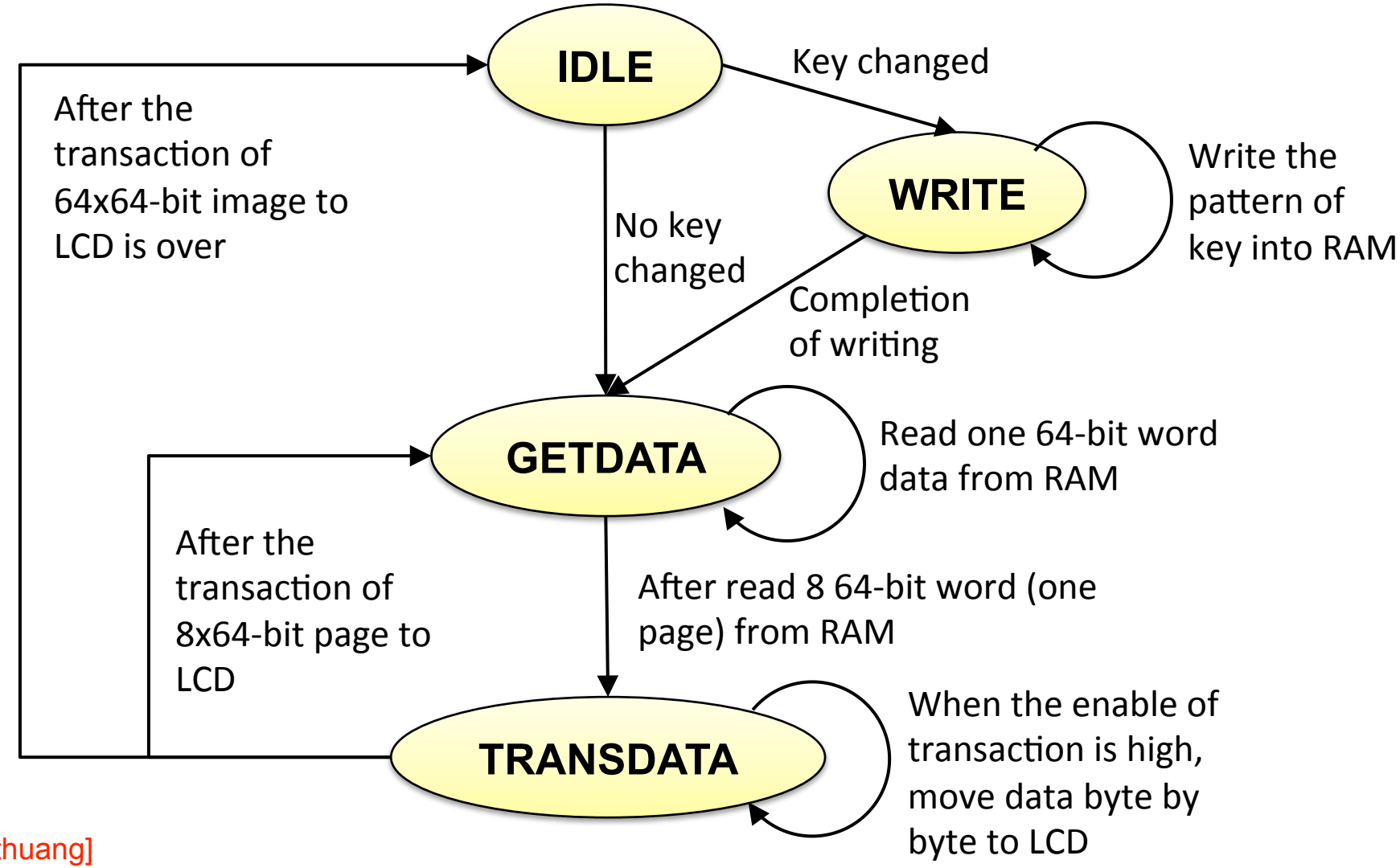


LCD Display with Keypad



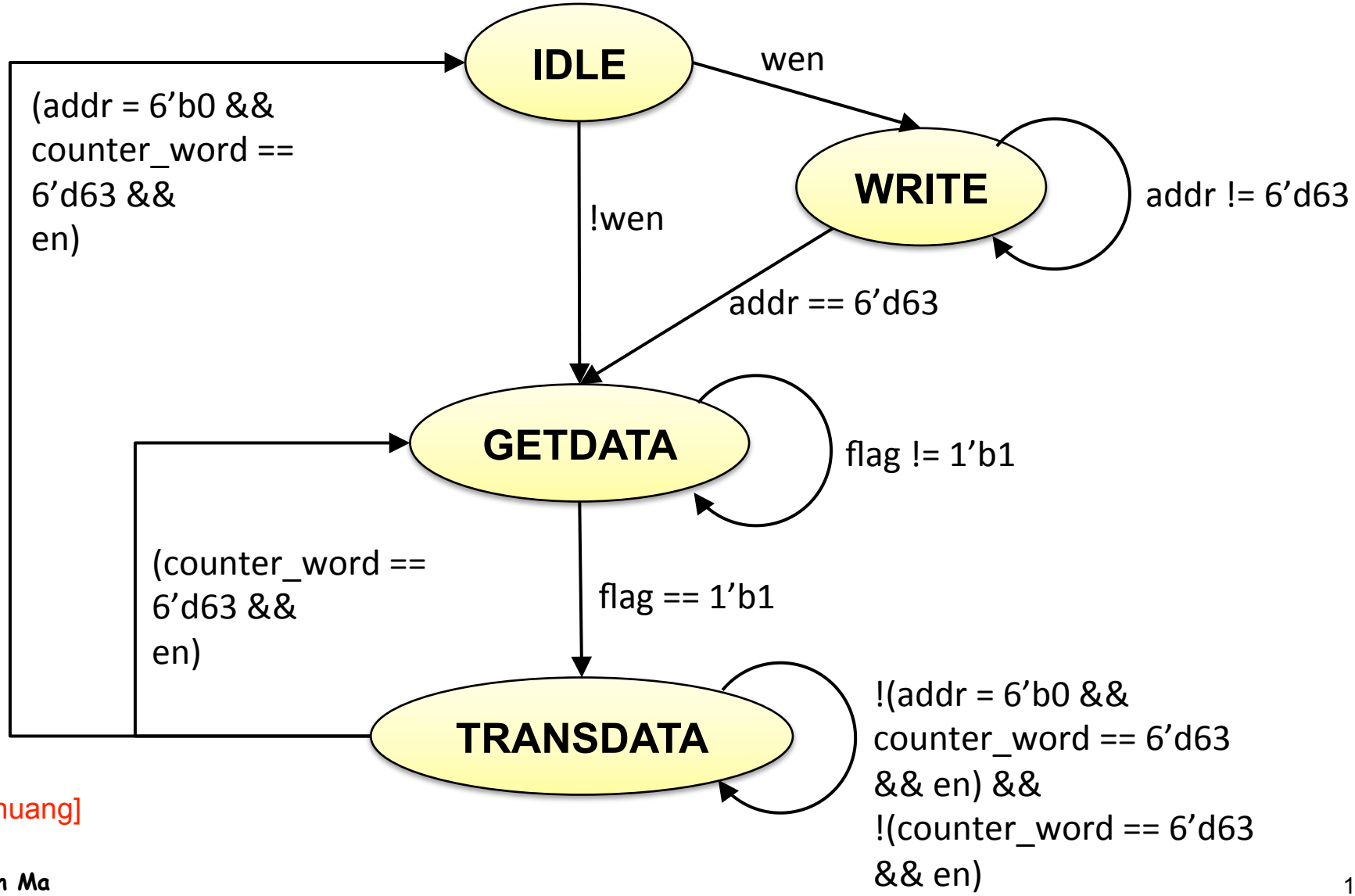
[cthuang]

RAM Controller



[cthuang]

RAM Controller



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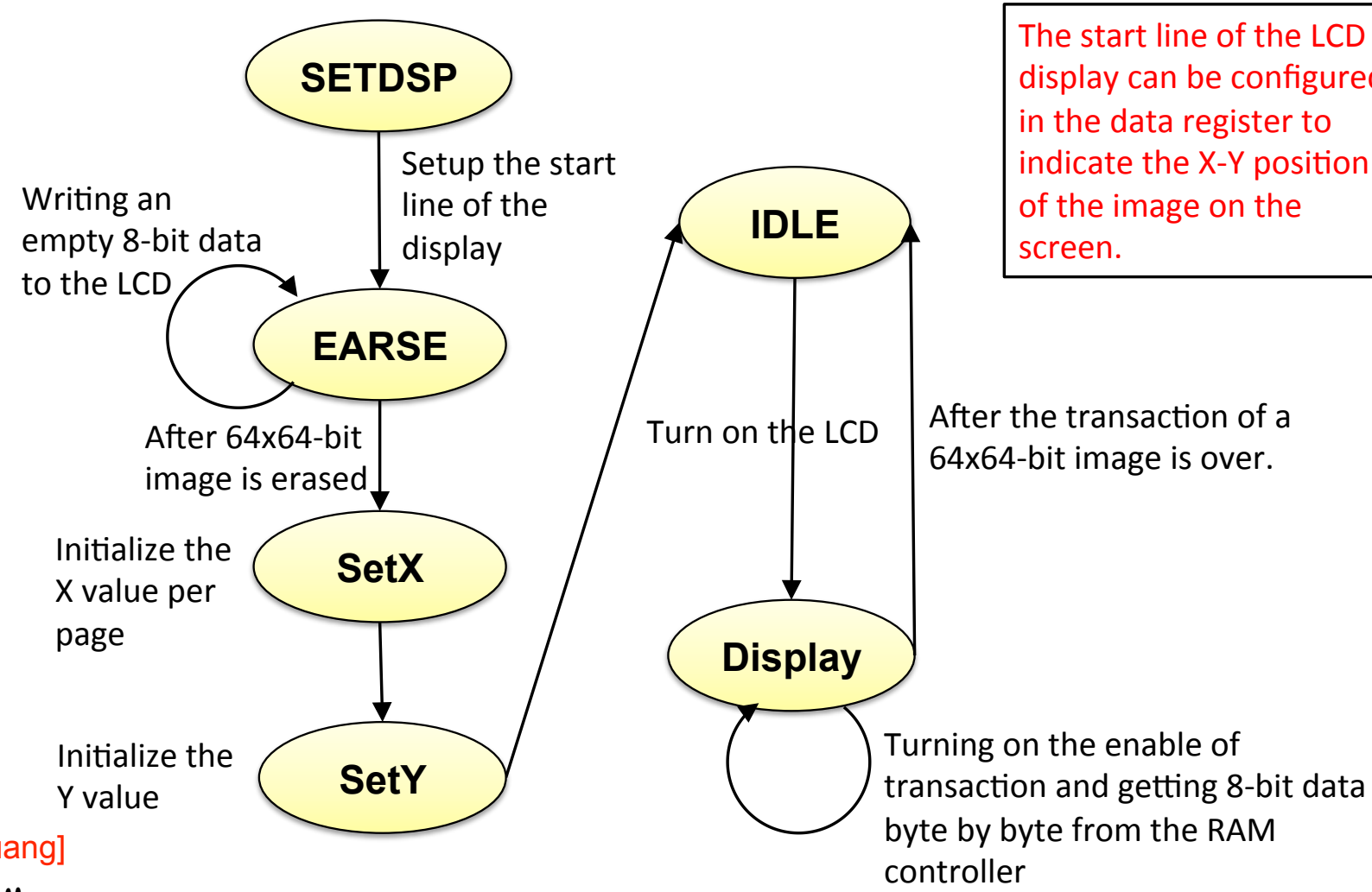
LCD Display Controller



The start line of the LCD display can be configured in the data register to indicate the X-Y position of the image on the screen.

[cthuang]