Lab 1: Introduction to Verilog HDL

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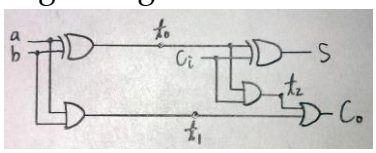
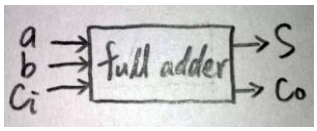
Design Specification

1. Full Adder

- ✓ Logic Equation: $\mathbf{S=a\oplus b\oplus C_i}$, $\mathbf{C_o=a'b+ac_i+bc_i}$
- ✓ Logic Diagram:



- ✓ Block Diagram:



- ✓ I/O:

  Half Adder:

  Inputs: a, b.

  Outputs: s, co.

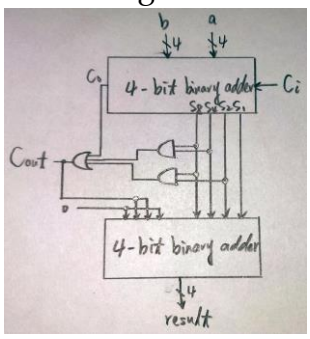
  Full Adder:

  Inputs: a, b, ci.

  Outputs: co, s.

2. Single Digit Decimal Adder

- ✓ Block Diagram:



- ✓ I/O:

  Inputs: a[3:0], b[3:0], ci.

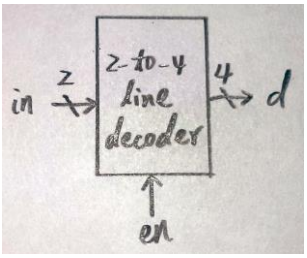
  Outputs: result[3:0], s[3:0], co, cout.

3. 2-to-4-Line Decoder

- ✓ Logic Equation: $\mathbf{d[0]=E\cdot in[1]'\cdot in[0]'}$, $\mathbf{d[1]=E\cdot in[1]'\cdot in[0]}$,

  $\mathbf{d[2]=E\cdot in[1]\cdot in[0]'}$, $\mathbf{d[3]=E\cdot in[1]\cdot in[0]}$.

- ✓ Block Diagram:



- ✓ I/O:
  Inputs: E, in[1:0].
  Output: d[3:0].

Design Implementation

1. **Full Adder**
   - ✓ a and b is the bit we like to add, and ci is an one bit carry in.
     s is the result, and co is an one bit carry out.
   - ✓ The logic function should be: $s=a\hat{}b\hat{}C_i$, $co=a'b|ac|bc$
2. **Single Digit Decimal Adder**
   - ✓ Logic function:
     When adding input a and b, if the result is larger than 9, it should add 6 to the result.
     So, we will get a one bit carry out and a four-bit binary number result[3:0].
     $C_{out}=K+Z_8Z_4+Z_8Z_2$
3. **2-to-4-Line Decoder**
   - ✓ Logic function
     E is enable. When E=0, the decoder will output 0000.
     D[0] = E & (~in[1]) & (~in[0])
     D[1] = E & (~in[1]) & (in[0])
     D[2] = E & (in[1]) & (~in[0])
     D[3] = E & (in[1]) & (in[0])

Discussion

- ✓ It was really a happy experiment, only when debugging made me disappointed. The only wrong thing a met is I forgot to link the full adders in the second 4-bit adder. So, it is not weird that the simulation turned out lots of red Xs. The experiment results went all correct, since I follow the references in the hangout, so it ran as I expected.

Conclusion

- ✓ I have got familiar with the use of Verilog, and know how to declare I/Os variables and write a testbench to test my circuit. During the debugging, I tried to understand the error messages. Hope it will help me to finish future projects.

References

- ✓ Teaching handouts <Introduction> p.52:
  It helps making a decimal adder without using any if statements, but by only using the simple logic gates to get the goal.