# Lab 4: Shift Registers

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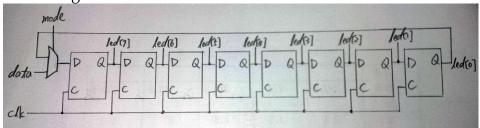
# **Design Specification**

# 1. Serial Shift Register

✓ Experiment Goal:

Cascade eight DFFs together. As the clock signal changes, let the output of LEDs be (01010101), (10101010) repeatedly.

✓ Block Diagram:



✓ I/O:

Inputs: mode, data, clk, rst\_n.

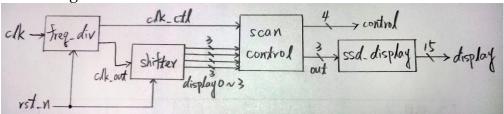
Output: [7:0] led.

## 2. NTHUEE

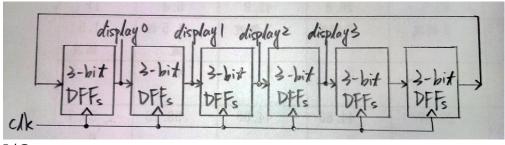
✓ Experiment Goal:

Make the four 14-segment displays print out the scrolling pattern NTHUEE. As the user press the reset button, the patter will reset to NTHU.

✓ Block Diagram:



shifter:



✓ I/O:

Inputs: clk, rst\_n.

Outputs: [14:0] display, [3:0] control.

# **Design Implementation**

# 1. Serial Shift Register

- ✓ Cascade eight DFFs together with a multiplexer before the first DFF. As mode equals to 0 input the data from user, otherwise the register will keep shifting the data already inside.
- ✓ I/O Pins Assignment:

mode	data	clk	rst_n	led[0]~led[7]
T1	P4	R10	N3	K4, K3, L5, K5, H4, H3, L7, K6

#### 2. NTHUEE

- ✓ Build six cascaded 3-bit DFFs, each stores a number which represents a letter. Shift 3-bit DFFs from one to another. And, send the first four 3-bit DFFs data to the scan controller to display the pattern.
- ✓ I/O Pins Assignment:

clk	R10
rst_n	N3
control[0]~control[3]	V8, U8, V6, T6
display[0]~display[14]	U5, T7, R7, V7, V4, T4, T3, R5, N5, R3, U7, T5, V5, N4, P6

### Discussion

✓ Everything works well before I finished demoing. When I demo the second experiment, TA told me that I can use another easier method which has the same result. So, I rewrite part of my code to reach what the TA required. At the end, I think the final version is more efficient than my previous one.

# Conclusion

✓ After this lab, I realize that shift register is very important in our daily life. The LED display which shows information on buses, MRT and other public places all uses this fundamental element to show words in a scrolling way.

### References

### 1. Serial Shift Register

✓ Teaching Handout < Verilog HDL (3)> p.12