Lab 9: Speaker

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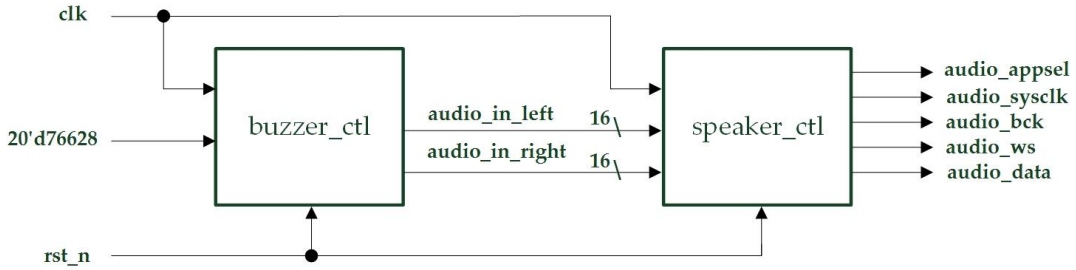
Design Specification

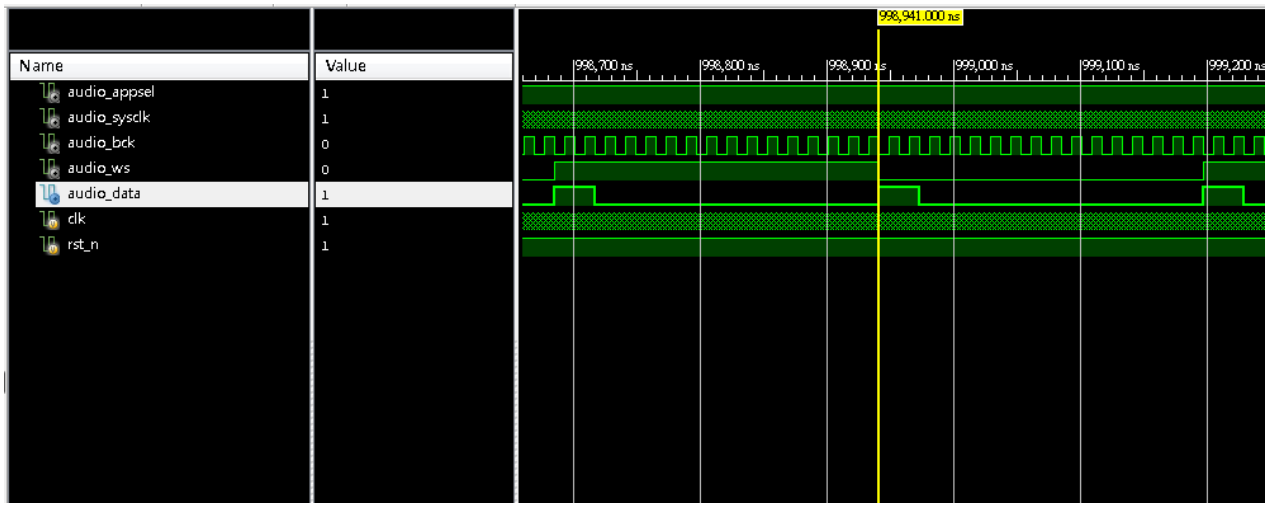
1. Speaker Simulation

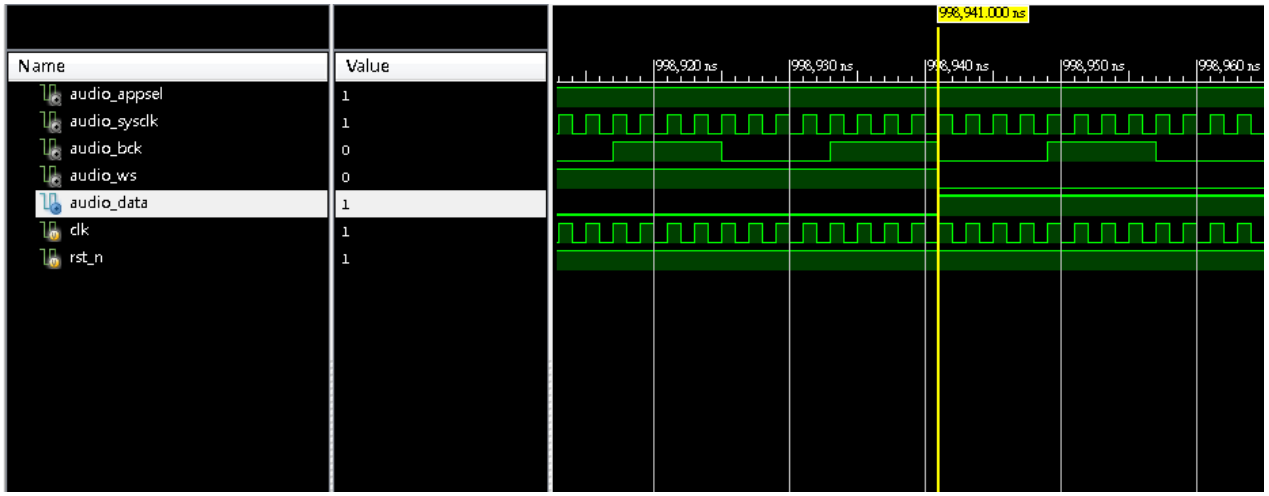
✓ Experiment Goal:
Finish rest of the module code "speaker_ctl" and simulate the speaker control signal.

✓ Block Diagram:



✓ Simulation Result:

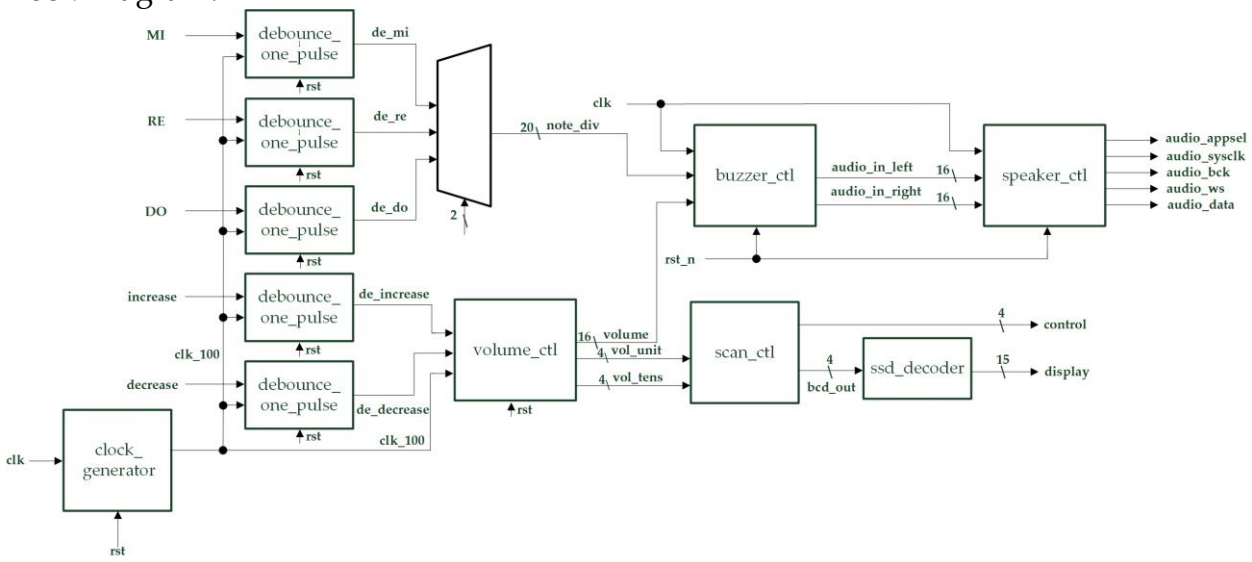




✓ I/Os:
Inputs: clk, rst_n.
Outputs: audio_appsel, audio_sysclk, audio_bcd, audio_ws, audio_data.

2. Speaker Control

- ✓ Experiment Goal:
  Set three buttons as **Do, Re, Mi**, when the buttons is pressed the speaker will play out the note that the button represent. Set another two buttons as increase or decrease the speaker volums.
- ✓ Block Diagram:



- ✓ I/Os:
  Inputs: clk, DO, RE, MI, increase, decrease, rst_n.
  Outputs: audio_appsel, audio_sysclk, audio_bcd, audio_ws, audio_data, [3:0] control, [14:0] display.
- ✓ Details about some module:
  - debounce_one_pulse: Debounce and do one pulse function for the input button.
  - volume_ctl: Use the increase and decrease button signal input to determine the volume output to the buzzer controller and output the volume value to the 14SD.

Design Implementation

1. Speaker Simulation

- ✓ First, connect buzzer_ctl, speaker_ctl together, and send constant value 20'd76628 to port "note_div" in buzzer_ctl module. Second write a testbench to verify the waveform.

2. Speaker Control

- ✓ First, do debounce and one pulse for all input buttons. Second, determine which note button is pressed and send the represent note_div signal to module "buzzer_ctl". Third, pass increase and decrease signal to module "volume_ctl" which will send the volume signal to buzzer controller and send the BCD value to scan controller. Fourth, finish connecting the scan controller and 14SD decoder.

- ✓ I/O Pins Assignment:

Port Name	Assignment	Function
clk	R10	FPGA board oscillator input
DO	M5	Note "DO" button input
RE	L6	Note "RE" button input
MI	P3	Note "MI" button input
increase	P4	Volume increase button input
decrease	N3	Volume decrease button input
rst_n	T2	
control[0]~control[3]	V8, U8, V6, T6	14-SD control signal output
display[0]~display[14]	U5, T7, R7, V7, V4, T4, T3, R5, N5, R3, U7, T5, V5, N4, P6	14-SD light control signal output

Discussion

- ✓ Since most of the code and design information are given to us on handout, so I did not meet any disastrous bugs. In experiment 2 most of the modules are copied from experiment 1, the only thing is to build a volume controller. So, I finished this lab in a very short time.

Conclusion

- ✓ After 8 labs we finally know how to use the speaker on board. With this additional ability, we can do more interesting things. Maybe someday we can be able to write a song on the FPGA board and it will automatically play and repeat it without me to press the buttons. Though there are still some things we have not learnt (such as LCD Display), I think we can start designing my final project to finish it on time.

References

1. Speaker Simulation

- ✓ Teaching Handout <Speaker> p.3~p.10

  →Helps me to understand how the buzzer control works and finish writing the module speaker control.