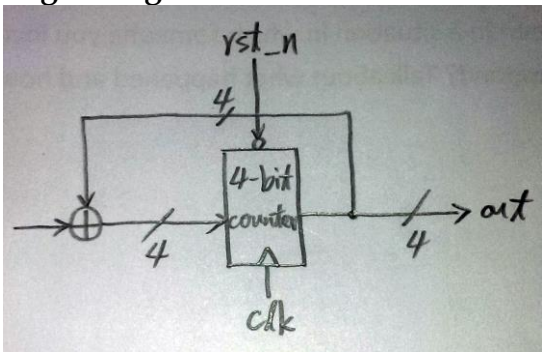
Lab 3: Counters (Pre-Lab)

103061207 徐安廷

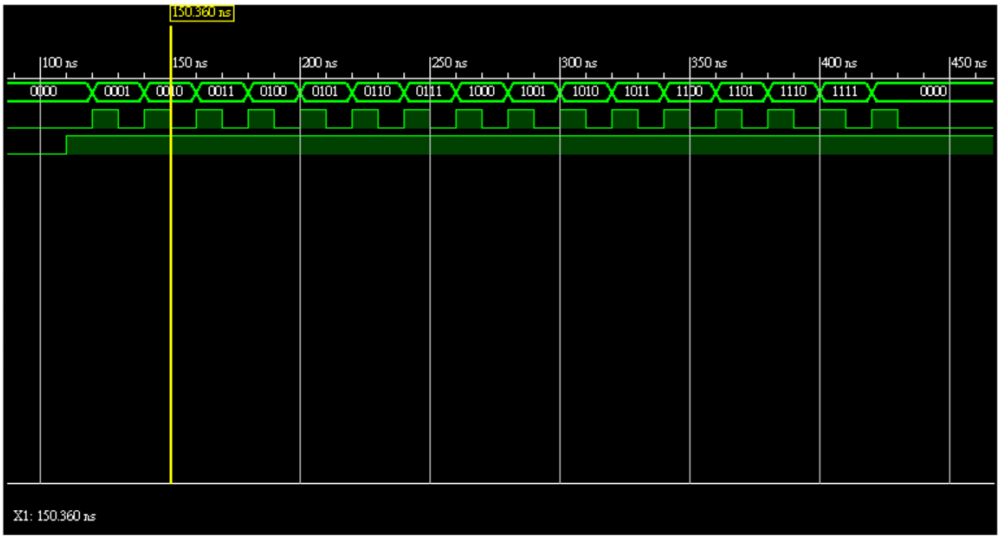
Design Specification

- ✓ **I/O:**
  Inputs: clk, rst_n
  Output: out
- ✓ **Logic Diagram:**



Design Implementation

- ✓ **Simulation Result:**



Conclusion

- ✓ Counter 一個看似很簡單的東西，其實有很大的應用，可當作除頻器得到設計者所需要的頻率，在之後的 Lab 裡應該會時常用到。

References

- ✓ Teaching Handout <Verilog HDL (2)> p.34