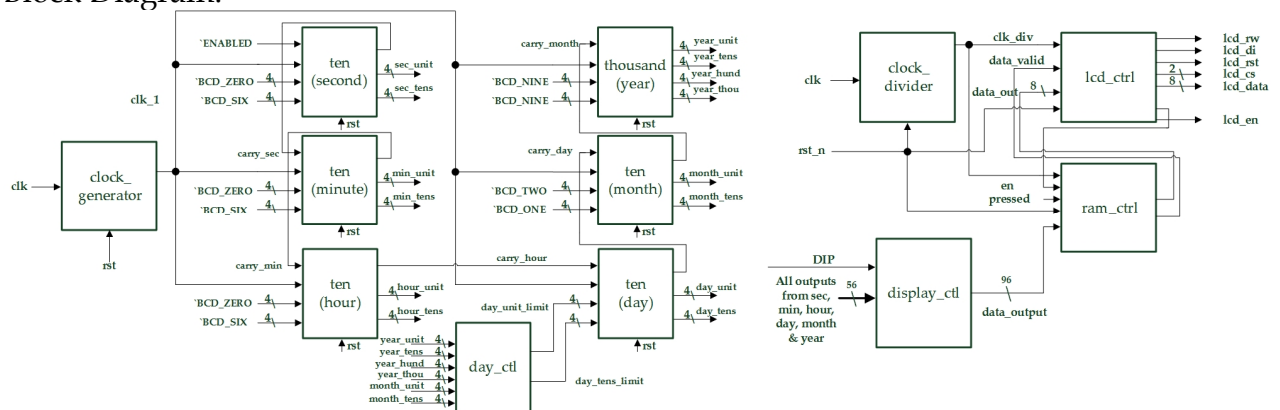# Lab 12: LCD Display (2)

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Design Specification

1. **LCD Electronic Clock**
   - ✓ Experiment Goal:
     Adjust the module in lab7-3 to show the numbers on the LCD screen instead of 14-SD.
   - ✓ Block Diagram:

   - ✓ I/Os:
     Inputs: clk, rst_n, [2:0] DIP.
     Outputs: lcd_rst, lcd_rw, lcd_di, lcd_en, [1:0] lcd_cs, [7:0] lcd_data.

Design Implementation

1. **LCD Electronic Clock**
   - ✓ First, remove the 14-SD modules in Lab7. Second, add LCD control modules and connect the data input with display controller's output.
   - ✓ I/O Pin Assignments:

Port Name	Assignment	Function
clk	R10	FPGA board oscillator input
rst_n	N3	Active low reset input button
DIP[0]~DIP[2]	L2, P2, T1	Adjust the clock frequency & Support 12/24 hour
LCD_rst	E3	LCD reset output
LCD_en	F5	LCD enable output
LCD_rw	C2	LCD read/write control output
LCD_di	C1	LCD data/instruction output
LCD_cs[0]~LCD_cs[1]	F4, E1	LCD frame selection output
LCD_data[0]~ LCD_data[7]	F6, D3, E4, G6, H7, D1, D2, F3	LCD data output

Discussion

✓ The problem I met was I don't know how the RAM controller works, so I had a discussion with my classmate. And, found out that the codes cut the LCD screen into 16 parts. Each part has a represent mark, and I add a mark decoder to send the graph data to RAM, so it can display the graphs correctly.

Conclusion

✓ After four months class, we finally learn all the skills to implement the function on an FPGA board. These skills are very important to us in future. We may use it to do lots of things or even DIY an useful tool at home some day.

References

✓ Teaching Handouts <LCD Display (2)> p.2~22
    →Helps me to understand how the states work in LCD controller and ROM controller.