**Lab 2: FPGA Emulation**

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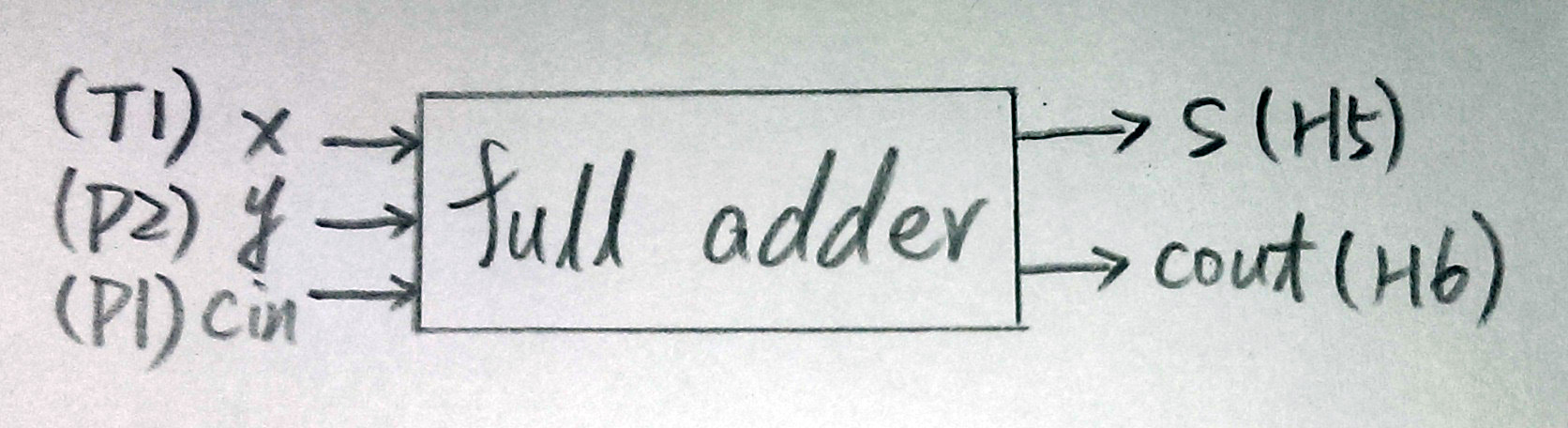
**Design Specification**

1. **Full Adder**

* Experiment Goal:

Alter the full adder in Lab1-1 to make the calculation result be shown on the LEDs.

* Block Diagram:



* I/O:

Inputs: x, y, cin.

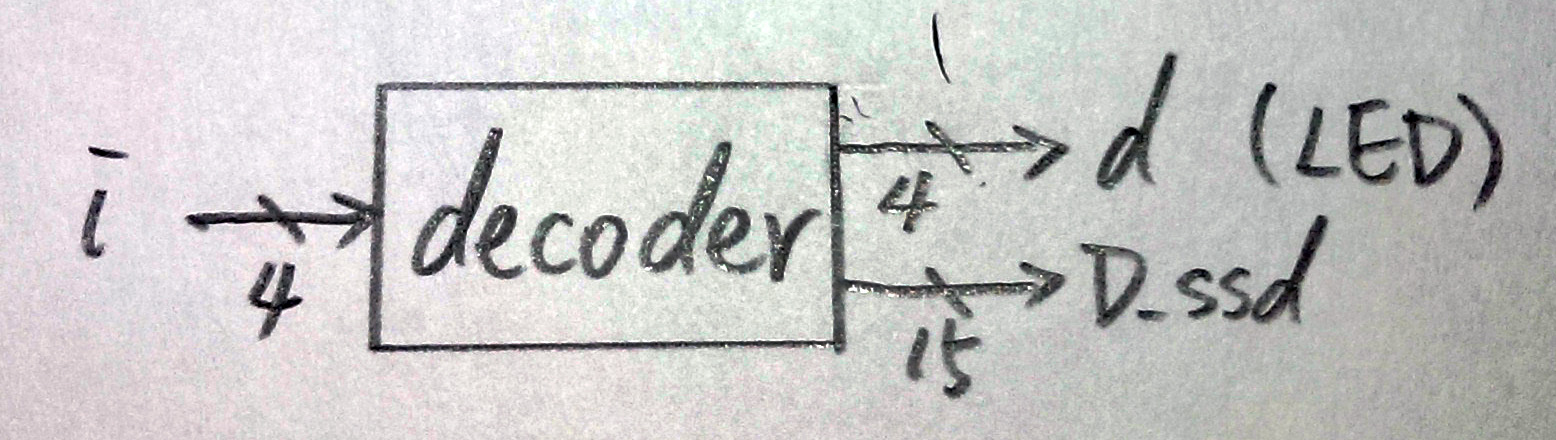
Outputs: s, cout.

1. **BCD to 14-Segment Display Decoder**

* Experiment Goal:

Give a BCD code to the FPGA board, and let the 14-segment display show the code in decimal numbers.

* Block Diagram:



* I/O:

Inputs: bcd[3:0].

Outputs: led[3:0], display[3:0].

**Design Implementation**

1. **Full Adder**

* Logic Function: s=x^y^cin, cout=x’･y|x･cin|y･cin
* I/O Pin Assignment:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **x** | **y** | **cin** | **s** | **cout** |
| T1 | P2 | P1 | H5 | H6 |

1. **BCD to 14-Segment Display Decoder**

* I/O Pin Assignment:

|  |  |
| --- | --- |
| bcd[0]~bcd[3] | N2, P1, P2, T1 |
| led[0]~led[3] | F2, F1, H6, H5 |
| display[0]~display[14] | U5, T7, R7, V7, V4, T4, T3, R5, N5, R3, U7, T5, V5, N4, P6 |

**Discussion**

* It has been one of my dream to handle an electrical board. It was excited that I saw the LEDs and 14-segment display showing the result. Since the experiment only need to follow the instruction, I did not meet any bogs or errors.

**Conclusion**

* I have got much familiar with the use of Verilog, know how to assign the I/O pins, and how to write my logic program to FPGA. Hope those basic concept and technique may help me in the following labs.

**References**

1. **Full Adder**

* Teaching Handout <FPGA Emulation> p.14~25

→Helps me to learn how to assign the I/O pins.

1. **BCD to 14-Segment Display Decoder**

* Teaching Handout <Verilog HDL (2)> p.28

→Telling me how to write the display decoder.