**Lab 3: Counters**

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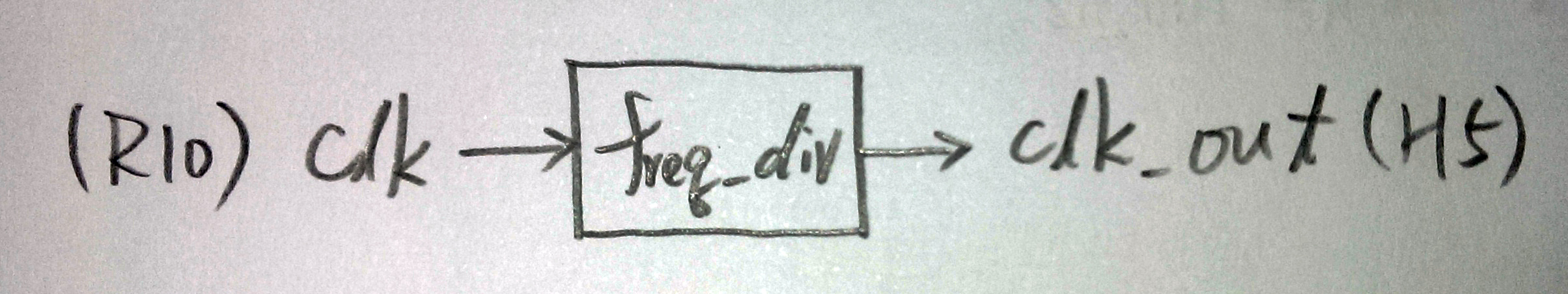
**Design Specification**

1. **Frequency Divider**

* Experiment Goal:

Construct a counter that can provide a 2-25 frequency output of the original clock on board, and show the signal on a LED.

* Block Diagram:



* I/O:

Input: clk.

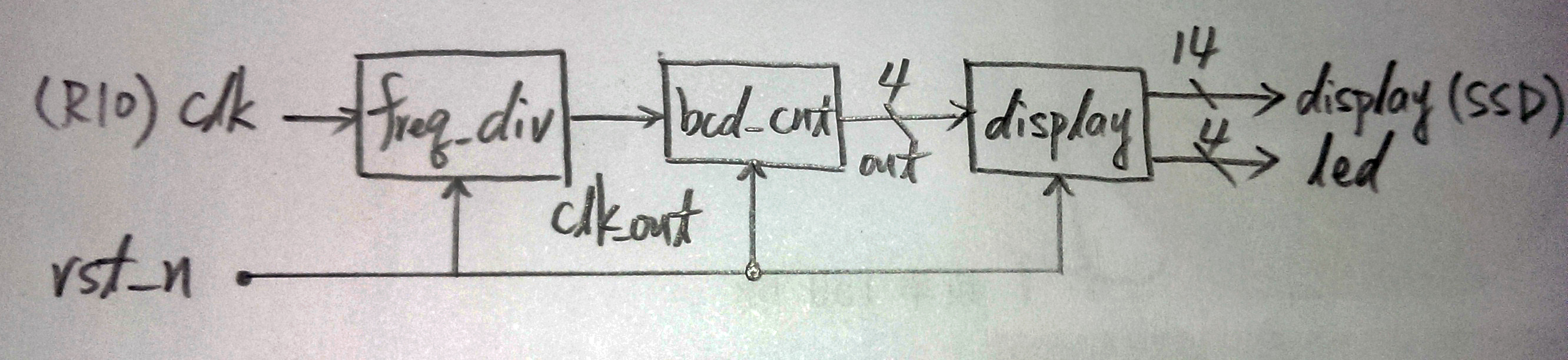
Output: clk\_out.

1. **Single Digit BCD Up Counter**

* Experiment Goal:

Use a frequency divider to send a signal to the counter, let it count from 0 to 9 repeatedly.

* Block Diagram:



* I/O:

Inputs: clk, rst\_n.

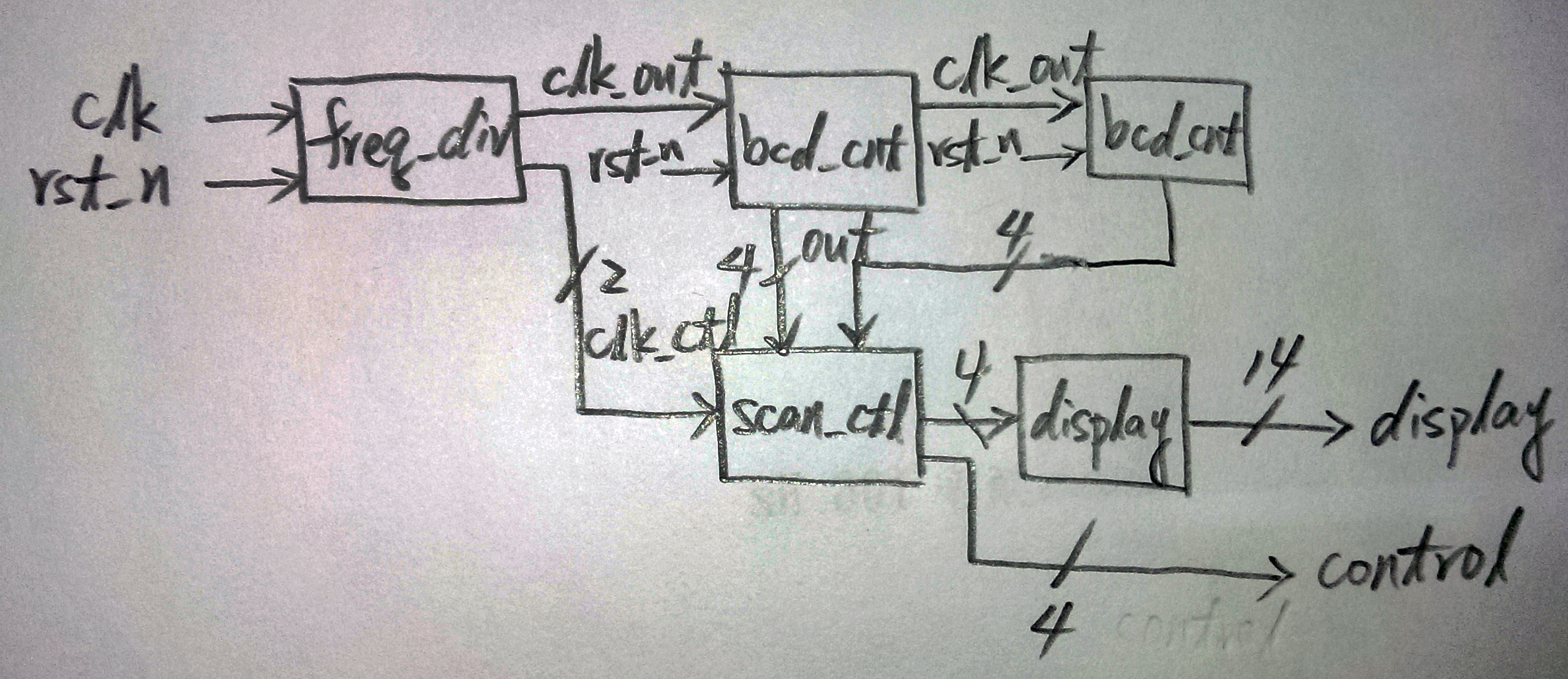
Outputs: [14:0] display, led[3:0].

1. **2-Digit BCD Up Counter**

* Experiment Goal:

Let the 14-segment display on FPGA board count from 00 to 99 repeatedly.

* Block Diagram:



* I/O:

Inputs: clk, rst\_n.

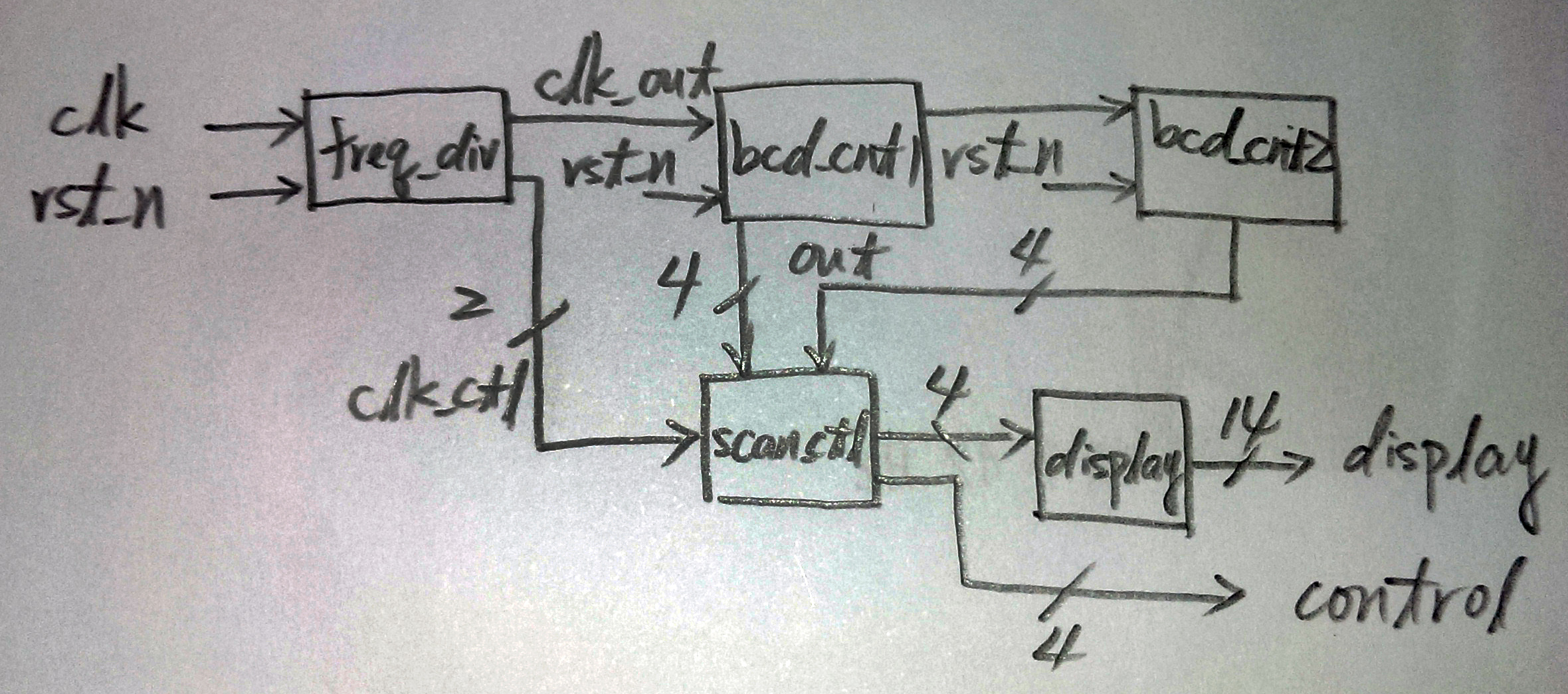
Outputs: [14:0] display, [3:0] control

1. **30 Seconds Down Counter**

* Experiment Goal:

Let the 14-segment display on FPGA board count from 30 to 00 and stop at 00.

* Block Diagram:



* I/O:

Inputs: clk, rst\_n.

Outputs: [14:0] display, [3:0] control

**Design Implementation**

1. **Frequency Divider**

* Using 25 counters to provide a 2-25 clock frequency of the original clock on board.
* I/O Pins Assignment:

|  |  |
| --- | --- |
| **clk** | **clk\_out** |
| R10 | H5 |

1. **Single Digit BCD Up Counter**

* Build a counter which its clock signal is from a frequency divider, and pass the counter output to the 14-segment display decoder.
* I/O Pins Assignment:

|  |  |
| --- | --- |
| **clk** | R10 |
| **rst\_n** | N3 |
| **led[0]~led[3]** | F2, F1, H6, H5 |
| **display[0]~display[14]** | U5, T7, R7, V7, V4, T4, T3, R5, N5, R3, U7, T5, V5, N4, P6 |

1. **2-Digit BCD Up Counter**

* Alter the previous up counter to two counters which represent the two digits respectively. Also, use a scan controller to show out the digit numbers.
* I/O Pins Assignment:

|  |  |
| --- | --- |
| **clk** | R10 |
| **rst\_n** | N3 |
| **control[0]~control[3]** | V8, U8, V6, T6 |
| **display[0]~display[14]** | U5, T7, R7, V7, V4, T4, T3, R5, N5, R3, U7, T5, V5, N4, P6 |

1. **30 Seconds Down Counter**

* Change the code in 2-digit BCD up counter which make it starts counting down from 30.
* I/O Pins Assignment:

|  |  |
| --- | --- |
| **clk** | R10 |
| **rst\_n** | N3 |
| **control[0]~control[3]** | V8, U8, V6, T6 |
| **display[0]~display[14]** | U5, T7, R7, V7, V4, T4, T3, R5, N5, R3, U7, T5, V5, N4, P6 |

**Discussion**

* Everything works well during the whole experiment. The only thing that went wrong is in the third frequency divider. I copied the entire divider code in the handout. Since there is a logic error in it, so I spend more than one hour to find out the bug and fix it.

**Conclusion**

* It is recommended to modularize the module, and recall it in the top module. Because I found that some of my classmates use a nest structure to write their code, which makes the structure more complicated and hard to debug.

**References**

1. **Frequency Divider**

* Teaching Handout < Verilog HDL (2)> p.35

1. **Single Digit BCD Up Counter**

* Teaching Handout <Verilog HDL (2)> p.39

→Telling me how to build the up counter.

1. **2-Digit BCD Up Counter**

* Teaching Handout <Verilog HDL (2)> p.40

→Helps me understand how the scan controller works.