**Lab 4: Shift Registers (Pre-Lab)**

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**Design Specification**

* **Experiment Goal:**

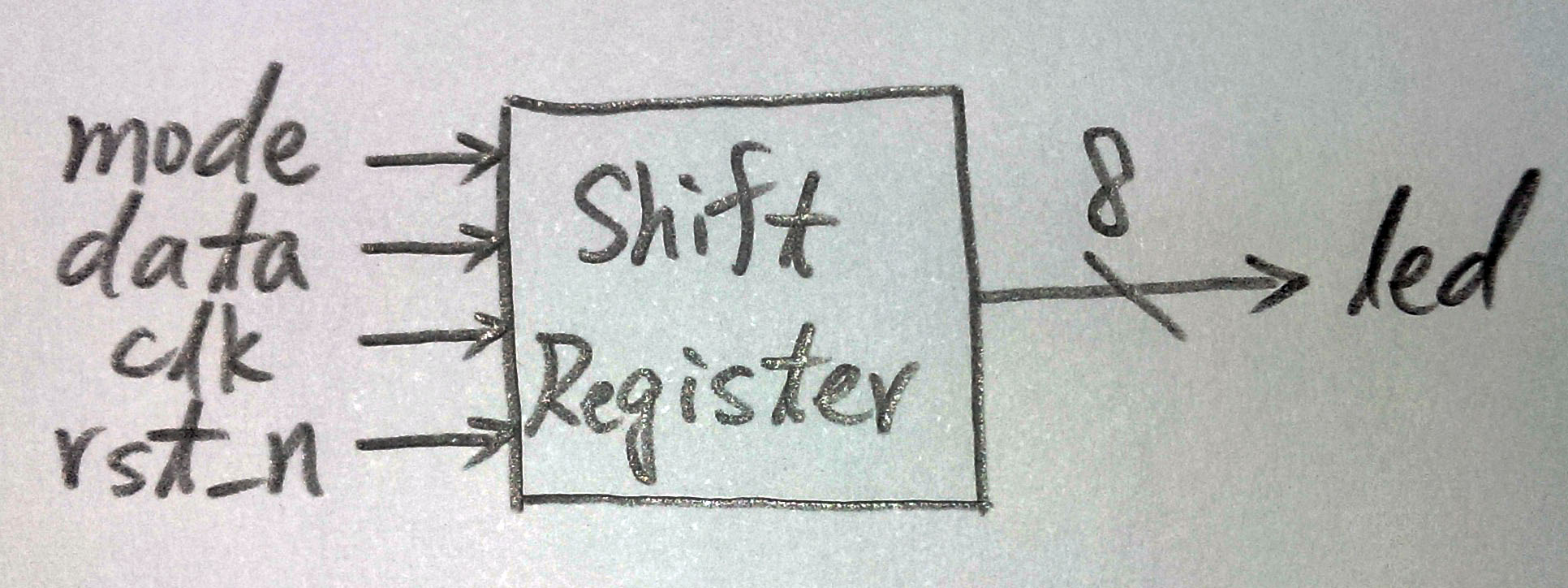
Cascade eight DFFs together. As the clock signal changes, let the output of LEDs be (01010101), (10101010) repeatedly.

* **I/O:**

Inputs: mode, data, clk, rst\_n

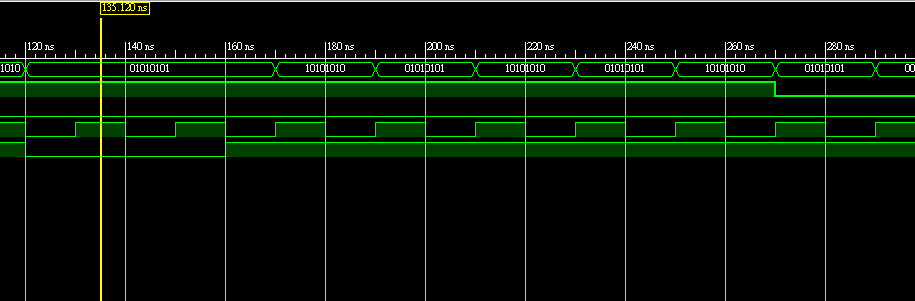
Output: [7:0] led

**Block Diagram:**



**Design Implementation**

* **Simulation Result:**

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**Conclusion**

* Register is a useful thing that it can help us show messages on a display reversely. It is also a significant component in our daily use electric devices.

**References**

* Teaching Handout <Verilog HDL (3)> p.12

→It helps to know how to write an eight bits shift register.