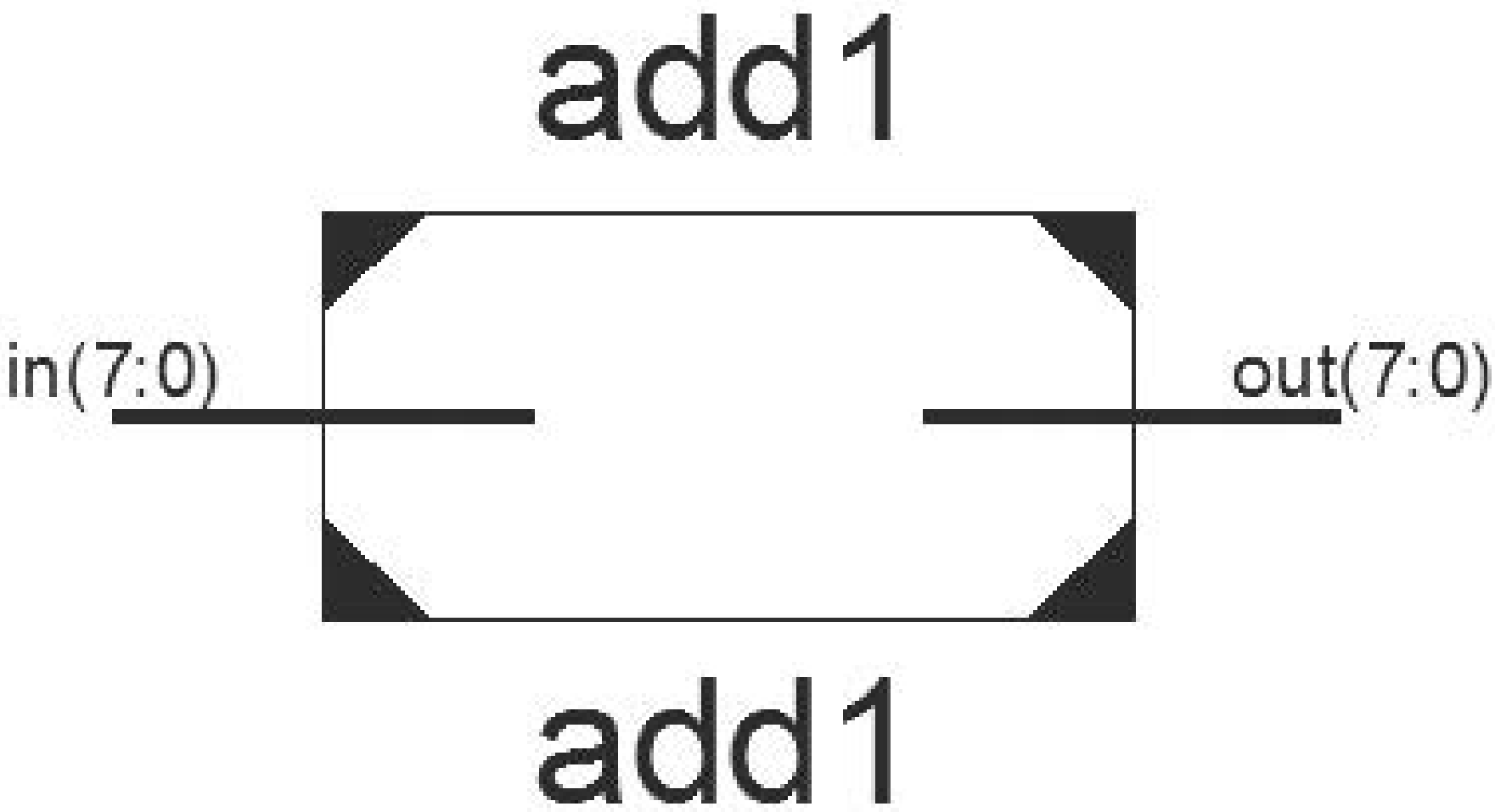
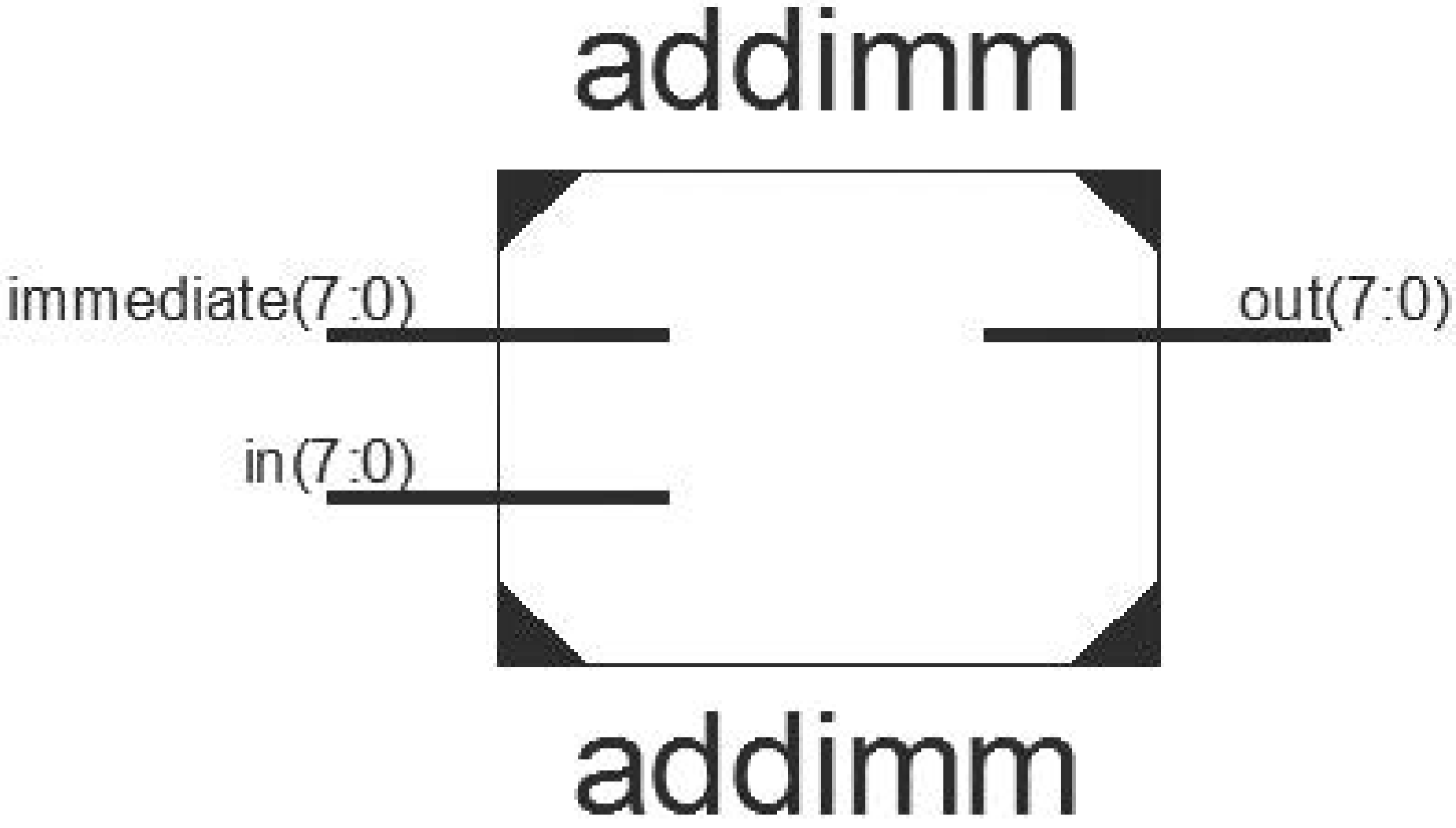
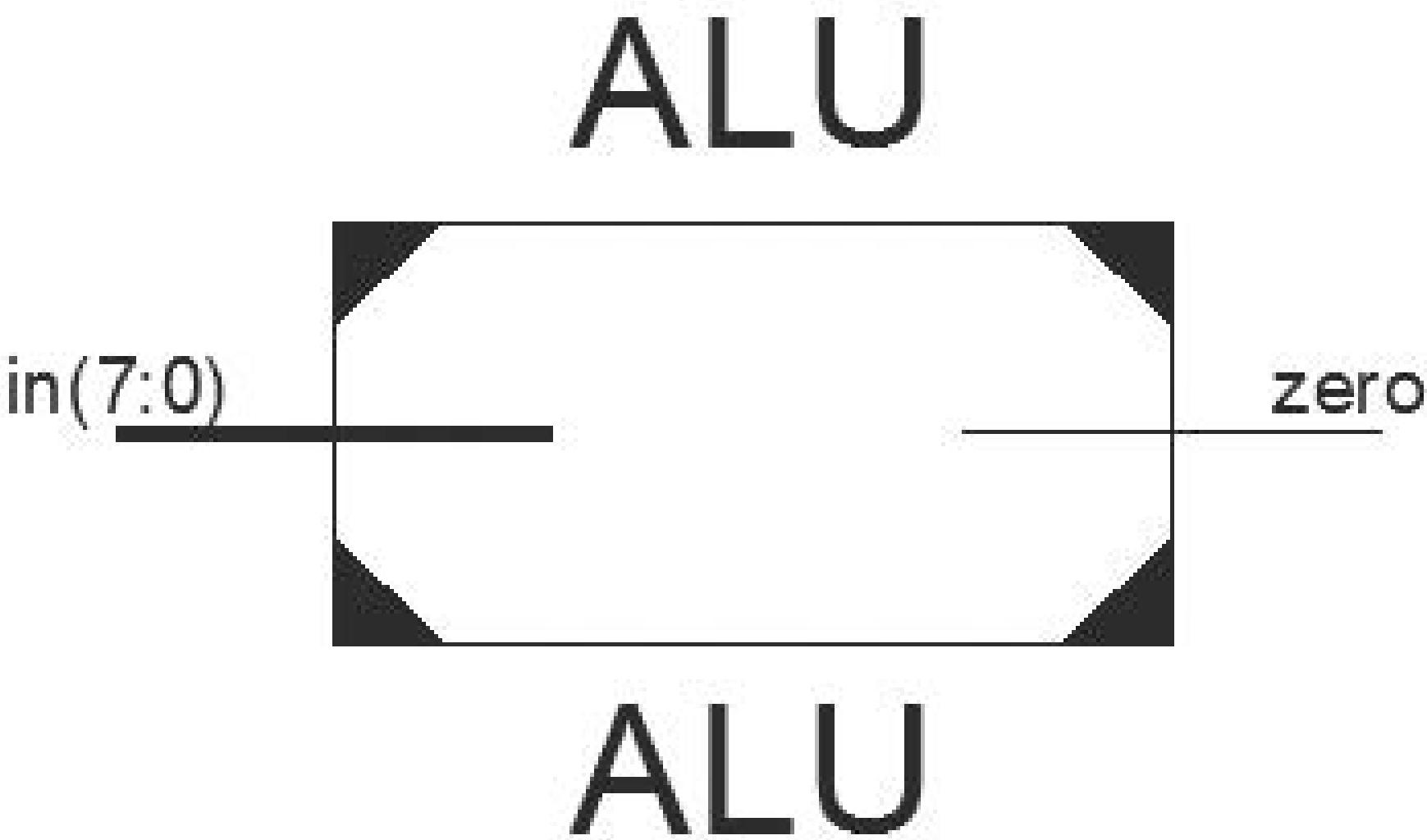
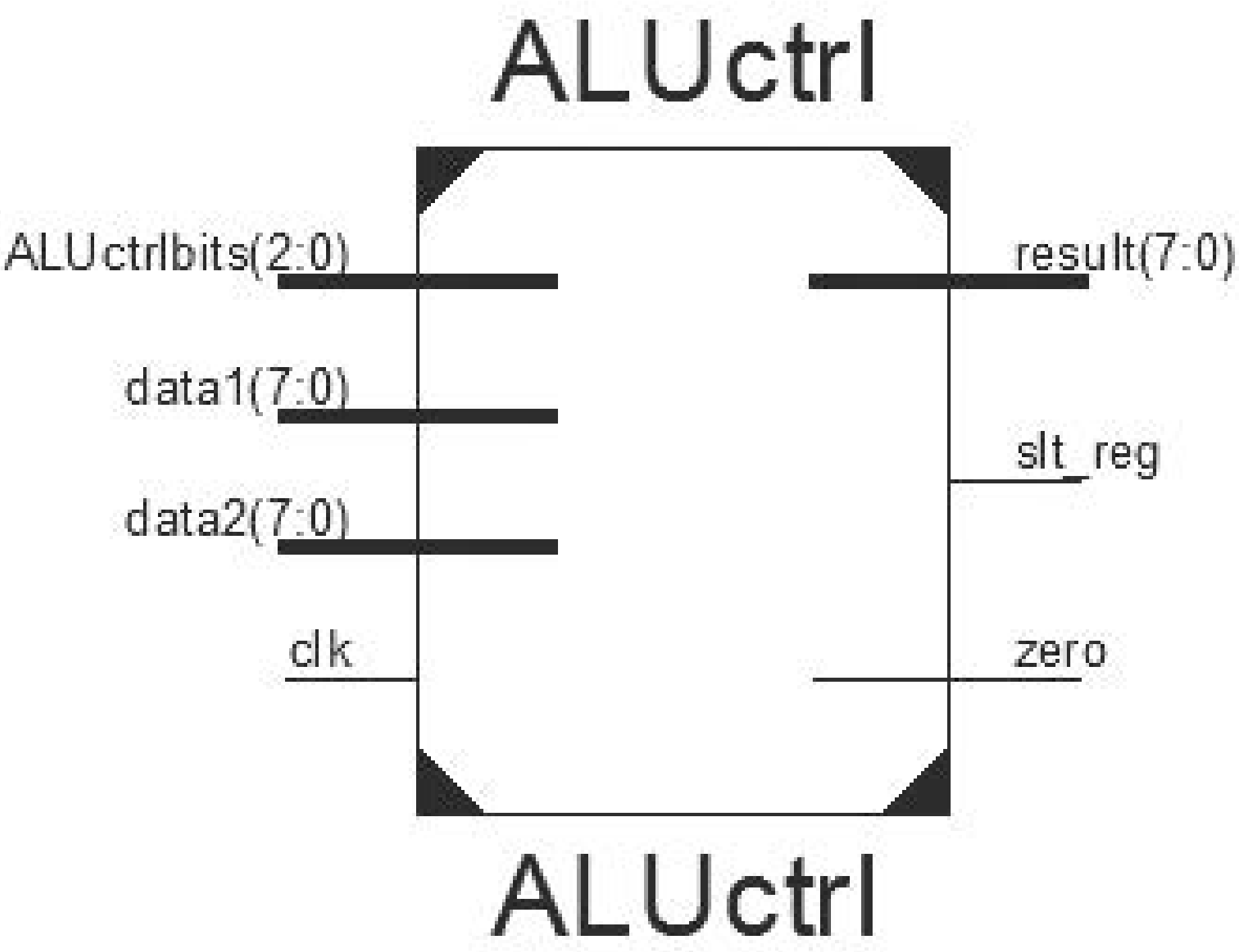
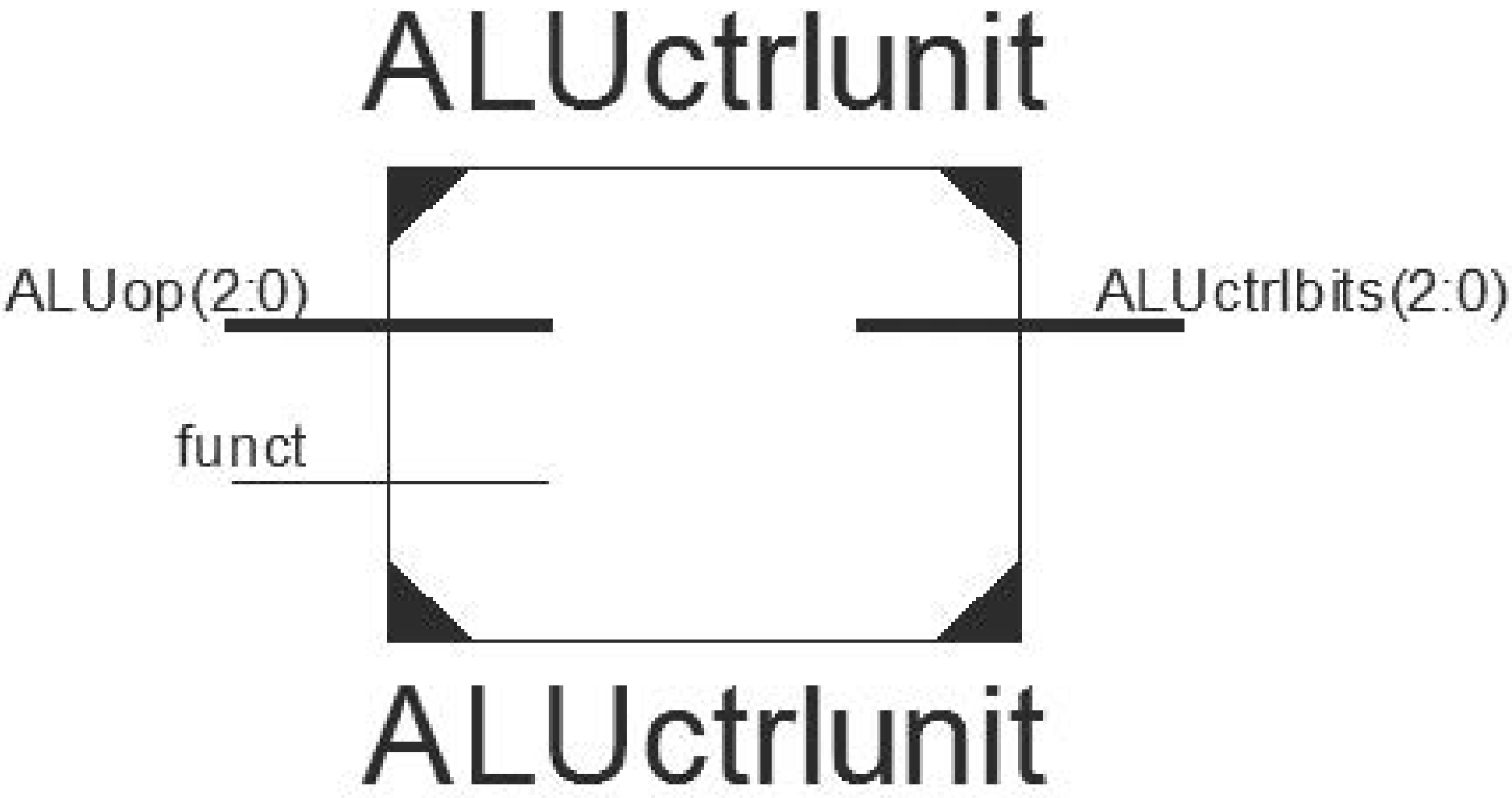

add1
in(7:0)
out(7:0)
add1


addimm
immediate(7:0)
in(7:0)
out(7:0)
addimm


ALU
in(7:0)
zero
ALU


ALUctrl
ALUctrlbits(2:0)
data1(7:0)
data2(7:0)
clk
result(7:0)
slt_reg
zero
ALUctrl


ALUctrlunit
ALUop(2:0)
ALUctrlbits(2:0)
funct
ALUctrlunit

ctrl

inst1(2:0)

ALUop(2:0)

memToReg(1:0)

nextctrl(1:0)

slotctrl(1:0)

ALUsrc

beqctrl

jalctrl

jctrl

jrctrl

memctrl

memRead

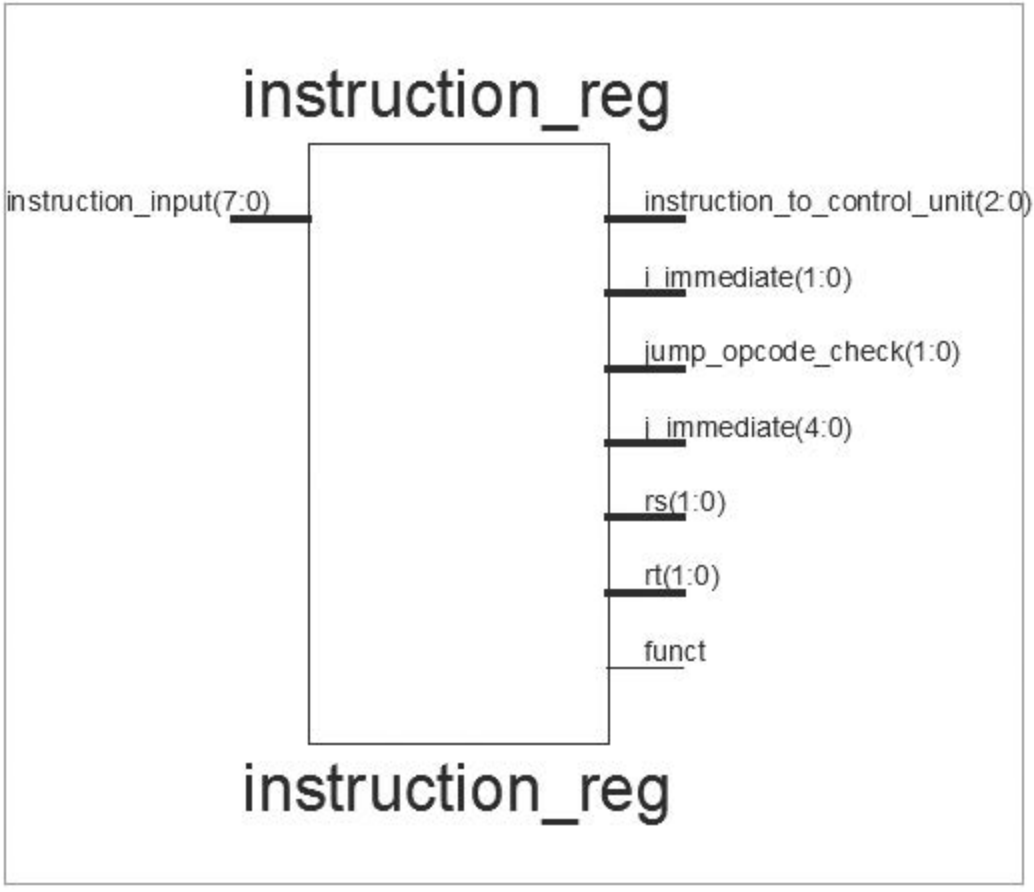
memWrite

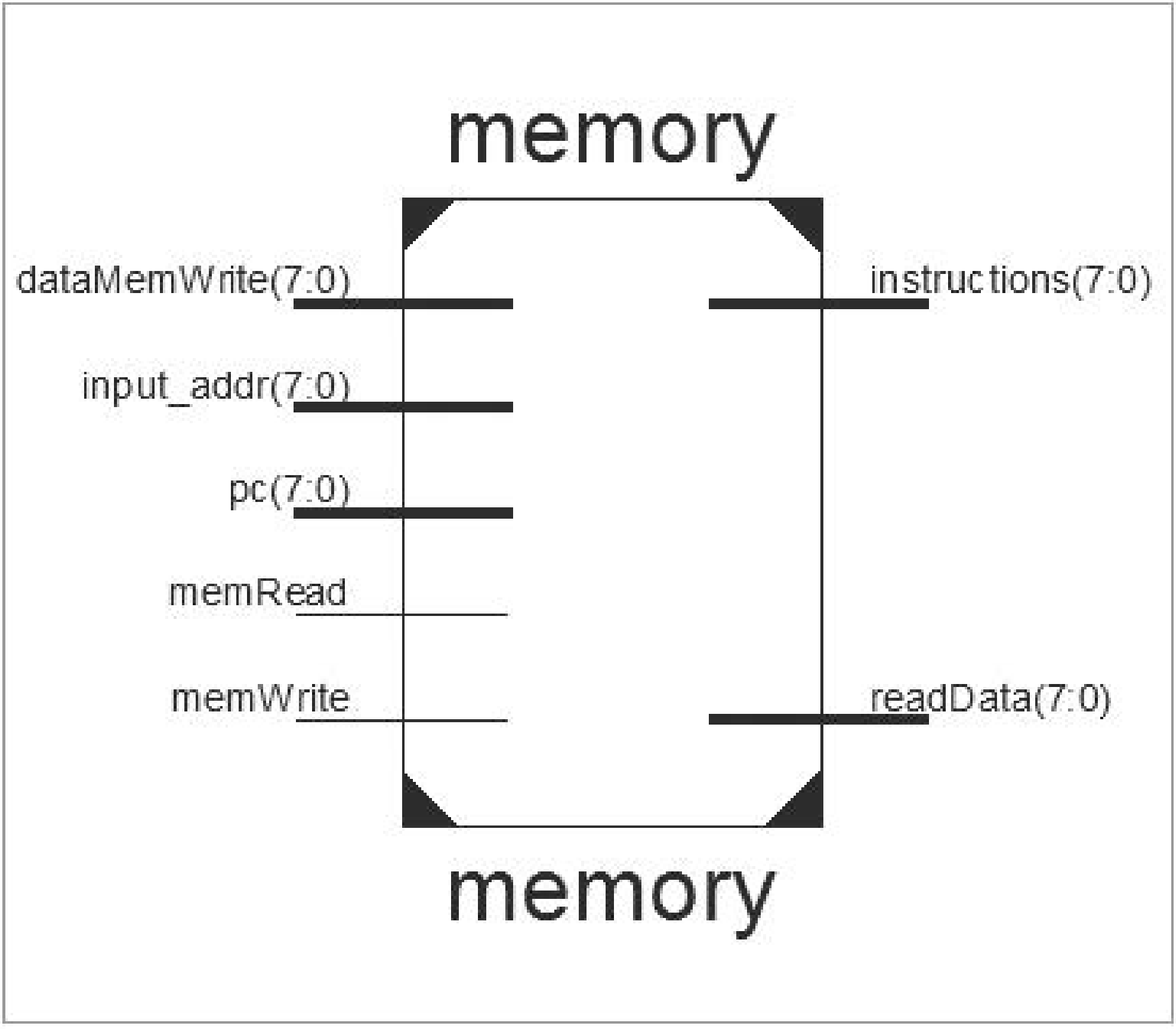
ractrl

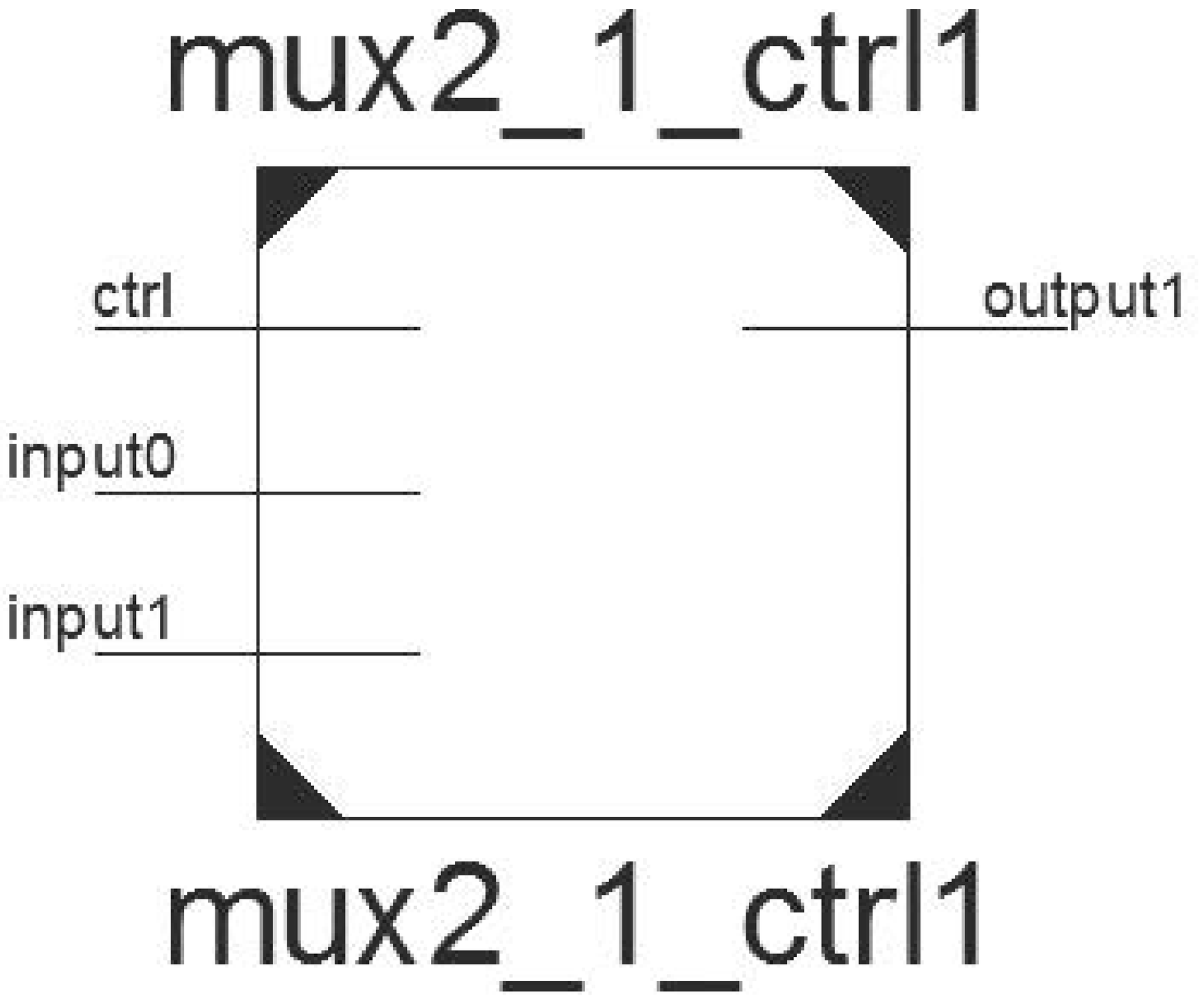
regWrite

inst2

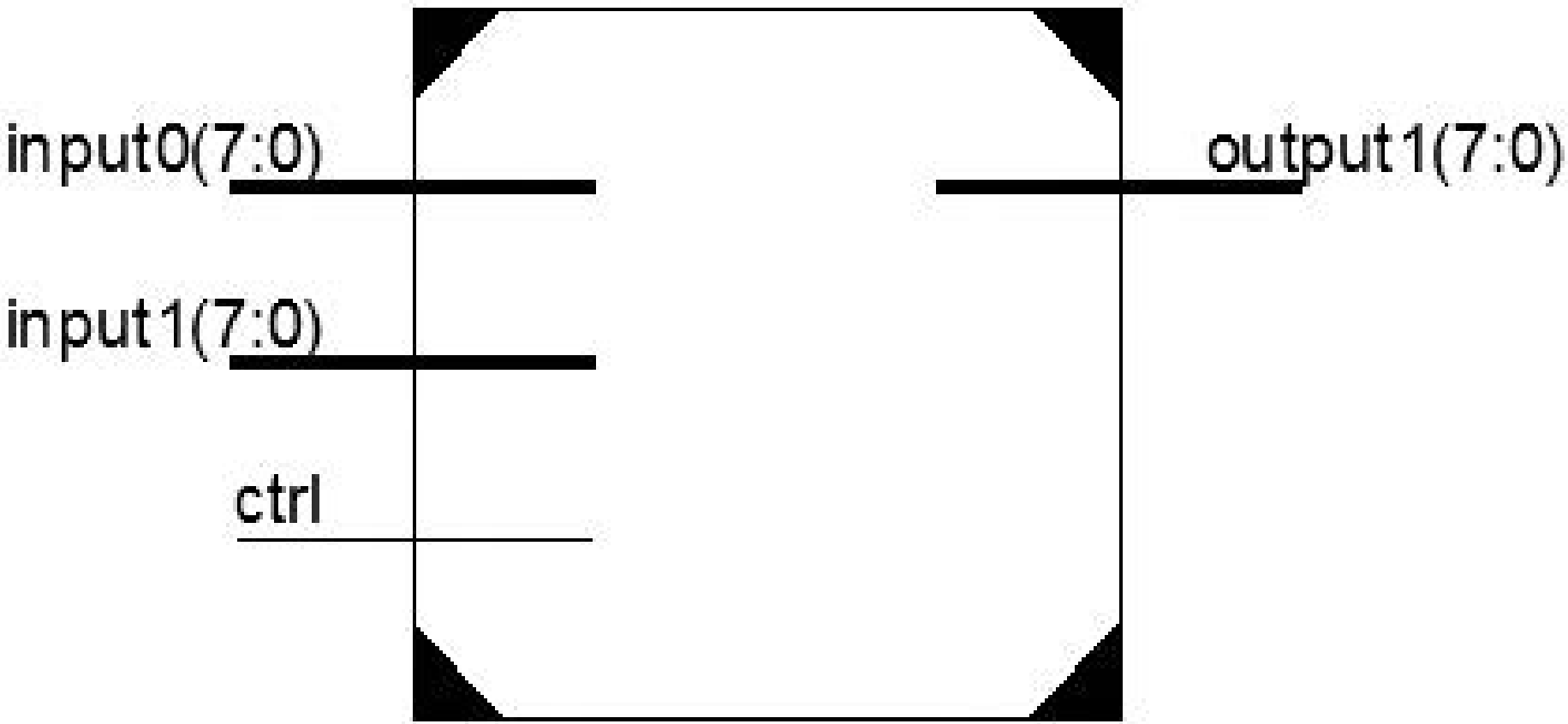
ctrl


instruction_reg
instruction_input(7:0)
instruction_to_control_unit(2:0)
i_immediate(1:0)
jump_opcode_check(1:0)
i_immediate(4:0)
rs(1:0)
rt(1:0)
funct
instruction_reg


memory
dataMemWrite(7:0)
input_addr(7:0)
pc(7:0)
memRead
memWrite
instructions(7:0)
readData(7:0)
memory

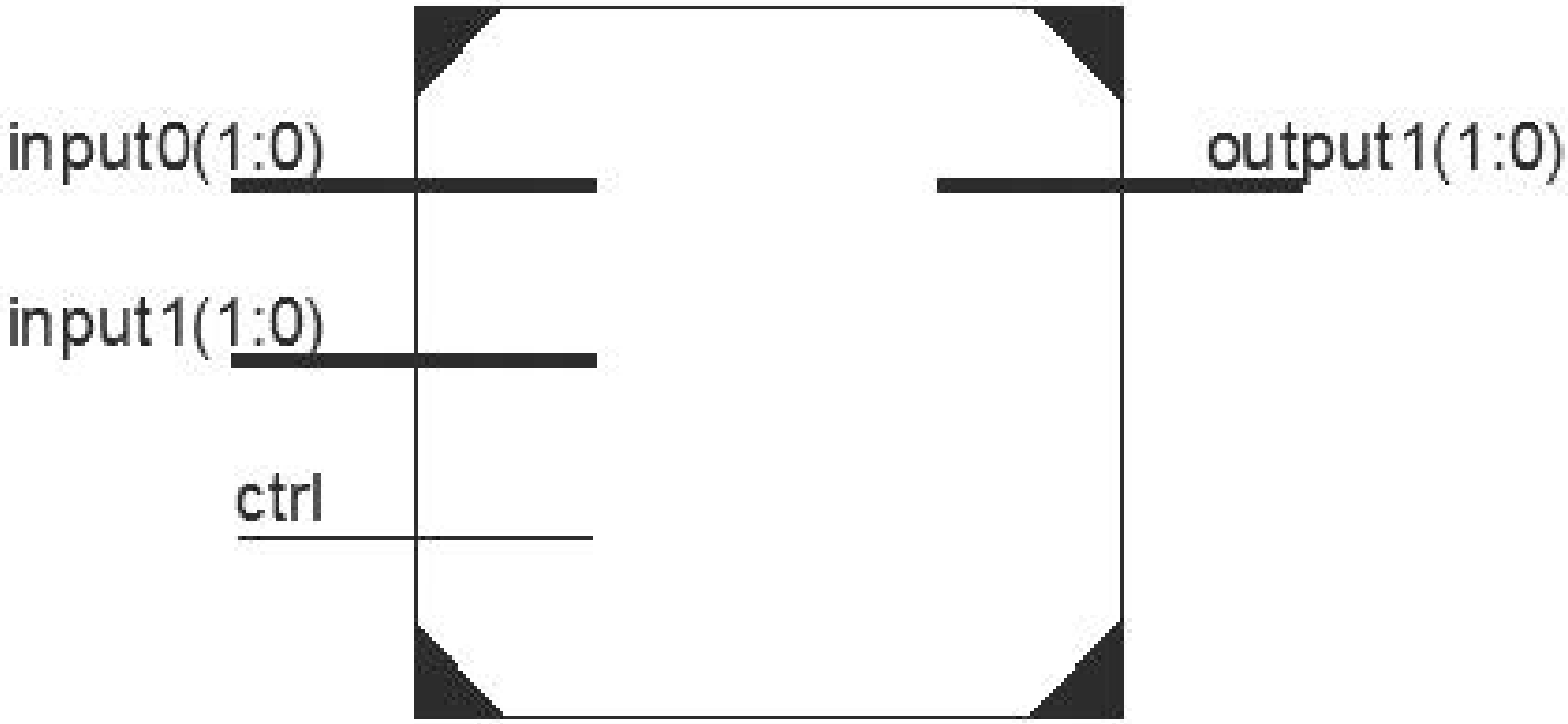

mux2_1_ctrl1
ctrl
output1
input0
input1
mux2_1_ctrl1

# mux2_1_ctrl1_in2

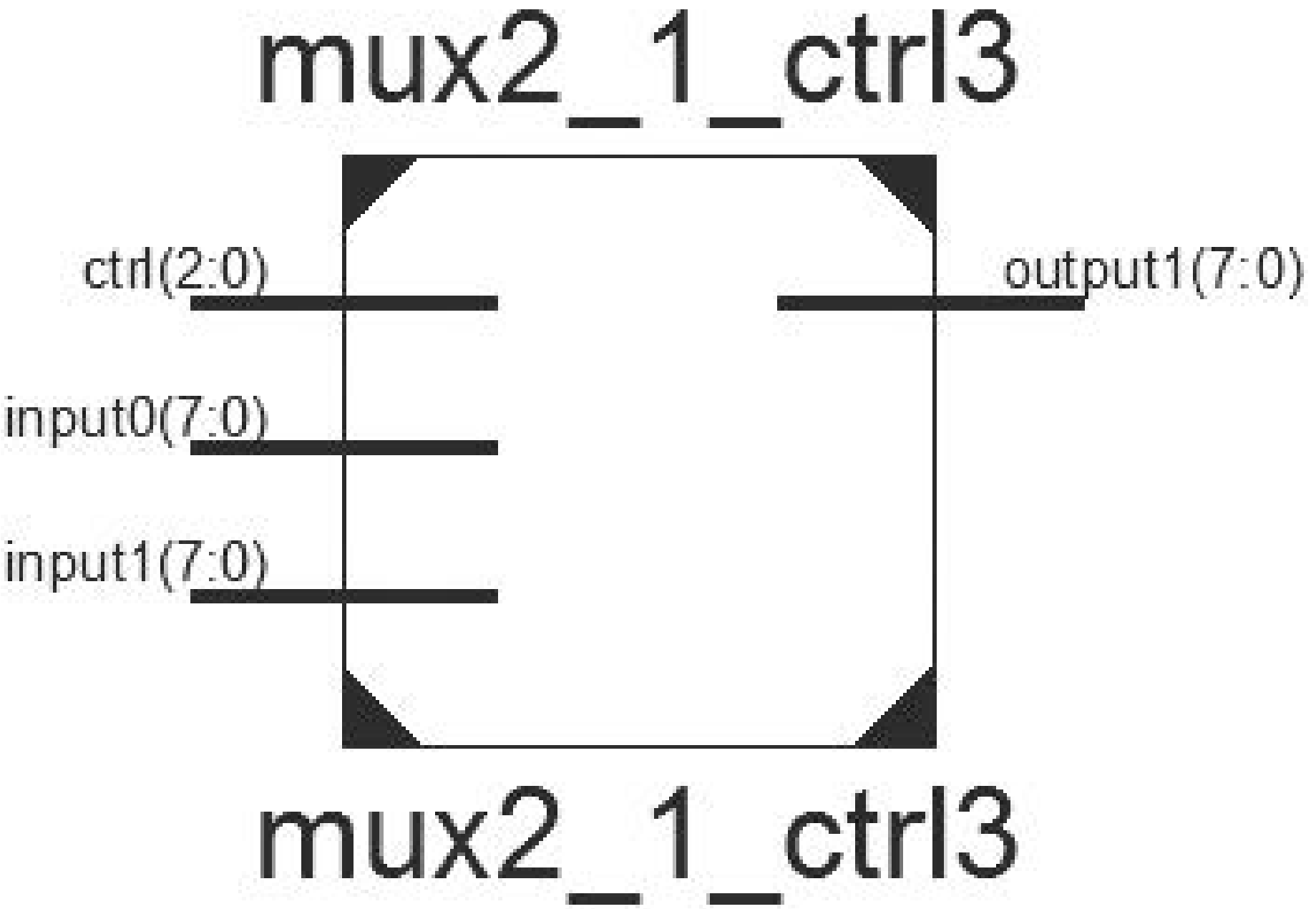


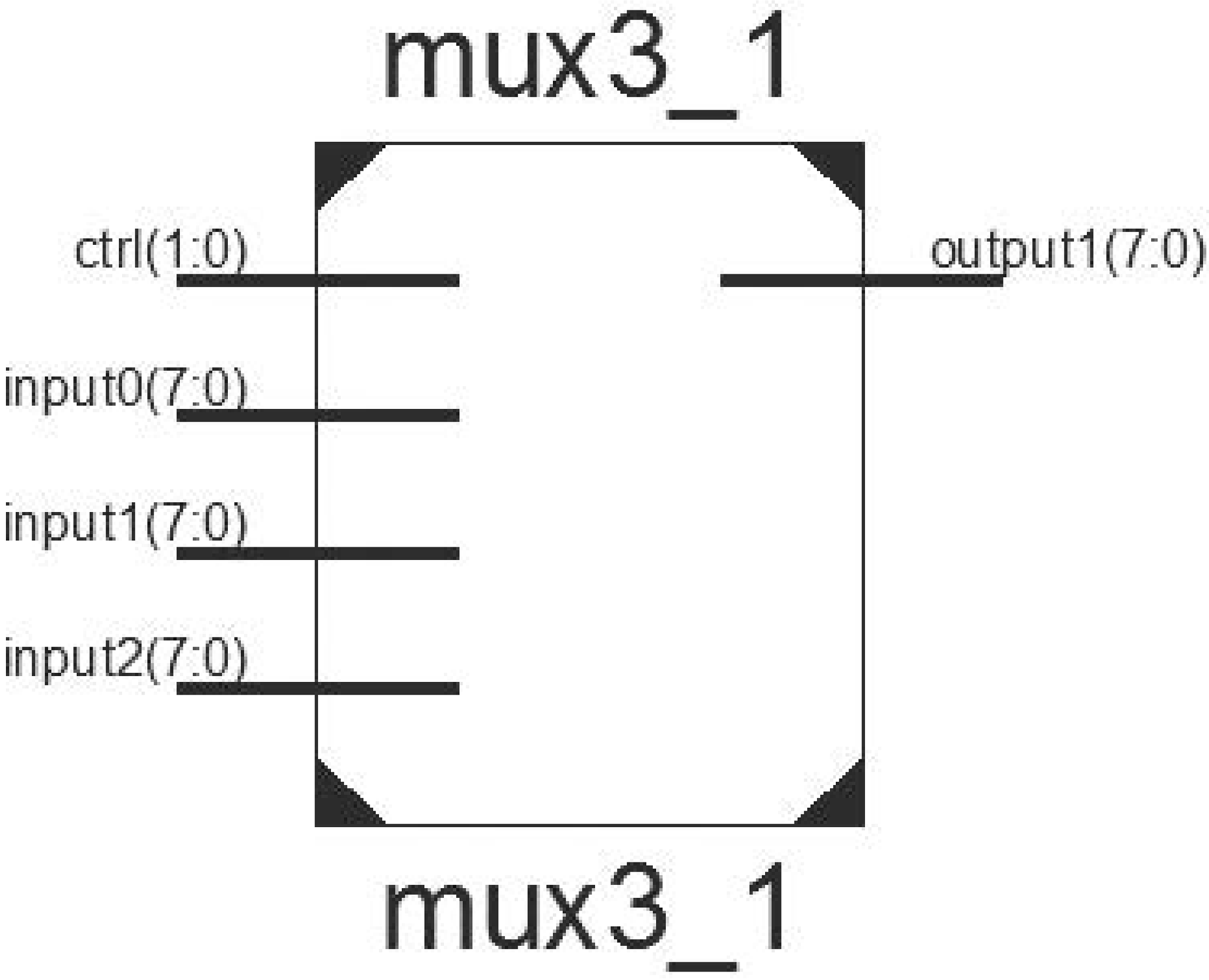

mux2_1_ctrl1_in2

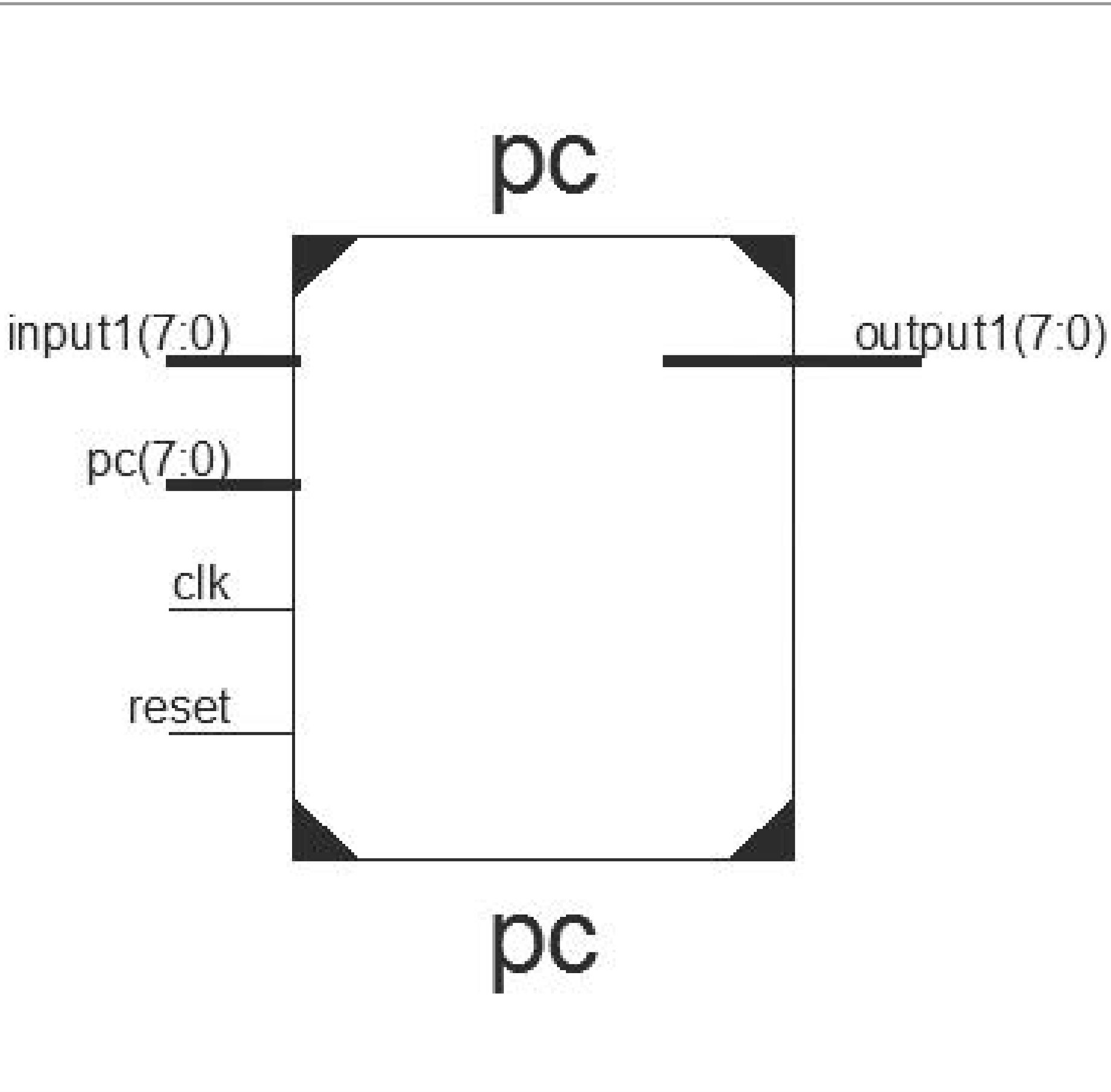
# mux2_1_ctrl1_out1

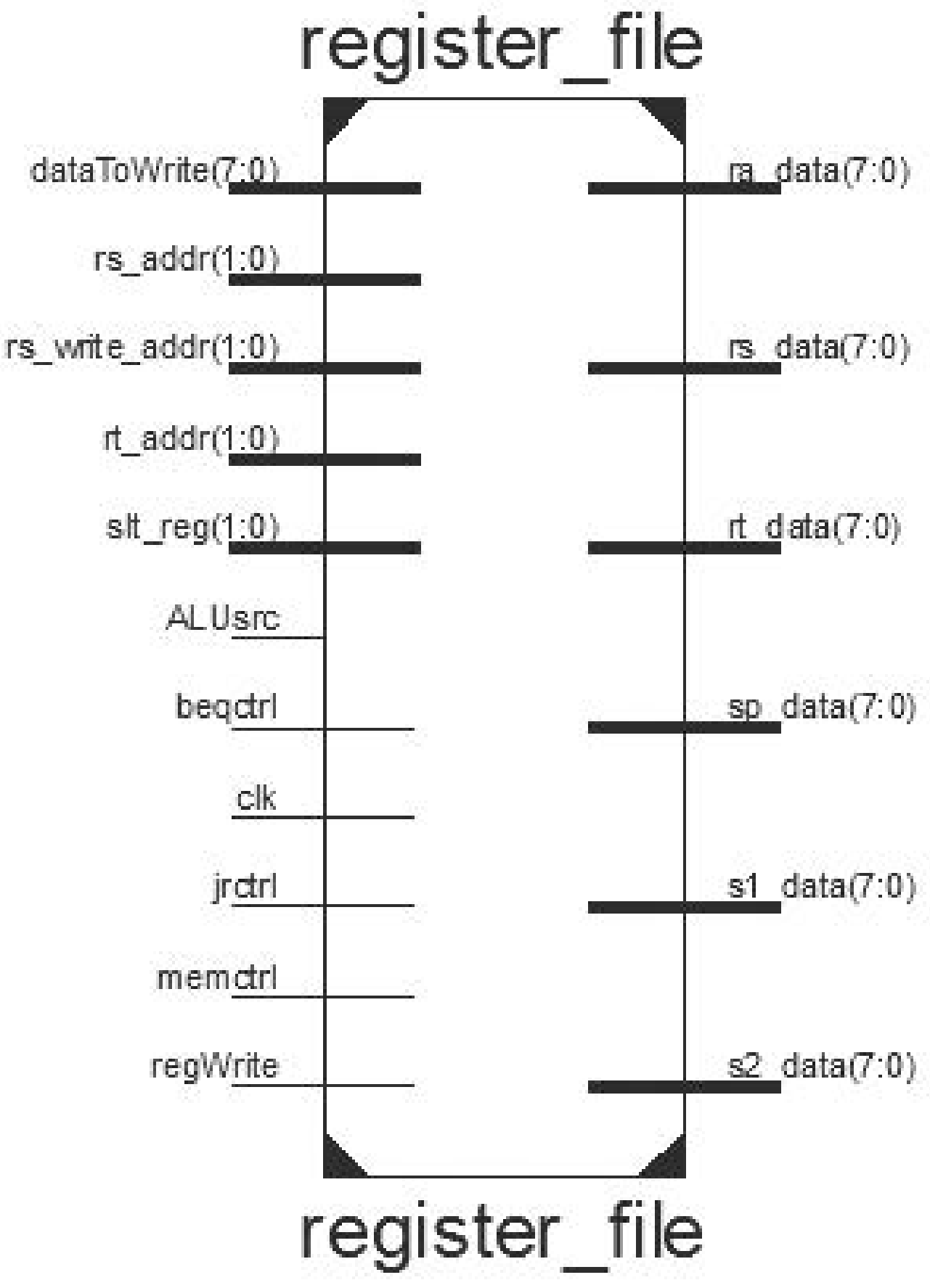


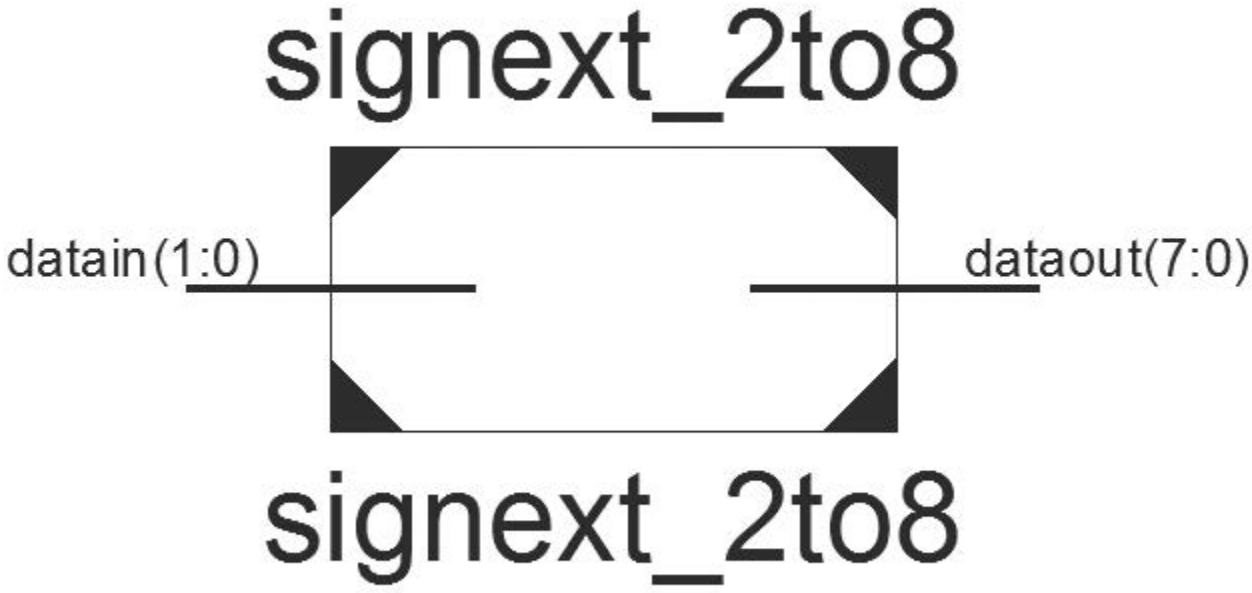

mux2_1_ctrl1_out1

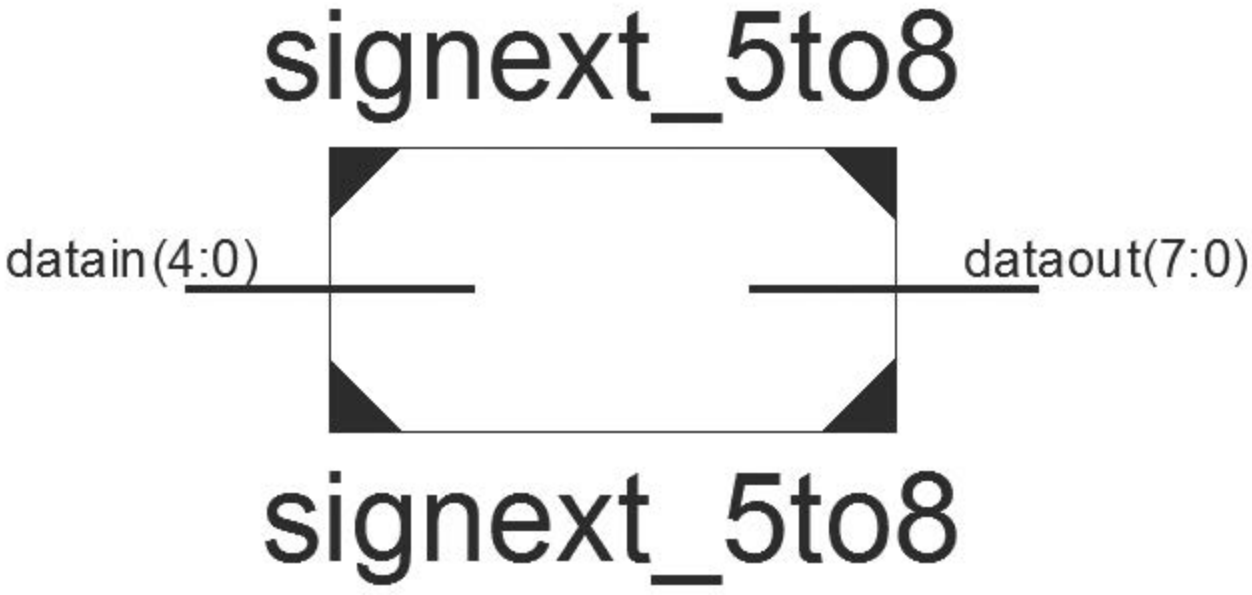

mux2_1_ctrl3
ctrl(2:0)
input0(7:0)
input1(7:0)
output1(7:0)
mux2_1_ctrl3


mux3_1
ctrl(1:0)
input0(7:0)
input1(7:0)
input2(7:0)
output1(7:0)
mux3_1


pc
input1(7:0)
output1(7:0)
pc(7:0)
clk
reset
pc


register_file
dataToWrite(7:0)
rs_addr(1:0)
rs_write_addr(1:0)
rt_addr(1:0)
slt_reg(1:0)
ALUsrc
beqctrl
clk
jrctrl
memctrl
regWrite
ra_data(7:0)
rs_data(7:0)
rt_data(7:0)
sp_data(7:0)
s1_data(7:0)
s2_data(7:0)
register_file


signext_2to8
datain(1:0)
dataout(7:0)
signext_2to8


signext_5to8
datain(4:0)
dataout(7:0)
signext_5to8