

Lab 8 - Op Amps I

Junior Projects II - ECE 394A

February 4, 2019

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Abstract

This experiment was conducted in order to gain an understanding Operational Amplifiers both intrinsically and when used in conjunction with different components in different setups. The operational amplifiers were studied to be used in an isolated environment and in larger circuits requiring any of its capabilities. In this experiment, eight different configurations of operational amplifiers were tested and measured to ascertain the benefits they may provide.

Introduction

The objective of the laboratory procedure is to build and analyze a set of op-amp circuits in practice, including an open-loop test circuit, an inverting amplifier, a non-inverting amplifier, a follower circuit, a current source, a current to voltage converter, a summing amplifier that provides a DC offset, and a push/pull buffer. Each of these circuits has its uniquely determined input and output impedances as well as voltage gain. By understanding the functionality of each stage of the aforementioned configurations, we seek to mitigate potential failures and undesired responses that might result from uncoordinated control of the inputs and resistances, while maintaining the advantages of each stage which can be beneficial for more complicated structures including, but not limited to, integrators, differentiators, and rectifiers in application.

Experiments

1 Lab 8.1 - Open-Loop Test Circuit

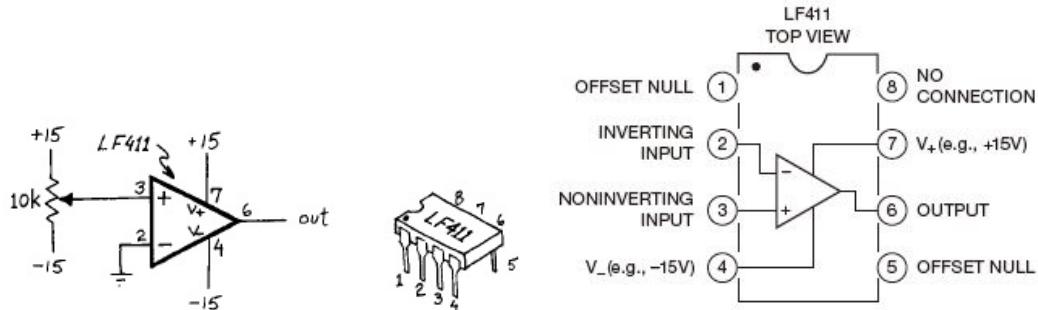


Figure 1: LF411 Op Amp Circuit and Pinouts

In this lab experiment, we show the consistency in the open loop gain of the operational amplifier as the potentiometer (10k) value is varied, which is at the input to the positive terminal of the op amp.

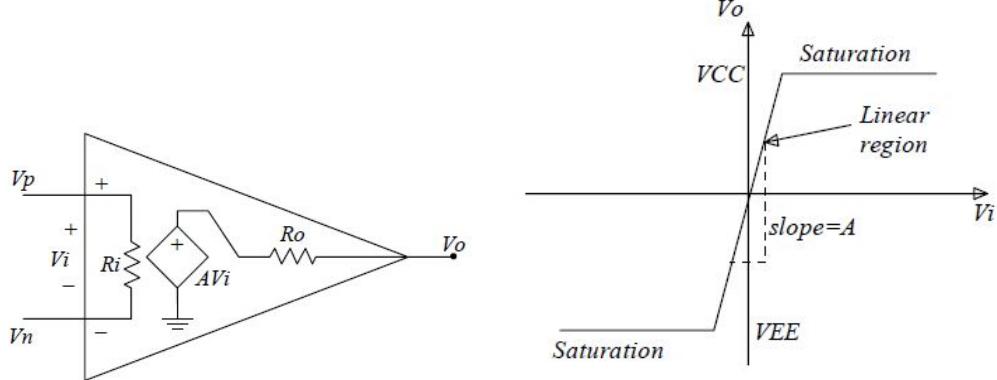


Figure 2: Equivalent Op Amp Circuit and I/O Voltage Graph

Open-loop Op Amp Circuit

An Operational Amplifier (Op-Amp) is a high gain amplifier that is powered using equal but opposite polarity voltage sources, as seen in Figure 1. Open loop Op-Amp circuit is a circuit with an operational amplifier without a feedback loop. The amplifier takes the difference between the two input signals, and amplifies the difference by an open-loop gain of A_o (Equation 1).

$$V_{out} = A_o V_{in} = A_o(V_+ - V_-) \quad (1)$$

Ideally, the open-loop gain is infinite, but for a real op-amp the gain is finite, typically about 10^5 , and it depends largely on frequency range. For a low frequency input, it takes on the maximum, while it decreases rapidly as the frequency is increased.

For an ideal op-amp, the input resistance looking into the input terminals is infinite, implying there is no current at the input. The output resistance, on the other hand, is ideally zero, making an op-amp ideal for driving low-resistance loads. In addition, an ideal op-amp has infinite bandwidth of operation and output voltage is zero when the difference of inputs is zero.

Throughout the experiments, we utilize a popular, all-around performer op-amp, LF411 silicon chip (Figure 1), which consists of 24 transistors, 11 resistors, and 1 capacitor, with pin connections as shown in Figure 1 [Art of Electronics, 225].

Components

- (1) 1 LF411 Op Amp
- (2) 10k Potentiometer
- (3) 1 Power Supply (for +15 V, -15 V, GND)
- (4) 1 DVM for voltage measurement

Assumptions

- (1) An op amp (LF411) goes into the breadboard in "dual in-line package" style.
- (2) An op amp always needs to be powered at two pins (+) and (-).
- (3) LF411 functionality does not deviate from the initial manufactured settings.

Simulation Results

An LTspice simulation was done using a subcircuit design of the LM411 chip (Appendix A). The potentiometer used in this section along with the whole lab had a linear wiper (Appendix B).

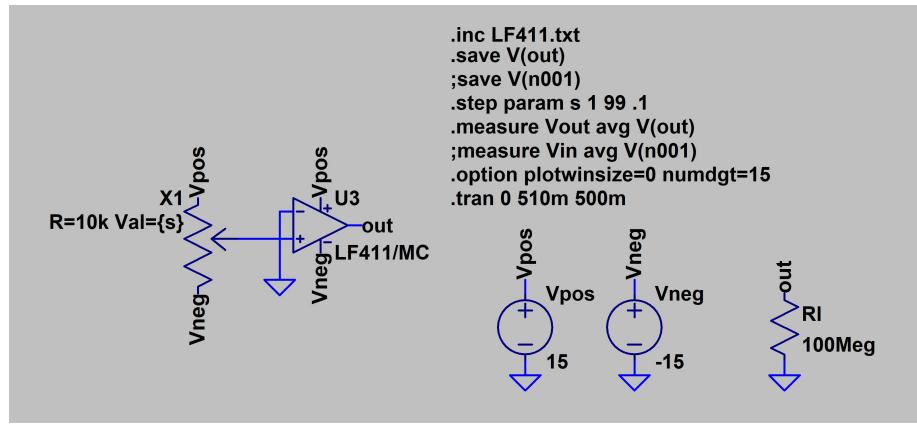


Figure 3: The Schematic of Lab 8.1 in LTSpice

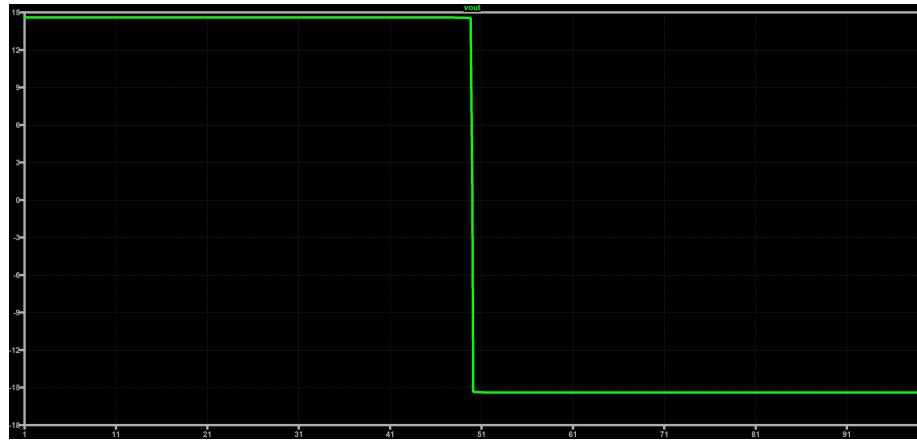


Figure 4: The sweep of the potentiometer and the voltage between the output of the op-amp and ground. The x-axis represents the percentage of the wiper position on the potentiometer.

Summary and Discussion

We expect the gain of the op amp to be infinitely high (maximum) for ideal op amps without an overall feedback in the circuit. The specification for LF411 has its gain = 200 V/mV, but in practical sense given a certain supply voltage, the output voltage can only be at the maximum of the power supply, which is +/- 15 Volts. As the collected data show, the highest (absolute) value it reaches at the output is limited by the voltage supplied to the op-amp.

Experimental Data

POT	Input	Output	Gain	Theoretical
lowest	15.0V	14.54 V	0.969	200
	9 mV	14.53 V	1614	
	-82 mV	-13.63 V	166	
highest	-13.046 V	-13.673 V	1.05	

Simulation Data

POT	Input	Output	Gain	Theoretical
lowest	14.7V	14.59 V	0.993	200
	307.22 nV	14.57 V	47.4M	
	-187.89 nV	1.26 V	6.71M	
	-307.22 nV	-15.38 V	50.1M	
highest	-14.69 V	-15.38 V	1.05	

The voltages gains found in both experimental and simulations demonstrate that the open-loop gain for the circuit is very high, except at extreme ends of the potentiometer resistances, in which case input and output matches in close identity (gain = 1).

2 Lab 8.2 - Inverting Amplifier

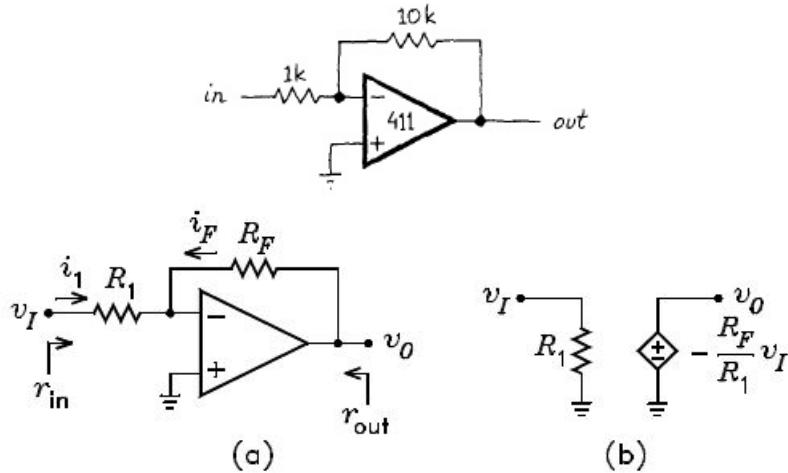


Figure 5: Inverting Amplifier

In this lab experiment, we demonstrate the limits of using an inverting amplifier by experimentally determining the gain, maximum output swing, and observing moments of deviation from the ideal response. Also we confirm the calculated input and output impedance values.

Inverting Amplifier Circuit

The circuit of interest is one with feedback configuration. Such feedback loop configuration decreases much of the gain A_o , but also provides an advantage of better controlling of the gain given the input signals. In this inverting op-amp circuit, the signal is input at the negative terminal, while the positive is grounded, giving an overall negative input difference voltage. For the circuit in Figure 5(a), the voltage at the inverting input is found by $v_- = -v_o/A$. For v_o finite and $A \rightarrow \infty$, it follows that $v_- \rightarrow 0$. Even though v_- is not grounded, it is referred to as a virtual ground because its voltage remains at ground potential (zero). Because $i_- = 0$, the sum of the currents at the negative terminal through the two resistors R_1 and R_F should be zero by KCL. From this relation, we obtain the voltage gain as shown in Equation 2.

$$\frac{v_o}{v_i} = -\frac{R_F}{R_1} \quad (2)$$

Impedance

The input resistance can be calculated from the relation $r_{in} = -\frac{v_i}{i_1}$. Because $v_- = 0$, it follows that $r_{in} = R_1$. The output resistance is equal to the output

resistance of the op-amp, such that $r_{out} = 0$. The equivalent circuit with these characteristics is shown in Figure 5(b).

Components

- (1) 1 LF411 Op Amp
- (2) 10k, 1k resistors
- (3) 1 Power Supply (for +15 V, -15 V, GND)
- (4) 1 DVM for voltage measurement
- (5) 1 Oscilloscope for wavegen, graphical output

Output

- (1) Gain: -10 V/V

The voltage gain with sinusoidal input driven with 0.1V at 1kHz and 100kHz showed no significant difference from the expected gain of -10 V/V; however, at high frequencies for the same input signal, the output voltage is observed to be lower than that at lower frequencies. The figure 6 shows that at the frequency of 1kHz, the output voltage is found to be 1.01V, while at 100kHz, 0.94V, approximately.

This fall in the gain roll-off is due to decrease in reactances of the capacitors within the op-amp model at high frequencies, which then causes shunt signal current paths and reduces the output voltage. In addition to a fall in the gain, the phase shift occurs simultaneously with respect to the input signal. It typically shifts by more than 180 degrees (typical at low frequencies) as the frequency increases to a higher range.

- (2) Maximum output swing

Figure 8 shows the maximum output swings just before and at the clipping off point. The yellow(output) fails to maintain a sinusoidal shape at the peak-to-peak voltage of approximately 2.75 V.

- (3) Linearity

As discussed in the difference in the op-amp gain, we observe some phase distortion present in the triangular wave input at high frequency, specifically at 100kHz as shown in Figure 9. At low frequencies, the inverting op-amp preserves the triangular wave shape of the input at the output terminal; however, at high enough frequency range, the sharp change in the triangular wave no longer appears and becomes a smoother curve due to distortions leading to non-linearity.

Impedances

- (1) Input

- Procedure: determine i_{in} and v_{in} by performing KCL analysis at v_- and v_{out} nodes of the op-amp.

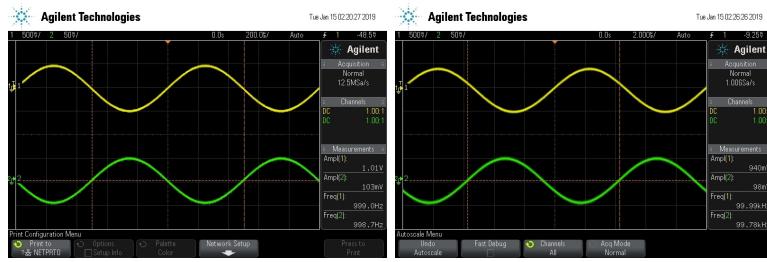


Figure 6: Gain with input of 100 mV at 1kHz and 100 kHz



Figure 7: Gain with triangular input of 100 mV at 1kHz and 100 kHz

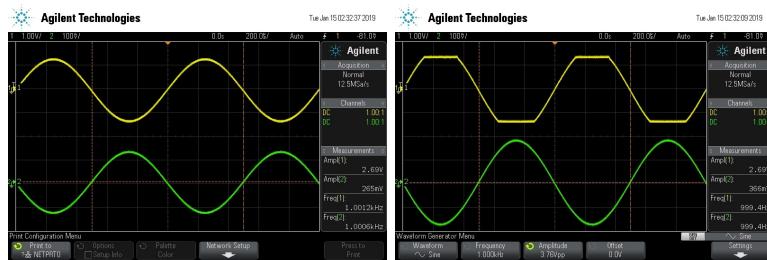


Figure 8: Maximum Output Swing just before and at clip-off point

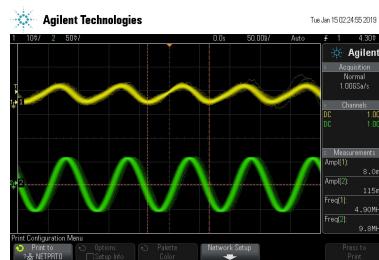


Figure 9: Deviation from linear behavior

KCL @ v_- :

$$i_{in} = \frac{v_-}{r_{in}} + \frac{v_- - v_{out}}{R_2}$$

KCL @ v_{out} :

$$0 = \frac{v_{out} - (-A_o v_-)}{r_o} + \frac{v_{out} - v_-}{R_2}$$

$$\frac{1}{R_{in}} = \frac{i_{in}}{v_{in}} = \frac{1}{r_{in}} + \frac{1 + A_o}{R_2(1 + \frac{r_o}{R_2})}$$

for $r_o = 0$ and $r_{in} = \infty$ if ideal, $R_{in} \approx \frac{R_2}{(1+A_o)} \approx R_1 = 1\text{k } \Omega$

Experimental value: $1.0001 \text{ k}\Omega$ (\approx theoretical value)

(2) Output

Procedure: find the relations among i_{out} , v_{out} , v_- by KCL at v_{out} and using the voltage divider equation.

KCL at v_{out} :

$$i_{out} + \frac{-A_o v_- - v_{out}}{r_o} + \frac{v_- - v_{out}}{R_2} = 0$$

Since $R_1 \parallel R_{in}$ and by voltage divider,

$$v_- = v_{out} \frac{\frac{R_1 r_{in}}{R_1 + r_{in}}}{\frac{R_1 r_{in}}{R_1 + r_{in}} + R_2}$$

$$\Rightarrow \frac{v_{out}}{v_{in}} = R_{out} = \frac{r_o(1 + \frac{R_2}{R_1} + \frac{R_2}{r_{in}})}{1 + \frac{R_2}{R_1} + \frac{R_2}{r_{in}} + A + \frac{r_o}{R_1} + \frac{r_o}{r_{in}}}$$

for $r_o = 0$ if ideal, $R_{out} \approx 0$

Experimental value: $32.58 \text{ }\Omega$ ($<<$ the input impedance); close to 0)

Simulation Results

The LF411 subcircuit design was used (Appendix A).

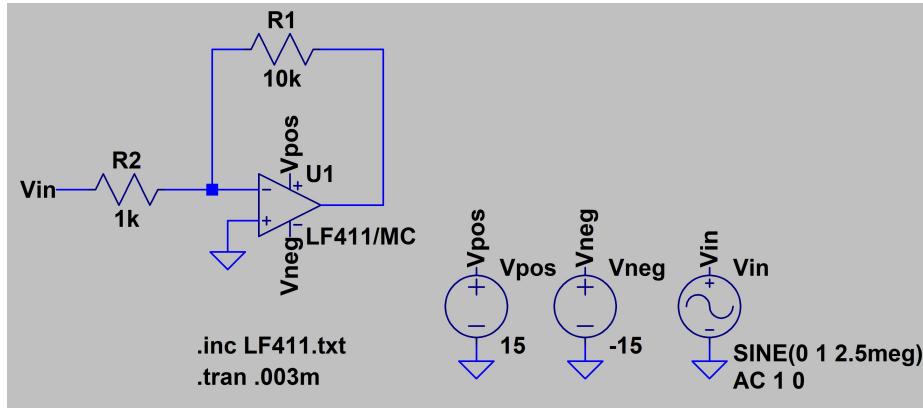


Figure 10: The Schematic of Lab 8.2 in LTSpice

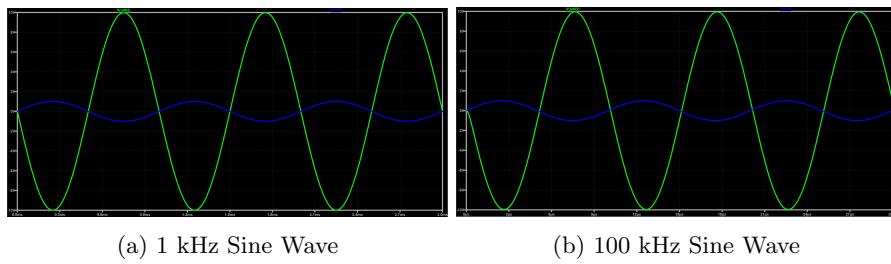


Figure 11: Sine wave applied to the input of the circuit to observe the gain

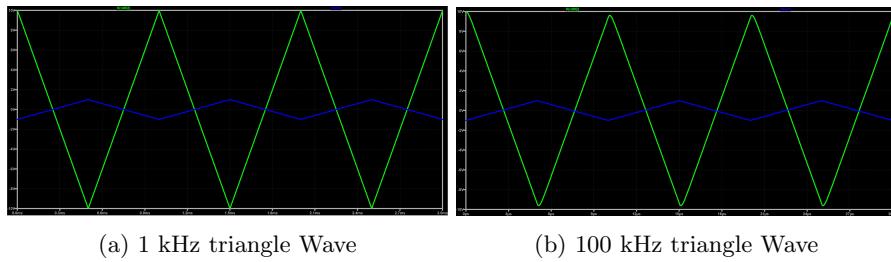


Figure 12: Triangle wave applied to the input of the circuit to observe the gain and linearity. At high frequencies, 100 kHz, the triangle wave at the output begins to round off.

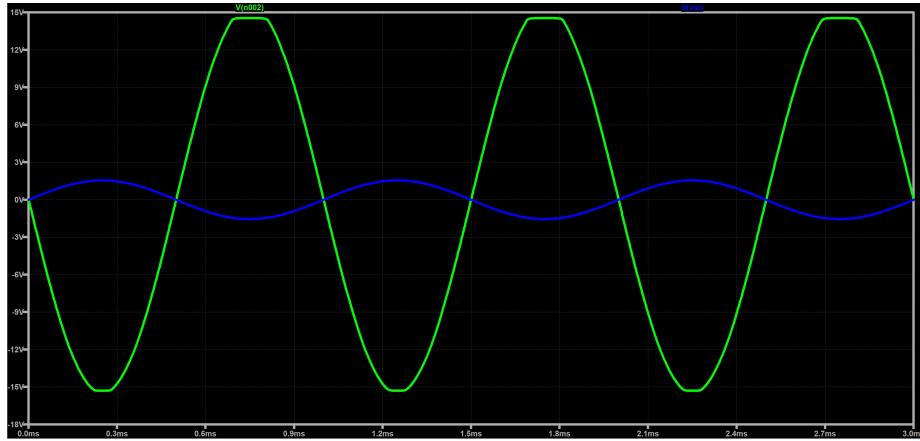


Figure 13: The waveform at the output to show maximum output swing. The max input voltage is different from the experimental value which was around 2.65V where as the simulation showed a max input voltage of 1.45 V

Summary and Discussion

	Input	Output	Gain
Experimental:	Sinusoidal 103 mV at 1 kHz	-1.01 V	-9.81
	Sinusoidal 98 mV at 100 kHz	-940 mV	-9.59
	Triangular 98 mV at 1 kHz	-980 mV	-10
	Triangular 98 mV at 100 kHz	-860 mV	-8.78

As the experimental (and simulation) data demonstrate, the output closely follows the calculated op-amp gain of -10 V/V, whereas at higher frequency ranges the gain starts to decrease relative to that at lower ranges. At higher frequencies, the capacitors in the op-amp unit tend to be shorted, causing greater phase shifts, thereby decreasing the overall output voltage and showing the presence of distortions through the oscilloscope.

3 Lab 8.3 - Non-inverting Amplifier

In this lab experiment, we note the difference from an inverting amplifier (8.2) by experimentally determining and comparing the voltage gain, input and output impedance values.

Non-inverting Amplifier Circuit

Non-inverting op-amp is in similar configuration as an inverting op-amp, with the input signal directly applied to the positive (+) terminal, such that the output signal is in-phase with the input signal. Feedback control of the circuit is managed by application of feeding the output signal through the voltage-divider network. In this closed-loop configuration, the circuit achieves stability and high input impedance (as $r_{in} \rightarrow \infty$, $i_{in} \rightarrow 0$ at the positive terminal and a

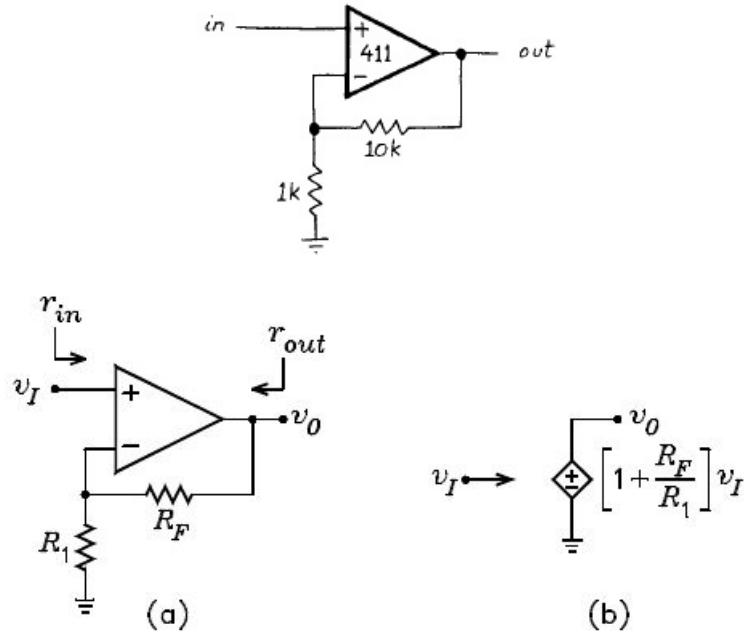


Figure 14: Non-inverting Amplifier

low output impedance.)

Components

- (1) 1 LF411 Op Amp
- (2) 10k, 1k resistors
- (3) 1 Power Supply (for +15 V, -15 V, GND)
- (4) 1 DVM for voltage measurement
- (5) 1 Oscilloscope for wavegen, graphical output

Output

- (1) Gain: 11 V/V
 $v_{in} = \frac{R_1}{R_1+R_2} v_{out}$, $A_o = \frac{v_{out}}{v_{in}} = 1 + \frac{R_2}{R_1}$, where $R_1 = 1\text{k}\Omega$, $R_2 = 10\text{k}\Omega$

Impedances

- (1) Input

- Procedure: determine i_{in} and v_{in} by performing KCL analysis at v_- and v_{out} nodes of the op-amp.

KCL @ v_- :

$$i_{in} = \frac{v_+}{R_1} + \frac{v_+ - v_{out}}{R_2}$$

KCL @ v_{out} :

$$0 = \frac{v_{out} - (A_o v_{in})}{r_o} + \frac{v_{out} - v_+}{R_2}$$

Substitute

$$v_+ = v_{in} + r_{in} i_{in}$$

Simplifies to

$$\frac{v_{in}}{i_{in}} = R_{in} = \frac{R_2(1 + \frac{r_{in}}{R_1} + r_{in}(1 + A))}{1 + \frac{R_2}{R_1}}$$

for $r_o = 0$ and $r_{in} = \infty$ if ideal, $R_{in} \approx \infty$

- Experimental value: $13.13 \text{ G}\Omega \approx \infty$

(2) Output Procedure: find the relations among i_{out} , v_{out} , v_- by KCL at v_{out} and using the voltage divider equation.

KCL at v_{out} :

$$i_{out} + \frac{-A_o v_+ - v_{out}}{r_o} + \frac{v_+ - v_{out}}{R_2} = 0$$

Since $R_1 \parallel R_{in}$ and by voltage divider,

$$v_+ = v_{out} \frac{\frac{R_1 r_{in}}{R_1 + r_{in}}}{\frac{R_1 r_{in}}{R_1 + r_{in}} + R_2}$$

\Rightarrow

$$\frac{v_{out}}{v_{in}} = R_{out} = \frac{r_o(1 + \frac{R_2}{R_1} + \frac{R_2}{r_{in}})}{1 + \frac{R_2}{R_1} + \frac{R_2}{r_{in}} + A + \frac{r_o}{R_1} + \frac{r_o}{r_{in}}}$$

for $r_o = 0$ if ideal, $R_{out} \approx 0$

- Experimental value: $32.49 \Omega \approx 0$ (in relative term)

Simulation Results

The LF411 subcircuit design was used (Appendix A).

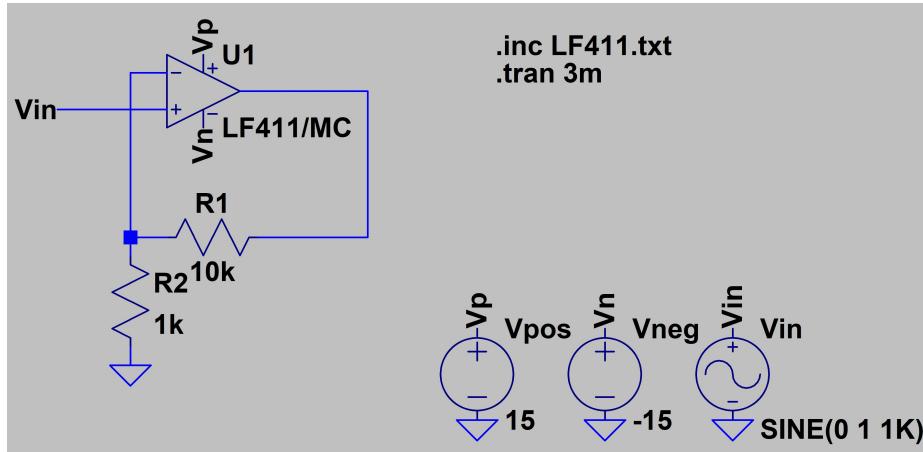


Figure 15: The Schematic of Lab 8.3 in LTSpice

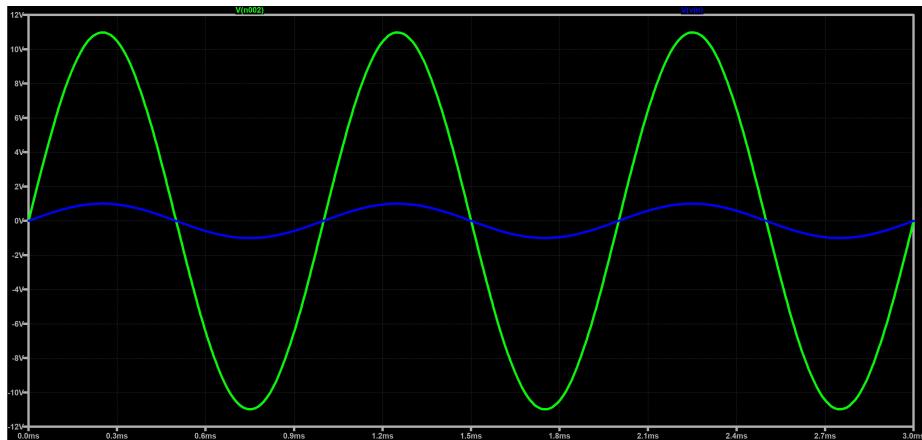


Figure 16: The Input, 1 kHz sine wave, and Output of the Non-inverting Amplifier

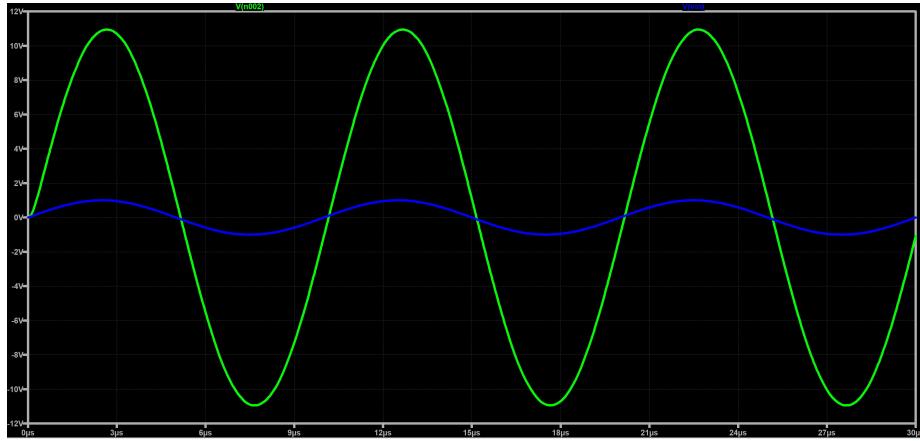


Figure 17: The Input, 100 kHz sine wave, and Output of the Non-inverting Amplifier

Summary and Discussion

	Input	Output	Gain
Experimental:	Sinusoidal 105 mV at 1 kHz	1.15 V	10.95
	Sinusoidal 993 mV at 100 kHz	10.95 V	11.03

Summary of results

The experimentally determined voltage gains for this non-inverting amplifier confirm the calculated gain of 11 V/V. The input and output impedances, in relative term, follow the theoretical values as well. The input impedance differs from the previously discussed inverting amplifier because the input is fed into a different terminal of the op-amp (positive in this part) and the amplification level is maintained, with a different sign.

4 Lab 8.4 - Follower

In this lab experiment, we aim to demonstrate the use of an op amp follower circuit. In particular, we experimentally determine and confirm the calculated input and output impedance values.

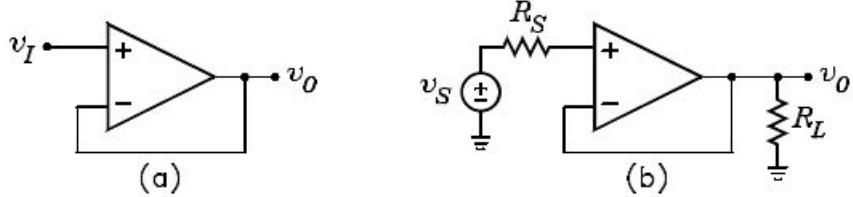


Figure 18: Follower

Op Amp Follower Circuit

Voltage follower circuit as shown in Figure 18 is simply a unity-gain buffer circuit with an op-amp. This is realized by setting the feedback resistor to zero and the input resistor to infinity in an inverting amplifier. One of the advantages to this configuration is its utility when impedance matching or circuit isolation is more important than amplifying the signal, since this maintains the signal voltage. The input impedance of a follower is typically very high and output low, assuming ideal conditions.

Components

- (1) 1 LF411 Op Amp
- (2) 1 Power Supply (for +15 V, -15 V, GND)
- (3) 1 DVM for voltage measurement

Output

- (1) Gain: 1 V/V

$$v_{out} = v_{in} \left(\frac{R_L}{R_s + R_L} \right)$$

Follower is Figure 4(b) with $R_s = R_L = 0$, so $v_{out} = v_{in}$

Impedances

To determine the input/output impedances, we attach a test source v_s and two resistors at each end R_s, R_L , respectively, as in Figure 18(b).

(1) Input

Procedure: connect a test source to input, and compute the input current using KCL in the equivalent circuit, such that $R_{in} = \frac{v_{test}}{i_{test}}$. Ideally, this is close to ∞ . When this was conducted experimentally, the input voltage was measured and by using the voltage divider equation, the intrinsic input impedance of the operation amplifier was revealed. In this case, the measured voltage was 0.001 V with a 10M resistor which yielded an intrinsic resistance of 5E11.

(2) Output

Procedure: connect a test source to output, and compute the output current using KCL in the equivalent circuit, such that $R_{out} = \frac{v_{test}}{i_{test}}$. Set input voltage to zero, and ignore the load resistance. Ideally, this is close to 0. When attempting

to solve for the intrinsic output impedance it is important to note that since the impedance is very low it will be difficult to find the true value.

Impedance	Input	Output
Theoretical	∞	0
Experimental	5E11	32.58
Simulated	13.13009 G Ω	32.583644 Ω

- As we expected, the experimental and simulated data confirm that the input impedance is of high order and the output is relatively very small, which behaves like an ideal op-amp.

Simulation Results

The LF411 subcircuit design was used (Appendix A).

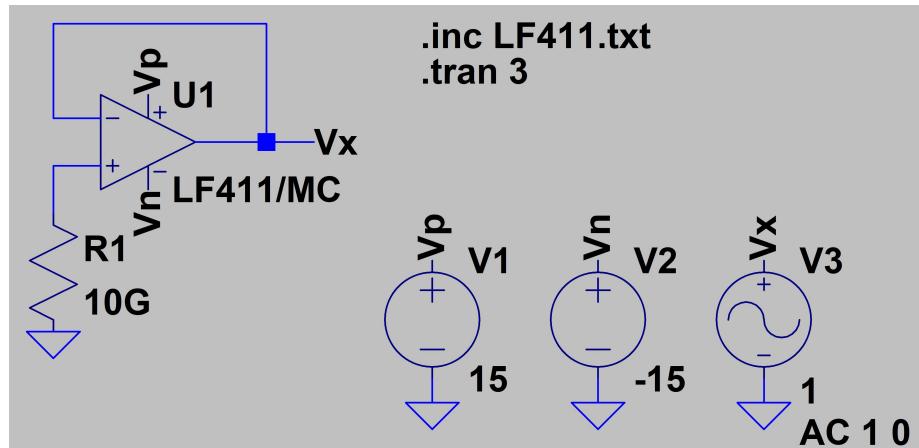


Figure 19: The Schematic of Follower Op-Amp in LTspice

The V_x net was applied to both the input and output in two separate runs. The trace, V_x/I_x was plotted and showed a horizontal line which was the input and output impedances.

Summary and Discussion

The input and output impedance values from the experiment and simulations demonstrate that the op-amp does behave in an ideal like manner, with infinite impedance at the input and nearly 0 at the output. Modeling the follower op-amp circuit as in Figure 18 with the resistances of 0, the experimental gain (≈ 1) does confirm close identity of the input to the output signals.

5 Lab 8.5 - Current Source

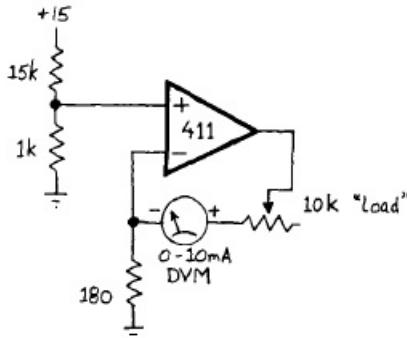


Figure 20: Current Source with Floating Load

In this lab experiment, we note the difference from an inverting amplifier by experimentally determining the voltage gain, input and output impedance values.

Current Source Op Amp Circuit

To build a current source using an op-amp, we employ a floating load as in Figure 20 with a current sensing resistor (connected to ground; placed at the emitter of the transistor). The current sensing resistor is placed in the feedback loop along with the floating load (= resistor at the collector of the transistor) into the negative input terminal of the op-amp. In this configuration, the circuit maintains the current at a relatively constant value regardless of the voltage drop across the load.

Components

- (1) 1 LF411 Op Amp
- (2) 15k, 1k, 180, 470, 2.7k, 12k, 10k (POT) resistors
- (3) 1 BJT(2N3906), 1 MOSFET(BS250P)
- (4) 1 Power Supply (for +15 V, -15 V, GND)
- (5) 1 DVM for voltage measurement
- (6) 1 Oscilloscope for wavegen, graphical output

Output

- (1) Current

BJT: 2N3906 (PNP) / MOSFET: BS250P (P-MOS; replacement for VP01)
(The MOSFET yields a more linear behavior than the BJT)

Vc	BJT		MOSFET		I_{out}
	Ve	I_{out}	Vd	Vs	
59.57 mV	12.45 V	5.64 mA	14.405 V	12.44 V	1.47 mA
12.496 mV	12.42 V	1.26 mA	12.42 V	12.44 V	5.72 mA
12.274 mV	12.4 V	5.7 mA			

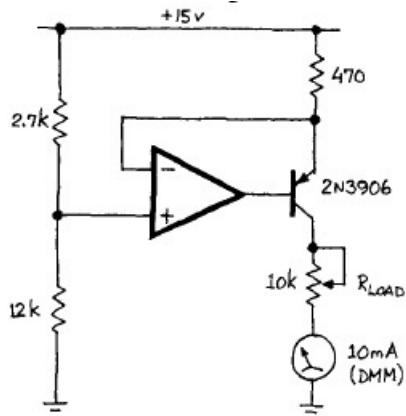


Figure 21: Current Source with load returned to ground

Simulation Results

The LF411 subcircuit design was used (Appendix A). The 10k linear potentiometer was used (Appendix B).

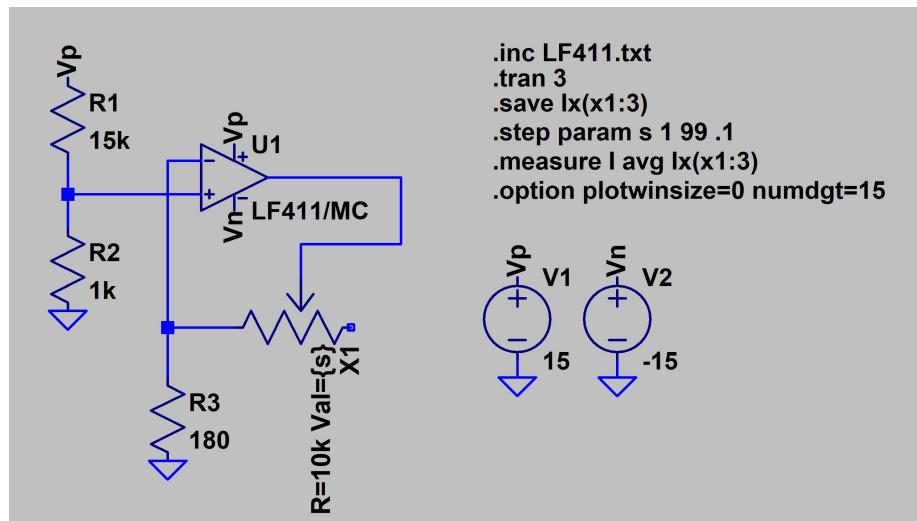


Figure 22: The Schematic of Lab 8.5 in LTSpice.

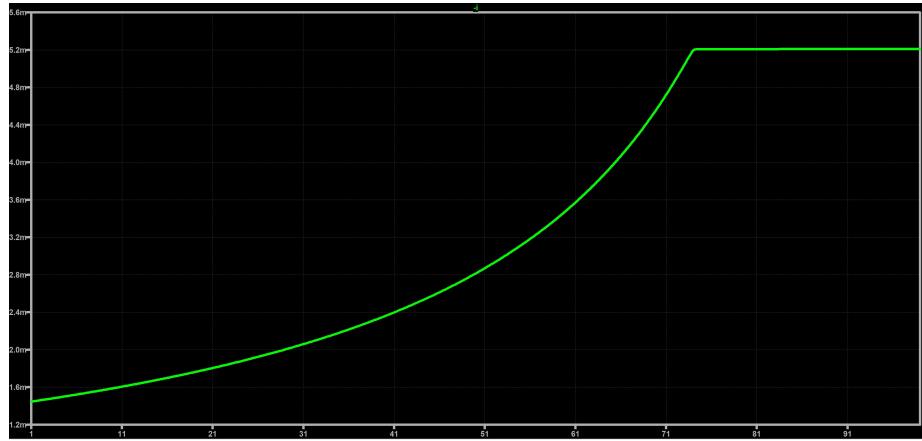


Figure 23: A sweep of the various potentiometer wiper percentages was taken and the current was measured at each.

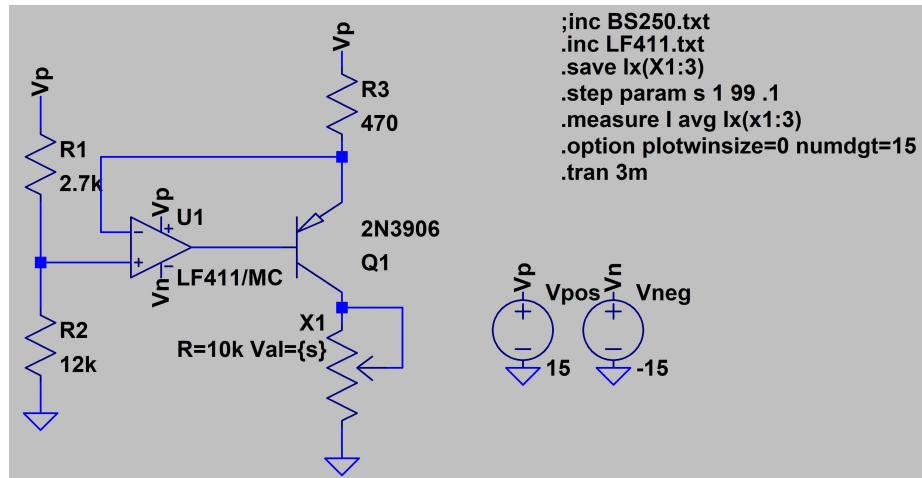


Figure 24: The Schematic of Lab 8.5 in LTSpice with the BJT alteration

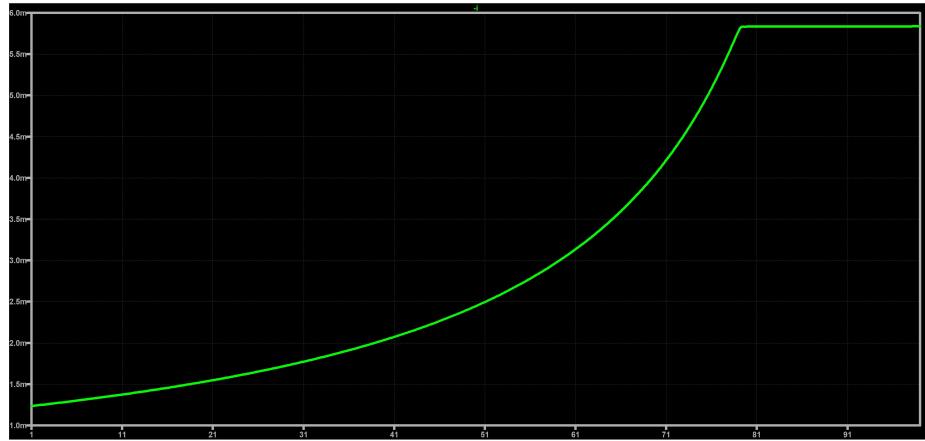


Figure 25: A sweep of the various potentiometer wiper percentages was taken with the BJT modification and the current was measured at each.

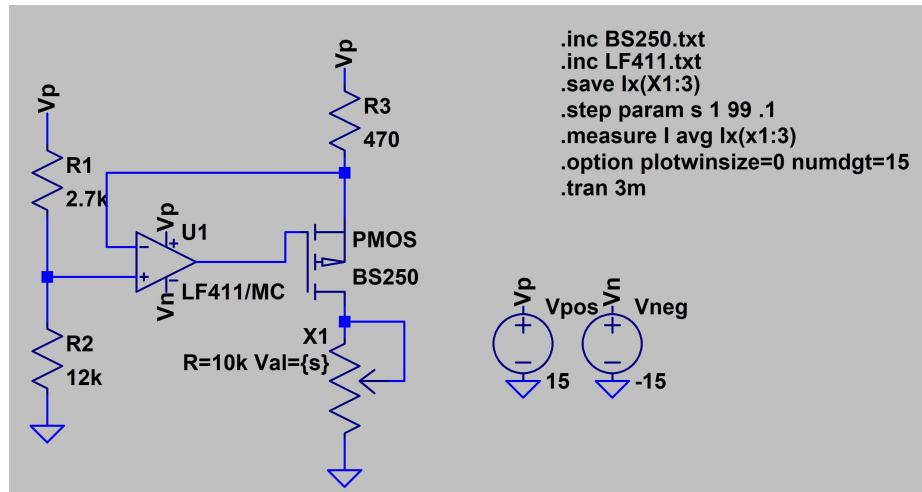


Figure 26: The Schematic of Lab 8.5 in LTSpice with the MOSFET alteration

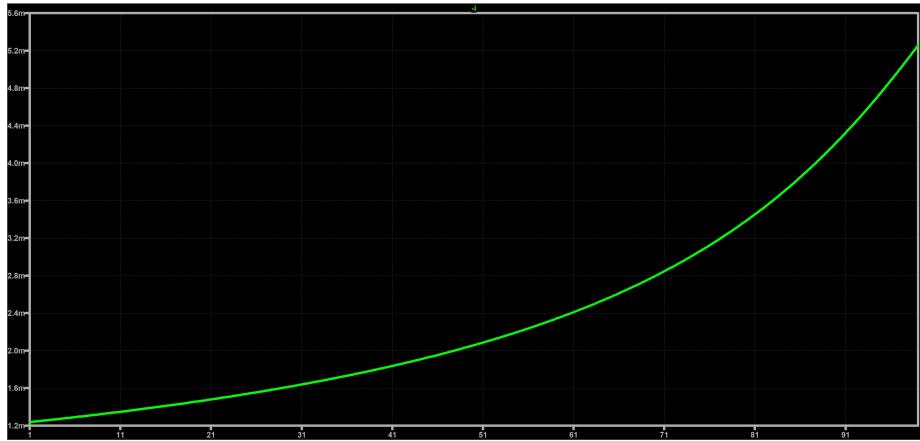


Figure 27: A sweep of the various potentiometer wiper percentages was taken with the MOSFET modification and the current was measured at each.

Summary and Discussion

Simulation Data	Observed range until clipping off [mA]
(1) With floating load (Figure 20)	1.5 - 5.2
(2) BJT (PNP) (Figure 21)	1.3 - 5.75
(3) MOSFET (P-MOS)	1.2 - 5.2

The simulation of lab 8.5 shows that the circuit using a MOSFET performs better as a current source, because the Figure 27 does not level off and changes constantly with the increasing resistance. While the currents for all three configurations fall in the similar observed range (in the order of [mA]), (1) and (2) exhibit some constant current past a certain wiper level for resistance. Through the experimental current data, we confirmed relatively small variations in the current with as the resistance from the potentiometer is varied.

6 Lab 8.6 - Current to Voltage Converter (b)

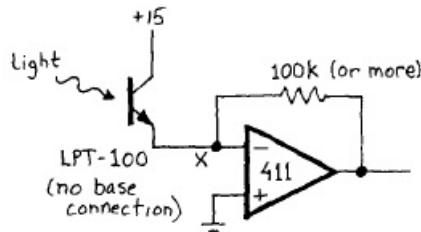


Figure 28: Current to Voltage Converter (Phototransistor)

In this lab experiment, we seek to observe changes in the voltage at the summing junction as the amount of light on the phototransistor varies. We chose to experiment with a phototransistor because LPT-100 device in the inventory only had the type without base connection.

Phototransistor

A phototransistor is a transistor with its base not connected; it is left disconnected for the light to enable current to flow through it. As the light strikes the base region, it causes hole electron pair generation in the reverse-biased base-collector region. These pairs move through the electric field, thereby providing a base current and causing electrons to be injected into the emitter. In comparison with photodiodes, phototransistors are more sensitive to the (current) gain of the transistor, allowing for more applications.

Components

- (1) 1 LPT-100
- (2) 1 LF411 Op amp
- (3) 100k Potentiometer
- (4) 1 Power Supply (for +15 V, -15 V, GND)
- (5) 1 DVM for voltage and current measurement

Simulation Results

The LF411 subcircuit design was used (Appendix A). Since a phototransistor could not be simulated in LTSpice properly, a voltmeter with incrementals steps was applied to the base. This would simulate different light levels on the LPT-100 phototransistor

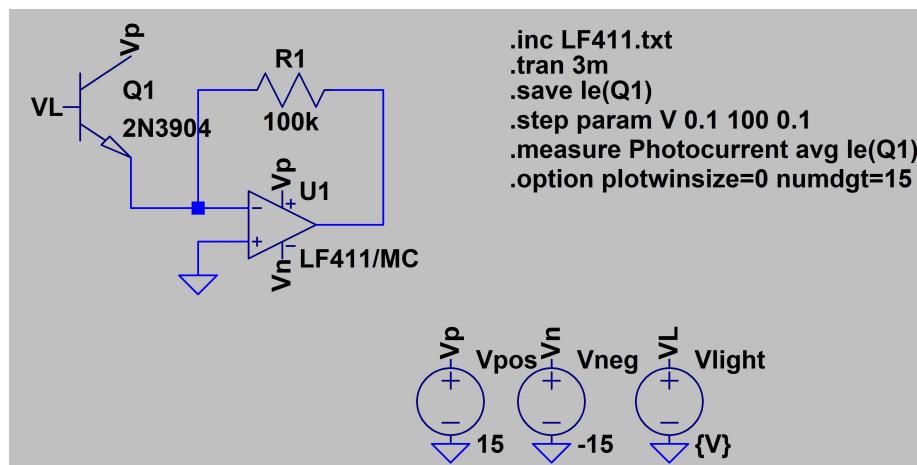


Figure 29: The Schematic of Lab 8.6 in LTSpice.

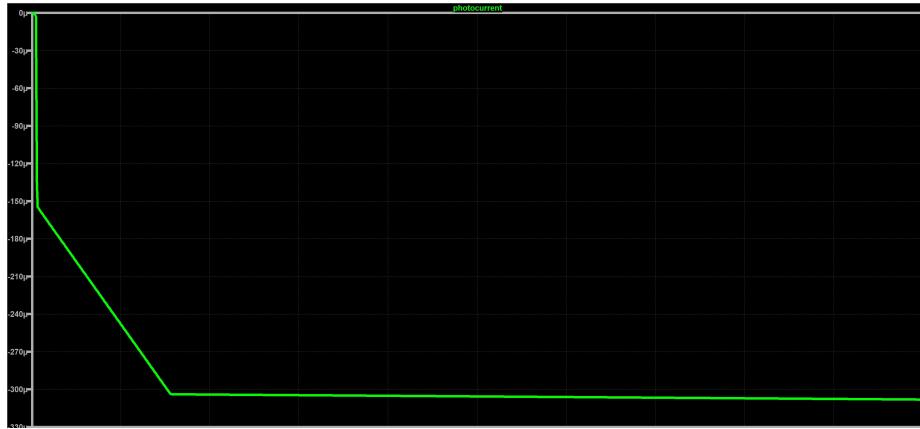


Figure 30: The current from the "phototransistor" was plotted against the voltage levels applied to the base

Summary and Discussion

Condition	Current	Voltage at summing junction
No(bare) Light	0.006 mA	17 mV
Ambient Light (Lab)	0.141 mA	470 mV
Flashlight	0.288 mA	14.96 V

We observe that as more light is shone onto the base of the phototransistor (LPT-100), the voltage at the summing junction increases as a result of the increase of the photocurrent.

7 Lab 8.7 - Summing Amplifier

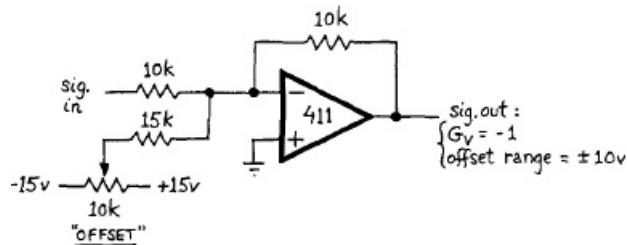


Figure 31: Summing Amplifier

In this lab experiment, we demonstrate a way of adding a DC offset to a signal using a summing op amp circuit.

Summing Amplifier Circuit

A summing amplifier is simply a(n) (non-)inverting amplifier with multiple DC

input signals that add up at the output signal. For the inverting and non-inverting op-amp configurations the superposition of the input voltages is found by the Equation 3. In this section, we experiment with the inverting op-amp configuration and a varying resistance to observe the effect on the output voltage signal.

$$v_{out} = \sum -\frac{R_F}{R_i} v_i \text{ for inverting} \quad (3)$$

$$v_{out} = (\sum -\frac{v_i}{R_i})(R_i \parallel R_j)(1 + \frac{R_F}{R_{v_-}}) \text{ for non-inverting}$$

Components

- (1) 1 LF411 Op Amp
- (2) 10k, 15k resistors
- (3) 1 Power Supply (for +15 V, -15 V, GND)
- (4) 1 DVM for voltage measurement
- (5) 1 Oscilloscope for wavegen

Simulation Results

The LF411 subcircuit design was used (Appendix A). The 10k linear potentiometer was used (Appendix B).

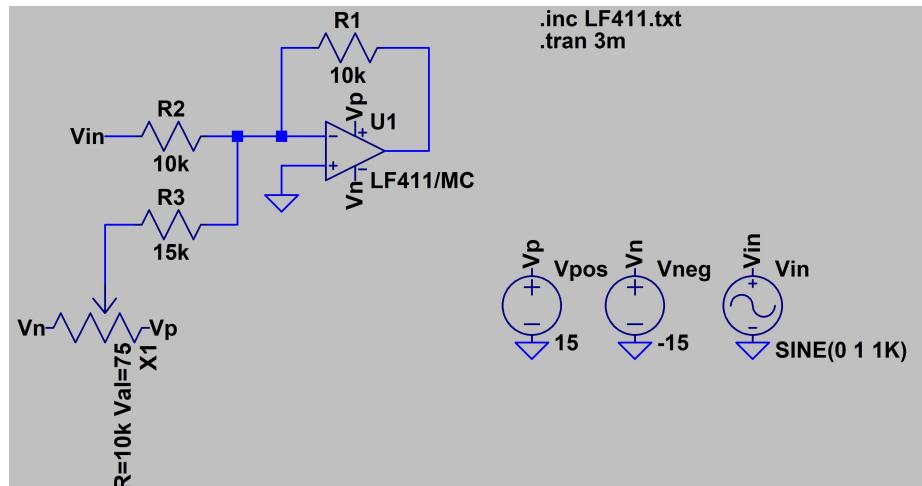


Figure 32: The Schematic of Lab 8.7 in LTSpice.

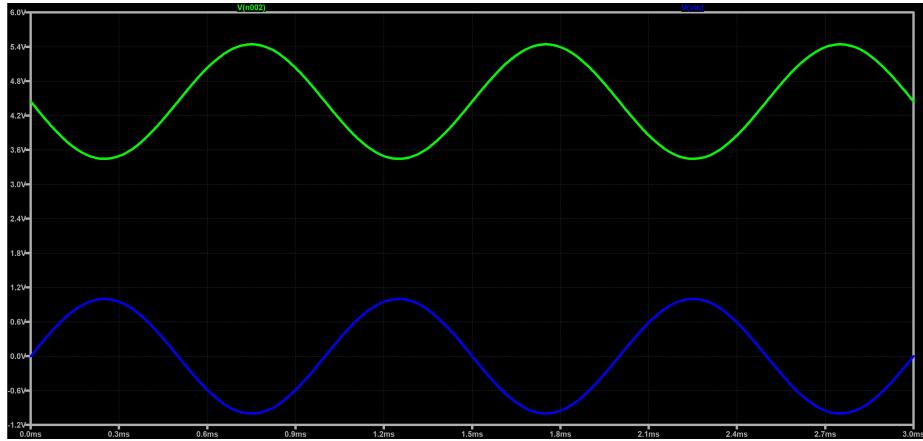


Figure 33: The waveform showing the effect of having the wiper at 75% and the offset on the input wave.

Summary and Discussion

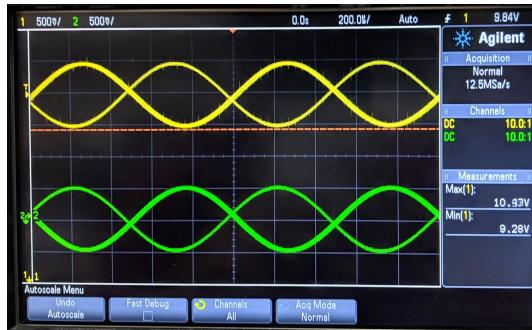


Figure 34: Output signal with DC offset

Input signal: 1.0 V sinusoidal at 1 kHz (Gain without offset = -1 V/V)

POT(10k)	Output Range	Offset Range
Min	-10.72 to -9.50 V	-9.72 to -8.50 V
Max	9.48 to 10.63 V	10.48 to 11.63 V

With 10k ohm potentiometer, we expect an offset of +/- 10V at the output as seen in Figure 34. Experimentally the range of the output offset is very close to [-10,10] range. The slight deviations from the expected may be attributed to potential bias currents within the transistors within the op-amp unit, and temperature variations.

8 Lab 8.8 - Push & Pull Buffer

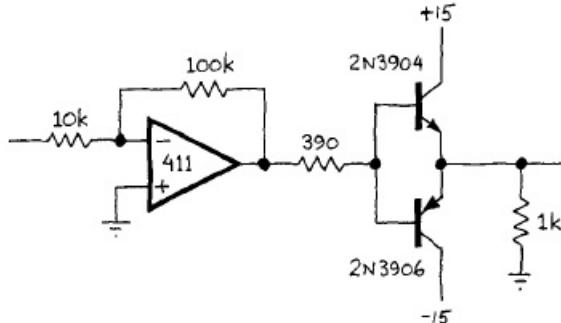


Figure 35: Push-Pull Buffer Amplifier

In this lab experiment, we verify the presence of distortion at the output of a push-pull stage of the circuit, and aim to mitigate the distortion levels by analyzing each stage functionality.

Components

- (1) 1 LF411 Op Amp
- (2) 10k, 100k, 470(replacement for 390), 1k- Ω resistors
- (3) BJT(2N3904, 2N3906)
- (4) 1 Power Supply (for +15 V, -15 V, GND)
- (5) 1 DVM for voltage measurement
- (6) 1 Oscilloscope for wavegen, graphical output

Practical Considerations

Upon connecting the 390- Ω resistance using multiple resistors in series, the amplified signal at the output of the op-amp could not be handled properly at the junction. Thus 470- Ω resistor was used instead.

Output

- (1) At the push-pull stage output as shown in Figure 35

	Input	Frequency	Output Voltage	Distortion
1	1.0 V	100 Hz	14.45 V	Yes
2	1.0 V	200 Hz	14.45 V	Yes
3	1.0 V	300 Hz	14.45 V	Yes

To mitigate distortions present at the output, one suggested method is to connect the output of the op-amp directly to the common emitter terminal. While this improves distortions, it does not function properly at high frequency ranges.

- (2) Reconnecting the right side of the feedback resistor to the push-pull output as shown in Figure 37, the distortion is reduced.



Figure 36: Distortions at 100Hz, 260 Hz

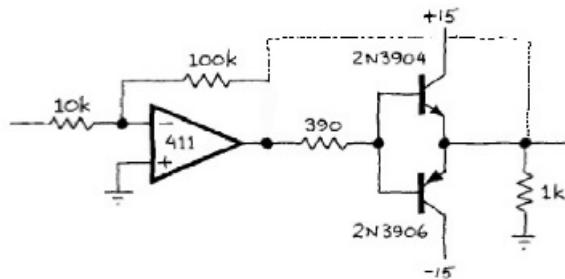


Figure 37: modified Push-Pull Buffer Amplifier

Simulation Results

The LF411 subcircuit design was used (Appendix A).

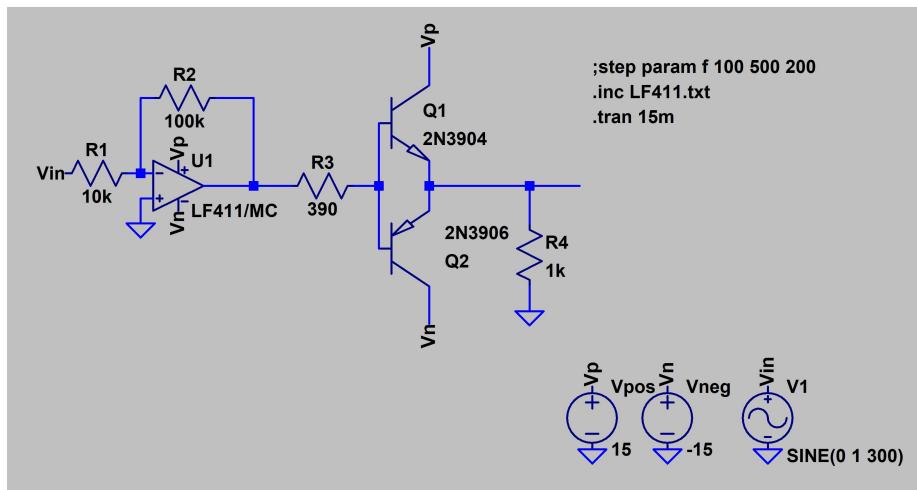


Figure 38: The Schematic of Lab 8.8 in LTSpice.

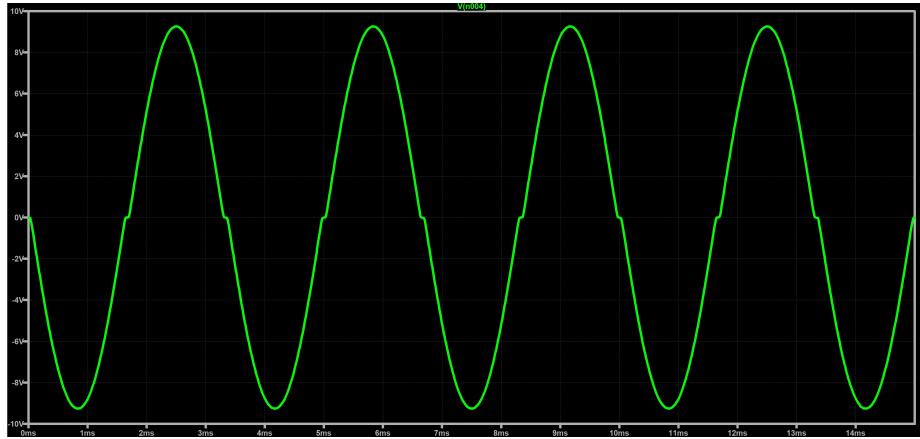


Figure 39: The output wave without the wire fix shows a clip in the wave



Figure 40: The output waveform with the fix connecting the negative input to the output of the whole system rather than the output of the op amp

Summary and Discussion

Questions

- (1) Explain how this push-pull buffer amplifier functions.

A push pull buffer stage consists of a NPN and a PNP BJTs in the upper and lower, respectively, configured together to amplify the signal at the output. The goal of this stage is to deliver the amplified power efficiently by current sink and source, as well as by yielding lower output impedance.

In Class A configuration, the stage is operated at a constant bias current, in which both halves of the devices share the input signal simultaneously in the

cycle. With the stage always conducting current, it has much less distortion than the other classes, though this results in higher power consumption, and thus lower efficiency of 25%.

In Class B configuration, each of the two active transistors conduct for half the operation cycle alternatively. While this offers a much higher efficiency of 78.5% relative to Class A due to absence of bias current, it suffers from crossover distortion in transition from one transistor to the other.

In Class AB, which is a hybrid of A and B, it runs Class A model at lower power levels, and functions as Class B amplifiers at the output currents determined by the set bias. This reduces distortion relative to Class B, but efficiency falls as well with respect to Class B.

- (2) Explain disadvantages of Class B amplifier over Class A amplifier.

Class B Push-Pull Amplifier Circuit

A class B push-pull amplifier gives a maximum efficiency of approximately 78.5%, a significant improvement over class A, since each transistor is switched off half of the time, preventing from dissipating excessive power. However, Class B amplifier, despite its relatively higher efficiency, has a drawback of a mismatch in the crossover region (at the "joins" between the two halves of the signals). Since the two transistors are shut off together half of the time, the distortion occurs at the output. In contrast to Class A, in which the stage requires significant base bias in the quiescent state (no input signal) and thus leading to heat dissipation, Class B has no current flowing through the devices in the quiescent stage. Such operation of a transistor at a time in comparison with Class A improves the efficiency.

- (3) Discuss possible (other) solutions to mitigate distortions and the associated trade-off.

Possible Solutions

Another approach to help improve the crossover distortion is implementing class AB amplifier, in which each device operates the same way for half the time, but also transmits small signal for the other half, instead of none, thereby reducing the time for which both are turned "off." However, there remains trade-off to preserving linearity. Class AB amplifier suffers from a lower efficiency than Class B in general, though higher than Class A, due to increased consumption of energy for the time of operation.

The crossover distortion region can be eliminated by a couple other methods other than class AB amplifier. (1) A simple addition of small resistance at the emitter in series, (2) adjustments in temperature and voltage biases, and (3) moving the resistor at the junction to across the output of op-amp and the emitter of the transistors could potentially lower the fluctuations in the region of operation. Such minor improvements could reduce the distorted regions in operation.

Overall Conclusions

Upon analysis of each of the operational amplifier circuits, each poses a unique set of behavioral characteristics for the impedances at the input and output, voltage gains, and possible breakdowns or clipping-off points past some threshold of amplitude or frequency ranges. The methods to mitigate distorted, undesired responses have been explored and discussed, such as in the push-pull circuit, and in the future application of these fundamental circuit configurations these techniques may be employed.

Appendix A Op Amp LF411 Subcircuit Design

```
1      * LF411 operational amplifier
2  * "macromodel" subcircuit
3  *
4  * connections:
5  *     1 - non-inverting input
6  *     2 - inverting input
7  *     3 - positive power supply
8  *     4 - negative power supply
9  *     5 - output
10 *
11 .subckt LF411/MC 1 2 3 4 5
12 *
13   c1    11 12 2.801E-12
14   c2    6  7  8.000E-12
15   css   10 99 3.200E-12
16   dc    5  53 dx
17   de    54 5  dx
18   dlp   90 91 dx
19   dln   92 90 dx
20   dp    4  3  dx
21   egnd  99 0 poly(2) (3,0) (4,0) 0 .5 .5
22   fb    7  99 poly(5) vb vc ve vlp vln 0 3.316E6
23 + -3E6 3E6 3E6 -3E6
24   ga    6  0 11 12 402.1E-6
25   gcm   0  6 10 99 12.72E-9
26   iss   3  10 dc 280.0E-6
27   hlim  90 0 vlim 1K
28   j1    11 2 10 jx
29   j2    12 1 10 jx
30   r2    6  9 100.0E3
31   rd1   4  11 2.487E3
32   rd2   4  12 2.487E3
33   ro1   8  5 40
34   ro2   7  99 60
35   rp    3  4 24.00E3
36   rss   10 99 714.3E3
37   vb    9  0 dc 0
38   vc    3  53 dc 1.100
39   ve    54 4  dc .3
40   vlim  7  8 dc 0
41   vlp   91 0 dc 30
42   vln   0  92 dc 30
```

```
43 .model dx D( Is=800.0E-18)
44 .model jx PJF( Is=30.00E-12 Beta=577.5E-6
45 + Vto=-1)
46 .ends
47 *$
```

Appendix B Potentiometer Design

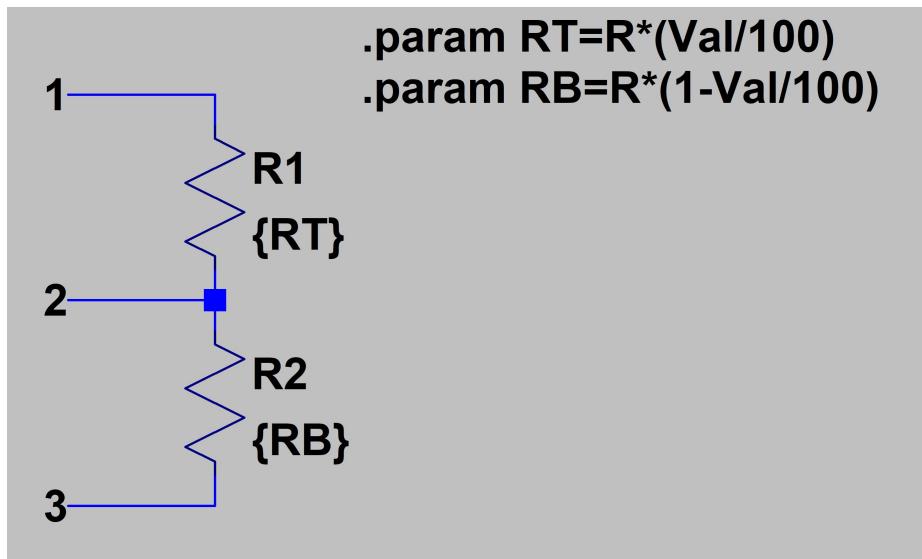


Figure 41: Potentiometer Design