Lab 12 - Voltage Regulator
Junior Projects II - ECE 394A

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Contents

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Abstract

In this series of lab experiments, voltage regulated power supply circuits are explored. One of the important characteristics of a voltage regulator, the dropout voltage of a linear type, which is simply the difference between input and output voltage is closely examined - without this characteristic, the output drops out of regulation, and thus the circuit falls out of proper and desired behavior. In addition, management of power dissipation through self-protection in fixed, adjustable regulator circuits is verified through analysis of the IC chip in detail.

Introduction

For the purposes of exploration with voltage regulators throughout this series of experiments, the components 78L05 and 317 have been used. The 317 chip is easier to use and is more versatile than 78L05, with regards to its adjustable output voltage. In addition, it is easier to rig up a current source with ease; for these reasons, this is employed in 12-3: Adjustable Regulator. For simple regulators, 78L05 is easy to implement, protects from current limiting and damage from excessive power dissipation ($I_{out}[V_{in}$ - $V_{out}]$). Prior to currently available fully-integrated regulators, 723 regulators were used, which consist of elements that are standard to a typical regulator: an op amp, "pass" transistors, and a reference voltage, as shown below in Figure 1. Since this is outdated is no longer readily available, experimentation with this chip is omitted.

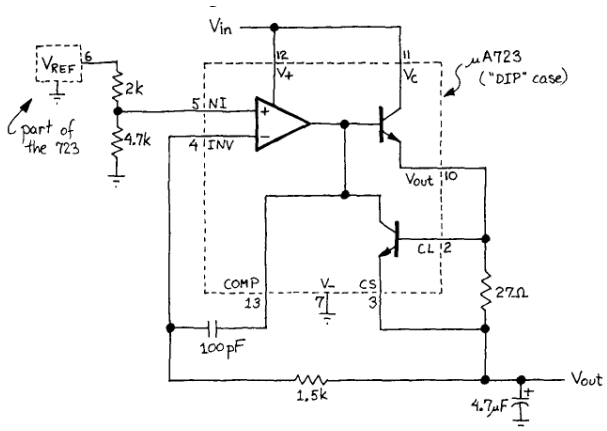


Figure 1: Traditional 723 Voltage Regulator IC Schematic

Experiments

1 Lab 12.2 - Three Terminal Fixed Regulator

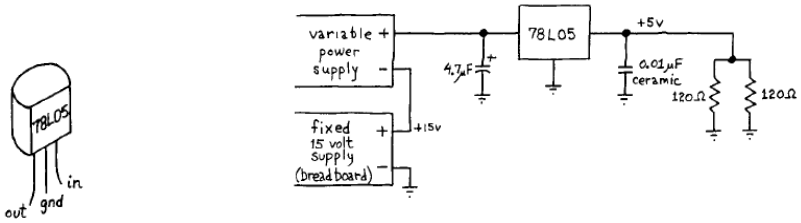


Figure 2: 78L05 Fixed 3-Terminal Regulator

Three Terminal Fixed Regulator
78L05 is an easy 3-terminal fixed (non-adjustable) regulator, that prevents from current limiting and excessive power dissipation. Upon dealing with this device, one should observe continued heat sinking effect due to power dissipation. In order to observe this heat sinking effect, a resistive load that draws less than the chip's maximum amount of current (100mA) is added on one end - namely 120Ω resistors in parallel, providing 60Ω. As per the datasheet for 78L05 chip, a common ground is required between the input and the output voltages. and the input voltage must remain typically 2.0 V above the output voltage even during the low point on the input ripple voltage. Therefore, as seen in Figure 2, the negative terminal of the variable supply is kept in float, not tied to common ground.

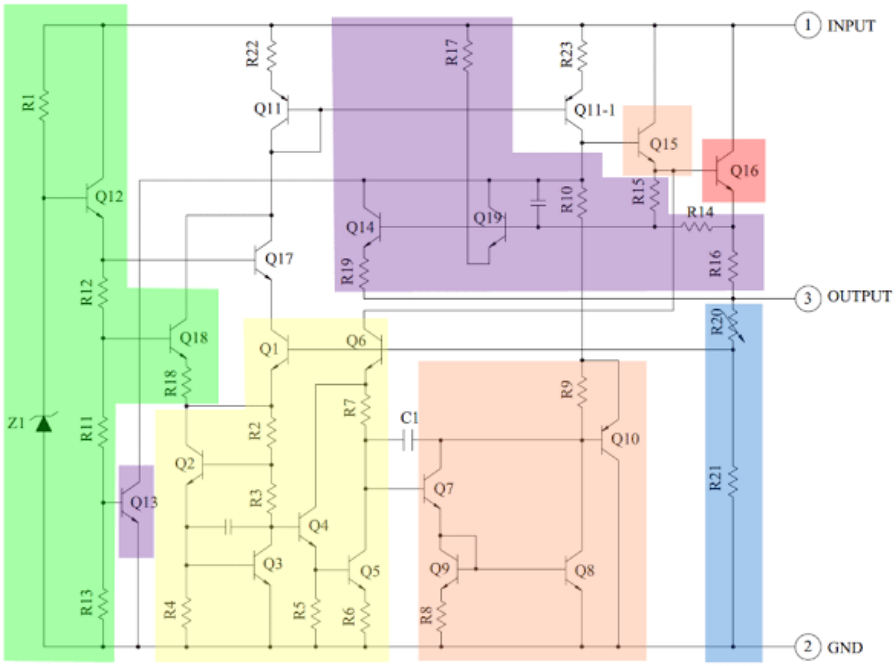


Figure 3: 78L05 Regulator Schematic

In the schematic for a fixed 78L05 IC regulator, there are multiple parts that serve different roles. Primarily, Q16 (in red), is what controls the current across input-output, and thus controlling the output voltage. The left section (green) serves to keep the circuit away from being stuck in "off" state by providing an initial current to the bandgap circuit with transistor. Then the following bandgap reference section (yellow) maintains stable voltage over a range of temperature conditions by taking the scaled output voltage as input to Q1 and Q6, and checks to see if the output is too high or low by sending the error signal

as input to Q7. Then, this error signal is amplified in the section to the right (orange), and the amplified signal controls the output transistor through Q15, closing the negative feedback loop that controls the output voltage. Throughout the flow, the section in (purple) serves to regulate the temperature from overheating (Q13), excessive input voltage (Q19) and excessive output current (Q14), by lowering the output current and thus protecting from excessive power dissipation damage. The blue section is simply for voltage divider, in which the output voltage is scaled down for bandgap reference input.

Components
(1) 1 78L05 Fixed Regulator
(2) 120Ω, Resistors
(3) 0.01μF, 4.7μF ceramic capacitor
(4) 1 Power Supply (for fixed 15V and variable supply)
(5) 1 Oscilloscope

Power Dissipation

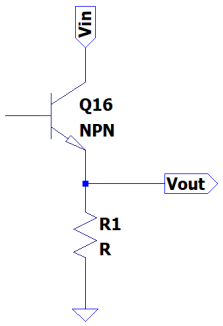


Figure 4: Power Dissipation

In reference to Figure 3 - Q16 specifically (Figure 4, power dissipation is determined by

$$P_{dissipation} = I_{out}(V_{in} - V_{out}). \tag{1}$$

Ideally, we would like observe the circuit heat sinking when the power dissipation is at maximu, so we determine the maximum allowable input voltage for the power dissipation to be at maximum, by first calculating the maximum value as follows.

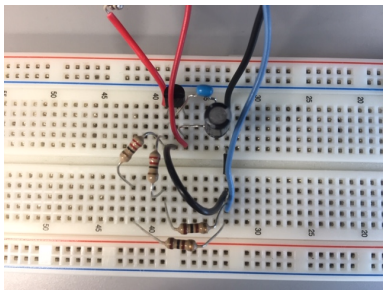
$$Power_{maxdissipation} = \frac{T_{junction} - T_{ambient}}{\Theta_{junction-ambient}} \tag{2}$$

where $\Theta_{junction-ambient} = [°C/W] and T_J$, $T_A = [°C]$
(for TO-92, plastic package, from datasheet)
We set the ambient(room) temperature to be in [20, 25] °C, and take average

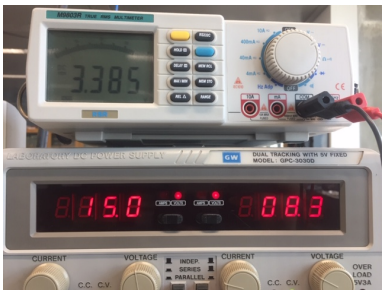
to be 23 °C, and then equate the dissipation to be the maximum and determine the maximum input.

$$Power_{maxdissipation} = \frac{150 - 23}{230.9} = 0.55W = (\frac{5V}{60\Omega})(V_{in} - 5) \tag{3}$$

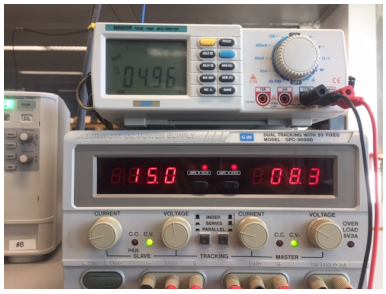
Thus $V_{in} \approx 8.3$ Volts. The output voltages at maximum power dissipation (with the determined input voltage of 8.3V) are shown below.
Assumptions
- The device begins to limit when its junction temperature reaches ≈ 150 °C



(a) 78L05 Circuit on Breadboard



(b) Min V_{out} at max power dissipation



(c) Max V_{out} at max power dissipation

Figure 5: At Maximum Power dissipation

The dropout voltage is found to be in range [3.34, 4.915] [Volts] at $V_{in} = 8.3$ Volts that evokes the chip's thermal self-protection. The point at which thermal self-protection action is taken was observed when the output reaches the minimum and no longer is reduced. The chip (as aforementioned in the schematic diagram for the chip) then uses a series of transistors to maintain stable temperature and limit heat dissipation.

$$V_{dropout-1} = V_{in} - Vout = 8.3 - 4.96 = 3.34V$$
$$V_{dropout-2} = V_{in} - Vout = 8.3 - 3.385 = 4.915V$$

Results
The maximum input voltage value at which the chip activates its thermal self-protection logic was determined and experimentally found to be at around 8.3 Volts, and the range of dropout voltage for the chip was computed to be in [3.34, 4.915] Volt range. An interesting observation was its variations in the output voltage as the chip was cooled down by a fan, changing the maximum input voltage need for thermal self-protection to increase for the maximum power dissipation.

Simulation Results

An LTspice simulation was done using a subcircuit design of the 78L05 (Appendix A).

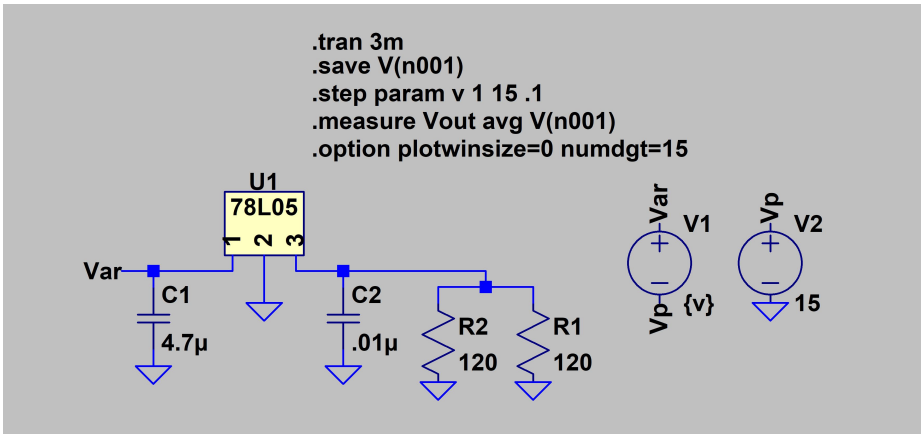


Figure 6: Schematic of LTSpice Simulation

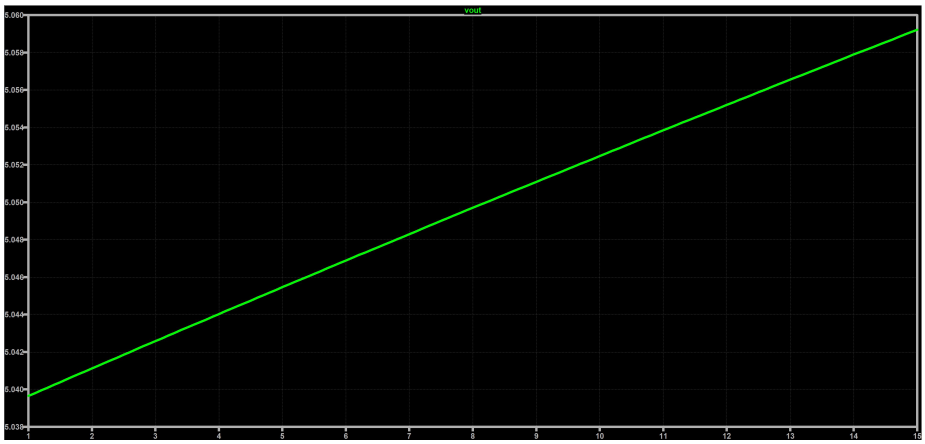


Figure 7: Sweep of Voltages from 1V to 15V of the Variable Voltage Source

The range of the output voltage form simulation was 5.04V to 5.05V. This shows that the voltage regulator is able to limit to around 5V when the input is changing.

Summary and Discussion

Upon completion of the experiment it is possible to see the use cases of the three terminal fixed regulator due to how it can be used to regulate the voltage input while maintaining heat dissipation. After calculating the theoretical results of the thermal dissipation, the numbers were tested as voltages which yielded the expected output. Any voltage of 8.3 V or lower on the second power supply would keep the system in equilibrium while any voltage higher would cause the device to thermally throttle, lowering the output voltage and giving off heat. This problem can be fixed in a few different ways such as a heat sink, fanning the regulator, blowing on it and using a wet tissue paper, all of which had caused the self-protection to be unnecessary for the circuit.

2 Lab 12.3 - Adjustable Three-Terminal Regulator: 317

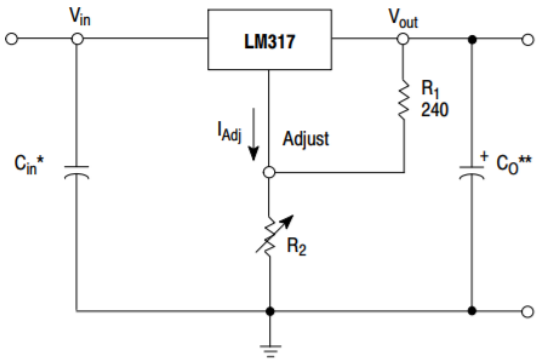


Figure 8: 317 Ad

* C_{in} is required if regulator is located an appreciable distance from power supply filter.
* C_O is not needed for stability, however, it does improve transient response.

Adjustable Three-Terminal Regulator: 317
The LM317 IC regulator chip is an adjustable 3-terminal positive voltage regulator, that can supply in excess of 1.5A over an output voltage range of [1.2, 37] Volts. This chip is also easier to use, as it is similar to a fixed regulator 78L05 with regards to its current and temperature sensing to protect itself from excessive loads(internal current limiting, thermal shutdown and safe area compensation), and also allows to select an output voltage with the addition of two resistors. Furthermore, a variable resistor could allow for a variable output supply. The applications include programmable output regulator and a precision current regulator by connecting a fixed resistor between the adjustment and output.

Components
(1) 1 LM317-IC-Regulator Chip
(2) 2 4.7μF ceramic capacitors
(3) 1 240Ω, 820Ω Resistors
(4) 1 Power Supply (for +15 V input)
(5) 1 Oscilloscope

The output voltage is determined by the following equation.
* Since I_{adj} is controlled to less than 100 A, the error associated with this term is negligible in most applications.

$$v_{out} = 1.25V(1 + \frac{R_2}{R_1}) + I_{adj}R_2 \tag{4}$$

Values	Resistance R [Ω]	Output Range [Volts]
1	820	5.81
2	1k POT	[1.241, 6.91]
3	0	1.241

Results

As expected, for a certain resistance value, the output voltage varied accordingly. Since the chip is designed to return an output voltage from range of [1.2, 37] Volts, the lowest with R = 0 of 1.241 Volts makes sense, and as the resistance is increased, the ratio of R2 and R1 is also increased, thereby increasing the output voltage overall.

Simulation Results

An LTspice simulation was done using a subcircuit design of the LM317 (Appendix B).

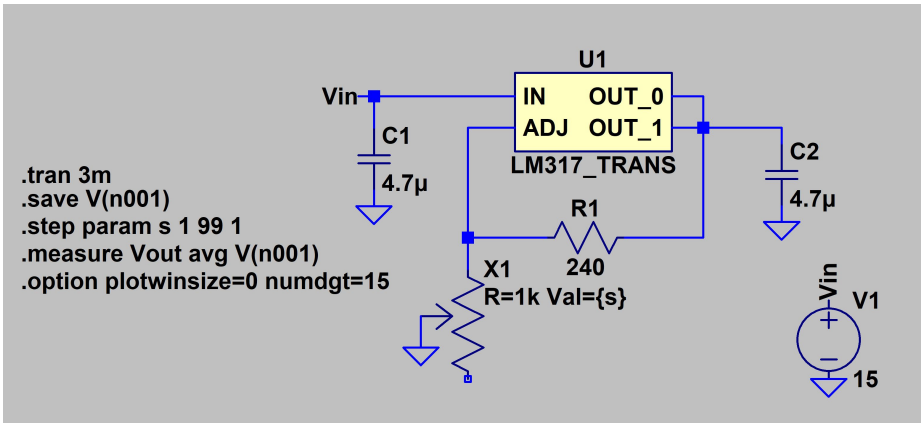


Figure 9: Schematic of LTSpice Simulation

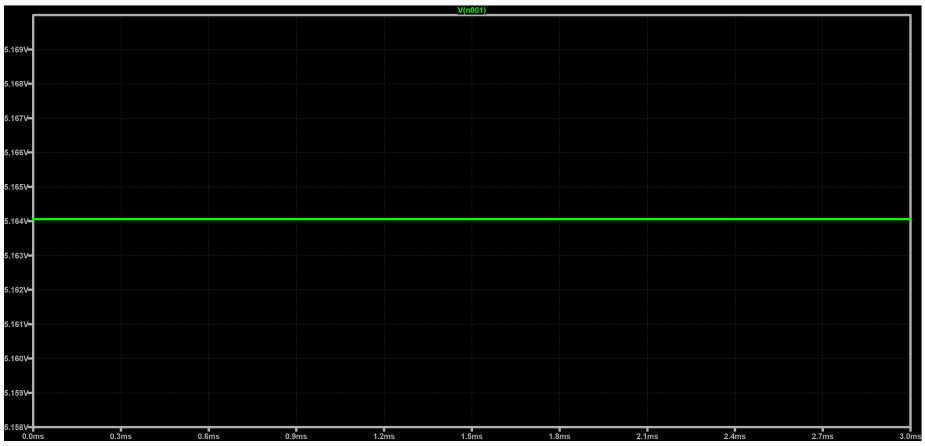


Figure 10: V_{out}, R = 750 Ω

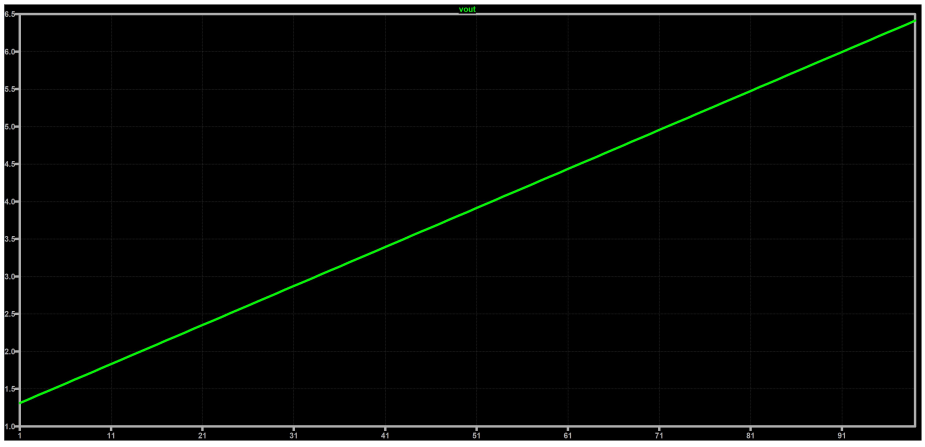


Figure 11: V_{out} with R sweep

Summary and Discussion

Based on the experimental results, the way that the circuit performs is as expected since the combination of resistors leads to different values for the output voltage. While the regulator has similar properties to the 78L05 in that both include current and temperature sensors to protect from overloads, that component of the 317 was not tested as it was already deemed to be accurate in the previous part of this experiment concerning the 78L05.

3 Lab 12.5 - "Crowbar" Over-Voltage Protection

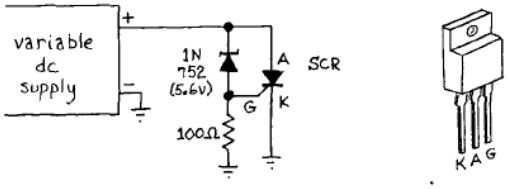


Figure 12: "Crowbar" Over-Voltage Protection

"Crowbar" Over-Voltage Protection
Crowbar" circuit is simply a circuit that shuts down the supply when the voltage climb is too high. For example, the Figure 12 shows a circuit consisted of a Zener diode and a resistor in series, and a thyristor (Silicon Controlled Rectifier, SCR) in parallel. When the voltage climb reaches above ≈ 5 Volts, the Zener diode begins to conduct, and when the voltage across the 100Ω resistor reaches ≈ 0.6 Volts (threshold), the thyristor activates, clamping the supply to ground. In a more practical configuration, a capacitor would be added at the gate of the SCR, to protect from triggering on brief transients.

Zener Diode
A Zener diode is a one-way current-conducting device that has a region in its reverse bias characteristics of almost a constant negative voltage regardless of the value of the current flowing through the diode, and maintains constant constant current even with large changes as far as the current remains between the breakdown current (min) and the maximum current rating (max). Zener Diodes can be used to produce a stable voltage output with low ripple under varying load current conditions. By passing a small current through the diode from a voltage source, via a suitable current limiting resistor, the zener diode will conduct sufficient current to maintain a voltage drop of Vout.

Thyristor
A thyristor is a semiconductor device with four layers of P-type and N-type bases. It serves as a bistable switch, conducting when the gate receives a current trigger and continuing to conduct until the voltage across the device is reverse-biased or removed. A 3-terminal thyristor is aimed to control the larger current from the anode to cathode by controlling the gate current (smaller). In contrast, while a 2lead thyristor is designed to turn on when the voltage across the two terminals becomes sufficiently large (breakdown voltage).

A thyristor have 3 states of operation:
(1) Reverse blocking mode: Voltage is applied in the direction that would be

blocked by a diode
(2) Forward blocking mode: Voltage is applied in the direction that would cause a diode to conduct, but the thyristor has not been triggered into conduction
(3) Forward conducting mode: The thyristor has been triggered into conduction and will remain conducting until the forward current drops below a threshold value known as the "holding current"

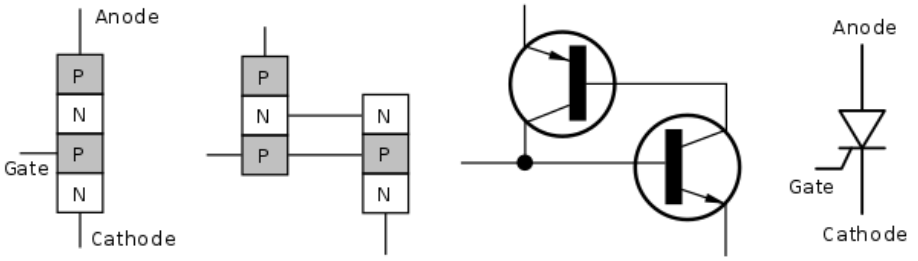
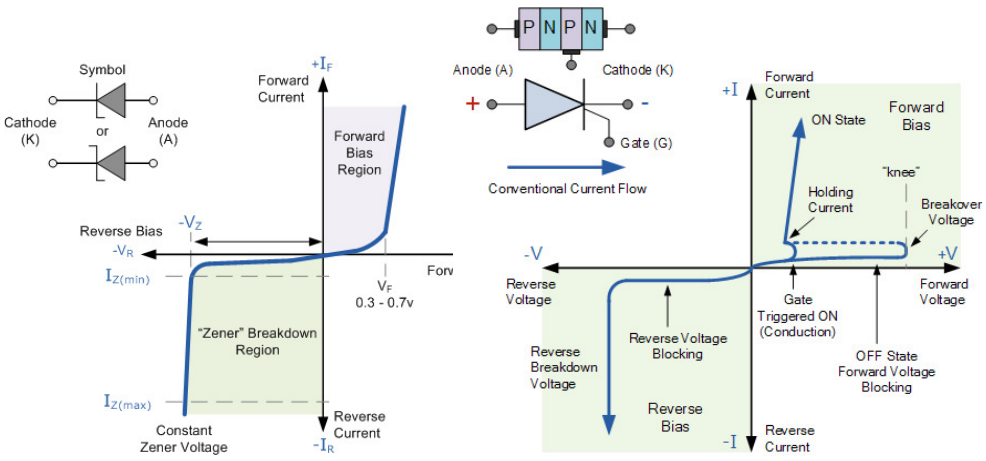


Figure 13: Thyristor

In summary, a thyristor operates as follows:
- A small gate current controls a larger anode current
- Conducts current only in forward-bias and triggers current applied at the gate
- Behaves like a rectifying diode once it is triggered ON
- Anode current must be greater than "holding current" to maintain conduction
- Blocks current flow when reverse biased, no matter if gate current is applied
- Once triggered ON, it will be latched ON conducting even when a gate current is no longer applied providing anode current is above "latching current".



(a) Zener Diode (b) Thyristor (SCR)

Figure 14: Comparison between Zener diode and SCR I/V Characteristics

Components
(1) 1 1N759A Zener diode
(2) 1 11C106D Thyristor (Silicon Controlled Rectifier)
(3) 0.1μF Capacitor
(4) 1 Power Supply (for +15 V, -15 V, GND)
(5) 1 Oscilloscope

The measurements taken at the supply and gate describe the behavior of the "crowbar" regulator circuit. As the supply voltage is increased up to 12.5 V (1st data point), the gate voltage remains below the threshold of 0.6 V, and thus the supply is maintained as what was adjusted at the input. However, a slight more increase of the supply causes clamping of the supply to almost ground, upon the gate voltage going over the threshold voltage of the Zener diode. Therefore upon triggering with input greater than 12.5 V causes the 2nd data point to be pulled down to the minimum supply voltage (minimum of the observed varying data) due to the protection measure of the circuit by the SCR.

	Supply Voltage	Gate Voltage
1	12.5 V (max)	0.5 V
2	1.0 V (min)	0.8 V

Simulation Results

An LTspice simulation was done using a subcircuit design of a thyristor (Appendix C).

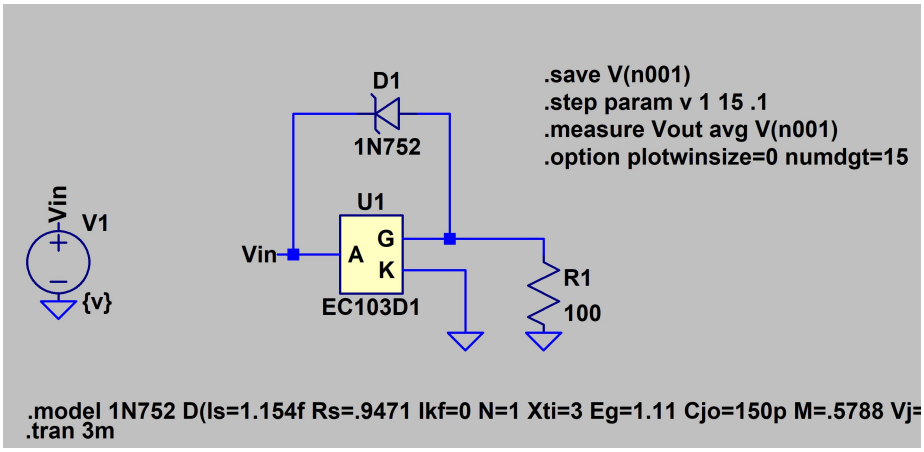


Figure 15: Schematic of LTSpice Simulation

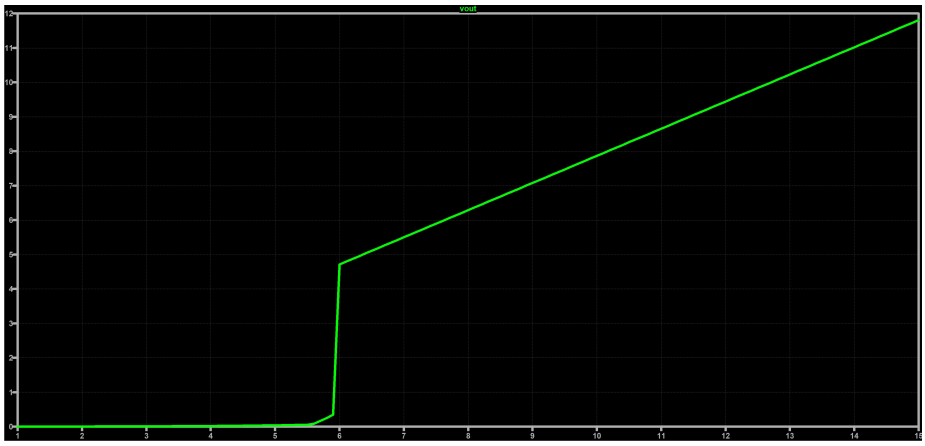


Figure 16: V_{gate} increases as V_{supply} increases

As seen in the experiment, the gate voltage of SCR increased once the input voltage reached a certain point.

Summary and Discussion

In this experiment, the thyristor was tested to show the "crowbar" over-voltage protection circuit and how there exists a boundary in the amount of input voltage the device can handle before it begins conducting, causing the device to be in its "ON State" as shown in Figure 9b with the holding current. Experimentally this voltage was discovered after increasing the voltage to 12.5 V which is the upper boundary of the input voltage which had decreased to 1.0 V when attempting to increase any further, indicating the lower bound of the input voltage.

Overall Conclusions

From experimenting with fixed- and adjustable- voltage regulators using 78L05 and LM317, as well as a "crowbar" circuit with a Zener diode and a thyristor (SCR), means of controlling the voltage given a variable supply voltage and parameters such as power dissipation have been explored. Determination of the point of failure, current at its "latching" and "holding" states for SCR, and understanding of sub-circuits that serve to minimize damage and protect from excessive heat sinking allowed to apply these acquired design considerations to a larger application.

Appendix A 78L05 Design

```
1  ********************************************************************************

2  *dummy subckt used only for symbol initialization
3  .subckt Vreg 1 2 3
4  .ends
5  ********************************************************************************

6  .subckt 7805 In Aj Out
7  F1 In 0 Vc 1
8  Rcon In 0 1e6
9  B1 4 Aj V= Table (V(In,Aj), 0,0, 1,0, 7,5, 35,5, 36,0)
10 Vc 4 Out 0
11 F2 In Aj Vc 4m
12 .ends
13 *78L05 MCE 7-12-95
14 *78L05 circuit taken from Signetics 1977 Analog Data Book page 160
15 *5V 100mA Voltage Regulator pkg:TO-92 1,2,3
16 .SUBCKT 78L05 1 2 3
17 Q1 5 5 1 QPNP
18 Q2 10 5 1 QPNP
19 Q3 1 11 12 QNPN
20 Q4 1 10 11 QNPN
21 Q5 10 13 14 QNPN
22 Q6 1 4 20 QNPN
23 Q7 10 19 21 QNPN
24 Q8 9 9 2 QNPN
25 Q9 18 9 22 QNPN OFF
26 Q10 8 18 2 QNPN
27 Q11 5 7 17 QNPN
28 Q12 5 16 17 QNPN
29 Q13 10 15 17 QNPN
30 C1 15 10 20E-12
31 D1 2 4 DZ5V
32 Q14 2 8 7 QPNP
33 R17 2 17 4E3
34 R16 4 1 20E3
35 R15 16 20 4E3
36 R14 19 16 700
37 R13 2 19 300
38 R12 2 21 100
39 R11 9 7 1E3
40 R10 18 7 10E3
41 R9 7 3 2.2E3
42 R8 2 22 1E3
43 R7 8 7 2E3
44 R6 2 15 1.4E3
45 R5 15 3 4.5E3
46 R4 3 14 100
47 R3 3 12 2
48 R2 13 11 500
49 R1 13 12 200
50
51 .MODEL QPNP PNP(IS=1.05E-15 BF=220 VAF=240 IKF=0.1 ISE=1.003E-9
52 + NE=4 ISC=1.003E-9 NC=4 RB=3 RE=0.5 RC=0.2 CJE=5.7E-12 VJE=0.75 TF
       =3.35E-10
```

```
53  + CJC=4.32E-12 VJC=0.75 TR=1.7E-7 VJS=0.75 KF=4E-15 )
54
55  .MODEL QNPN NPN(IS=8.11E-14 BF=205 VAF=113 IKF=0.5 ISE=1.06E-11
56  + NE=2 BR=4 VAR=24 IKR=0.225 RB=1.37 RE=0.343 RC=0.137 CJE=2.95E-11
57  + TF=3.97E-10 CJC=1.52E-11 TR=8.5E-8 XTB=1.5 )
58
59  .MODEL DZ5V D(IS=1E-11 RS=7.708 N=1.27 TT=5E-8 CJO=4.068E-10 VJ
        =0.75
60  + M=0.33 BV=4.946 IBV=0.01 )
61  .ENDS 78L05
62  * LM7805 model.
63  * No need to use .inc - I've set the .asy symbol to remove the need
        for .inc.
64  * (I used the symbol of LT1084, just replaced the LT1084 by LMxxxx
        and LTC.LIB by regulators.lib)
65
66  .SUBCKT LM7805  1     2     3
67  * In GND Out
68  QT6             23    10    2     Q_NPN 0.1
69  QT7             5     4     10    Q_NPN 0.1
70  QT5             7     6     5     Q_NPN 0.1
71  QT1             1     9     8     Q_NPN 0.1
72  QT3             11    8     7     Q_NPN 0.1
73  QT2             11    13    12    Q_NPN 0.1
74  QT17            1     15    14    Q_NPN 10
75  C2              10    23          4P
76  R16             12    5           500
77  R12             16    2           12.1K
78  QT18            17    23    16    Q_NPN 0.1
79  D1              18    19          D_D
80  R11             20    21          850
81  R5              22    3           100
82  QT14            24    18    2     Q_NPN 0.1
83  R21             6     2           2.67K
84  R20             3     6           640
85  DZ2             25    26          D_5V1
86  R19             1     26          16K
87  R18             14    3           250M
88  R17             25    14          380
89  R15             25    15          1.62K
90  QT16            1     20    15    Q_NPN 1
91  QT15            2     24    21    Q_PNP 0.1
92  *OFF
93  R14             21    24          4K
94  C1              27    24          20P
95  R13             19    2           4K
96  QT13            24    27    18    Q_NPN 0.1
97  QT12            20    25    22    Q_NPN 1
98  *OFF
99  QT11            20    28    2     Q_NPN 0.1
100 *OFF
101 QT10            20    11    1     Q_PNP 0.1
102 R10             17    27          16.5K
103 R9              5     4           1.9K
104 R8              4     23          26
105 R7              10    2           1.2K
106 R6              29    2           1K
```

```
QT9             11   11   1    Q_PNP  0.1
QT8             27   16   29   Q_NPN  0.1
QT4             15   6    17   Q_NPN  0.1
DZ1             2    9         D_5V6
R4              1    9         80K
R3              28   2         830
R2              13   28        4.97K
R1              8    13        7K
*
.MODEL D_5V1 D( IS=10F N=1.16 BV=5.1 IBV=0.5M CJ0 = 1P TT = 10p )
.MODEL D_5V6 D( IS=10F N=1.16 BV=5.6 IBV=5U CJ0 = 1P TT = 10p )
.MODEL Q_NPN NPN( IS=10F NF=1.16 NR=1.16 BF=80 CJC=1P CJE=2P
+        TF=10P TR=1N )
.MODEL Q_PNP PNP( IS=10F NF=1.16 NR=1.16 BF=80 CJC=1P CJE=2P
+       TF=10P TR=1N )
.MODEL D_D D( IS=1F N=1.16 CJ0 = 1P TT = 10p )

.ENDS LM7805
*
*=======================================
```

Appendix B LM317 Design

```
* PSpice Model Editor - Version 16.2.0
*$
* LM317
*********************************************************************************
* (C) Copyright 2014 Texas Instruments Incorporated. All rights
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*********************************************************************************
** This model is designed as an aid for customers of Texas
    Instruments.
** TI and its licensors and suppliers make no warranties, either
    expressed
** or implied, with respect to this model, including the warranties
     of
** merchantability or fitness for a particular purpose. The model
    is
** provided solely on an "as is" basis. The entire risk as to its
    quality
** and performance is with the customer.
*********************************************************************************
*
** Released by: WEBENCH Design Center, Texas Instruments Inc.
* Part: LM317
* Date: 11DEC2014
* Model Type: TRANSIENT
* Simulator: PSPICE
* Simulator Version: 16.2.0.p001
* EVM Order Number:
* EVM Users Guide:
* Datasheet:SLVS044VSEPTEMBER 1997REVISED FEBRUARY 2013
*
* Model Version: Final 1.00
```

```
26  *
27  ********************************************************************************

28  *
29  * Updates:
30  *
31  * Final 1.00
32  * Release to Web
33  *
34  ********************************************************************************

35  .SUBCKT LM317_TRANS IN ADJ OUT_0 OUT_1
36  R_R1          VXX IN  {RINP}
37  R_R6          N242982 VYY  10 TC=0,0
38  R_R5          VZZ VYY  {ROUT}
39  E_ABM1          N242982 0 VALUE { MIN(V(VXX), (V(Vzz)+(ILIM*ROUT)))
          }
40  R_R2          N222524 VXX  {PSRR*RINP}
41  R_U1_R2          0 U1_N26728  1G
42  E_U1_ABM5          U1_N31197 0 VALUE { MIN(V(U1_N26728),
43  + MAX(V(IN) - {DROP}, 0))    }
44  C_U1_C2          0 U1_N26728  1n
45  R_U1_R1          0 U1_N08257  1G
46  R_U1_R4          U1_N28933 U1_N26728  10 TC=0,0
47  R_U1_R5          U1_N31197 N222524  10 TC=0,0
48  C_U1_C3          0 N222524  1n
49  X_U1_U2          IN U1_N12783 U1_N12664 U1_UVLO_OK COMPHYS_BASIC_GEN
       PARAMS:
50  +  VDD=1 VSS=0 VTHRESH=0.5
51  C_U1_C1          0 U1_N08257  {1e-6*SQRT(TTRN)}
52  V_U1_V4          U1_N12783 0 {UVLO}
53  V_U1_V3          U1_N12664 0 {UHYS}
54  E_U1_ABM6          U1_EN_OUT 0 VALUE { IF(V(U1_UVLO_OK)> 0.6, {VREF
       }, 0)     }
55  R_U1_R3          U1_EN_OUT U1_N08257  {3.333e5*SQRT(TTRN)} TC=0,0
56  E_U1_ABM4          U1_N28933 0 VALUE { V(U1_N08257)*
57  +  (ABS(V(OUT_0))/(ABS(V(OUT_0)-v(ADJ))))     }
58  X_U2          0 OUT_0 d_d PARAMS:
59  X_F1     VZZ OUT_0 IN VYY LM317_TRANS_F1
60  C_C1          VXX IN  {1/(6.28*RINP*POLE)}
61  C_C2          VXX N222524  {1/(6.28*PSRR*RINP*ZERO)}
62  C_C3          0 VYY  1n
63  .PARAM  psrr=7.9432e-4 uvlo=0 ilim=2.2 pole=15k rinp=1e7 zero=100e6
       rout=0.4m
64  +  ttrn=1e-4 vref=1.25 uhys=0 drop=.5
65  .ENDS LM317_TRANS
66  *$
67  .SUBCKT LM317_TRANS_F1 1 2 3 4
68  F_F1          3 4 VF_F1 1
69  VF_F1          1 2 0V
70  .ENDS LM317_TRANS_F1
71  *$
72  .SUBCKT COMP_BASIC_GEN INP INM Y PARAMS: VDD=1 VSS=0 VTHRESH=0.5
73  E_ABM Yint 0 VALUE {IF (V(INP) >
74  + V(INM), {VDD},{VSS})}
75  R1 Yint Y 1
76  C1 Y 0 1n
```

```
.ENDS COMP_BASIC_GEN
*$
.SUBCKT COMPHYS_BASIC_GEN INP INM HYS OUT PARAMS: VDD=1 VSS=0
    VTHRESH=0.5
EIN INP1 INM1 INP INM 1
EHYS INP1 INP2 VALUE { IF( V(1) > {VTHRESH},-V(HYS),0) }
EOUT OUT 0 VALUE { IF( V(INP2)>V(INM1), {VDD} ,{VSS}) }
R1 OUT 1 1
C1 1 0 5n
RINP1 INP1 0 1K
.ENDS COMPHYS_BASIC_GEN
*$
.SUBCKT COMPHYS2_BASIC_GEN INP INM HYS OUT PARAMS: VDD=1 VSS=0
    VTHRESH=0.5
+ T=10
EIN INP1 INM1 INP INM 1
EHYS INM2 INM1 VALUE { IF( V(1) > {VTHRESH},-V(HYS)/2,V(HYS)/2) }
EOUT OUT 0 VALUE { IF( V(INP1)>V(INM2), {VDD} ,{VSS}) }
R1 OUT 1 1
C1 1 0 {T*1e-9}
RINP1 INP1 0 10K
RINM2 INM2 0 10K
.ENDS COMPHYS2_BASIC_GEN
*$
.SUBCKT D_D 1 2
D1 1 2 DD
.MODEL DD D (IS=1E-015 N=0.01 TT=1e-011)
.ENDS D_D
*$
```

Appendix C Thyristor (SCR) Design

```
**********************************
**********************************
**
** Littelfuse, LP
** SCR SPICE Models
** EC103xx-SxSx
**
** T. Chenoski
** Irving Technical Center
**
** A 06/13/08
**
**********************************
**********************************
.SUBCKT EC103D1     1   2              3
*         TERMINALS: A   G              K
Qpnp      6         4   1              Pfor       OFF
Qnpn      4         6   5              Nfor       OFF
Rfor      6         4   5G
Rrev      1         4   5G
Rshort    6         5   1MEG
Rlat      2         6   9.09
Ron       3         5   513.4m
Dfor      6         4   Zbrk
```

```
25  Drev      1              4   Zbrk
26  Dgate     6              5   Zgate
27  .MODEL    Zbrk           D   (IS=3.2E-16     IBV=100U    BV=400)
28  .MODEL    Zgate          D   (IS=1E-16       IBV=100U    BV=10       VJ=0.3)
29  .MODEL    Pfor           PNP(IS=5E-15        BF=6.10     CJE=5p      CJC=2p
              TF=0.3U)
30  .MODEL    Nfor           NPN(IS=1E-12        ISE=1E-9    BF=10.0     RC=0.45
              CJE=30p        CJC=2p          TF=0.3U)
31  .ENDS
32
33  .SUBCKT   EC103M1        1   2               3
34  *         TERMINALS:     A   G               K
35  Qpnp      6              4   1               Pfor        OFF
36  Qnpn      4              6   5               Nfor        OFF
37  Rfor      6              4   5G
38  Rrev      1              4   5G
39  Rshort    6              5   1MEG
40  Rlat      2              6   9.09
41  Ron       3              5   513.4m
42  Dfor      6              4   Zbrk
43  Drev      1              4   Zbrk
44  Dgate     6              5   Zgate
45  .MODEL    Zbrk           D   (IS=3.2E-16     IBV=100U    BV=600)
46  .MODEL    Zgate          D   (IS=1E-16       IBV=100U    BV=10       VJ=0.3)
47  .MODEL    Pfor           PNP(IS=5E-15        BF=6.10     CJE=5p      CJC=2p
              TF=0.3U)
48  .MODEL    Nfor           NPN(IS=1E-12        ISE=1E-9    BF=10.0     RC=0.45
              CJE=30p        CJC=2p          TF=0.3U)
49  .ENDS
50
51  .SUBCKT   EC103D2        1   2               3
52  *         TERMINALS:     A   G               K
53  Qpnp      6              4   1               Pfor        OFF
54  Qnpn      4              6   5               Nfor        OFF
55  Rfor      6              4   5G
56  Rrev      1              4   5G
57  Rshort    6              5   1MEG
58  Rlat      2              6   9.09
59  Ron       3              5   513.4m
60  Dfor      6              4   Zbrk
61  Drev      1              4   Zbrk
62  Dgate     6              5   Zgate
63  .MODEL    Zbrk           D   (IS=3.2E-16     IBV=100U    BV=400)
64  .MODEL    Zgate          D   (IS=1E-16       IBV=100U    BV=10       VJ=0.3)
65  .MODEL    Pfor           PNP(IS=5E-15        BF=2.20     CJE=5p      CJC=2p
              TF=0.3U)
66  .MODEL    Nfor           NPN(IS=1E-12        ISE=1E-9    BF=10.0     RC=0.45
              CJE=30p        CJC=2p          TF=0.3U)
67  .ENDS
68
69  .SUBCKT   EC103M2        1   2               3
70  *         TERMINALS:     A   G               K
71  Qpnp      6              4   1               Pfor        OFF
72  Qnpn      4              6   5               Nfor        OFF
73  Rfor      6              4   5G
74  Rrev      1              4   5G
75  Rshort    6              5   1MEG
```

```
76  Rlat      2              6   9.09
77  Ron       3              5   513.4m
78  Dfor      6              4   Zbrk
79  Drev      1              4   Zbrk
80  Dgate     6              5   Zgate
81  .MODEL    Zbrk           D   (IS=3.2E-16    IBV=100U   BV=600)
82  .MODEL    Zgate          D   (IS=1E-16      IBV=100U   BV=10      VJ=0.3)
83  .MODEL    Pfor           PNP(IS=5E-15       BF=2.20    CJE=5p     CJC=2p
              TF=0.3U)
84  .MODEL    Nfor           NPN(IS=1E-12       ISE=1E-9   BF=10.0    RC=0.45
            CJE=30p        CJC=2p         TF=0.3U)
85  .ENDS
86
87  .SUBCKT   EC103D         1   2              3
88  *         TERMINALS:     A   G              K
89  Qpnp      6              4   1              Pfor       OFF
90  Qnpn      4              6   5              Nfor       OFF
91  Rfor      6              4   5G
92  Rrev      1              4   5G
93  Rshort    6              5   1MEG
94  Rlat      2              6   9.09
95  Ron       3              5   513.4m
96  Dfor      6              4   Zbrk
97  Drev      1              4   Zbrk
98  Dgate     6              5   Zgate
99  .MODEL    Zbrk           D   (IS=3.2E-16    IBV=100U   BV=400)
100 .MODEL    Zgate          D   (IS=1E-16      IBV=100U   BV=10      VJ=0.3)
101 .MODEL    Pfor           PNP(IS=5E-15       BF=1.10    CJE=5p     CJC=2p
              TF=0.3U)
102 .MODEL    Nfor           NPN(IS=1E-12       ISE=1E-9   BF=10.0    RC=0.45
            CJE=30p        CJC=2p         TF=0.3U)
103 .ENDS
104
105 .SUBCKT   EC103M         1   2              3
106 *         TERMINALS:     A   G              K
107 Qpnp      6              4   1              Pfor       OFF
108 Qnpn      4              6   5              Nfor       OFF
109 Rfor      6              4   5G
110 Rrev      1              4   5G
111 Rshort    6              5   1MEG
112 Rlat      2              6   9.09
113 Ron       3              5   513.4m
114 Dfor      6              4   Zbrk
115 Drev      1              4   Zbrk
116 Dgate     6              5   Zgate
117 .MODEL    Zbrk           D   (IS=3.2E-16    IBV=100U   BV=600)
118 .MODEL    Zgate          D   (IS=1E-16      IBV=100U   BV=10      VJ=0.3)
119 .MODEL    Pfor           PNP(IS=5E-15       BF=1.10    CJE=5p     CJC=2p
              TF=0.3U)
120 .MODEL    Nfor           NPN(IS=1E-12       ISE=1E-9   BF=10.0    RC=0.45
            CJE=30p        CJC=2p         TF=0.3U)
121 .ENDS
122
123 .SUBCKT   EC103D3        1   2              3
124 *         TERMINALS:     A   G              K
125 Qpnp      6              4   1              Pfor       OFF
126 Qnpn      4              6   5              Nfor       OFF
```

```
Rfor 6 4 5G
Rrev 1 4 5G
Rshort 6 5 1MEG
Rlat 2 6 9.09
Ron 3 5 513.4m
Dfor 6 4 Zbrk
Drev 1 4 Zbrk
Dgate 6 5 Zgate
.MODEL Zbrk D (IS=3.2E-16 IBV=100U BV=400)
.MODEL Zgate D (IS=1E-16 IBV=100U BV=10 VJ=0.3)
.MODEL Pfor PNP(IS=5E-15 BF=0.95 CJE=5p CJC=2p
TF=0.3U)
.MODEL Nfor NPN(IS=1E-12 ISE=1E-9 BF=10.0 RC=0.45
CJE=30p CJC=2p TF=0.3U)
.ENDS

.SUBCKT EC103M3 1 2 3
* TERMINALS: A G K
Qpnp 6 4 1 Pfor OFF
Qnpn 4 6 5 Nfor OFF
Rfor 6 4 5G
Rrev 1 4 5G
Rshort 6 5 1MEG
Rlat 2 6 9.09
Ron 3 5 513.4m
Dfor 6 4 Zbrk
Drev 1 4 Zbrk
Dgate 6 5 Zgate
.MODEL Zbrk D (IS=3.2E-16 IBV=100U BV=600)
.MODEL Zgate D (IS=1E-16 IBV=100U BV=10 VJ=0.3)
.MODEL Pfor PNP(IS=5E-15 BF=0.95 CJE=5p CJC=2p
TF=0.3U)
.MODEL Nfor NPN(IS=1E-12 ISE=1E-9 BF=10.0 RC=0.45
CJE=30p CJC=2p TF=0.3U)
.ENDS

.SUBCKT S4S1 1 2 3
* TERMINALS: A G K
Qpnp 6 4 1 Pfor OFF
Qnpn 4 6 5 Nfor OFF
Rfor 6 4 5G
Rrev 1 4 5G
Rshort 6 5 1MEG
Rlat 2 6 9.09
Ron 3 5 513.4m
Dfor 6 4 Zbrk
Drev 1 4 Zbrk
Dgate 6 5 Zgate
.MODEL Zbrk D (IS=3.2E-16 IBV=100U BV=400)
.MODEL Zgate D (IS=1E-16 IBV=100U BV=10 VJ=0.3)
.MODEL Pfor PNP(IS=5E-15 BF=6.10 CJE=5p CJC=2p
TF=0.3U)
.MODEL Nfor NPN(IS=1E-12 ISE=1E-9 BF=10.0 RC=0.45
CJE=30p CJC=2p TF=0.3U)
.ENDS

.SUBCKT S6S1 1 2 3
```

```
178  *          TERMINALS:  A  G              K
179  Qpnp       6           4  1              Pfor        OFF
180  Qnpn       4           6  5              Nfor        OFF
181  Rfor       6           4  5G
182  Rrev       1           4  5G
183  Rshort     6           5  1MEG
184  Rlat       2           6  9.09
185  Ron        3           5  513.4m
186  Dfor       6           4  Zbrk
187  Drev       1           4  Zbrk
188  Dgate      6           5  Zgate
189  .MODEL     Zbrk        D  (IS=3.2E-16    IBV=100U    BV=600)
190  .MODEL     Zgate       D  (IS=1E-16      IBV=100U    BV=10       VJ=0.3)
191  .MODEL     Pfor        PNP(IS=5E-15      BF=6.10     CJE=5p      CJC=2p
                TF=0.3U)
192  .MODEL     Nfor        NPN(IS=1E-12      ISE=1E-9    BF=10.0     RC=0.45
                CJE=30p     CJC=2p        TF=0.3U)
193  .ENDS
194
195  .SUBCKT    S4S2        1  2              3
196  *          TERMINALS:  A  G              K
197  Qpnp       6           4  1              Pfor        OFF
198  Qnpn       4           6  5              Nfor        OFF
199  Rfor       6           4  5G
200  Rrev       1           4  5G
201  Rshort     6           5  1MEG
202  Rlat       2           6  9.09
203  Ron        3           5  513.4m
204  Dfor       6           4  Zbrk
205  Drev       1           4  Zbrk
206  Dgate      6           5  Zgate
207  .MODEL     Zbrk        D  (IS=3.2E-16    IBV=100U    BV=400)
208  .MODEL     Zgate       D  (IS=1E-16      IBV=100U    BV=10       VJ=0.3)
209  .MODEL     Pfor        PNP(IS=5E-15      BF=2.20     CJE=5p      CJC=2p
                TF=0.3U)
210  .MODEL     Nfor        NPN(IS=1E-12      ISE=1E-9    BF=10.0     RC=0.45
                CJE=30p     CJC=2p        TF=0.3U)
211  .ENDS
212
213  .SUBCKT    S6S2        1  2              3
214  *          TERMINALS:  A  G              K
215  Qpnp       6           4  1              Pfor        OFF
216  Qnpn       4           6  5              Nfor        OFF
217  Rfor       6           4  5G
218  Rrev       1           4  5G
219  Rshort     6           5  1MEG
220  Rlat       2           6  9.09
221  Ron        3           5  513.4m
222  Dfor       6           4  Zbrk
223  Drev       1           4  Zbrk
224  Dgate      6           5  Zgate
225  .MODEL     Zbrk        D  (IS=3.2E-16    IBV=100U    BV=600)
226  .MODEL     Zgate       D  (IS=1E-16      IBV=100U    BV=10       VJ=0.3)
227  .MODEL     Pfor        PNP(IS=5E-15      BF=2.20     CJE=5p      CJC=2p
                TF=0.3U)
228  .MODEL     Nfor        NPN(IS=1E-12      ISE=1E-9    BF=10.0     RC=0.45
                CJE=30p     CJC=2p        TF=0.3U)
```

```
.ENDS

.SUBCKT S4S 1 2 3
* TERMINALS: A G K
Qpnp 6 4 1 Pfor OFF
Qnpn 4 6 5 Nfor OFF
Rfor 6 4 5G
Rrev 1 4 5G
Rshort 6 5 1MEG
Rlat 2 6 9.09
Ron 3 5 513.4m
Dfor 6 4 Zbrk
Drev 1 4 Zbrk
Dgate 6 5 Zgate
.MODEL Zbrk D (IS=3.2E-16 IBV=100U BV=400)
.MODEL Zgate D (IS=1E-16 IBV=100U BV=10 VJ=0.3)
.MODEL Pfor PNP(IS=5E-15 BF=1.10 CJE=5p CJC=2p
+ TF=0.3U)
.MODEL Nfor NPN(IS=1E-12 ISE=1E-9 BF=10.0 RC=0.45
+ CJE=30p CJC=2p TF=0.3U)
.ENDS

.SUBCKT S6S 1 2 3
* TERMINALS: A G K
Qpnp 6 4 1 Pfor OFF
Qnpn 4 6 5 Nfor OFF
Rfor 6 4 5G
Rrev 1 4 5G
Rshort 6 5 1MEG
Rlat 2 6 9.09
Ron 3 5 513.4m
Dfor 6 4 Zbrk
Drev 1 4 Zbrk
Dgate 6 5 Zgate
.MODEL Zbrk D (IS=3.2E-16 IBV=100U BV=600)
.MODEL Zgate D (IS=1E-16 IBV=100U BV=10 VJ=0.3)
.MODEL Pfor PNP(IS=5E-15 BF=1.10 CJE=5p CJC=2p
+ TF=0.3U)
.MODEL Nfor NPN(IS=1E-12 ISE=1E-9 BF=10.0 RC=0.45
+ CJE=30p CJC=2p TF=0.3U)
.ENDS

.SUBCKT S4S3 1 2 3
* TERMINALS: A G K
Qpnp 6 4 1 Pfor OFF
Qnpn 4 6 5 Nfor OFF
Rfor 6 4 5G
Rrev 1 4 5G
Rshort 6 5 1MEG
Rlat 2 6 9.09
Ron 3 5 513.4m
Dfor 6 4 Zbrk
Drev 1 4 Zbrk
Dgate 6 5 Zgate
.MODEL Zbrk D (IS=3.2E-16 IBV=100U BV=400)
.MODEL Zgate D (IS=1E-16 IBV=100U BV=10 VJ=0.3)
.MODEL Pfor PNP(IS=5E-15 BF=0.95 CJE=5p CJC=2p
```

```
                TF=0.3U)
282  .MODEL   Nfor        NPN(IS=1E-12      ISE=1E-9   BF=10.0     RC=0.45
               CJE=30p     CJC=2p       TF=0.3U)
283  .ENDS
284
285  .SUBCKT  S6S3        1   2            3
286  *        TERMINALS:  A   G            K
287  Qpnp     6           4   1            Pfor       OFF
288  Qnpn     4           6   5            Nfor       OFF
289  Rfor     6           4   5G
290  Rrev     1           4   5G
291  Rshort   6           5   1MEG
292  Rlat     2           6   9.09
293  Ron      3           5   513.4m
294  Dfor     6           4   Zbrk
295  Drev     1           4   Zbrk
296  Dgate    6           5   Zgate
297  .MODEL   Zbrk        D   (IS=3.2E-16   IBV=100U   BV=600)
298  .MODEL   Zgate       D   (IS=1E-16     IBV=100U   BV=10      VJ=0.3)
299  .MODEL   Pfor        PNP(IS=5E-15      BF=0.95    CJE=5p      CJC=2p
                TF=0.3U)
300  .MODEL   Nfor        NPN(IS=1E-12      ISE=1E-9   BF=10.0     RC=0.45
               CJE=30p     CJC=2p       TF=0.3U)
301  .ENDS
```