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ECE 150B

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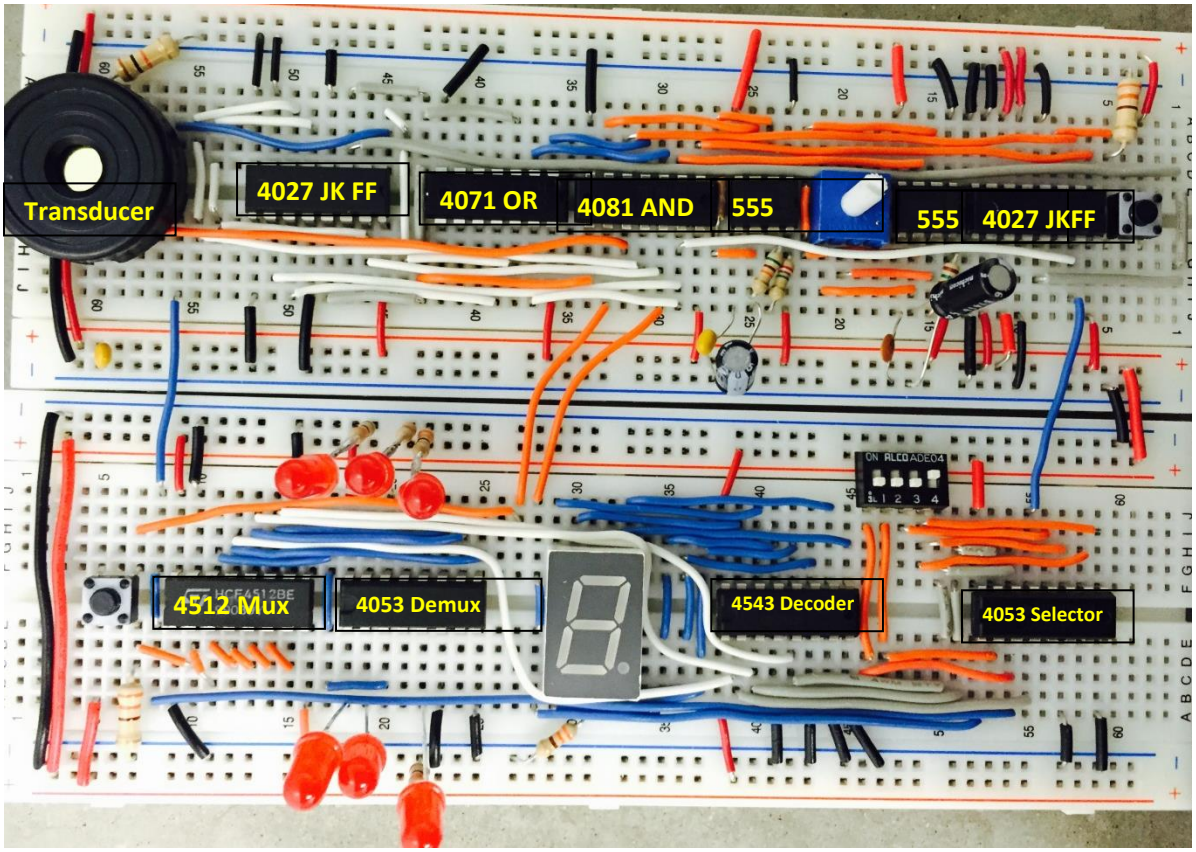
Project 2: Timing, Multiplexing, and Demultiplexing

Abstract

This project aims to construct a circuit that resembles the functionalities of a 6-channel telegraph system. With 6 inputs through a multiplexer, the output through a demultiplexer is produced at the clock pulses of varying speeds.

Diagram

Image 1 [Top view]



Explanation of Design

1. *Inventory of parts (#)*
    a. Push toggle switch (2 units)
        i. The function of a push button switch is to toggle a flip flop when closed. Debouncing was not necessary as the toggling of JK flip flop worked fine without it.
    b. 4027 [JK Flip Flop] (4 gates, 2 chips)
        i. A JK flip flop gate was used to toggle between the two timer speeds with some logic involving an AND and an OR gate. 3 gates were used for counter setup configuration with synchronous clock.
    c. 555 [Astable model] (2 units)
        i. Calculation of the frequency to meet max. 1 kHz and 0.5 Hz
        ii. The formula for the frequency of a 555 astable timer is defined as the following: f = 1.44 / [(R1+2R2)C]

            Therefore,

            1. **1 kHz**: f= 1.44/[(R1)C]; R1 = 1.44 kΩ, C = 1.0 µF
            2. **0.5 Hz**: f= 1.44/[(R1+2R2]C]; R1 = 2.7 MΩ, R2 = 51 kΩ, C = 1.0 µF

The maximum of 1 kHz frequency was met by setting R2, the resistance through a potentiometer, equal to zero. As turning the knob on the potentiometer increases the resistance, this action increases the total resistance value, R1+2R2, which then decreases the frequency. Thus, R1 was set to 1.44 Ω and C = 1.0 µF. The frequency is then bounded by the upper limit at 1 kHz. The lower requirement of 0.5 Hz was met by setting R1 = 2.7 MΩ, R2 = 51 kΩ, and C = 1.0 µF.

    d. Potentiometer 103 [10k Ω] (1 unit)
        i. The role of a potentiometer is to be able to adjust the resistance for the timer to change its frequency
    e. 4081 [AND] (4 gates, 1 chip)
        i. Two as part of the logic to toggle between two timer speeds and to provide an input combination for the counter; one as a logic for counter j, k input; one as a combinational logic for the transducer
    f. 4071 [OR] (2 gates, 1 chip)
        i. As part of the logic to toggle between two timer speeds and to provide an input combination for the counter; one as a logic for counter j, k input
    g. 4053 [triple 2-bit selector(mux)] (1 chip)
        i. Used to select between DIP switch inputs and counter inputs, depending upon a designated select switch
    h. 4543 [BCD-decimal decoder] (1 chip)
        i. Necessary for display on 7-seg display module
    i. 7-segment display (1 unit)
        i. Necessary for displaying the channel number 1-6
    j. 4051 [Demux]

    i. Needed to produce 6 outputs based on the control bits
k. 4512 [Mux]
    i. In order to input 6 data and output 1 single line, to be transferred to the demux
l. Piezoelectric transducer (1 unit)
    i. To indicate whether the inputs (HIGH) to the mux have been added by a toggle push button switch
m. DIP Switch
    i. To switch between manual and counter modes in counting; to supply LOW for 0 inputs for the selector (mux)
n. Resistors (330 Ω, 2.1 M Ω, 51 k Ω, 1.5 k Ω)
o. LED's
p. Capacitors
    i. Decoupling, astable timers

Color Coding

a. Red: Vdd
b. Gray: clock inputs; inputs to the BCD-to-binary decoder from the 2:1 selector
c. White: inputs for the j and k's of the jk flip flops for the counter
d. Blue: OR-ing the timer outputs of different speeds; inputting the decoded outputs into the 7-segment display; inputs for the 2:1 selector (HIGH states)
e. Orange: inputs for the 2:1 selector (LOW states), DIP switch control inputs into the 2:1 selector, the inputs for both timers until combined in an OR gate; inputs from a toggle push button switch to the multiplexer and transducer activation
f. Black: Vss

Use of Breadboards

a. As highlighted in Image 1, the two breadboards consist of a set of two astable timers, a 3-bit jk flip flop binary counter (1-6), 7 segmented display with a decode, a piezoelectric transducer and a set of mux-demux for transferring data and selecting based on the controls.
b. Two breadboards were used to build a 6-channel telegraph. The positions were determined based on the sequence from the functional block diagram. Although the transducer could have been AND-ed with a new timer to activate a higher pitch, this would require another breadboard allotted just for one purpose. By using a remaining AND gate I was able to put it on the bottom of the first board.

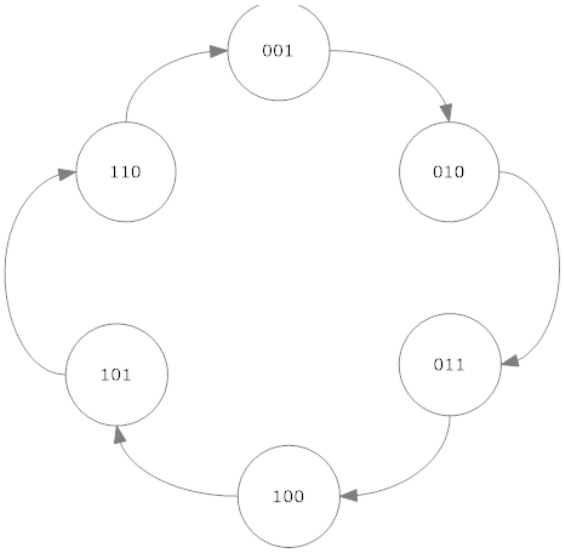
Design

Counter

State Table

Q2	Q1	Q0	Q2	Q1	Q0	J0	K0	J1	K1	J2	K2
0	0	1	0	1	0	x	1	1	X	0	X
0	1	0	0	1	1	1	X	x	0	0	X
0	1	1	1	0	0	x	1	x	1	1	X
1	0	0	1	0	1	1	X	0	X	x	0
1	0	1	1	1	0	x	1	1	X	x	0
1	1	0	0	0	1	1	X	x	1	x	1

State Diagram



Karnaugh Map

J0 = 1

q2q1 / q0	00	01	11	10
0	x	1	1	1
1	x	X	X	X

K0 = 1

q2q1 / q0	00	01	11	10
0	x	X	X	X
1	1	1	X	1

J1 = Q_0

q2q1 / q0	00	01	11	10
0	X	x	x	0
1	1	x	x	1

K1 = $Q_1 + Q_2$

q2q1 / q0	00	01	11	10
0	x	0	1	X
1	x	1	X	X

J2 = Q_0Q_1

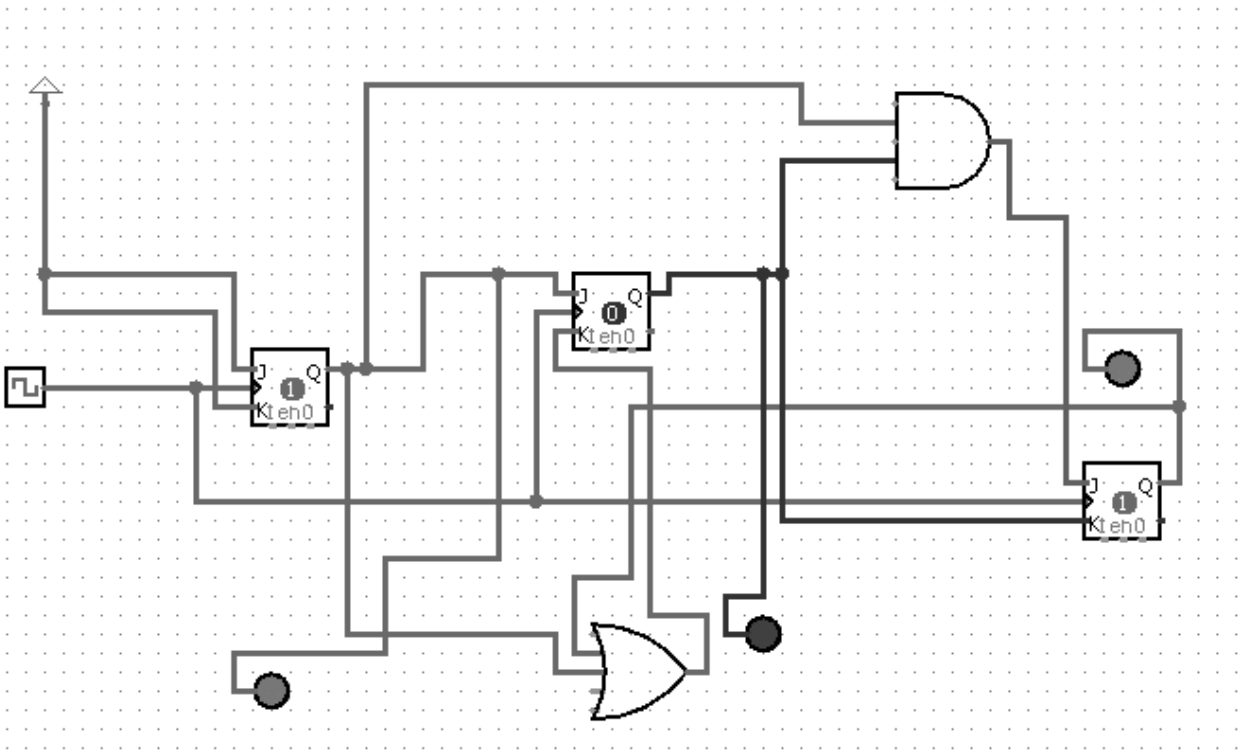
q2q1 / q01	00	01	11	10
0	x	0	x	x
1	0	1	x	X

K2 = Q_1

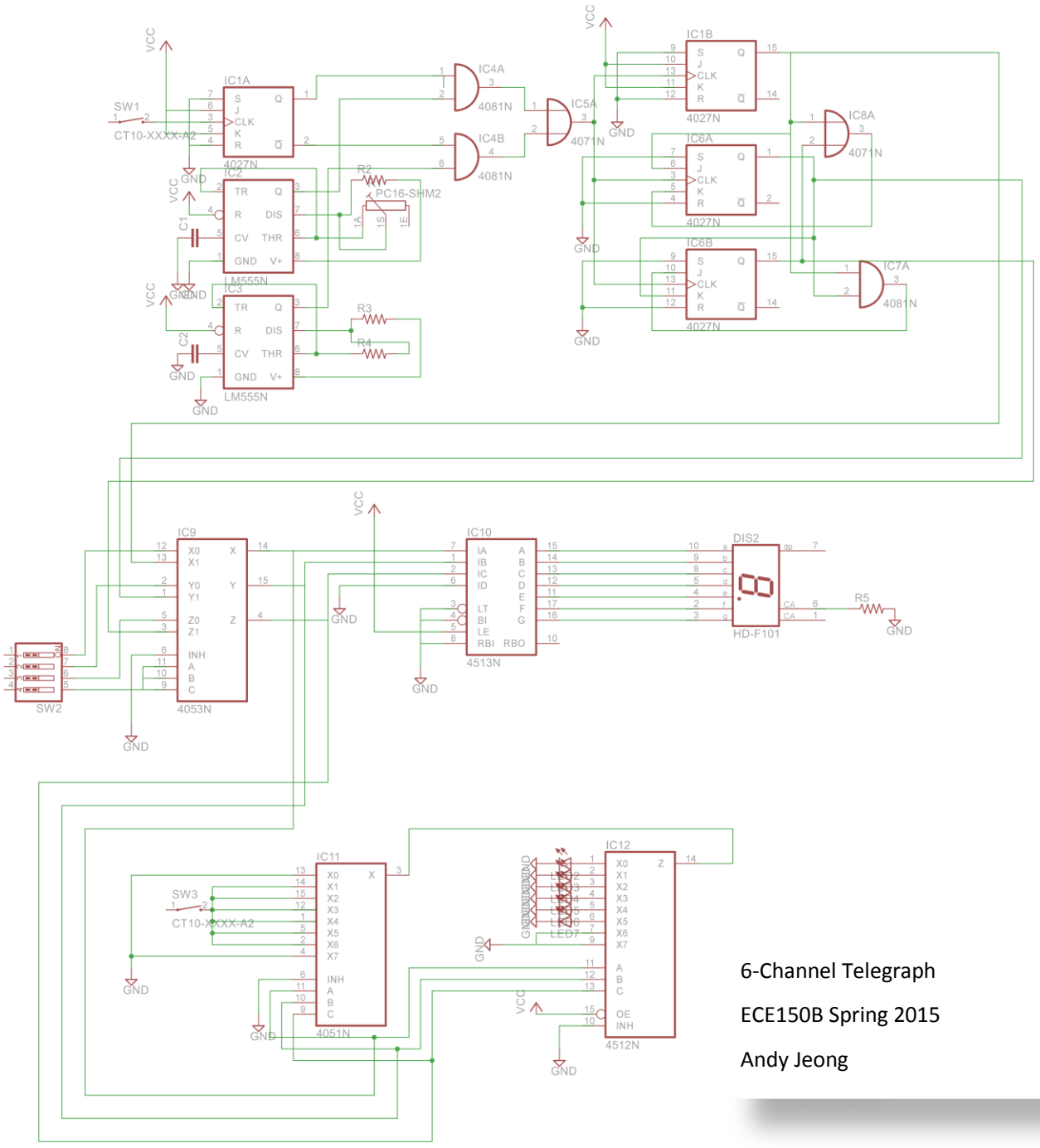
q2q1 / q0	00	01	11	10
0	x	x	1	0
1	x	x	x	0

Logic Diagram

3-bit Counter using JK Flip Flop



Schematic Diagram



Functional Block diagram