

# Lab 9 - Op Amps II

## Junior Projects II - ECE 394A

February 25, 2019

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### Abstract

In these lab experiments on operational amplifiers, potential deviations from the ideal behavior are observed through a larger scope of applications of the circuit and any non-idealistic behavior at a certain range of frequencies and input amplitudes is to be minimized.

# Introduction

This series of lab experiments seeks to demonstrate non-idealistic behavior in various operational amplifier circuit applications including integrator, differentiator, microphone amplifier, active rectifier and active clamp circuits, as well as aim to correct the causes of the distortions and glitches that might incur at high frequency ranges and input signals. In addition to general behavioral characteristics, observations on error-prone op amp chips are made through comparison between output responses from LF411 and LM741 chips, which are typically employed in op amp circuits.

# Experiments

## 1 Lab 9.1 Op-amp Limitations

### *Terms*

- (1) Input offset voltage: differential input voltage to force op-amp output to 0 volts
- (2) Input bias current: input current flowing into inputs of op-amp
- (3) Input offset current: differential input current at input terminals of op-amp
- (4) Slew rate: maximum rate at which voltage changes at the output

### *Components*

- (1) 1 LF411, 1 LM741 Op Amp
- (2) 10k $\Omega$ , 100 $\Omega$ , 100k $\Omega$  Resistors
- (3) 10k $\Omega$  potentiometer
- (4) 1 Power Supply (for +15 V, -15 V, GND)
- (5) 1 Oscilloscope

### 1.1 Slew Rate

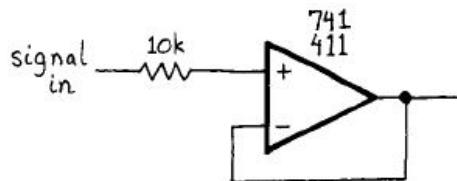


Figure 1: Slew rate measuring circuit

### *Slew Rate*

Slew Rate is the rate at which the signal changes at the output with respect to time. In general, for a square wave the two points in the peak-to-peak interval (each 10% apart from the ends of the interval) are measured and the

slope is determined to be the slew rate (these measurements assure that the slope is somewhat more straight line); For a sinusoidal wave input, the formula  $SR = 2\pi f A$ , where  $f$  is the maximum frequency and  $A$  is the maximum amplitude of the input signal, is used to determine the slew rate. As in Figure 1, a resistor is inserted at the input to lower the input impedance, which may be infinitely high.

## LF411

### Square Wave Input



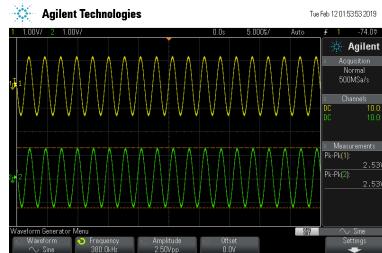
(a) Square Wave 1V at 1kHz, LF411



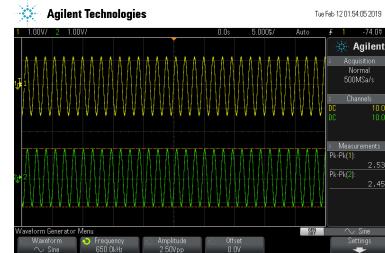
(b) Square Wave 1.25V at 1kHz, LF411

As the amplitude is increased, we begin to observe increased fluctuations in the signal in the transition.

### Sine Wave Input



(a) Sine Wave 2.5V at 380Hz, LF411



(b) Sine Wave 2.5V at 650Hz, LF411

Output amplitude begins to drop at  $V_{out}=2.53V$  as in (a),  
Output dropped by 0.08V (to 2.45V) in (b)

### Slew Rate Calculation

To calculate the slew rate, one would take points at 10% and 90% of the peaks of the output signal. By definition it involves 10-90 rise time in transition from one peak to the other, one needs to determine the relationship between the rise time and the bandwidth in the interval.

$$risetime[sec] = \frac{0.35}{Bandwidth[Hz]} \quad (1)$$

(1) frequency(f) = 1 kHz, period(T) =  $\frac{0.35}{f} = 3.5 * 10^{-4}$  seconds

(2)  $t_{rise} = duty_{cycle} (=50\%) * T$  seconds =  $1.75 * 10^{-4}$  seconds

(3) peak-to-peak( $dV_{out}$ ) = 0.6 - (-0.7) = 1.3 V

$$SlewRate_{Square} = \frac{dV_{out}}{t_{rise}} = \frac{1.3V}{1.75 * 10^{-4} sec} = 7428.57V/s = 7.43 * 10^{-3}V/\mu s \quad (2)$$

For sine wave input, slew rate =  $2\pi f A$  at zero crossings

where f = highest frequency of the signal, A = max peak voltage of the signal

$$SlewRate_{Sinusoidal} = 2\pi * 1kHz * 1.25V = 7853.98V/s = 7.853 * 10^{-3}V/\mu s \quad (3)$$

$$SlewRate_{SineWave} = 2\pi * 380Hz * 2.5V = 5969.02V/s = 5.969 * 10^{-3}V/\mu s \quad (4)$$

$$SlewRate_{SineWave} = 2\pi * 650Hz * 2.5V = 10210.18V/s = 1.021 * 10^{-2}V/\mu s \quad (5)$$

### Results

The slew rates obtained from square wave input is approximately equal to that obtained from sine wave, as  $7.43 * 10^{-3} V/\mu s \approx 7.853 * 10^{-3} V/\mu s$ , because using the same op amp chip which has defined slew rate (experimentally, according to the data sheet), it should give similar, if not the same, rate for different input signals.

### LM741

#### Square Wave Input



Figure 4: Square Wave 1.25V at 1kHz, LM741

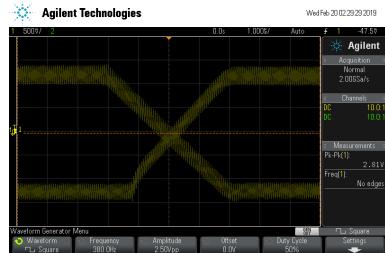
(1) frequency(f) = 1 kHz, period(T) =  $0.35/f = 3.5 * 10^{-4}$  seconds

(2)  $t_{rise} = duty_{cycle}(= 50\%) * period(T$  sec) =  $1.75 * 10^{-4}$  seconds

(3) peak-to-peak( $dV_{out}$ ) = 0.6 - (-0.7) = 1.3 V

$$SlewRate_{Square} = \frac{dV_{out}}{t_{rise}} = \frac{1.53V}{1.75 * 10^{-4}sec} = 8742.86V/s = 8.74 * 10^{-3}V/\mu s \quad (6)$$

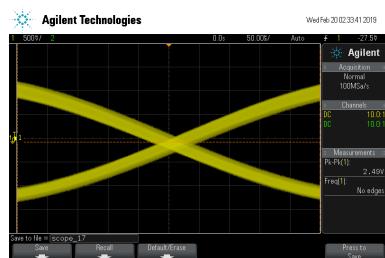
Sine Wave Input



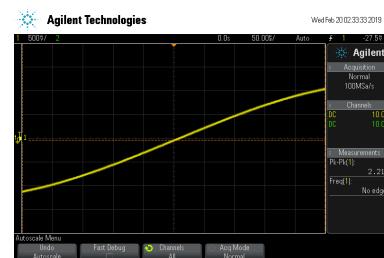
(a) Sine Wave input 2.5V at 380Hz, LM741



(b) Sine Wave output 2.5V at 380Hz, LM741



(c) Sine Wave input 2.5V at 650kHz, LM741



(d) Sine Wave output 2.5V at 650kHz, LM741

Similar to LF411,

$$SlewRate_{Sinusoidal} = 2\pi * 1kHz * 1.25V = 7853.98V/s = 7.853 * 10^{-3}V/\mu s \quad (7)$$

$$SlewRate_{SineWave} = 2\pi * 380Hz * 2.5V = 5969.02V/s = 5.969 * 10^{-3}V/\mu s \quad (8)$$

$$SlewRate_{SineWave} = 2\pi * 650Hz * 2.5V = 10210.18V/s = 1.021 * 10^{-2}V/\mu s \quad (9)$$

### Results

The slew rate for the sine wave input is observed to be higher than that of the square wave. This may be due to less stable responses produced by LM741 than by LF411 with presence of distortions in the output, as seen in the oscilloscope.

*Due to lack of available probes in the lab, input-output relationship could not be seen simultaneously; however, the only difference between the two chips is the presence of distortions due to less stable response in LM741.*

## 1.2 Offset Voltage

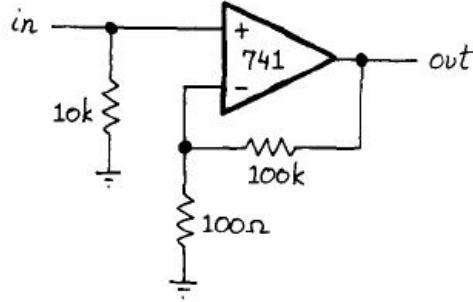


Figure 6: Slew Rate

The above Figure 6 shows a non-inverting amplifier with gain of 1,000. The output signal is shifted from the input signal by the offset voltage present in the op amp. Generally, offset voltage is incurred due to fabrication scattering parameters, and thus may not be seen in simulation.

### 1) Effects of $V_{offset}$

The circuit in Figure 6 itself shows the output with offset and bias voltage combined; therefore we can short the input in order to eliminate the bias current.

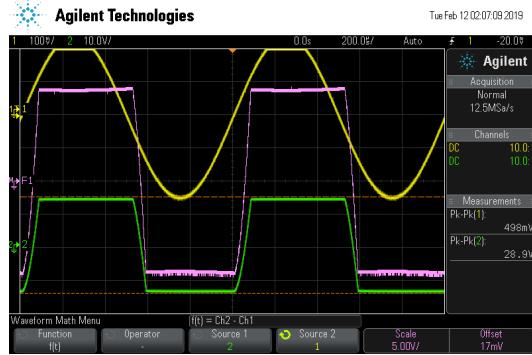


Figure 7:  $V_{offset}$

Figure 7 shows the input and amplified waveforms. In order to determine the offset in voltage, output-input operation is performed via math(subtraction operator) tool in the oscilloscope, displaying the offset (in pink) (which is the output wave(in green) minus the input wave (in yellow)).

$$V_{offset} = \frac{V_{max} - V_{min}}{10 * 1000} = \frac{28.7V}{10^4} = 2.87 \text{ mV} \quad (10)$$

The above equation is determined by taking the difference between the amplified waved and dividing by the total gain of the circuit which was  $10^4$ . The specification for LM741 has  $I_{bias} = 0.08\mu A$ , and the experimental value is  $I_{bias} = \frac{2.87mV}{10k\Omega} = 0.287\mu A$ , which is somewhat close in value.

## 2) Minimize the effect of $V_{offset}$ : offset trim

In order to minimize the effect of the offset voltage, we added an additional potentiometer across the amplifier as in Figure 8. In Figures 9a and 9b, we varied potentiometer and observed the output response.

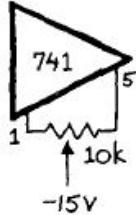


Figure 8:  $V_{offset}$

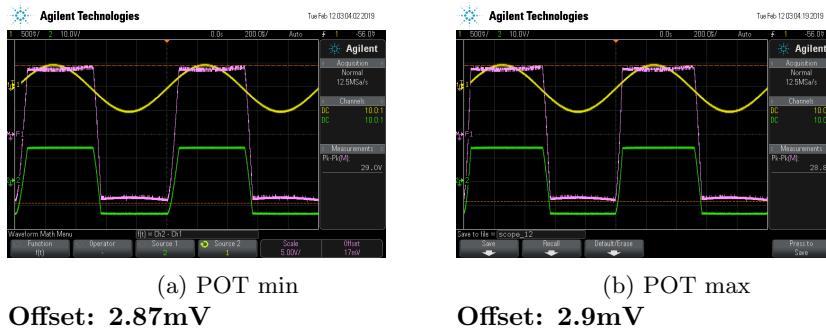


Figure 9:  $V_{offset}$  for each POT value

### 1.3 Bias Current

Since the offset voltage is minimized close to zero, only the effect of bias current remains. Since we already found the actual offset voltage, we can measure the bias current through the resistor  $R_{in}$  ( $10k$ ) with the input signal, creating an apparent additional  $V_{offset}$  equal to  $I_{Bias} * R_{in}$ . If the actual V offset has previously been measured and recorded, the change in apparent V offset due to the change in  $R_s$  can be determined, and  $I_{Bias}$  can then be easily computed. Experimental bias current is found to be  $0.287 \mu A$  and the reference values bound from  $0.08$  to  $0.5 \mu A$ .

$$I_{Bias} = \frac{V_{offset}}{R_{in}} = \frac{2.87mV}{10k\Omega} = 0.287 \mu A \quad (11)$$

#### 1.4 Offset Current

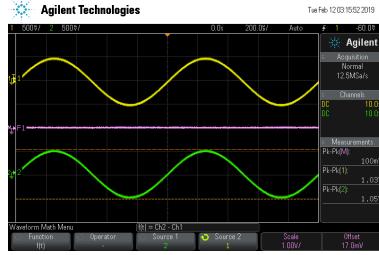


Figure 10: Bias Current Cancellation

In order to minimize the effect of bias current as input signal is added, we placed  $10k\Omega$  equivalent resistance using  $11k\Omega$  and  $100k\Omega$  resistors at the shorted input terminal ( $Req = R_{feedback1} \parallel R_{feedback2}$ ). This resistor carries the bias current that is flowing into the inverting terminal of the op amp, so that at the junction of the two feedback resistors remain in ground while the inverting terminal is allowed to go below ground. This allows for cancellation of the bias effect and only the offset current could be factored into the error, which we then measured as in Figure 10.

$$R_{eq} = 10k\Omega = \left(\frac{1}{R_1} + \frac{1}{R_2}\right)^{-1} \quad (12)$$

where  $R_1 = 11k\Omega$ ,  $R_2 = 100k\Omega$

The offset current from the adjusted voltage offset gives

$$I_{offset} = \frac{V_{offset}}{R_{in}} = \frac{100mV}{10k\Omega} = 10\mu A \quad (13)$$

In comparison with the specifications in the range from  $0.02\mu A$  to  $0.2\mu A$ , the value is relatively high. This may be due to poor adjustments in bias current adjustments and changes due to temperature in the amplifier chip.

#### Simulation Results

An LTspice simulation was done using a subcircuit design of the LM411 chip and LM741 chip (Appendix A & B). The 411 operational amplifier matched the input more than the 741 which transitioned much slower. For the later parts, the LM411 sub-circuit design did not have the proper pins, one and five (null pins), to simulate.

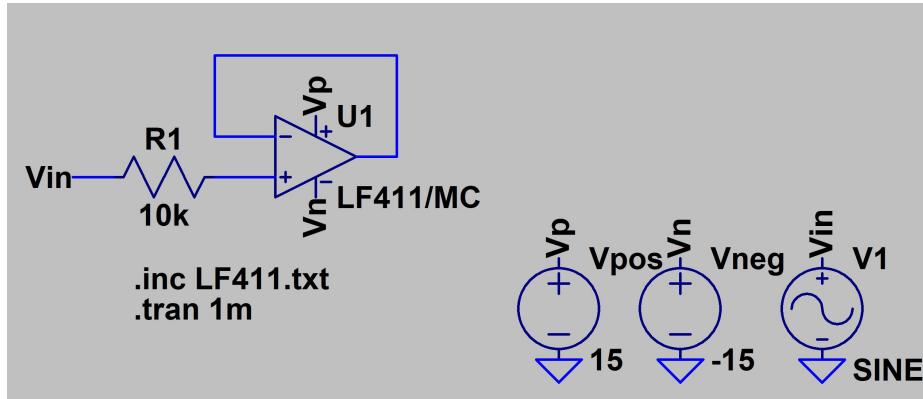


Figure 11: The Schematic of Lab 9.1 in LTSpice

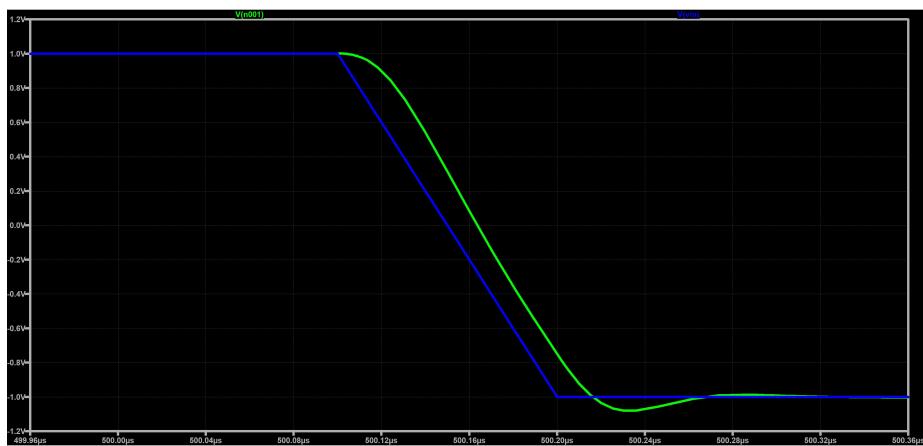


Figure 12: A square wave was the input for the LM411 chip. The transition from high to low was zoomed in on



Figure 13: A square wave was the input for the LM741 chip. The transition from high to low was zoomed in.

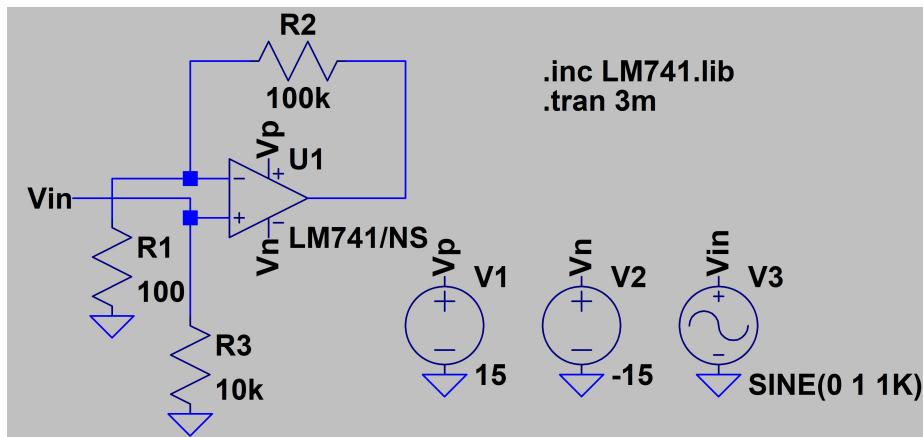


Figure 14: The Schematic of Lab 9.1 part 2 in LTSpice

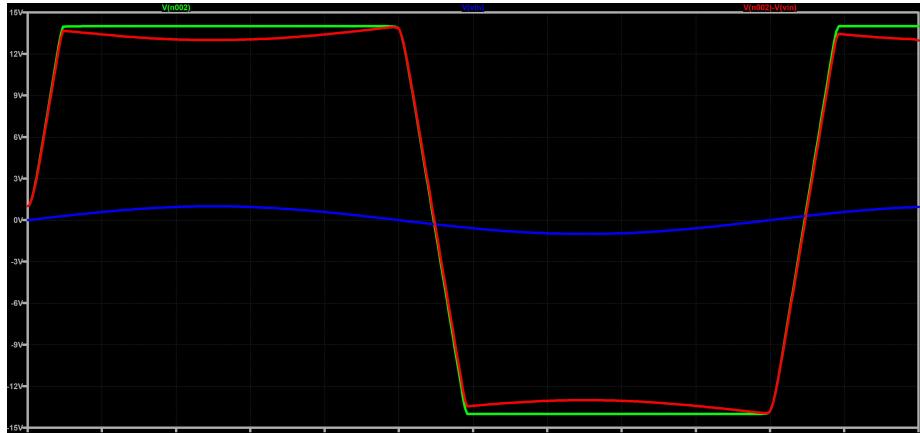


Figure 15: The offset from the input and output waves is shown in red. The effects of  $V_{offset}$  is shown.

### Summary and Discussion

Overall, the slew rate for LF411 showed better proximity in values for the square and sine waves, while the values for LM741 showed a larger difference between the rates for square and sine waves. This is due to the difference in input resistance - LM741 has  $2M\Omega$  while LF411 has much larger input resistance of  $10^{12} \Omega$ .

The voltage offset was determined by shorting the input, which eliminates the effect of the inherent bias in the op amp. Dividing the voltage difference in the input and output by the total gain, and then dividing by the input resistance, the experimental bias current of  $0.29\mu A$  came somewhat close to the theoretical value in the datasheet for LM741. This difference in the offset could be due to multiple factors including temperature, time(aging of the chip) and trimming considerations. These measures could yield a greater error in large op-amp implementations.

In order to nullify the effect of offset voltage, a potentiometer is inserted in the null pin of the op amp. This null pin connection increases the temperature drift in the op amp, but in general, it is a poor and rather error-prone practice with regards to temperature effects and stability, if applied to interconnected circuits.

## 2 Lab 9.2 - Integrator

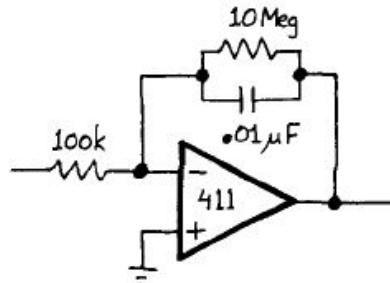


Figure 16: Integrator

### *Integrator*

An op-amp based integrator is realized by replacing the resistor(s) in the feedback loop with a capacitor. If there is only capacitor ( $X_C$ ) in the loop, it is a DC integrator, while if R-C network is in the feedback loop, it is referred to as an AC integrator.

### *DC integrator*

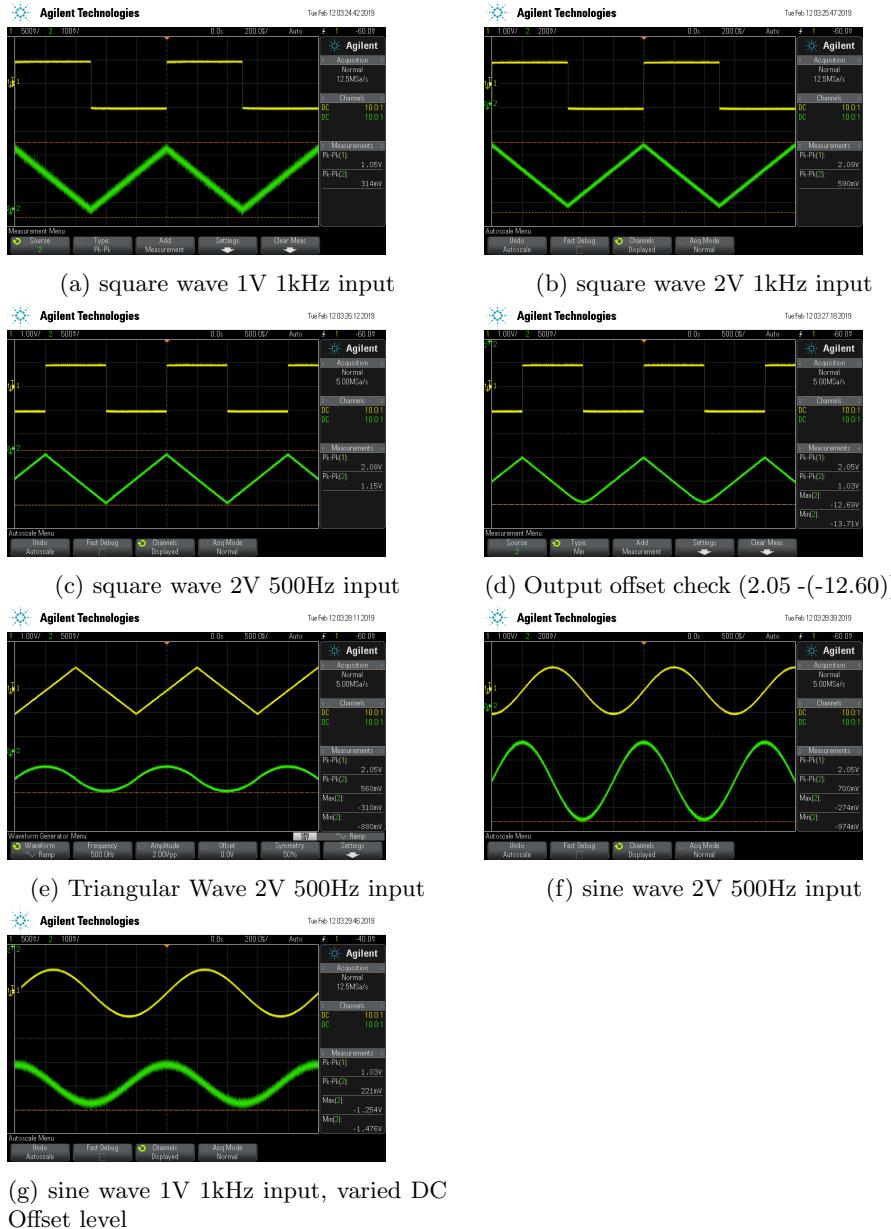
As the feedback capacitor, C begins to charge up due to the influence of the input voltage, its impedance  $X_C$  slowly increase in proportion to its rate of charge. The capacitor charges up at a rate determined by the RC time constant,  $\tau$ , of the series RC network. Negative feedback forces the op-amp to produce an output voltage that maintains a virtual earth at the op-amps inverting input.

Since the capacitor is connected between the op-amps inverting input (which is at earth potential) and the op-amps output (which is negative), the potential voltage,  $V_C$  developed across the capacitor slowly increases causing the charging current to decrease as the impedance of the capacitor increases. This results in the ratio of  $X_C/R_{IN}$  increasing producing a linearly increasing ramp output voltage that continues to increase until the capacitor is fully charged. The rate at which the output voltage increases (the rate of change) is determined by the value of the resistor and the capacitor, RC time constant.

### *AC integrator*

For an AC integrator, a sinusoidal input will produce another sine wave as its output which will be 90 degrees out-of-phase with the input producing a cosine wave.

$$\text{DC Gain} = -\frac{R_2}{R_1}, \text{ AC Gain} = -\frac{R_2}{R_1} * \frac{1}{1+2\pi f C R_2}, \text{ corner freq} = \frac{1}{2\pi C R_2}$$



### Components

- (1) 1 LF411 Op Amp
- (2) 100kΩ, 10MegΩ Resistors
- (3) 0.01μF capacitor (or equivalent)
- (4) 1 Power Supply (for +15 V, -15 V, GND)
- (5) 1 Oscilloscope

## Simulation Results

The LF411 subcircuit design was used (Appendix A).

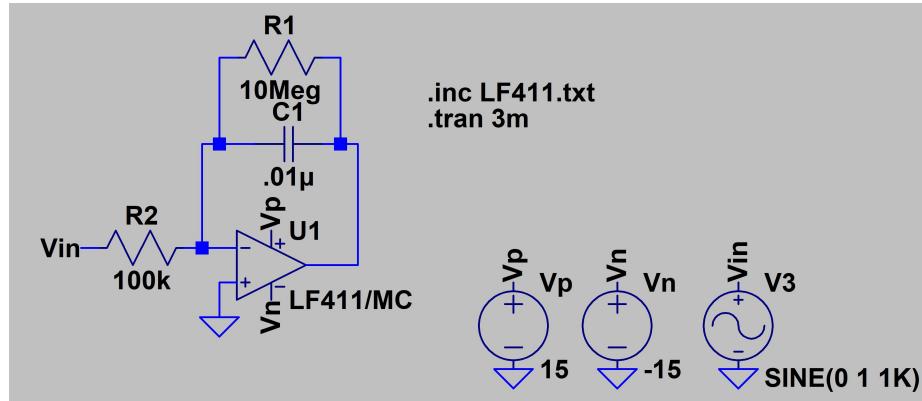


Figure 18: The Schematic of Lab 9.2 in LTSpice

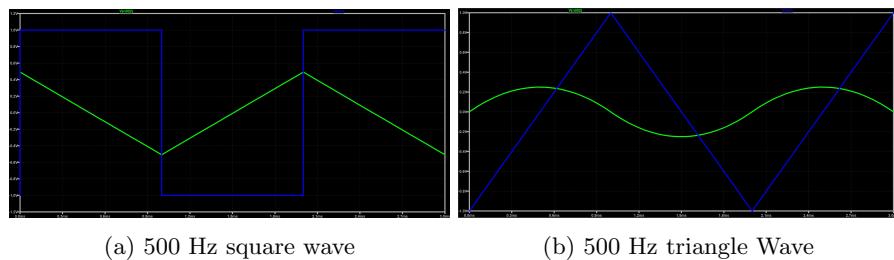


Figure 19: Different wave types applied to the AC integrator



Figure 20: 1 kHz Sine Wave

### Summary and Discussion

With the  $10 \text{ Meg}\Omega$  resistor added to the feedback loop in parallel with the capacitor for an R-C network, this integrates triangular and sinusoidal input waves into sinusoidal waves at the output as in Figures 19b and 20.

### 3 Lab 9.4 - AC Amplifier: Microphone Amplifier

In this experiment, a "single-supply" op amp is employed, allowing  $V_-$  to be ground, instead of at -15V, since the input operating common-mode range includes  $V_-$  and the output can swing up to  $V_-$ .

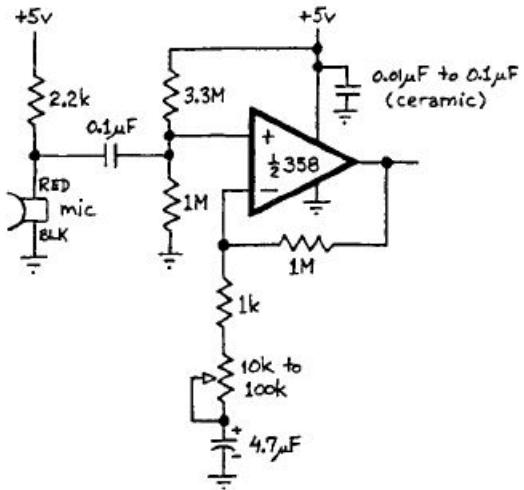


Figure 21: AC Amplifier

#### *Microphone Amplifier*

The purpose of a microphone amplifier is to amplify a signal of very small voltage (as little as 20mV) to a few volts level. In the AC amplifier configuration as in 21, the gain is 1 at DC as the input bias voltage is passed onto the output without amplification factor (since at DC  $4.7\mu\text{F}$  capacitor has infinite impedance). The microphone, which exploits variations in sound pressure, creating change the capacitance and thus voltage across the capacitor, and its internal FET buffer, generates output voltage through the pull-up  $2.2\text{k}\Omega$  resistor (by Ohm's Law). Thus the output impedance is simply the resistor value of  $2.2\text{k}\Omega$ .

#### *Components*

- (1) 1 LM324 "quad" Op Amp (replacement for LM358)
- (2)  $2.2\text{k}\Omega$ ,  $3.3\text{M}\Omega$ ,  $1\text{M}\Omega$ ,  $1\text{k}\Omega$  Resistors
- (3)  $10\text{k}\Omega$  Potentiometer
- (4)  $0.01\mu\text{F}$ ,  $4.7\mu\text{F}$ ,  $15\mu\text{F}$  Capacitor
- (5) 1 Microphone
- (6) 1 Power Supply (for  $+15\text{ V}$ ,  $-15\text{ V}$ , GND)
- (7) 1 Oscilloscope

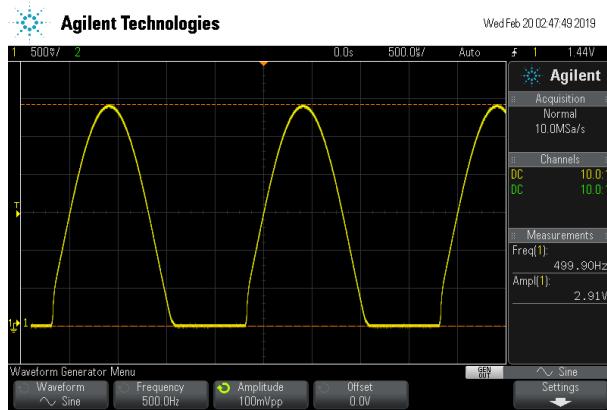


Figure 22: 100mV at 500Hz Input

### Simulation Results

The LM358 subcircuit design was used (Appendix C).

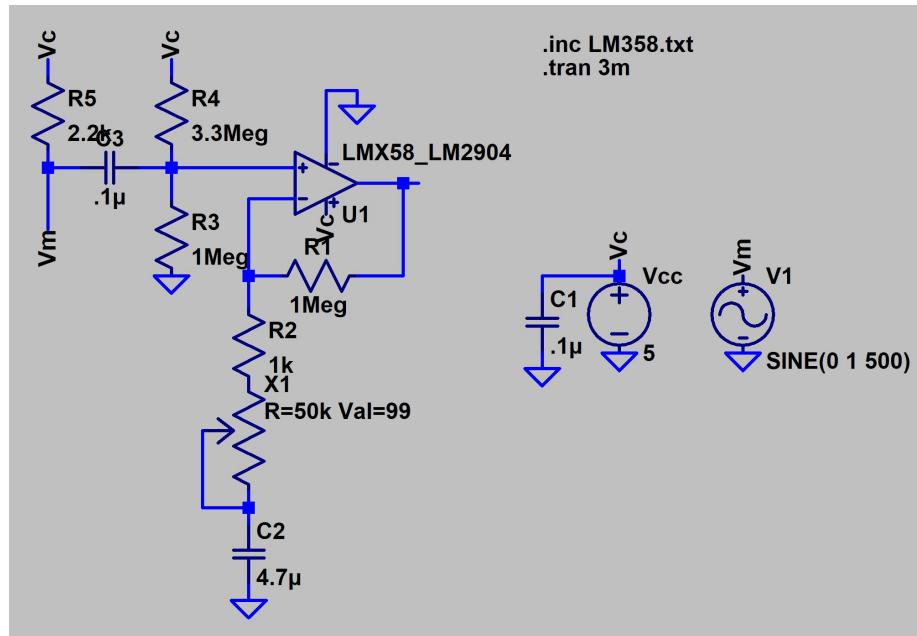


Figure 23: The Schematic of 9.4 in LTspice with the microphone being replaced with a signal generator

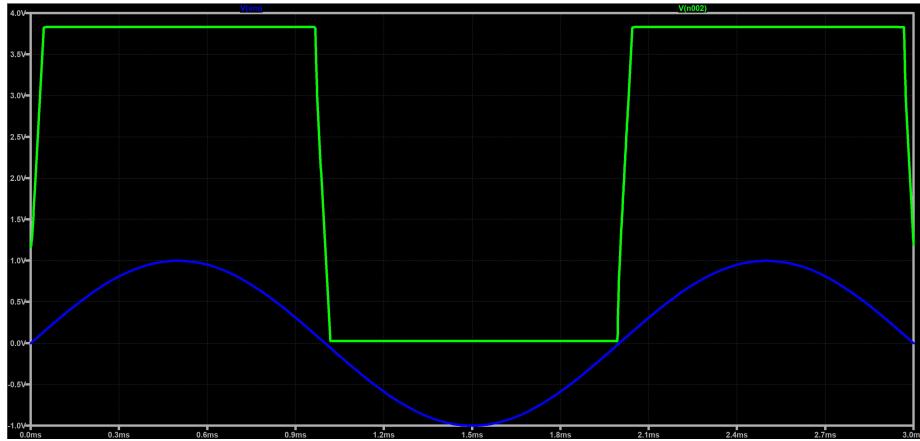


Figure 24: The input and output waves when using a sine wave at 500 Hz. The result differs from our experimental results where the wave at the output had noise as a factor where as in the simulation the noise is not present and the wave is clean.

### Summary and Discussion

Figure 22 shows output pulses from sine wave input of 100mV at 500Hz, which are voltage developed in the ground lines as the power supply filter capacitor is being recharged by the peaks of the rectifier output. These ground noise pulses appear due to poorly defining ground in the circuit. Specifically in this circuit, the type of microphone was important since the first type of microphone that was attempted resulted in no signal while a second microphone in the same configuration had worked correctly. Due to the nature of specific input required of a microphone, a simulation of this circuit as in Figure 23 was difficult to achieve.

## 4 Lab 9.5 - Active Rectifier

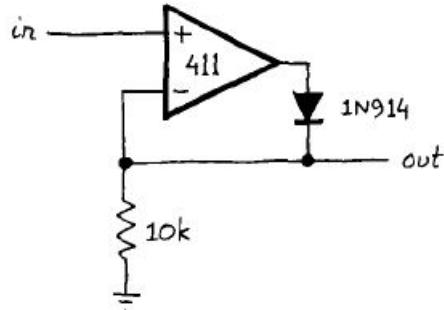
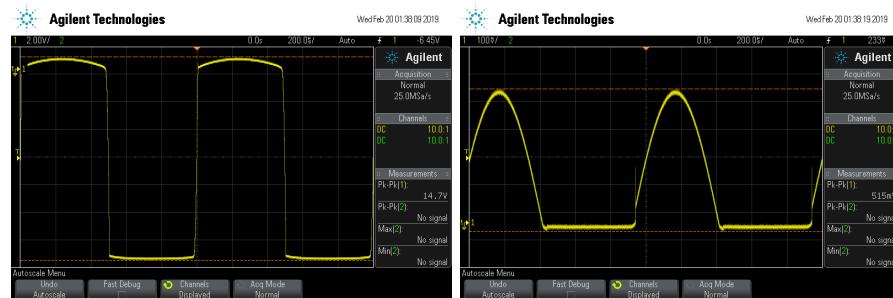


Figure 25: Active Rectifier



(a) output from low frequency sine wave (b) output from higher frequency sine wave input  
(100Hz)

Figure 26: Outputs of active rectifier

### Active Rectifier Circuit

Similar to a half-wave rectifier circuit with a diode, this rectifier circuit with op-amp performs similarly depending on the orientation of the diode. When the diode is forward biased, the current flows and the output matches the positive input signal, while for negative input signal, the diode is reverse biased and the output is 0.

- If diode is shorted(non-conducting), the circuit serves as a non-inverting amplifier.

- If diode is not shorted, then the results are as follows.

Bias Direction(F/R)	$V_{in}$	$V_{op\text{-}amp\text{-}output}$	$V_{out}$
Reverse	negative	negative( $=-V_{ee}$ )	0
Forward	positive	$V_{in} + V_{diode}$	$V_{in}$

The circuit is slew-rate limited, as the op amp output is  $-V_{ee}$  for negative input signals.

### Components

- (1) 1 LF411 Op Amp
- (2)  $10k\Omega$  Resistor
- (3) 1N914 Diode
- (4) 1 Power Supply (for +15 V, -15 V, GND)
- (5) 1 Oscilloscope for wavegen, graphical output

### Simulation Results

The LF411 subcircuit design was used (Appendix A). The distortion at the low voltage values at the output are similar to the ones seen on the oscilloscope in the lab.

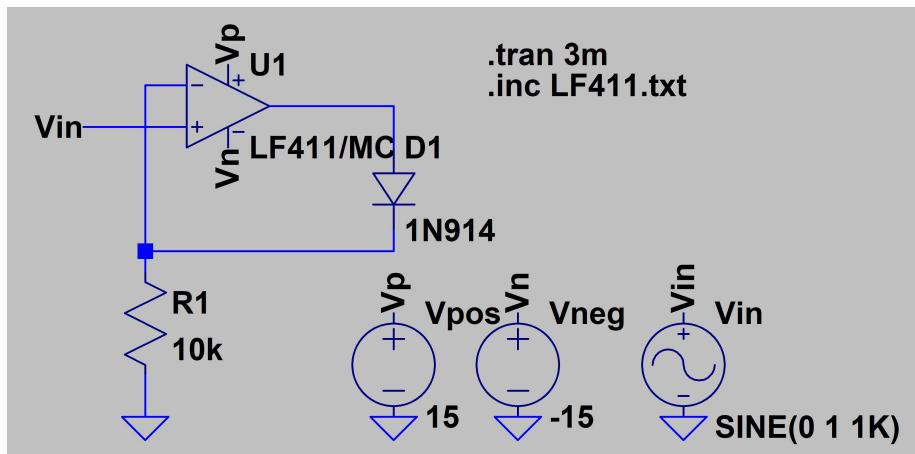


Figure 27: The Schematic of Lab 9.5 in LTSpice.

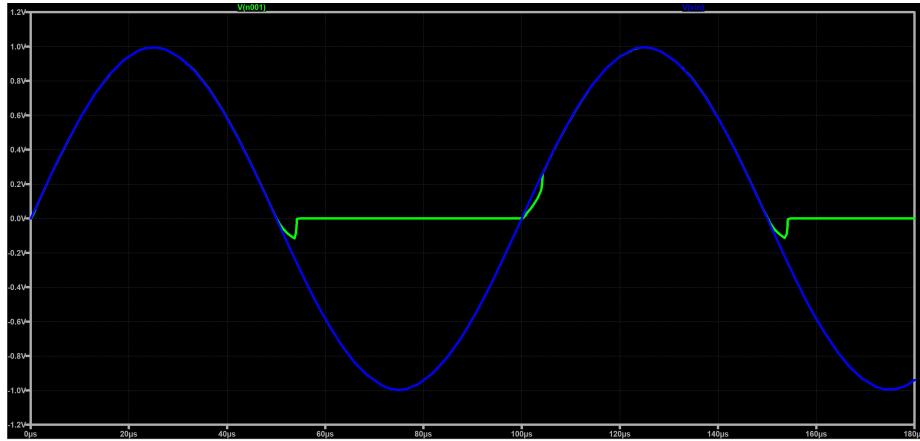


Figure 28: A high frequency sine wave was used as the input and the distortion of the rectifier is shown.

## Summary and Discussion

### *Questions*

(1) What causes the glitch?

Due to the voltage drop that occurs across the diode, there is a glitch created between the input and output.

(2) What happens at higher input frequencies? At the higher frequency, the delay between the input and output is more significant, causing greater level of distortion.

(3) Can this rectify signals of less than 0.6 volts?

This circuit cannot rectify input signals of less than 0.6 volts ( $V_{diode}$ )

(4) Explain distortions at transitions. When the input signal transitions from negative to positive, distortions occur as the circuit makes transition from an open-loop to closed-loop state. At the output of the op-amp, when the input is negative it remains at  $-V_{cc}$  level, and if it changes to positive the output response jumps to  $V_{in}$ .

## 5 Lab 9.6 - Improved Active Rectifier

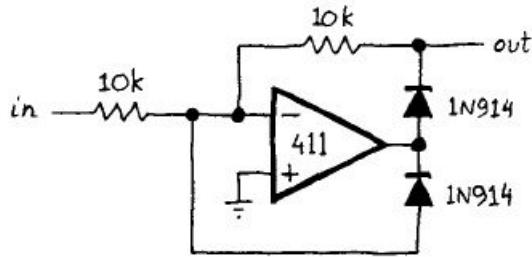
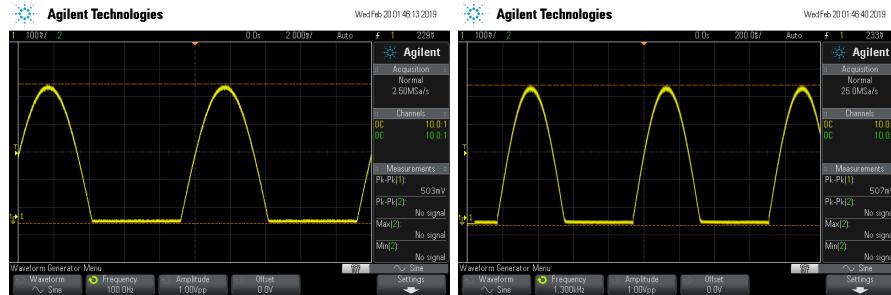


Figure 29: Improved Active Rectifier

### *Improved Active Rectifier Circuit*

This improved active rectifier circuit is an extension of the lab 9-5 with improvement of the circuit not reaching -Vee at the output for negative input signals and allowing faster response for the same slew rate as the lab 9-5.



(a) output from low frequency sine wave (100Hz) (b) output from higher frequency sine wave (1.3khz)

Figure 30: Outputs of improved active rectifier

### *Components*

- (1) 1 LF411 Op Amp
- (2) 2 10kΩ Resistor
- (3) 2 1N914 Diode
- (4) 1 Power Supply (for +15 V, -15 V, GND)
- (5) 1 Oscilloscope

$V_{in}$	$V_{op\text{-}amp\text{-}output}$	$V_{out}$
negative	$V_{out} + V_{diode}$	$-V_{in}$
positive	negative ( $V_{in} - V_{diode}$ )	0
from neg to pos	$+V_{diode}$ to $-V_{diode}$	$-V_{in}$ to 0

faster transition from -Vee to  $V_{diode}$  for the same slew rate than lab 9-5

## Simulation Results

The LF411 subcircuit design was used (Appendix A). Since a phototransistor could not be simulated in LTSpice properly, a voltmeter with incrementals steps was applied to the base. This would simulate different light levels on the LPT-100 phototransistor

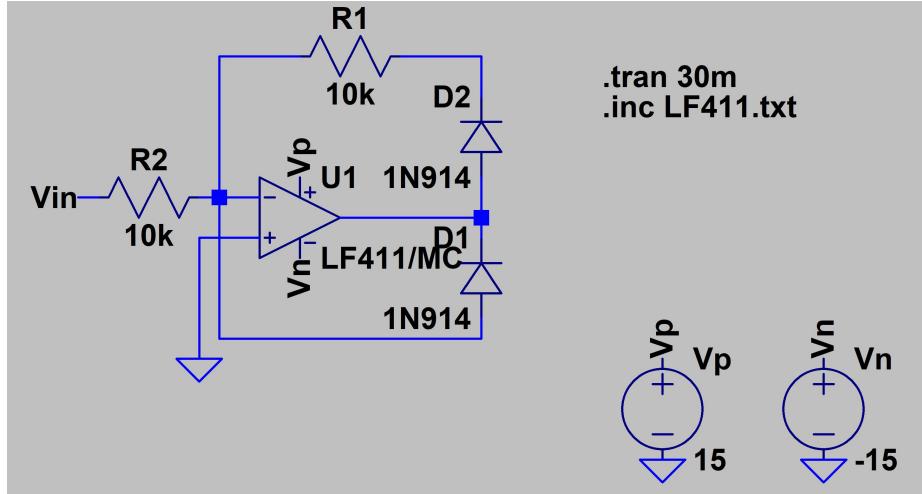
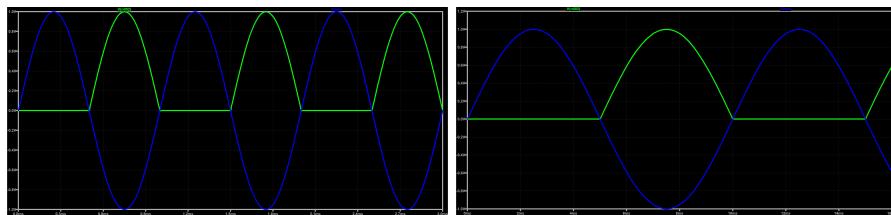


Figure 31: The Schematic of Lab 9.6 in LTSpice.



(a) High frequency Sine wave

(b) Low frequency Sine wave

Figure 32: Different frequencies applied to the improved rectifier.

## Summary and Discussion

### *Glitch Removal*

As shown above in the figures of this section and the previous section, there are slight differences in that in figure 25 there is distortion around the edges of the sine wave at high frequencies but in the graphs in figure 29 there is no distortion around the edges.

## 6 Lab 9.7 - Active Clamp

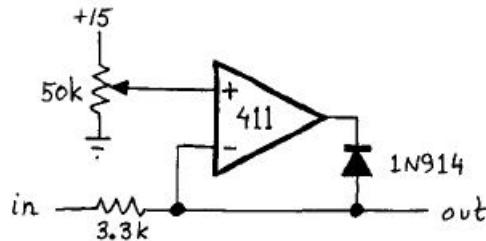


Figure 33: Active Clamp

In this lab experiment, we demonstrate a way of adding a DC offset to a signal using a summing op amp circuit.

### *Active Clamp Circuit*

Clipping and clamping operations are widely used with diodes in rectification for power supplies and radio frequency detection; clipping is simply bounding an input signal to a limited amplitude, and clamping is preventing a signal from going above or below a certain DC value or desired clamping level. While a diode and a few passive components realize such a clamp circuit, the addition of an op amp achieves an active clamp circuit. This clamp circuit, with the positive input terminal at zero volt, does not alter the peak-to-peak amplitude of the signal, but just shifts it up or down by a fixed value without the influence of the diode. This circuit using diodes exploits the property of diode in which it conducts current only in one direction and only input signal greater than its turn-on voltage of 0.6 V is transmitted across it.

In the circuit as in Figure 33, the circuit encloses the diode within the feedback loop, in which the diode is reverse biased from the output of the op amp to the measured output. This diode in the feedback loop causes the overall voltage gain at the output to significantly drop (almost negligible), due to the infinite gain of the op amp (diode voltage drop divided by large op amp gain). Since reverse-biased (unbiased), the circuit fixes the lower limit of the signal to zero volts, as the ground shows in (a), (b), (c), whereas for the case of forward-biased state, the voltage levels are shifted down due to negative bias as in (d).

In terms of impedance, the 3.3k ohm resistor at the input sets the input impedance of the circuit. When the diode is reversed-biased,

### Components

- (1) 1 LF411 Op Amp
- (2) 3.3k $\Omega$  resistors
- (3) 1 50k $\Omega$  Potentiometer
- (4) 1 1N914 Diode
- (5) 1 Power Supply (for +15 V, -15 V, GND)
- (6) 1 Oscilloscope for wavegen

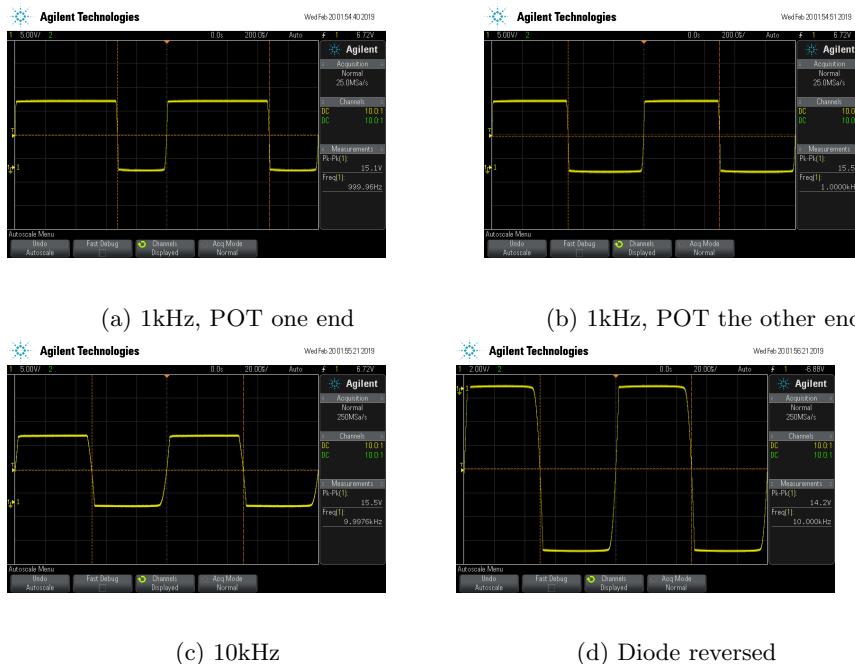


Figure 34: Active Clamp

### Simulation Results

The LF411 subcircuit design was used (Appendix A). The 50k linear potentiometer was used (Appendix D).

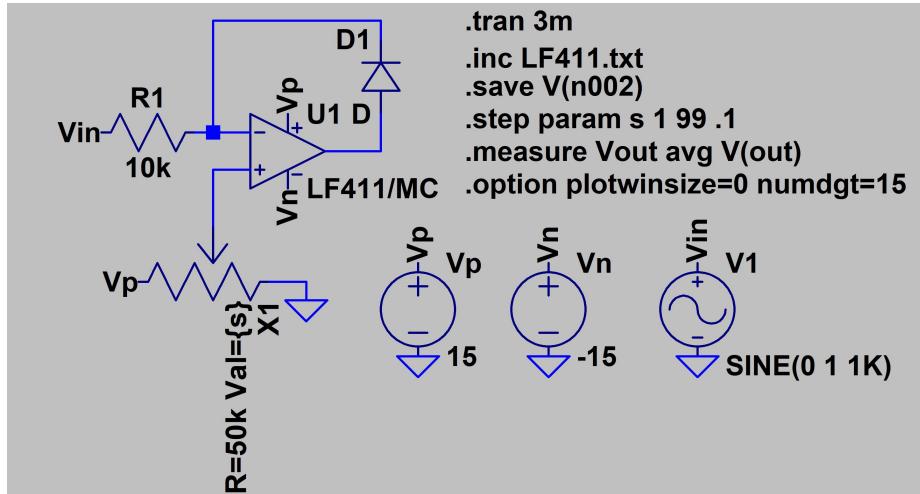
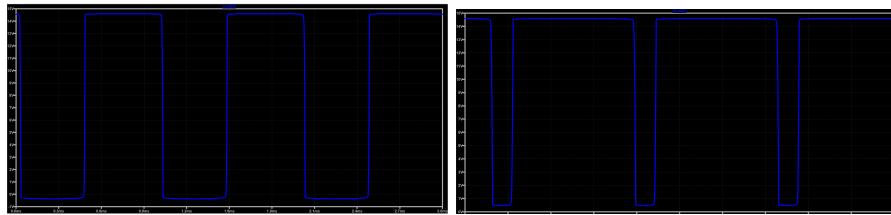


Figure 35: The Schematic of Lab 9.7 in LTSpice.



(a) At the edge of the potentiometer with the lowest impedance      (b) At the edge of the potentiometer with the highest impedance

Figure 36: Altering the potentiometer to achieve different wave forms from the clamp circuit

### Summary and Discussion

The results of the lab and simulation showed how the potentiometer could be used to control the width of the output wave. The clamping circuit keeps the current in one direction using the diode and the pot adjust the on time at the output. The active aspect shifts the voltage up and

### Overall Conclusions

Throughout implementations of various op-amp circuits of diverse applications, methods of mitigating distortions and imperfections at the output such as glitches have been explored and discussed in detail both experimentally on board and in simulation on LTSpice program. By analyzing the circuit behavior for

different inputs as well as by adjusting inherent bias in the op amp and induced offsets that may lead to practical error, future applications of these aforementioned circuit units could be better employed in a larger scale.

## Appendix A LF411 Subcircuit Design

```
1 * LF411 operational amplifier
2 * "macromodel" subcircuit
3 *
4 * connections:
5 *   1 - non-inverting input
6 *   2 - inverting input
7 *   3 - positive power supply
8 *   4 - negative power supply
9 *   5 - output
10 *
11 .subckt LF411/MC 1 2 3 4 5
12 *
13   c1    11 12 2.801E-12
14   c2     6  7  8.000E-12
15   css   10 99 3.200E-12
16   dc     5  53 dx
17   de     54  5 dx
18   dlp    90 91 dx
19   dln    92 90 dx
20   dp     4  3 dx
21   egnd  99  0 poly(2) (3,0) (4,0) 0 .5 .5
22   fb    7 99 poly(5) vb vc ve vlp vln 0 3.316E6
23 + -3E6 3E6 3E6 -3E6
24   ga    6  0 11 12 402.1E-6
25   gcm   0  6 10 99 12.72E-9
26   iss    3 10 dc 280.0E-6
27   hlim  90  0 vlim 1K
28   j1    11  2 10 jx
29   j2    12  1 10 jx
30   r2    6  9 100.0E3
31   rd1   4 11 2.487E3
32   rd2   4 12 2.487E3
33   ro1   8  5 40
34   ro2   7 99 60
35   rp    3  4 24.00E3
36   rss   10 99 714.3E3
37   vb    9  0 dc 0
38   vc    3 53 dc 1.100
39   ve    54  4 dc .3
40   vlim  7  8 dc 0
41   vlp   91  0 dc 30
42   vln   0 92 dc 30
43 .model dx D( Is=800.0E-18)
44 .model jx PJF( Is=30.00E-12 Beta=577.5E-6
45 + Vto=-1)
46 .ends
47 *$
```

## Appendix B LM741 Subcircuit Design

```
1 *///
2 * (C) National Semiconductor, Inc.
```

```

3 * Models developed and under copyright by:
4 * National Semiconductor, Inc.
5
6 *//*
7 * Legal Notice: This material is intended for free software support
8 * The file may be copied, and distributed; however, reselling the
9 * material is illegal
10
11 *//*
12 * For ordering or technical information on these models, contact:
13 * National Semiconductor's Customer Response Center
14 * 7:00 A.M.--7:00 P.M. U.S. Central Time
15 * (800) 272-9959
16 * For Applications support, contact the Internet address:
17 * amps-apps@galaxy.nsc.com
18
19 *///////////
20 *LM741 OPERATIONAL AMPLIFIER MACRO-MODEL
21 *///////////
22 *
23 * connections:      non-inverting input
24 *                  |      inverting input
25 *                  |      |      positive power supply
26 *                  |      |      negative power supply
27 *                  |      |      |      output
28 *
29 *
30 .SUBCKT LM741/NS    1    2    99   50   28
31 *
32 *Features:
33 *Improved performance over industry standards
34 *Plug-in replacement for LM709,LM201,MC1439,748
35 *Input and output overload protection
36 *
37 *****INPUT STAGE*****
38 *
39 IOS 2 1 20N
40 *^Input offset current
41 R1 1 3 250K
42 R2 3 2 250K
43 I1 4 50 100U
44 R3 5 99 517
45 R4 6 99 517
46 Q1 5 2 4 QX
47 Q2 6 7 4 QX
48 *Fp2=2.55 MHz
49 C4 5 6 60.3614P
50 *
51 *****COMMON MODE EFFECT*****
52 *
53 I2 99 50 1.6MA
54 *^Quiescent supply current

```

```

55 EOS 7 1 POLY(1) 16 49 1E-3 1
56 *Input offset voltage.^
57 R8 99 49 40K
58 R9 49 50 40K
59 *
60 *****OUTPUT VOLTAGE LIMITING*****
61 V2 99 8 1.63
62 D1 9 8 DX
63 D2 10 9 DX
64 V3 10 50 1.63
65 *
66 *****SECOND STAGE*****
67 *
68 EH 99 98 99 49 1
69 G1 98 9 5 6 2.1E-3
70 *Fp1=5 Hz
71 R5 98 9 95.493MEG
72 C3 98 9 333.33P
73 *
74 *****POLE STAGE*****
75 *
76 *Fp=30 MHz
77 G3 98 15 9 49 1E-6
78 R12 98 15 1MEG
79 C5 98 15 5.3052E-15
80 *
81 *****COMMON-MODE ZERO STAGE*****
82 *
83 *Fpcm=300 Hz
84 G4 98 16 3 49 3.1623E-8
85 L2 98 17 530.5M
86 R13 17 16 1K
87 *
88 *****OUTPUT STAGE*****
89 *
90 F6 50 99 POLY(1) V6 450U 1
91 E1 99 23 99 15 1
92 R16 24 23 25
93 D5 26 24 DX
94 V6 26 22 0.65V
95 R17 23 25 25
96 D6 25 27 DX
97 V7 22 27 0.65V
98 V5 22 21 0.18V
99 D4 21 15 DX
100 V4 20 22 0.18V
101 D3 15 20 DX
102 L3 22 28 100P
103 RL3 22 28 100K
104 *
105 *****MODELS USED*****
106 *
107 .MODEL DX D( IS=1E-15)
108 .MODEL QX NPN(BF=625)
109 *
110 .ENDS
111 *$
```

## Appendix C LM358 Subcircuit Design

```

1 ****
2 * LM358 *
3 ****
4 * LM358 OPERATIONAL AMPLIFIER "MACROMODEL" SUBCIRCUIT
5 * CREATED USING PARTS RELEASE 4.01 ON 09/08/89 AT 10:54
6 * (REV N/A) SUPPLY VOLTAGE: +/-5V
7 * CONNECTIONS: NON-INVERTING INPUT
8 * | INVERTING INPUT
9 * | | POSITIVE POWER SUPPLY
10 * | | | NEGATIVE POWER SUPPLY
11 * | | | | OUTPUT
12 * | | | |
13 .SUBCKT LM358 1 2 3 4 5
14   C1 11 12 5.544E-12
15   C2 6 7 20.00E-12
16   DC 5 53 DX
17   DE 54 5 DX
18   DLP 90 91 DX
19   DLN 92 90 DX
20   DP 4 3 DX
21   EGND 99 0 POLY(2) (3,0) (4,0) 0 .5 .5
22   FB 7 99 POLY(5) VB VC VE VLP VLN 0 15.91E6 -20E6 20E6 20E6 -20
      E6
23   GA 6 0 11 12 125.7E-6
24   GCM 0 6 10 99 7.067E-9
25   IEE 3 10 DC 10.04E-6
26   HLIM 90 0 VLIM 1K
27   Q1 11 2 13 QX
28   Q2 12 1 14 QX
29   R2 6 9 100.0E3
30   RC1 4 11 7.957E3
31   RC2 4 12 7.957E3
32   RE1 13 10 2.773E3
33   RE2 14 10 2.773E3
34   REE 10 99 19.92E6
35   RO1 8 5 50
36   RO2 7 99 50
37   RP 3 4 30.31E3
38   VB 9 0 DC 0
39   VC 3 53 DC 2.100
40   VE 54 4 DC .6
41   VLIM 7 8 DC 0
42   VLP 91 0 DC 40
43   VLN 0 92 DC 40
44 .MODEL DX D( IS=800.0E-18)
45 .MODEL QX PNP( IS=800.0E-18 BF=250)
46 .ENDS
47 *

```