

# Lab 10 - Op Amps III

## Junior Projects II - ECE 394A

March 22, 2019

### Contents

1	Lab 10.1 - Two Comparators . . . . .	2
2	Lab 10.2 - RC Oscillator . . . . .	9
3	Lab 10.3 - 7555 IC Oscillator(square wave) . . . . .	12
4	Lab 10.4 - Sawtooth Oscillator . . . . .	16
5	Lab 10.6 - Sine Wave Oscillator: Wien Bridge . . . . .	18
<b>A</b>	<b>LF411 Subcircuit Design</b>	<b>24</b>
<b>B</b>	<b>LM311 Subcircuit Design</b>	<b>24</b>
<b>C</b>	<b>7555 Subcircuit Design</b>	<b>25</b>

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### Abstract

In these lab experiments, various comparators and oscillator circuits were implemented to show how each component, mode of operation, and presence of input signals vary the output waveform response. By understanding of the intrinsic properties of the circuit in each stage of procession, the output characteristic waveform behaviors were examined and noted in detail for application in larger circuit designs. For comparators, op-amp based circuit, special comparator, and Schmitt Trigger circuits were closely tested in order such that the successive design improved a potential undesired effect of the previous one. For timer-based circuits and Wein Bridge oscillators, the waveforms for each mode of operation were observed to be varying by how the capacitor states fluctuate, and the desired gain was verified from root locus plot of multiple RC-networks.

## Introduction

This series of lab experiments seek to demonstrate the importance of comparators and different oscillator circuits. Specifically, the oscillator circuits each had properties that allowed for the different types of waveforms that were produced. In order to create the RC, IC, Sawtooth, and Sine Wave oscillators different timer configurations were used around the 7555 timer as well as modification of the waveforms using different resistor and capacitor combinations.

\* note: 7555 timer simulation of LTspice could not be conducted properly with desired parameters due to inability to adjust the parameters on the available subcircuit model.

## Experiments

### 1 Lab 10.1 - Two Comparators

#### *Comparator*

A comparator is a high-gain differential amplifier that compares two analog input voltages or currents and outputs a digital binary signal indicating which input is larger, such that

$$V_{out} = \begin{cases} V_{cc}, & \text{if } V_+ > V_- \\ 0, & \text{if } V_+ < V_- \end{cases} \quad (1)$$

In general, comparators function best with positive feedback, as it produces an unstable response in a negative feedback loop. Typically op-amps are designed to produce stable response even in negative feedback loop, while comparators have been designed purposefully to serve with better speed, not with negative feedback. In this part of the experiments, two comparators with poor behavior are examined – one with op-amp and the other with a special-purpose comparator IC chip.

#### *Components*

- (1) 1 LF411, 1 LM311 Op Amp
- (2) 1k, 4.7k, 10k, 100k $\Omega$  Resistors
- (3) 1 Power Supply (for +15 V, -15 V, GND)
- (4) 1 Oscilloscope

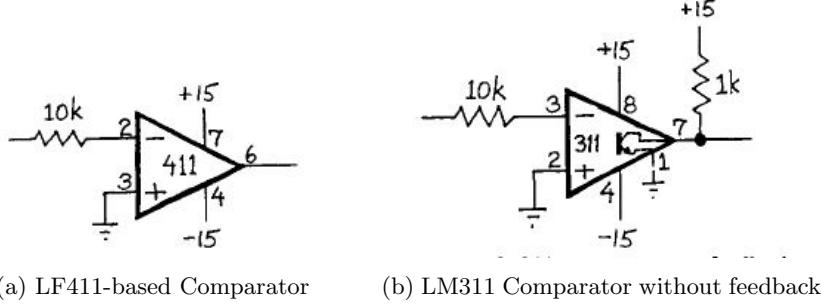


Figure 1: Op amp-based comparator using LF411 & LM311

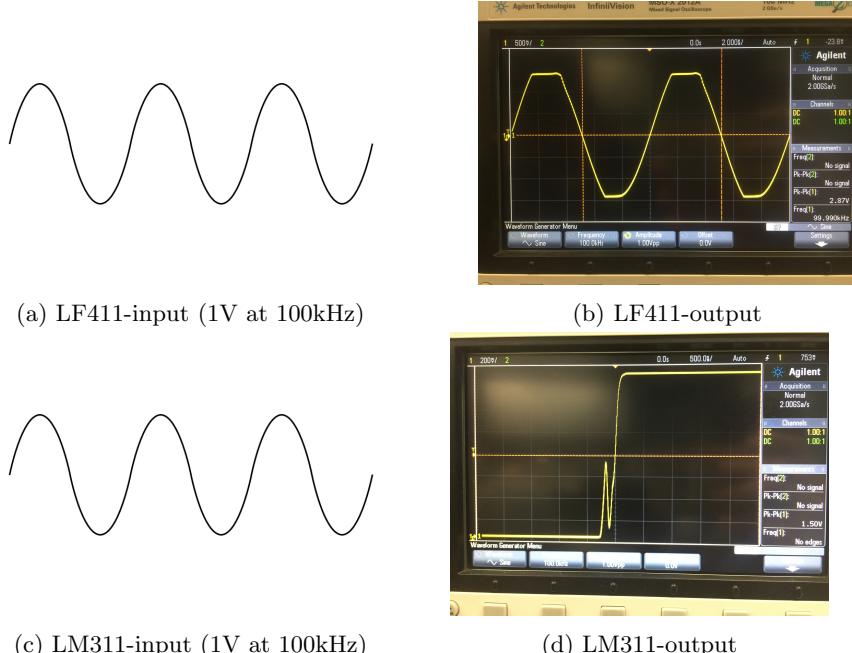


Figure 2: Waveform responses of LF411 & LM311

### *LF411 vs. LM311*

The chosen frequency of 100kHz allows for clearer observation of the delay present at the transitions. Due to the nature of slewing in the LF411 op amp, the transition delay is greater than that in LM311, a specialized comparator. However, despite faster transition in LM311 from a larger picture, there are present multiple transitions on the leading and falling edges as seen in Figure 2d. These multiple intermediate transitions(fluctuations) are due to the noise in the input induced by the current drawn upon trigger to switch in a comparator.

*Behavior of a Comparator without a Positive Feedback*

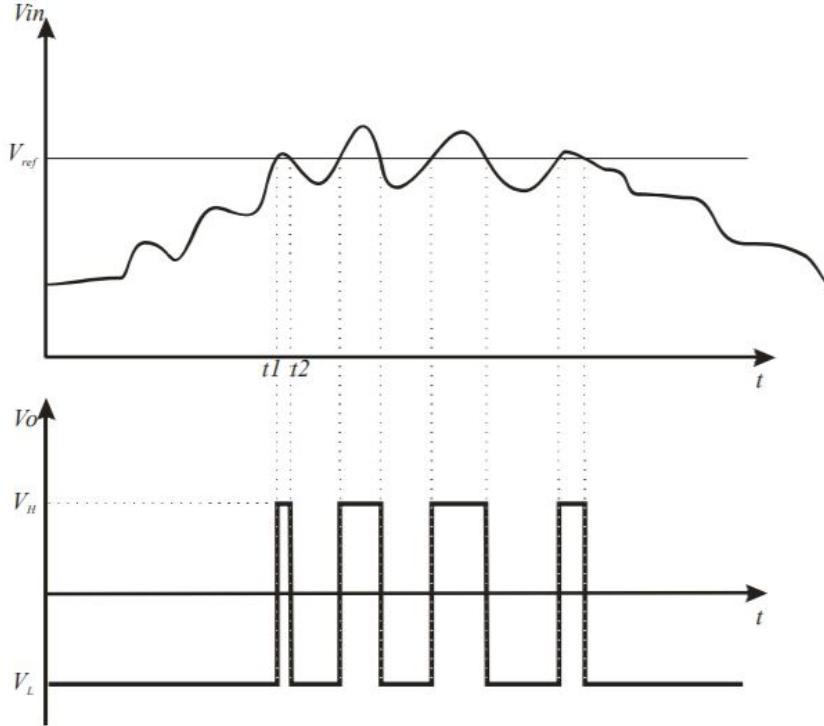


Figure 3: Comparator output with Noise, without positive feedback

The straight lines going across the input and output signals in Figure 3 indicate the reference voltage at which the comparator (op amp) compares the input against. As  $V_{in}$  exceeds  $V_{ref}$ , the output of the comparator switches from low to high, and when the input decreases below the reference, the output switches back down from high to low. The fluctuations in the input indicate possible noise at the input terminal, which is typically undesirable behavior, and due to switches in the output voltage on every 'zero-crossing,' this op amp-based comparator is not desirable to use for a comparator.

*Source of Noise*

When a comparator makes a transition upon the input signal, it draws a large current from the power supply, and dumps into ground. This current swing from the power supply to the ground causes voltage spikes (change in  $V_+$  threshold), with some feeding back into the input. This fluctuation continues until the induced voltage spike(noise) doesn't cause any more multiple (intermediate) transitions at the output.

### Minimize Noise

In order to minimize multiple transitions, exploiting hysteresis could effectively yield a better result. Hysteresis is an effect in which a state in a system depends on the history of the system - in this context,  $V_{out}$  depends on  $V_{in}^-$ . Because  $V_+$  threshold changes in the opposite direction of the varying input signal upon transition, the output signal is thus dependent upon the other  $V_{in}^-$ . Therefore by setting two threshold levels for  $V_+$  and  $V_-$ , noisy input signals within the newly set bounds would be ignored, or at least minimize, oscillations at the output as much. This is realized by connecting the comparator in a positive feedback loop, which is called a Schmitt Trigger, explored next.

*A good comparator: Schmitt Trigger*

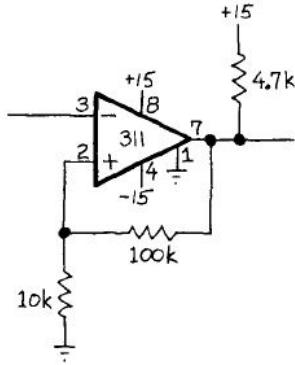


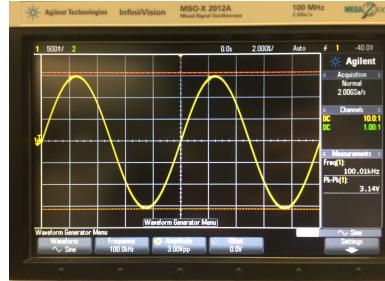
Figure 4: Schmitt Trigger Circuit

### Schmitt Trigger

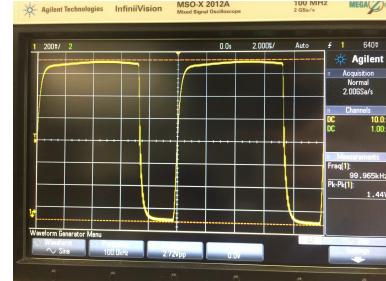
Condition	$V_{out}$	$V_{TH}$
$V_{in} < V_{ref}$	$V_{cc} = +15V$	$15V * \frac{R_1}{R_1+R_2} = 1.36V$ (High)
$V_{in} > V_{ref}$	$V_{ee} = -15V$	$-15V * \frac{R_1}{R_1+R_2} = -1.36V$ (Low)

Table 10-1: Thresholds for each condition

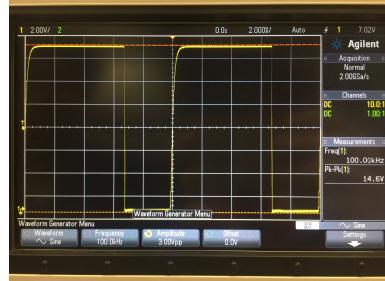
\*  $V_{TH}$  is the junction of the two resistors -  $10k\Omega$  and  $100k\Omega$



(a) input to Schmitt trigger



(b) Schmitt trigger at the edge



(c) Schmitt trigger at 3V

Figure 5: (a) Schmitt Trigger Input, (b), At the Edge of Trigger, (c) After Point of Trigger

The positive feedback used in the Schmitt Trigger eliminates the intermediate multiple oscillations. As calculated in table above, the low and high reference voltage interval in which hysteresis could occur indicates that an input signal of magnitude greater than that interval is necessary to stop triggering for sine waves  $\approx 2.7$  Volts, as seen in Figure 5b. In Figure 5c, which is well above  $\approx 2.7V$ , the triggering is removed.

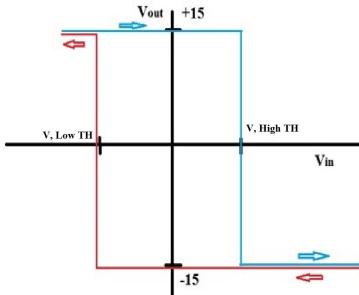


Figure 6: Hysteresis

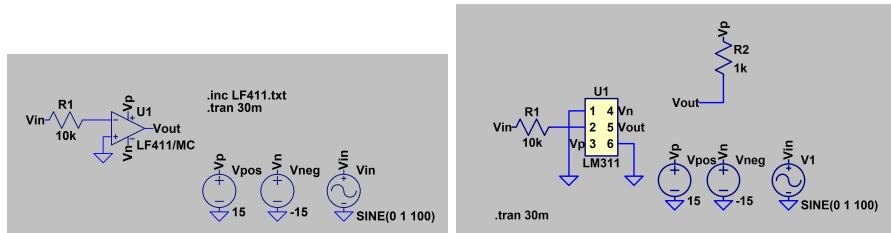
### Results

In this part of the experiments, two poorer comparators using an op amp

(LF411) and a special comparator (LM311) with triggering delays and multiple oscillations at the transition points due to noise are observed. In addition, an improved comparator using a positive feedback loop, a Schmitt Trigger, is explored, with the effect of hysteresis in consideration. With the two newly set thresholds at  $\pm 1.36V$ , the effect of minor oscillations in the interval could be neglected to some degree, as seen in Figure 5. As the input signal amplitude exceeded the difference between the high and low threshold voltages for  $V_+$ , the triggering of the sine wave at the transitions was minimized. To further reduce trigger delay, which could still be inherent in the design, an AC feedback using a capacitor between the output and the resistor connecting the output and threshold could be employed. This is possible as the threshold voltages could vary as the capacitor enters charging and discharging states according to the input, and then the noise is also taken into account for the capacitor, thereby cancelling it out at the output.

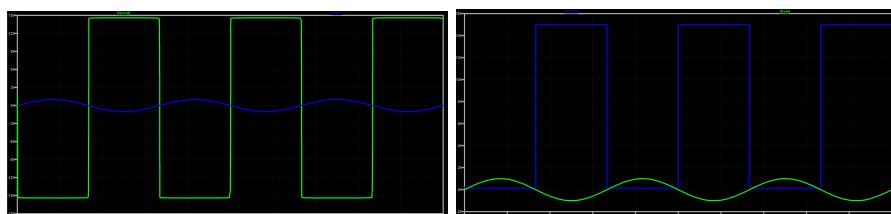
### Simulation Results

An LTspice simulation was done using a subcircuit design of the LF411 chip and LM311 chip (Appendix A & B).



(a) The schematic (LF411) in LTspice      (b) The schematic (LM311) in LTspice

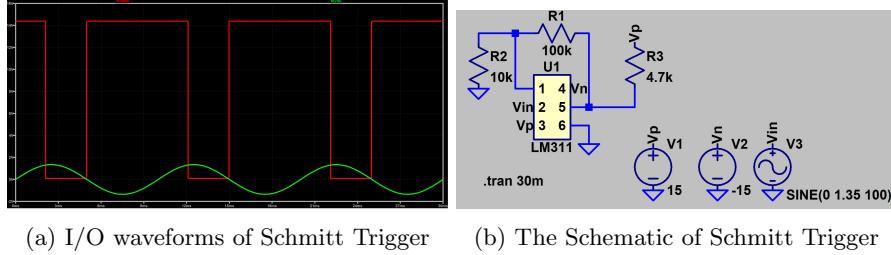
Figure 7: Schematic of Simulation for Comparators (10-1)



(a) I/O waveforms (LF411) in LTspice      (b) I/O waveforms (LM311) in LTspice

Figure 8: Simulation for Comparators (10-1)

### Schmitt Trigger



(a) I/O waveforms of Schmitt Trigger      (b) The Schematic of Schmitt Trigger

Figure 9: Schmitt Trigger

As the experimental waveforms in Figure 5 show that at the edge of trigger of  $\approx 2.7V$  it ceases to be sine wave, the simulations show that sinusoidal inputs (blue for LF411, green for LM311) become square waves from -15V to +15V.

### Summary and Discussion

While LF411 op amp can be used as a comparator, its performance as a simple "polarity detector" gives poorer response than that LM311 comparator circuit would result. Instead of using a slowly-transitioning linear op amp like LF411, both experimental and theoretical results demonstrate a specialized comparator like LM311 (with a pull-up resistor) provide a better switch (not necessarily with amplification, however). This is realizable because LM311 is made up of four transistors, the last of which is never set to saturation, such that the switching time is not increased. Even better, a Schmitt Trigger realizes the desired switching response relatively better by exploiting hysteresis - at inputs of magnitude greater than the difference of two newly defined thresholds (from positive feedback), the output starts to break away from sinusoidal behavior and shows the desired response as seen in Figure 9.

## 2 Lab 10.2 - RC Oscillator

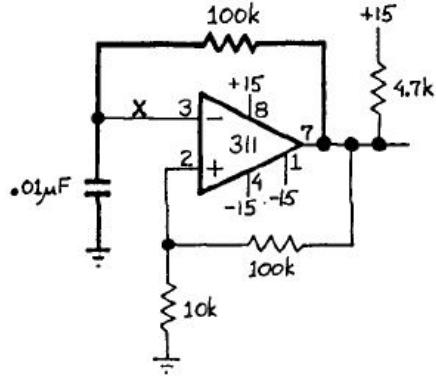


Figure 10: RC Oscillator

### *RC Oscillator*

This circuit is similar to a Schmitt Trigger, but with a negative feedback loop with a capacitor. The presence of the capacitor causes the output to vary with the effect of capacitor charge/discharge varying states. In steady state, the capacitor is simply an open-circuit, so it is  $V_{cc}$  (+15V). In transient state, the output oscillates due to the capacitor charging towards  $V_{cc}$  (+15V) when  $V_x < V_{TH}$  and discharging towards  $-V_{ee}$  (-15V). The threshold voltages for low and high are the same as for a Schmitt Trigger:  $\pm 15V \cdot \frac{R_1}{R_1+R_2} = \pm 15V \cdot \frac{10k}{110k} = \pm 1.36V$ . The current through the capacitor is  $\approx 15V / 100k\Omega = 0.15$  mA.



Figure 11: RC Oscillator Response Example

The transition time could be determined from the capacitance equation,

$$C \frac{dV}{dt} = I \quad (2)$$

which can then be turned into

$$\delta t = \frac{C * dV}{I} = \frac{0.01\mu F * 2.7V}{0.15mA} \approx 180\mu A. \quad (3)$$



Figure 12: RC Oscillator Responses

The time constant (time required to charge or discharge) can be found by the resistance and capacitance in the negative feedback loop,

$$\tau = RC = 100k\Omega * 0.01\mu F = 10^{-3} sec \quad (4)$$

#### *Derivation of Frequency of Oscillation*

$$V_{TH} = \frac{R1}{R1 + R2 + R3} V_{out} \quad (5)$$

$$V_{cap} = V_{out} - (V_{TH} + V_{out}) e^{\frac{t}{RC}} \quad (6)$$

$V_{out}$  is set to  $+V_{cc}$  or  $-V_{cc}$  according to the relative values of  $V_{cap}$  and  $V_{TH}$ , and the period depends on  $V_{TH}/V_{out}$ .

$$\frac{V_{out}}{2} = V_{out} - (V_{TH} + V_{out}) e^{\frac{T/2}{RC}} \quad (7)$$

$$T = 2RC \ln(1.19) \approx 0.3479RC \quad (8)$$

$$f_{osc} = \frac{1}{T} = \frac{1}{(0.3479 * 100k\Omega * 0.01\mu F)} = 2.874 kHz \quad (9)$$

\* Observed frequency of oscillation observed: 2.881 kHz

### Components

- (1) 1 LM311 Op Amp
- (2) 100kΩ, 10kΩ, 4.7kΩ Resistors
- (3) 0.01μF capacitor (or equivalent)
- (4) 1 Power Supply (for +15 V, -15 V, GND)
- (5) 1 Oscilloscope

### Simulation Results

An LTspice simulation was done using a sub-circuit design of the LM311(Appendix B).

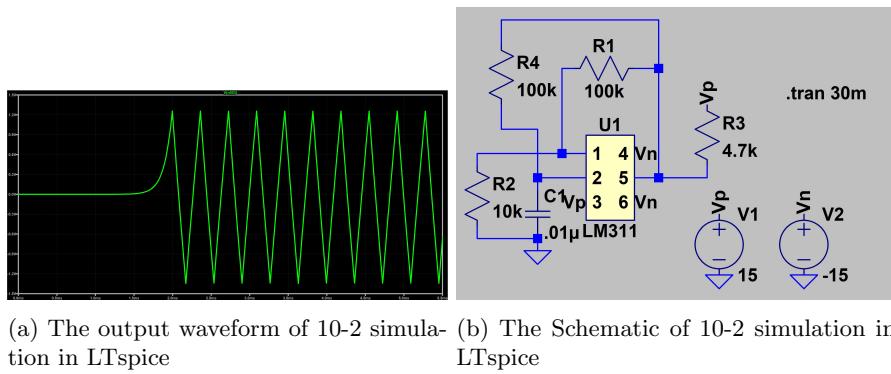


Figure 13: 10-2 Simulation in LTspice

### Summary and Discussion

The op amp-based RC oscillator utilizes the fact that it is inverting and the RC network both cause 180 deg phase shifts, such that the phase shift sum is not in effect. Its ability to provide a constant frequency sine wave output under varying load conditions poses a great advantage in various high-frequency applications as the bandwidth limitations only allow phases shifts to take place at high enough frequency ranges.

### 3 Lab 10.3 - 7555 IC Oscillator(square wave)

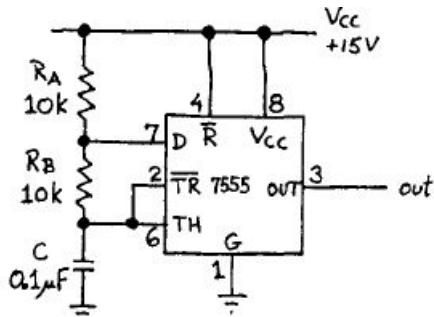


Figure 14: 7555 Relaxation Oscillator (traditional 555 timer astable mode)

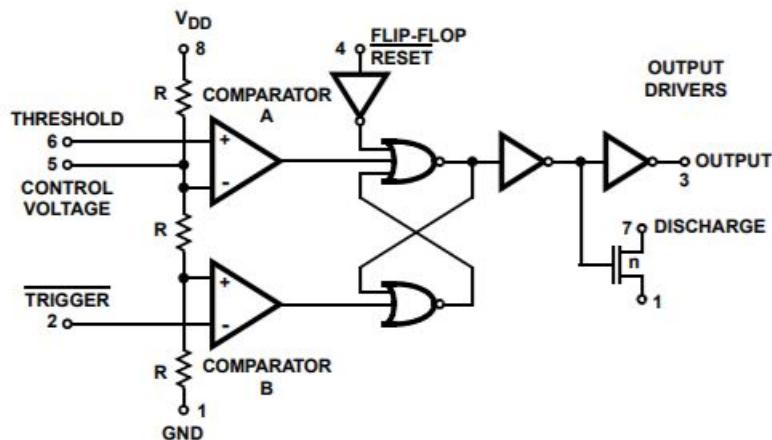


Figure 15: 7555 Functional Diagram

#### 7555 IC Oscillator

7555 IC timer chip could be used for oscillator (vibrator), specifically for delay timer, precision timer, synchronized timer, pulse width modulation, and high speed one-shot pulse. The oscillator can operate in two modes - monostable and stable.

In monostable mode, with a single resistor  $R_A$ , it works as a one-shot pulse generator. The capacitor at pin 6 is initially held discharged, and when trigger (pin 2) is at falling edge, the internal flip flop is set, yielding low impedance on pin 7 - Discharge. This drives the capacitor into charging cycle and the output becomes high. The capacitor voltage increases exponentially with time constant being  $\tau = R_A * C$ . Then when the voltage across the capacitor equals  $2/3$  of  $V_{cc}$ , the comparator resets the flip-flop and, capacitor starts to discharge

and pulls the output to low state.

In astable mode using two resistors  $R_A$  and  $R_B$ , the capacitor charges through both resistors while discharging is done through only  $R_B$ . The duty cycle is managed by the RC network of these two resistors and the capacitor, as determined by the Equation 10. The voltage across the capacitor runs between  $1/3$  and  $2/3$  of  $V_{cc}$ , independent of the supply voltage.

$$f = \frac{1}{0.7(R_A + 2R_B)C} \quad (10)$$

### Components

- (1) 1 7555 Oscillator
- (2) 2 10kΩ Resistors
- (3) 0.1μF Capacitor
- (4) 1 Power Supply (for +15 V, -15 V, GND)
- (5) 1 Oscilloscope

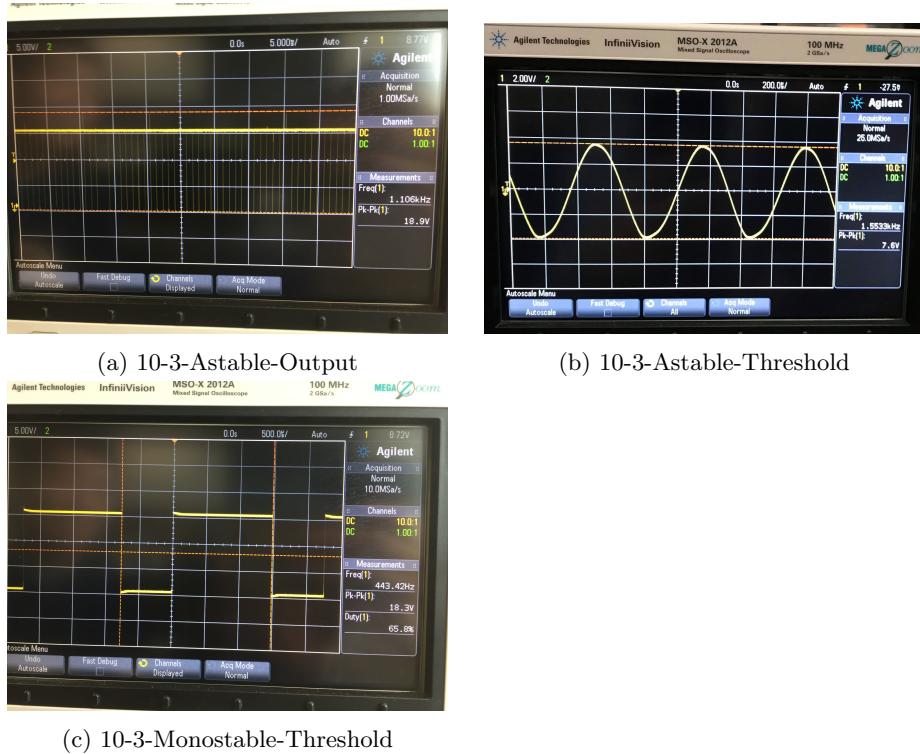


Figure 16: Astable Mode Output and Threshold, and Monostable Threshold

*Frequency of oscillation with both resistors*

$$f_{osc} = \frac{1}{0.7[R_A + 2R_B]C} = \frac{1}{0.7[10k\Omega + 2 * 10k\Omega]0.1\mu F} = 476.19Hz$$

*Explain what bistable, astable means and verify  $f_{osc}$*

An astable circuit is not stable in either state of the oscillator therefore it continually switches from one state to the other which is similar to a relaxation oscillator, while a bistable circuit is stable in either state and can be flipped from state to the other using an external trigger pulse, which is also known as a flip-flop that can be used in digital logic and computer memory. The experimental frequency of oscillation of 443.42 Hz comes close to theoretical value calculated above. The deviation in the values could be due to capacitor functionality and imprecise resistances in the manufacturing limitations.

*Alternative Astable Circuit - 50% Duty Cycle*

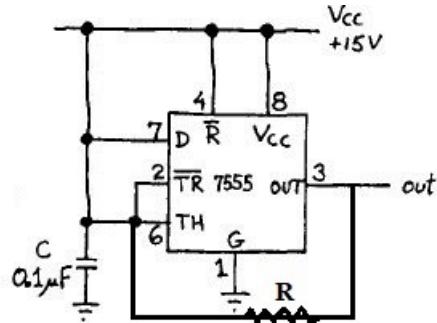


Figure 17: 50% Duty Cycle Design

Changes:  $R_B$  shorted, 10k $\Omega$  resistor added across the output and threshold.

*How is this design realizable?*

This circuit is realizable because of the way the 7555 timer is viewed by any exterior circuits. By moving the 10k resistor between the output and threshold, pins 2, 6, and 10 all receive the same voltage rather than having differing amounts. This node is also connected to the capacitor which allows for the charging and discharging which gives an almost exact 50% duty cycle.

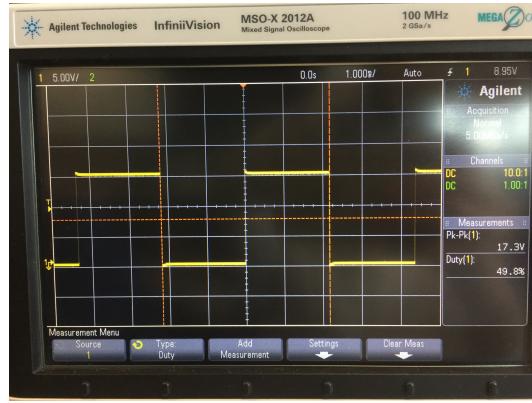


Figure 18: 50% Duty Cycle 7555 Design

*In what way does the output waveform of this circuit differ from the output of the traditional 555 astable?*

When comparing the output waveform of this circuit to the traditional 555 astable circuit, the waveform is shown to have less distortion at the edges of the square wave, showing a more precise wave.

*Is the oscillator's period sensitive to loading? See what a 10k resistive load does, for example.*

The oscillator's period was not affected by a resistive load at the output when tested and it should not alter the waveform since the circuit is self contained. Now the frequency of oscillation should match that for the 'classic' configuration, except that it eliminates the complication of the differing charge and discharge paths.

#### *Frequency of oscillation with 50% Duty Cycle Design*

$$f_{osc} = \frac{1}{(1.4)(R)(C)} = \frac{1}{(1.4)(10k)(0.1\mu F)} = 714.29Hz$$

#### **Simulation Results**

The 7555 timer could not be simulated, because of the way LTspice handles the the open circuit at pin 5 of the provided sub-circuit online (Appendix C).

#### **Summary and Discussion**

While 7555 and 555 both function to generate oscillatory behavior, 7555 - CMOS version - consumes less power. The operation in astable mode produced capacitor charge-discharge states with 476.19 Hz of frequency of oscillation, and in monostable mode, the threshold and output pins showed similar waveforms.

The duty cycle manipulation was highly dependent upon the capacitor charge-discharge states as both  $R_A$  and  $R_B$  were removed in the path for charging and discharging for the capacitor. With the new RC network connected between the capacitor and the output, the duty cycle of 49.8 % was achieved.

#### 4 Lab 10.4 - Sawtooth Oscillator

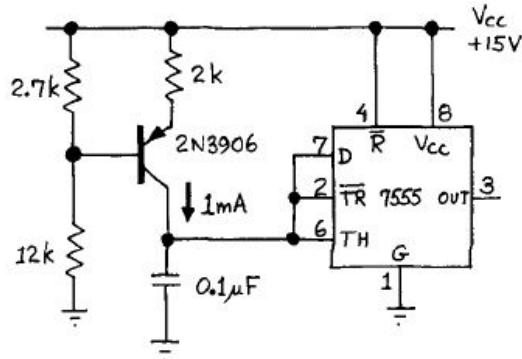


Figure 19: Sawtooth Oscillator

##### *Sawtooth Oscillator*

A sawtooth oscillator is similar to a triangular wave oscillator, but with the rising and falling periods not identical. The pnp transistor acts as a current source that charges the capacitor. The capacitor starts charging to supply voltage because the internal transistor of 7555 shorting the capacitor to ground and it opens. During charging, the output goes low if the voltage increases above 2/3rd of supply voltage. During discharging, the output goes high if the voltage across C decreases below 1/3rd supply voltage. Thus the capacitor charges and discharges between 2/3rd and 1/3rd of supply voltage. This was shown on the oscilloscope in Figure 20a where the sawtooth wave is shown to have the same frequency as the output square wave.

The frequency is determined by the following equation, and is found to be around 2kHz for this oscillator.

$$f = (V_{cc} - 2.7) / (R_{emitter} * C * V_{ppout}) \quad (11)$$

$$f = (15V - 2.7V) / (2k\Omega * 0.1\mu F * 30.6V) = 2.009kHz$$



(a) At the threshold

(b) At the output

Figure 20: RC Oscillator Responses

The rising edge of the sawtooth is the steady increase of the voltage across the capacitor. The falling edge is after the voltage reaches a point where it is discharged and resets the capacitor. The output waveform is a square wave because once the voltage reaches past  $\frac{2}{3} V_{in}$ , the output is switched to high.

#### Components

- (1) 1 7555 Oscillator
- (2) 2 10kΩ Resistors
- (3) 0.1μF Capacitor
- (4) 1 Power Supply (for +15 V, -15 V, GND)
- (5) 1 Oscilloscope

#### Simulation Results

The 7555 timer could not be simulated, because of the way LTspice handles the the open circuit at pin 5 of the provided subcircuit online (Appendix C).

#### Summary and Discussion

The sawtooth oscillator was observed to follow the general behavior as expected - When the threshold voltage reached  $2/3$  of  $V_{in}$  the output was put to high, and when below, low. Given the output peak-to-peak voltage, the frequency of oscillation was determined to be around 2kHz. As for simulation, the available 7555 subcircuit model on LTspice could not be simulated due to its management of voltage at floating nodes.

## 5 Lab 10.6 - Sine Wave Oscillator: Wien Bridge

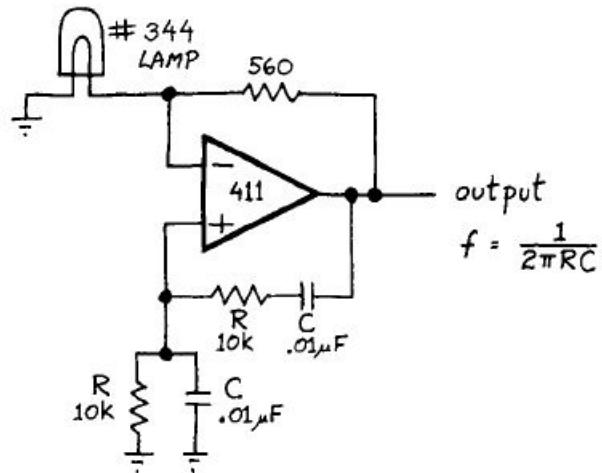
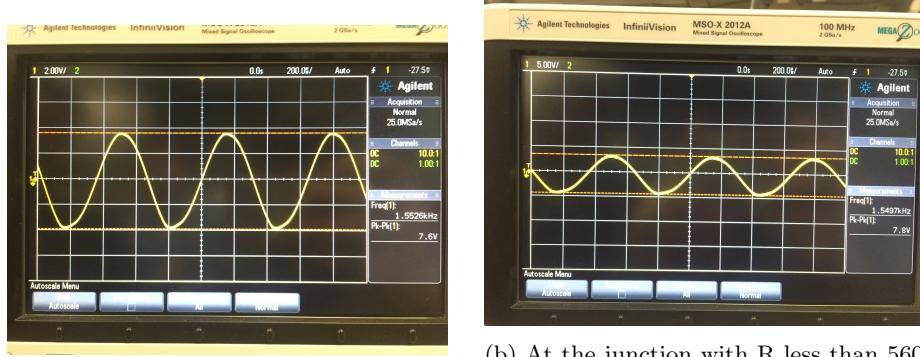


Figure 21: Sine Wave Oscillator

### Wein Bridge Sine Wave Oscillator

A Wein Bridge Oscillator takes two different RC configurations - high-pass and low-pass - at the non-inverting input to produce oscillatory behavior from the output. These resistor-capacitor divider network allows for the voltage gain to be controllable within narrow limits. The two RC networks have different phase shifts, but at the specific (resonant) frequency of oscillation,  $f_r$ , found below, the inputs to positive and negative terminals will be in-phase and equal, such that the positive RC feedback loop will cancel out the negative resistive feedback, thereby oscillation is observable at the output. Since the input is  $\frac{1}{3}$  of the output in this circuit, the gain is set to be 3 with the feedback networks described in equations above.

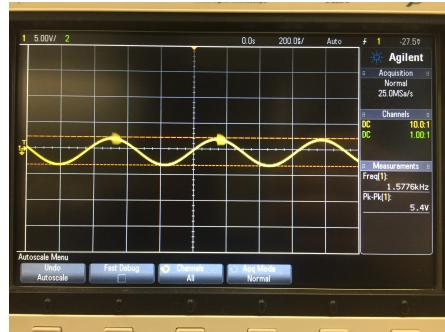
$$f_r = \frac{1}{2\pi RC} = \frac{1}{2\pi * 10k\Omega * 0.01\mu F} = 1.591kHz \quad (12)$$



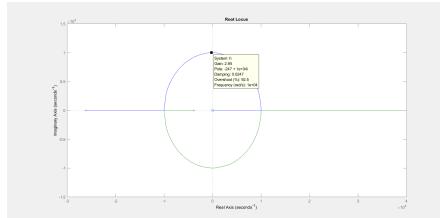
(a) At the junction of 2 RC-networks



(c) Poking the non-inverting input causes fluctuations - bumps higher



(d) Too little amplification



(e) Root Locus Plot, Gain = 2.95

Figure 22: Sine Wave Oscillator

\* In (f), we verify that there are two poles and one zero, and the gain at which real axis = 0 is 2.95 (top and bottom), which is close to 3 (expected). The range for the gain extends from as low as 0.99 to 3e4 - the closer it gets to the pole the gain increases.

Let  $V_X = V_+$ ,

$$\frac{V_X}{V_{out}} = \frac{RCs}{R^2C^2s^2 + 3RCs + 1}$$

Let  $s = j\omega = j \frac{1}{RC}$

$$\left| \frac{V_X}{V_{out}} \right| = \frac{1}{3}$$

$$V_X = \frac{1}{3 + (\omega RC - \frac{1}{\omega RC})j}$$

Setting  $\omega RC - \frac{1}{\omega RC} = 0$ , then  $\omega = \frac{1}{RC}$ ,  $f_{osc} = \frac{1}{2\pi RC}$ .

At this frequency, the signal fed back is in phase with the output (0 deg or 360 deg shift) and  $\frac{1}{3}$  the amplitude of  $V_{out}$ .

$$1 + \frac{R_F}{R_{bulb}} = 3$$

Thus the resistance value should be twice the lamp resistance, as follows:

$$R_F = 2R_{bulb}. \quad (13)$$

\* Since # 344 light bulb was not available in the inventory, a potentiometer of  $1k\Omega$  was used and adjusted accordingly; the approximate resistance that gave the sinusoidal wave at the junction was  $260k\Omega$ , which is desirable.

*MATLAB code for root locus*

```

1 R = 10e3; C = 0.01e-6;
2 Req = 1/(1/R+1/R); Ceq = C+C;
3 h = tf([0 -R*C 0],[ (R^2)*(C^2), 3*R*C, 1]);
4 rlocus(h)

```

*Components*

- (1) 1 LF411 Op Amp
- (2)  $560\Omega$ ,  $10k\Omega$  resistors
- (3)  $1k\Omega$  Potentiometer (replacement for light bulb)
- (4)  $0.01 \mu F$  capacitors
- (5) 1 Power Supply (for +15 V, -15 V, GND)
- (6) 1 Oscilloscope for wavegen, graphical output

## Simulation Results

An LTspice simulation was done using a subcircuit design of the LF411 (Appendix A). As the  $200\Omega$  resistor was decreased the time needed for oscillation to start increased. At around  $260\Omega$ , the output waveform was constant.



Figure 23: The Output wave from Simulation of 10.6 in LTspice with the Lamp being replaced with a  $200\Omega$  resistor

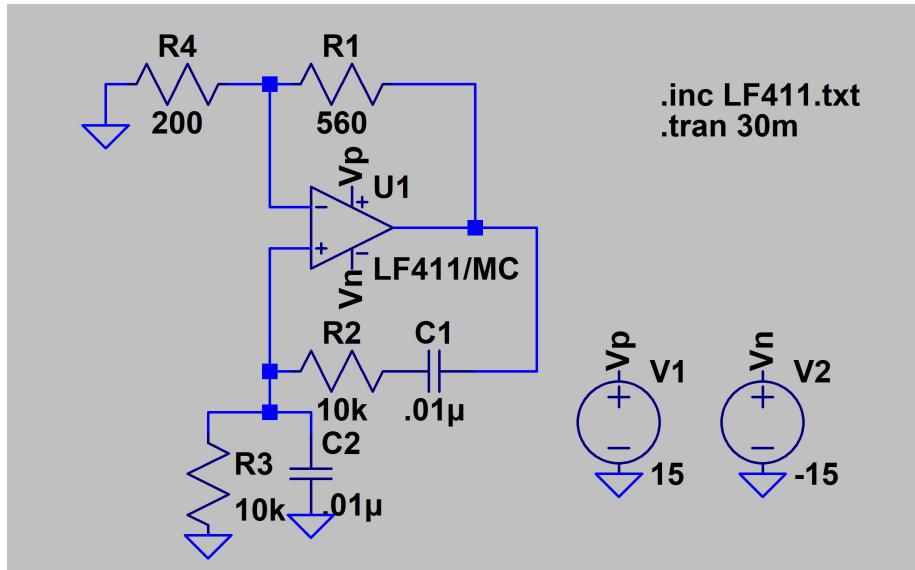


Figure 24: The Schematic of the Simulation of 10.6 in LTspice

### Summary and Discussion

In Figure 22(b), the gain of the Wein Bridge is adjusted so as to prevent clipping. Poking the non-inverting input with a finger caused some oscillatory movement in the output because it caused the resistance value in the two RC-networks to vary due to the squeezing and poking. The finger disturbance increases resistance as resistors are squeezed, and thus lowers the frequency of oscillation.

In (d), the oscillation of the sine's envelope is observed to be dying away because the gain decreases, as the gain becomes lower. As shown in the equations above, the gain necessary to sustain oscillations without clipping is 3, and the root locus diagram shows that the gain of 2.95 at the top closely matches the theoretical value of 3.

## Overall Conclusions

In this set of experiments, the comparator circuits based on op-amp and special-purpose 311 chip were explored and exploiting hysteresis effect, new thresholds were set, allowing for noise to be mitigated. In an effort to improve transitions at the rising and falling edges, a comparator with positive feedback, Schmitt Trigger, was then employed, yielding a more effective functionality for a comparator. In the RC oscillator circuit in which no input signal was necessary, the frequency of oscillation was verified both experimentally and theoretically at around 470Hz. Using 7555 timer chip models, the waveform behaviors in monostable, astable modes depending on the presence of resistors connected to pins 7 and 6, respectively, confirmed the resistors through which the capacitor charges and discharges act to vary the output responses and control the duty cycle. In the Wein Bridge, the gain of 3 was needed to prevent clipping while keeping the oscillation from dying away, and was confirmed by root locus plot (yielding gain of 2.95).

## Appendix A LF411 Subcircuit Design

```
1 * LF411 operational amplifier
2 * "macromodel" subcircuit
3 *
4 * connections:
5 *   1 - non-inverting input
6 *   2 - inverting input
7 *   3 - positive power supply
8 *   4 - negative power supply
9 *   5 - output
10 *
11 .subckt LF411/MC 1 2 3 4 5
12 *
13   c1    11 12 2.801E-12
14   c2     6  7  8.000E-12
15   css   10 99 3.200E-12
16   dc     5  53 dx
17   de     54  5 dx
18   dlp    90 91 dx
19   dln    92 90 dx
20   dp     4  3 dx
21   egnd  99  0 poly(2) (3,0) (4,0) 0 .5 .5
22   fb    7 99 poly(5) vb vc ve vlp vln 0 3.316E6
23 + -3E6 3E6 3E6 -3E6
24   ga    6  0 11 12 402.1E-6
25   gcm   0  6 10 99 12.72E-9
26   iss    3 10 dc 280.0E-6
27   hlim  90  0 vlim 1K
28   j1    11  2 10 jx
29   j2    12  1 10 jx
30   r2    6  9 100.0E3
31   rd1   4 11 2.487E3
32   rd2   4 12 2.487E3
33   ro1   8  5 40
34   ro2   7  99 60
35   rp    3  4 24.00E3
36   rss   10 99 714.3E3
37   vb    9  0 dc 0
38   vc    3  53 dc 1.100
39   ve    54  4 dc .3
40   vlim  7  8 dc 0
41   vlp   91  0 dc 30
42   vln   0  92 dc 30
43   .model dx D( Is=800.0E-18)
44   .model jx PJF( Is=30.00E-12 Beta=577.5E-6
45 + Vto=-1)
46   .ends
47 *$
```

## Appendix B LM311 Subcircuit Design

```
1 * LM311 VOLTAGE COMPARATOR "MACROMODEL" SUBCIRCUIT
2 * CREATED USING PARTS VERSION 4.03 ON 03/07/90 AT 08:15
3 * REV (N/A)
4 * CONNECTIONS: NON-INVERTING INPUT
```

```

5 * | INVERTING INPUT
6 * | | POSITIVE POWER SUPPLY
7 * | | | NEGATIVE POWER SUPPLY
8 * | | | | OPEN COLLECTOR OUTPUT
9 * | | | | | OUTPUT GROUND
10 *
11 .SUBCKT LM311 1 2 3 4 5 6
12 *
13   F1    9  3 V1  1
14   IEE   3  7 DC 100.0E-6
15   VI1   21 1 DC .45
16   VI2   22 2 DC .45
17   Q1    9 21 7 QIN
18   Q2    8 22 7 QIN
19   Q3    9  8 4 QMO
20   Q4    8  8 4 QMI
21 .MODEL QIN PNP(IS=800.0E-18 BF=500)
22 .MODEL QMI NPN(IS=800.0E-18 BF=1002)
23 .MODEL QMO NPN(IS=800.0E-18 BF=1000 CJC=1E-15 TR=102.5E-9)
24   E1    10 6 9 4 1
25   V1    10 11 DC 0
26   Q5    5 11 6 QOC
27 .MODEL QOC NPN(IS=800.0E-18 BF=103.5E3 CJC=1E-15 TF=11.60E-12 TR
   =48.19E-9)
28   DP    4  3 DX
29   RP    3  4 6.667E3
30 .MODEL DX D(IS=800.0E-18)
31 *
32 .ENDS

```

## Appendix C 7555 Subcircuit Design

```

1 * ICM7555 MACROMODEL
2 * _____
3 * Revision 1.0 4/2006
4 * _____
5 * The ICM7555 is a general purpose RC timer capable of generating
   accurate
6 * time delays or frequencies. This device feature and extremely low
   supply
7 * current combined with virtually non-existent current spike during
   output
8 * transitions.
9 * _____
10 * Connections
11 *     1 = GND
12 *     2 = TRIGGERB
13 *     3 = OUTPUT
14 *     4 = RESETB
15 *     5 = CONTROL VOLTAGE
16 *     6 = THRESHOLD
17 *     7 = DISCHARGE
18 *     8 = VCC
19 * Parameters which are modeled.
20 * 1) Full timer functionality
21 * 2) Supply bias current and load current
22 * 3) Output rise/fall times

```

```

23 * 4) Reset threshold
24 * 5) Output VOL/VOH
25 * 6) Discharge voltage with current
26 ****
27 .SUBCKT ICM7555 1 2 3 4 5 6 7 8
28 XOPAMP 1 2 3 4 5 6 7 8 ICM7555_S
29 .ENDS
30 ****
31 .SUBCKT ICM7555_S 18 11 12 13 14 15 16 10
32 ****
33 *COMPARATORS
34 ES1 A11 18 10 18 1
35 IABIAS A11 A12 10UA
36 MA1 A13 A16 A12 A11 MOSP
37 MA2 A14 A15 A12 A11 MOSP
38 VAOS A17 A16 0.5M
39 RAD1 A13 18 10K
40 RAD2 A14 18 10K
41 DAC3 A15 10 DA
42 DAC4 18 A15 DA
43 GCA1 18 A20 A13 A14 1000M
44 RCA1 A20 18 100K
45 VCA1 A21 18 1V
46 DCA1 A20 A21 DY
47 DCA2 18 A20 DY
48 ****
49 IBBIAS A11 B12 10UA
50 MB1 B13 B16 B12 A11 MOSP
51 MB2 B14 B15 B12 A11 MOSP
52 VBOS B17 B16 0.5M
53 RBD1 B13 18 10K
54 RBD2 B14 18 10K
55 DBC1 B16 10 DA
56 DBC2 18 B16 DA
57 GCB1 18 B20 B13 B14 100M
58 RCB1 B20 18 100K
59 VCB1 B21 18 1V
60 DCB1 B20 B21 DY
61 DCB2 18 B20 DY
62 ****
63 RB1 10 B22 60K
64 RB2 B22 B23 60K
65 RB3 B23 18 60K
66 VR1 B23 A15 0
67 VR2 B22 B17 0
68 VIN1 A17 11 0
69 VIN2 B15 15 0
70 VIN3 B22 14 0
71 ****
72 *SR LATCH
73 EL1 A25 18 10 18 1
74 RLA A25 A26 10K
75 CLA A26 18 1P
76 MLA1 A26 A27 18 18 MOSN
77 MLA2 A26 A28 18 18 MOSN
78 RLB A25 B26 10K
79 CLB B26 18 1P

```

```

80  MLB1 B26 B27 18 18 MOSN
81  MLB2 B26 B28 18 18 MOSN
82  MLB3 B26 B29 18 18 MOSN
83  VFB1 B27 A26 0
84  VFB2 A27 B26 0
85  EFB1 A28 18 POLY(2) A20 18 10 18 0 0 0 0 1
86  EFB2 B28 18 POLY(2) B20 18 10 18 0 0 0 0 1
87  ****
88  *PD
89  EPD1 B33 18 B26 18 1
90  RPD1 B33 B34 10K
91  CPD1 B34 18 50P
92  *OUTPUT
93  MO1 B30 B34 A25 A25 MOSPA
94  MO2 B30 B34 18 18 MOSNA
95  MO3 B31 B30 A25 A25 MOSPA
96  MO4 B31 B30 18 18 MOSNA
97  CO1 B31 18 0.1P
98  CO2 B30 18 0.1P
99  VO1 B31 12 0
100 *DISCHARGE
101 MD1 16 B30 18 18 MOSNA
102 *RESET
103 RRST B29 A25 20K
104 MRST B29 13 18 18 MOSN
105 RRSTB 13 18 50G
106 *SUPPLY CURRENT
107 ISUP 10 18 12.3U
108 FSUP 18 A36 VO1 1
109 DSUP1 18 A36 DZ
110 DSUP2 A36 A37 DZ
111 RSUP A37 18 1
112 GSUP 10 18 A37 18 1
113 ****
114 .MODEL DA D( IS=100E-14 RS=0.5k)
115 .MODEL MOSP PMOS(VTO=-0.7 KP=12.57E-4)
116 .MODEL MOSN NMOS(VTO=0.7 KP=12.57E-3)
117 .MODEL MOSPA PMOS(VTO=-2.0 KP=78.5E-4)
118 .MODEL MOSNA NMOS(VTO=2.0 KP=78.5E-4)
119 .MODEL DX D( IS=100E-14)
120 .MODEL DZ D(N=10M)
121 .MODEL DY D( IS=100E-14 N=0.1M)
122 ****
123 .ENDS

```