邏輯設計 Hw#5
Answer

1. Design a combinational circuit that forms the 2-bit binary sum S_1S_0 of two 2-bit number A_1A_0 and B_1B_0 and has both a carry input C_0 and carry output C_2. Design the entire circuit implementing each of the three outputs with a two-level circuit plus inverters for the input variables. Begin the design with the following equations for each of the two bits of the adder:

$$S_i = A_i'B_i'C_i + A_i'B_iC_i' + A_iB_i'C_i' + A_iB_iC_i$$
$$C_{i+1} = A_iB_i + A_iC_i + B_iC_i$$

<Ans>

就是把要求的outputs, S_1, S_0, C_2 down 到用inputs A_1, A_0, B_1, B_0, C_0表示

$C_1 = A_0B_0 + A_0C_0 + B_0C_0$

$S_0 = A_0'B_0'C_0 + A_0'B_0C_0' + A_0B_0'C_0' + A_0B_0C_0$

$$\begin{aligned} S_1 &= A_1'B_1'C_1 + A_1'B_1C_1' + A_1B_1'C_1' + A_1B_1C_1 \\ &= A_1'B_1'(A_0B_0 + A_0C_0 + B_0C_0) + A_1'B_1(A_0B_0 + A_0C_0 + B_0C_0)' + \\ &\quad A_1B_1'(A_0B_0 + A_0C_0 + B_0C_0)' + A_1B_1(A_0B_0 + A_0C_0 + B_0C_0) \\ &= A_1'B_1'A_0B_0 + A_1'B_1'A_0C_0 + A_1'B_1'B_0C_0 + \\ &\quad A_1'B_1A_0'B_0' + A_1'B_1A_0'C_0' + A_1'B_1B_0'C_0' + \\ &\quad A_1B_1'A_0'B_0' + A_1B_1'A_0'C_0' + A_1B_1'B_0'C_0' + \\ &\quad A_1B_1A_0B_0 + A_1B_1A_0C_0 + A_1B_1B_0C_0 \end{aligned}$$

$$\begin{aligned} C_2 &= A_1B_1 + A_1C_1 + B_1C_1 \\ &= A_1B_1 + A_1(A_0B_0 + A_0C_0 + B_0C_0) + B_1(A_0B_0 + A_0C_0 + B_0C_0) \\ &= A_1B_1 + A_1A_0B_0 + A_1A_0C_0 + A_1B_0C_0 + B_1A_0B_0 + B_1A_0C_0 + B_1B_0C_0 \end{aligned}$$

2. The following binary numbers have a sign in the leftmost position and, if negative, are in 2's complement form. Perform the indicated arithmetic operations and verify the answers.

(a) 100111 + 111001 (b) 110001 – 010010

Indicate if overflow occurs for each computation.

<Ans>

(a)

```
 111111
  100111      (-25)
 +111001    +( -7)
 -------    ------
 1100000      (-32)
 => 100000   (-32) verified
```

∵ MSB的carry in = carry out

∴無overflow

(b) - 010010 = + 101110

```
 10
  110001    (-15)
 +101110   +(-18)
 -------   ------
 1011111     -33
 => 011111   +31 verified
```

∵ MSB的carry in ≠ carry out

∴ overflow發生，所以兩個負數相加竟得到正數

3. Use contraction beginning with an 8-bit adder-subtractor without carry out to design an 8-bit circuit without carry out that increments its input by 00000010 for input S = 0 and decrements its input by 00000010 for input S = 1. Perform the design by designing the distinct 1-bit cells needed and indicating the type of cell use in each of the eight bit positions.

<Ans>

當S = 0，就是加00000010；當S = 1，是減00000010，也就是加11111110

把 00000010、11111110當作 $B_7 \sim B_0$。

$B_0 = 0$，$C_0 = 0$ $\Rightarrow S_0 = A_0 \oplus 0 \oplus 0 = A_0$

$\Rightarrow C_1 = A_0B_0 + A_0C_0 + B_0C_0 = 0$

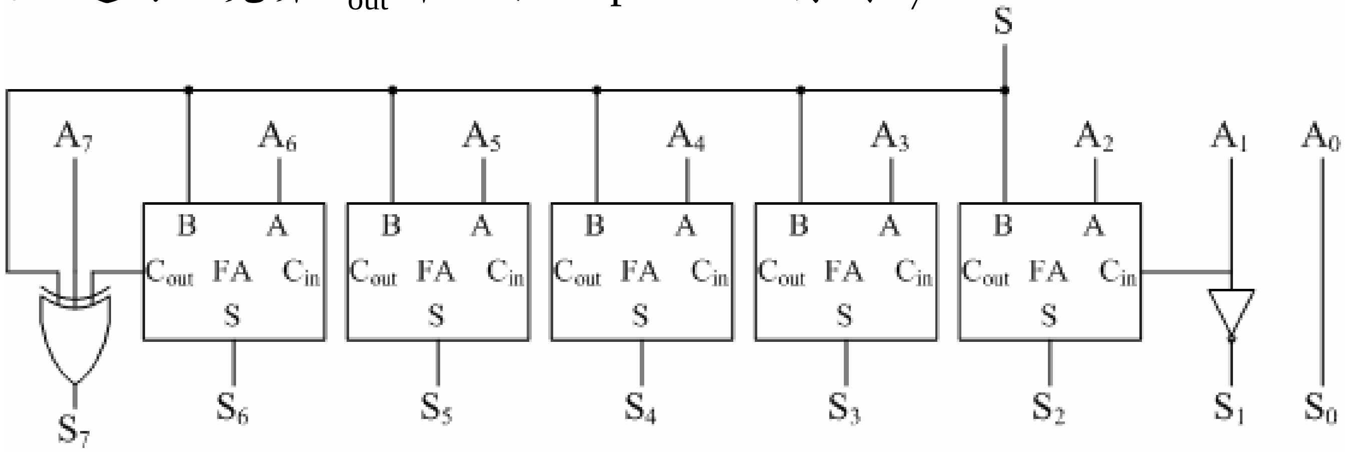
$B_1 = 1$，$C_1 = 0$ $\Rightarrow S_1 = A_1 \oplus 1 \oplus 0 = A_1'$

$\Rightarrow C_2 = A_1B_1 + A_1C_1 + B_1C_1 = A_1$

(接下來就沒法化簡了，因為 $B_2 \sim B_7$可能是0也可能是1)

S_0直接拉線，S_1接個inverter，$S_{2\sim6}$是用Full Adders產生，

而最左邊的bit免算C_{out}所以用3-input XOR得到S_7。



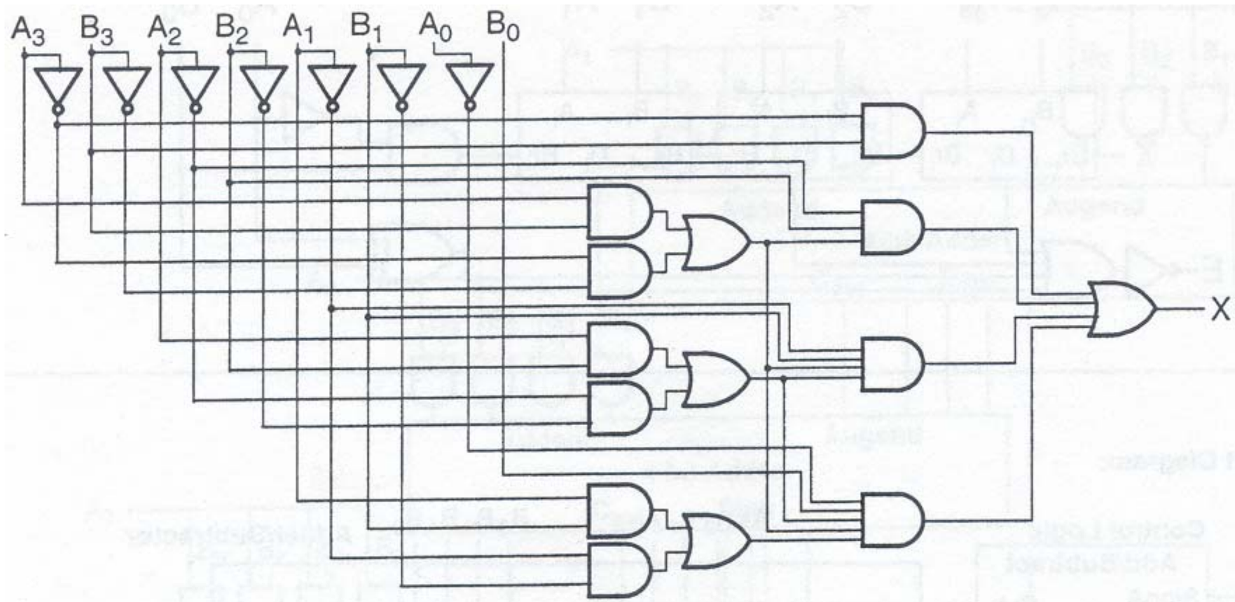
4. Design a combinational circuit that compares two 4-bit unsigned numbers A and B to see whether B is greater than A. The circuit has one output X, so that X = 1 if A < B and X = 0 if A ≧ B.

<Ans>

A < B，發生在某一位 $A_i = 0, B_i = 1$，而更高位都相等($A_j = B_j$, for all j > i)

$$\therefore X = A_3'B_3 + (A_3B_3 + A_3'B_3')A_2'B_2 + (A_3B_3 + A_3'B_3')(A_2B_2 + A_2'B_2')A_1'B_1 + (A_3B_3 + A_3'B_3')(A_2B_2 + A_2'B_2')(A_1B_1 + A_1'B_1')A_0'B_0$$

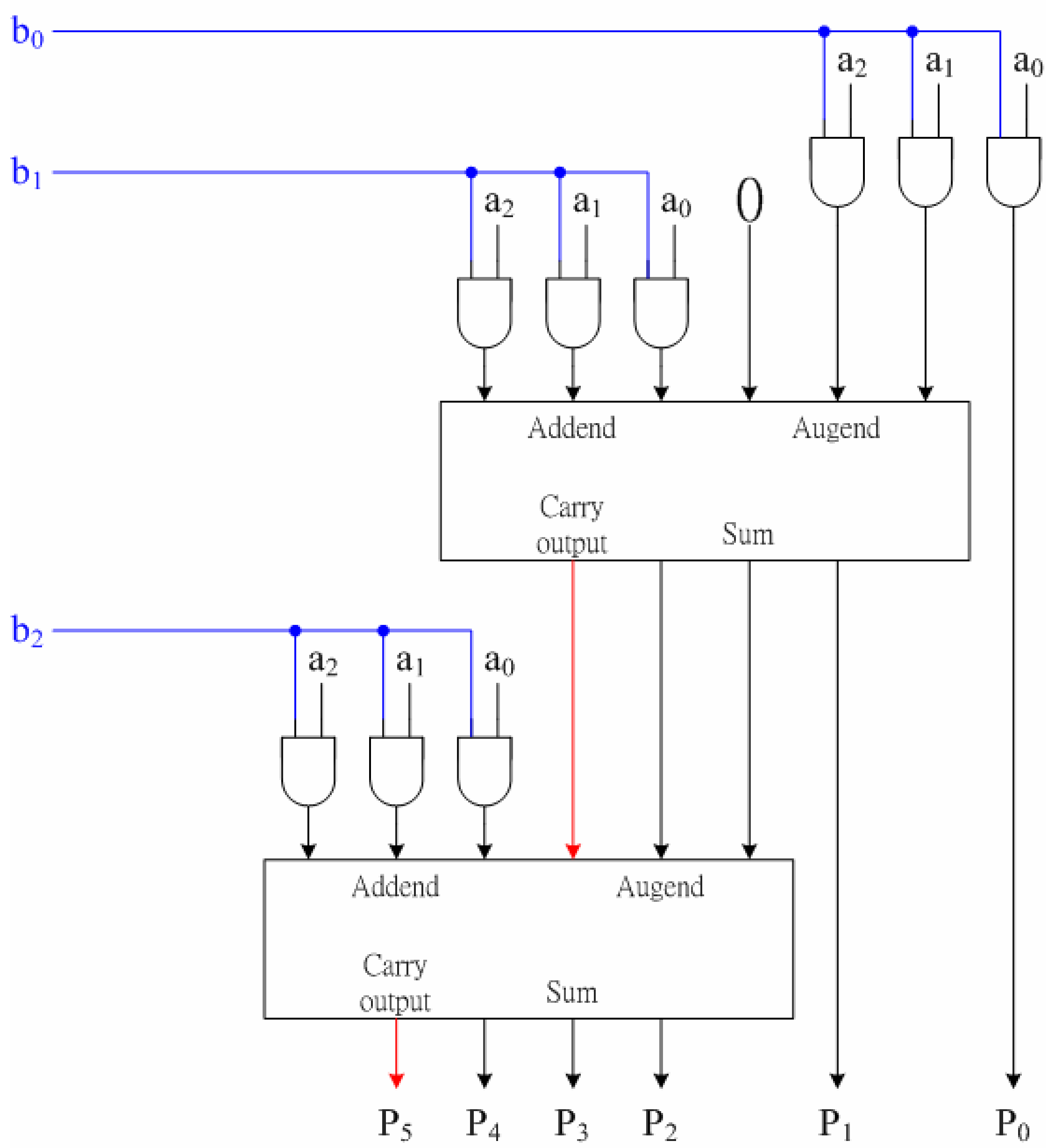
不經簡化的電路圖如下(不畫沒關係)：



5. Design a binary multiplier that multiplies two 3-bit unsigned numbers. Use AND gates and binary adders.

<Ans>

$$
\begin{array}{rcccccc}
 & & & & a_2 & a_1 & a_0 \\
 & & & \text{x)} & b_2 & b_1 & b_0 \\
\hline
 & & & & a_2b_0 & a_1b_0 & a_0b_0 \\
 & & & a_2b_1 & a_1b_1 & a_0b_1 & \\
\text{+)} & & a_2b_2 & a_1b_2 & a_0b_2 & & \\
\hline
 & P_5 & P_4 & P_3 & P_2 & P_1 & P_0
\end{array}
$$



6. Design a circuit that multiplies a 4-bit multiplicand (被乘數) by the constant 1010 by applying contraction to the solution to Problem 5.

<Ans>

$$
\begin{array}{cccccccc}
 & & & & a_3 & a_2 & a_1 & a_0 \\
 & & & \text{x)} & 1 & 0 & 1 & 0 \\
\hline
 & & & & 0 & 0 & 0 & 0 \\
 & & & a_3 & a_2 & a_1 & a_0 & \\
 & & 0 & 0 & 0 & 0 & & \\
+) & a_3 & a_2 & a_1 & a_0 & & & \\
\hline
P_7 & P_6 & P_5 & P_4 & P_3 & P_2 & P_1 & P_0
\end{array}
$$

$a_3a_2a_1a_0$ x 1010 = $P_7P_6P_5P_4P_3P_2P_1P_0$

$P_0 = 0$

$P_1 = a_0$

$P_2 = a_1$

$P_3 = S(a_2 + a_0)$

$P_4 = S(C(P_3) + a_3 + a_1)$

$P_5 = S(C(P_4) + a_2)$

$P_6 = S(C(P_5) + a_3)$

$P_7 = C(P_6)$