Department of Computer Science, National Chengchi University

Digital Systems Final Examination

1. **[Synchronous Counter Design]** (a) Fill in the blanks in the following J-K excitation table. (4%)

Transition at Output	Present State	Next State	J	K
0→0	0	0		
0→1	0	1		
1→0	1	0		
1→1	1	1		

(b) Write down the counting sequence of a MOD-8 Johnson counter with an initial state 0000. (2%)

(c) Implement a MOD-8 Johnson counter using D flip-flops by converting a MOD-4 ring counter. (4%)

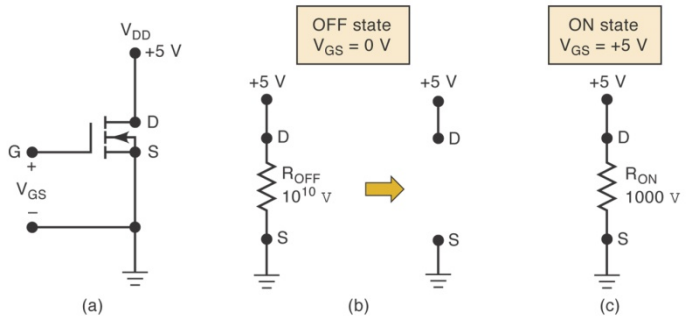
(d) Use the above J-K excitation table to design a synchronous counter that has the same counting sequence as the Johnson counter. You should write down the complete design procedure and draw the final implementation using J-K flip-flops. (10%)

(e) Repeat part (d) using D flip-flops. (5%)

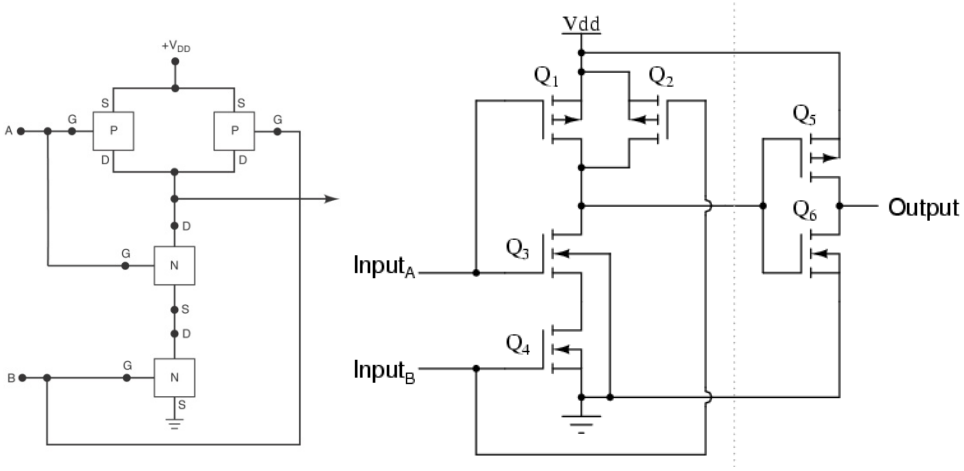
2. **[Digital IC families: TTL]** Given the following table: (1) Calculate the noise margin of 74 and 74F series. (4%) (b) Which series has the highest clock rate? Which series has the lowest clock rate? (4%) (c) Name two advantages of TTL over CMOS. (2%)

	74	74S	74LS	74AS	74ALS	74F
Performance ratings						
Propagation delay (ns)	9	3	9.5	1.7	4	3
Power dissipation (mW)	10	20	2	8	1.2	6
Max. clock rate (MHz)						
Fan-out (same series)	10	20	20	40	20	33
Voltage parameters						
V_{OH}(min) (V)	2.4	2.7	2.7	2.5	2.5	2.5
V_{OL}(max) (V)	0.4	0.5	0.5	0.5	0.5	0.5
V_{IH}(min) (V)	2.0	2.0	2.0	2.0	2.0	2.0
V_{IL}(max) (V)	0.8	0.8	0.8	0.8	0.8	0.8

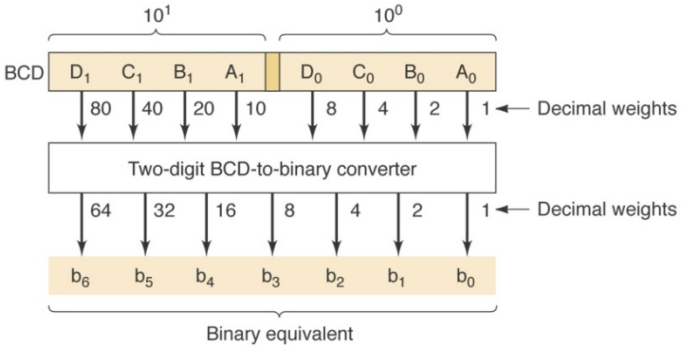
3. **[Digital IC Families]** Given the following switching states for N-channel MOSFET,



Analyze and explain the function of the following circuits. (10%)



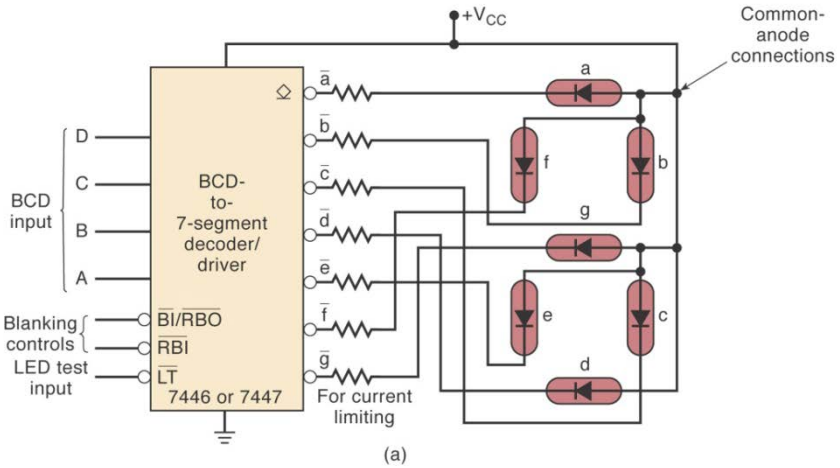
4. **[BCD-to-Binary Code Converter]** (a) Convert the BCD number ***267*** into binary by referencing to the conversion process illustrated below for a **2-digit number.** (5%)



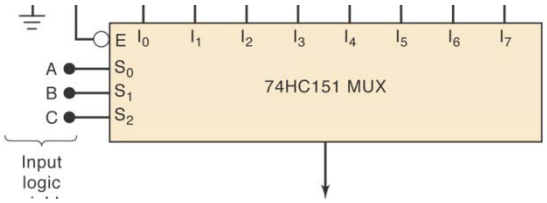
(b) Modify the following code to perform a 3-digit BCD-to-binary converter. (5%)

```
1   SUBDESIGN fig9_68
2   (  ones[3..0], tens[3..0]     :INPUT;
3      binary[6..0]               :OUTPUT;  )
4
5   VARIABLE times10[6..0]        :NODE;    % variable for tens digit times 10%
6
7   BEGIN
8      times10[] = (tens[],B"000") + (B"00",tens[],B"0");
9            % shift left 3X (times 8) + shift left 1X (times 2) %
10     binary[] = times10[] + (B"000",ones[]);
11           % tens digit times 10 + ones digit %
12  END;
```

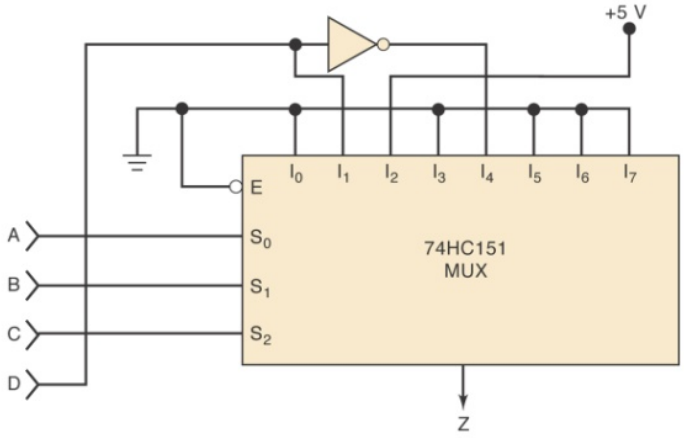
5. **[HEX Decoder]** (a) Construct the truth table of a BCD-to-7-segment decoder by referring to the following figure. (2%) (b) Using the following BCD-to-7-segment decoder as a reference to design a HEX decoder/driver for a 7-segment display. First you need to decide what to display for DCBA=1010,1011,1100,1101,1110,1111. (2%) (c) Construct the truth tables for a,b,c,d,e,f,g. (2%) (d) Write down the logic expression for b and f in terms of the inputs D(MSB),C,B,A(LSB).(4%) (Ignore blanking control and test inputs.)



6. **[Multiplexer]** (a) Show how to generate the logic function Z= AB +BC +AC. (4%)



(b) The following circuit shows how an eight-input MUX can be used to generate a four-variable logic function, even though the MUX has only 3 SELECT inputs. Three of the logic variables A,B and C are connected to the SELECT inputs. The fourth variable D and its inverse D' are connected to selected data inputs as required by the desired logic function. The other MUX data inputs are tied to a LOW or a HIGH as required by the function. Set up a truth table showing the output Z for the 16 possible combinations of input variables. (3%) (c) Write the SOP expressions for Z and simplify the result. (3%)



7. **[Analog to Digital Converter]** (a) Illustrate how a 4-bit successive-approximation ADC converter works assuming that the analog input V_A is 3.1 V and the step size is 1V. (6%) (b) Both 3.1V and 3.9V will be converted to 0011 using the standard SAC converter. Suggest how to modify the conversion process so that 3.1V will be converted to 0011 and 3.9V will be converted to 1000 (i.e., with round-off). (2%) (c) For each of the following statements, indicate which type of ADC (digital-ramp, SAC or flash) is being described: (7%)

(1) Fastest method of conversion (2) Needs a START signal (3) Requires most circuitry

(4) Does not use a DAC. (5) Generates a staircase signal. (6) Uses an analog comparator.

(7) Has a relatively fixed conversion time independent of V_A.

8. **[Memory devices]** (a) DRAM stands for ? SAM stands for? ROM stands for? (6%) (b) For a DRAM cell shown below, which switches are closed during the WRITE operation? Which switches are closed during the READ operation? (4%)