邏輯設計 Hw#6

請於6/13(五)下課前繳交

1. A sequential circuit with two D flip-flops A and B, two inputs X and Y, and one output Z is specified by the following input equations:

$$D_A = X'A + XY \quad D_B = X'A + XB \quad Z = XB$$

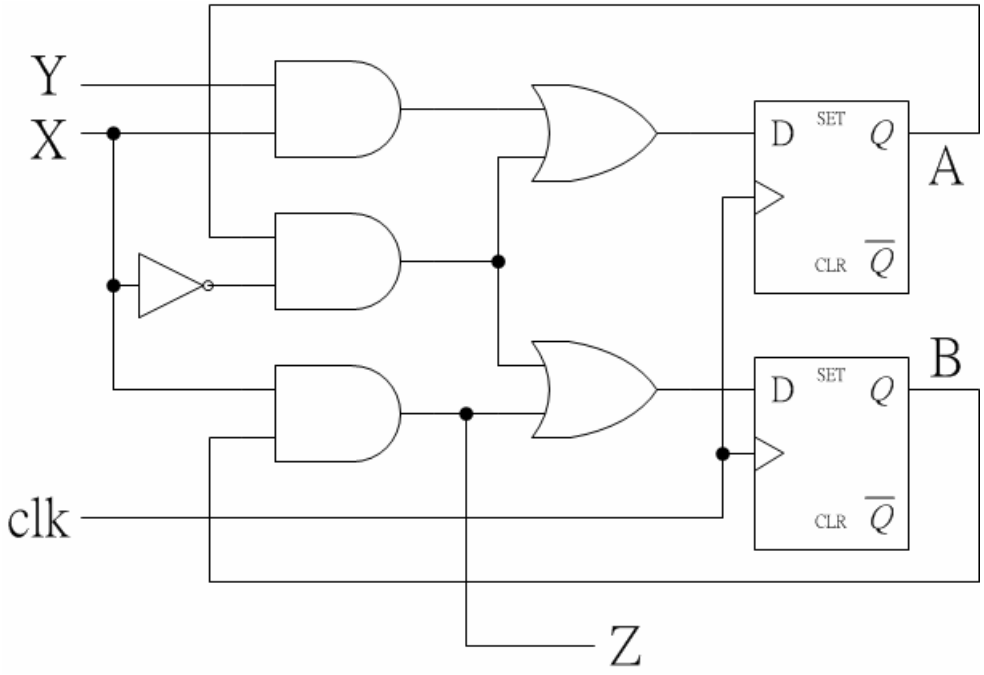
(a) Draw the logic diagram of the circuit.

(b) Derive the state table.

(c) Derive the state diagram.

<Ans.>

(a)



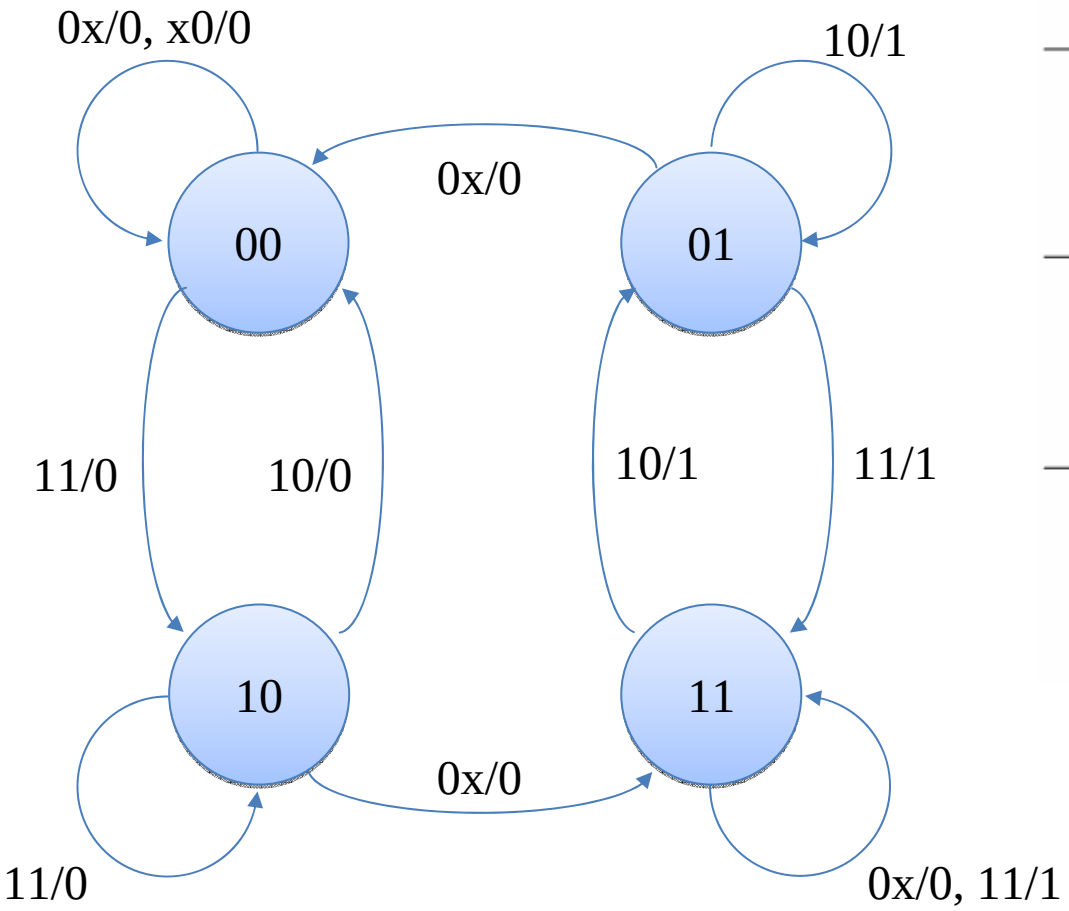
(b)

Present state		Inputs		Next state		Output
A	B	X	Y	A^+	B^+	Z
0	0	0	0	0	0	0
0	0	0	1	0	0	0
0	0	1	0	0	0	0
0	0	1	1	1	0	0
0	1	0	0	0	0	0
0	1	0	1	0	0	0
0	1	1	0	0	1	1
0	1	1	1	1	1	1
1	0	0	0	1	1	0
1	0	0	1	1	1	0
1	0	1	0	0	0	0
1	0	1	1	1	0	0
1	1	0	0	1	1	0
1	1	0	1	1	1	0
1	1	1	0	0	1	1
1	1	1	1	1	1	1

<Ans.>

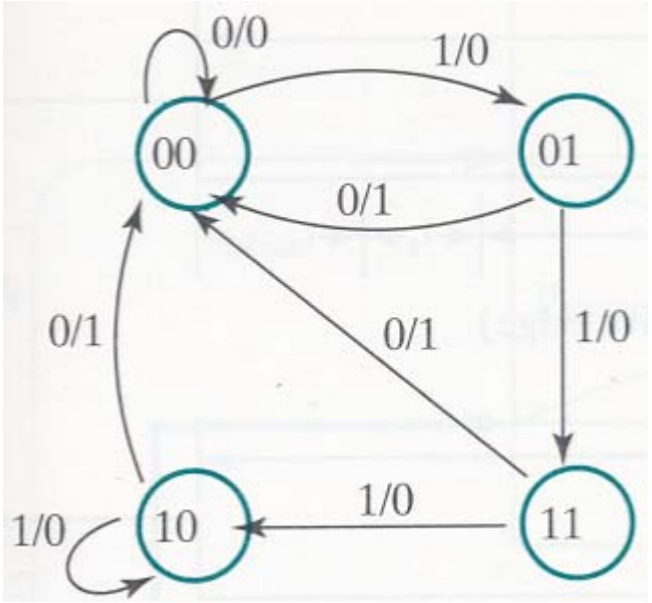
(c)

Format: XY/Z
(x = don't care)



Present state		Inputs		Next state		Output
A	B	X	Y	A^+	B^+	Z
0	0	0	0	0	0	0
0	0	0	1	0	0	0
0	0	1	0	0	0	0
0	0	1	1	1	0	0
0	1	0	0	0	0	0
0	1	0	1	0	0	0
0	1	1	0	0	1	1
0	1	1	1	1	1	1
1	0	0	0	1	1	0
1	0	0	1	1	1	0
1	0	1	0	0	0	0
1	0	1	1	1	0	0
1	1	0	0	1	1	0
1	1	0	1	1	1	0
1	1	1	0	0	1	1
1	1	1	1	1	1	1

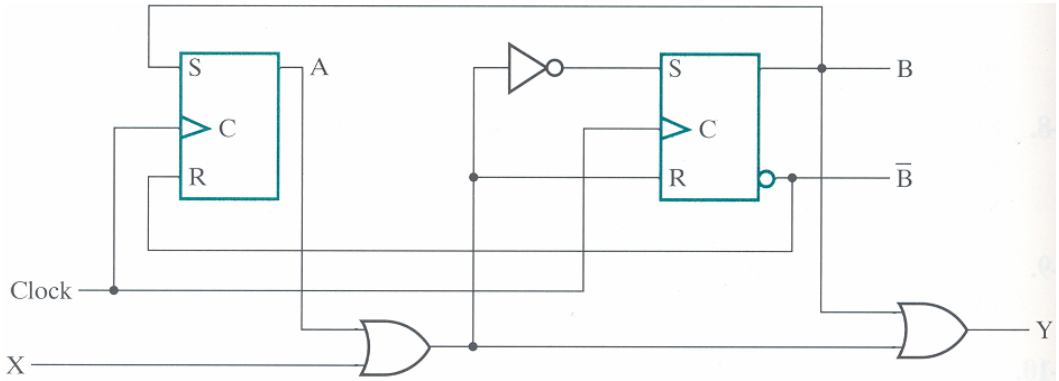
2. Starting from state 00 in the diagram of figure, determine the state transitions and output sequence that will be generated when an input sequence of 10011011110 is applied.



<Ans.>

State 變化	Input	Output
00	1	0
01	0	1
00	0	0
00	1	0
01	1	0
11	0	1
00	1	0
01	1	0
11	1	0
10	1	0
10	0	1
00		

3. A sequential circuit has two SR flip-flops, one input X, and one output Y. The logic diagram of the circuit is shown in figure. Derive the state table and state diagram of the circuit.



<Ans.>

$S_A = B$ $R_A = B'$

$S_B = (X + A)'$ $R_B = X + A$

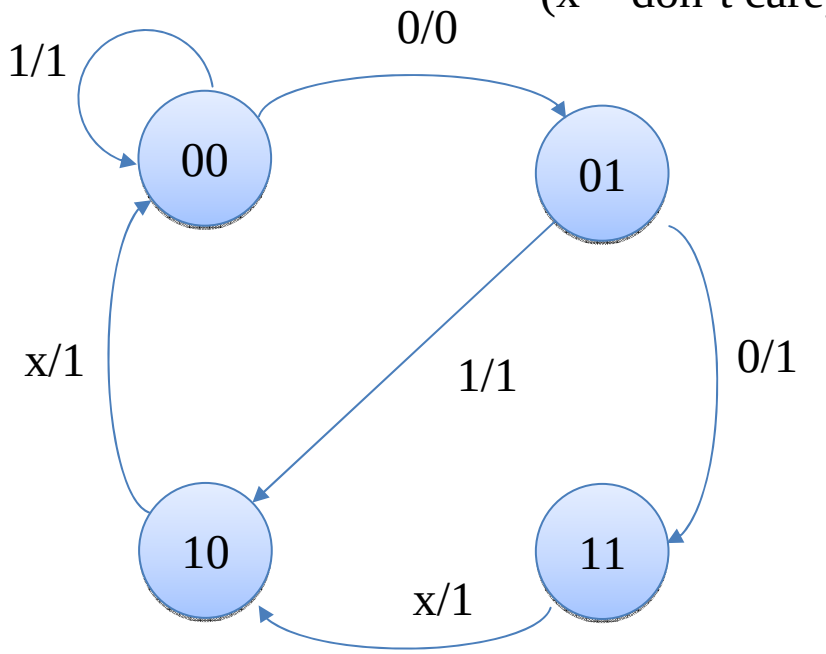
$Y = A + B + X$

$A^+ = S_A + R_A' A = B + (B')'A = B$

$B^+ = S_B + R_B' B = (X + A)' + ((X + A)')' B = (X + A)'$

Present state		Input	Next state		Output
A	B	X	A^+	B^+	Y
0	0	0	0	1	0
0	0	1	0	0	1
0	1	0	1	1	1
0	1	1	1	0	1
1	0	0	0	0	1
1	0	1	0	0	1
1	1	0	1	0	1
1	1	1	1	0	1

Format: X/Y
(x = don't care)



4. A sequential circuit is given in figure. The timing parameters for the gates and flip-flops are as follows:

Inverter: t_{pd} = 0.5 ns XOR Gate: t_{pd} = 2.0 ns

Flip-flop: t_{pd} = 2.0 ns, t_s = 1.0 ns and t_h = 0.25 ns

(a) Find the longest path delay from an external circuit input passing through gates only to an external circuit output.

(b) Find the longest path delay in the circuit from an external input to positive clock edge.

(c) Find the longest path delay from positive clock edge to output.

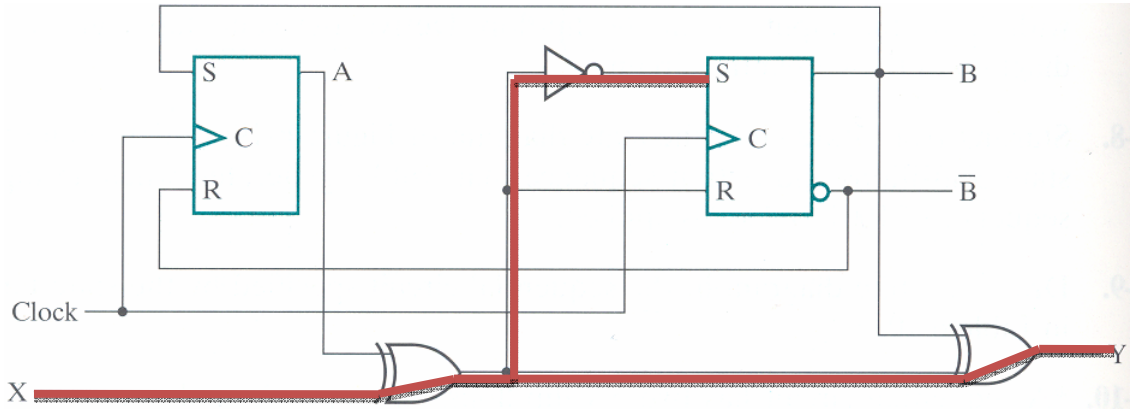
(d) Find the longest path delay from positive clock edge to positive clock edge.

(e) Determine the maximum frequency of operation of the circuit in megahertz (MHz).

<Ans.>

(a) $t_{delay} = t_{pdXOR} \times 2$
$= 4.0$ ns

(b) $t_{delay} = t_{pdXOR} + t_{pbINV} + t_{sFF}$
$= 3.5$ ns



4.

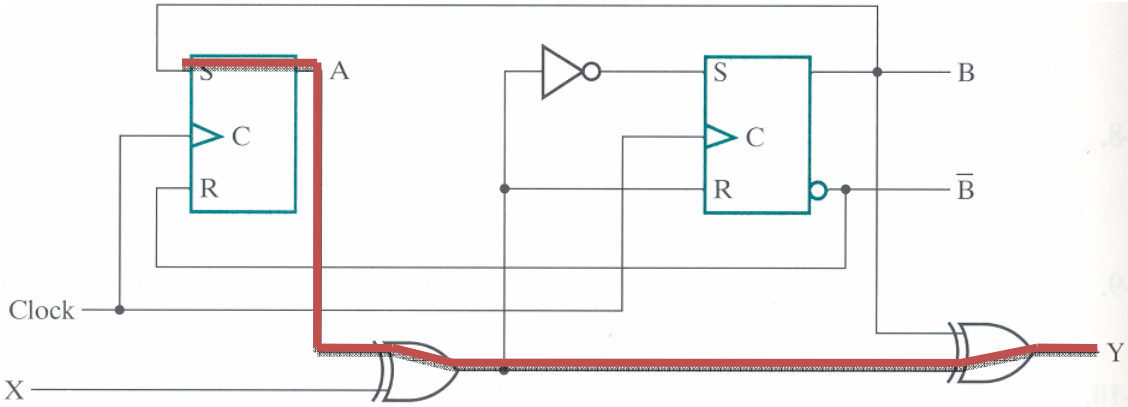
(c) Find the longest path delay from positive clock edge to output.

(d) Find the longest path delay from positive clock edge to positive clock edge.

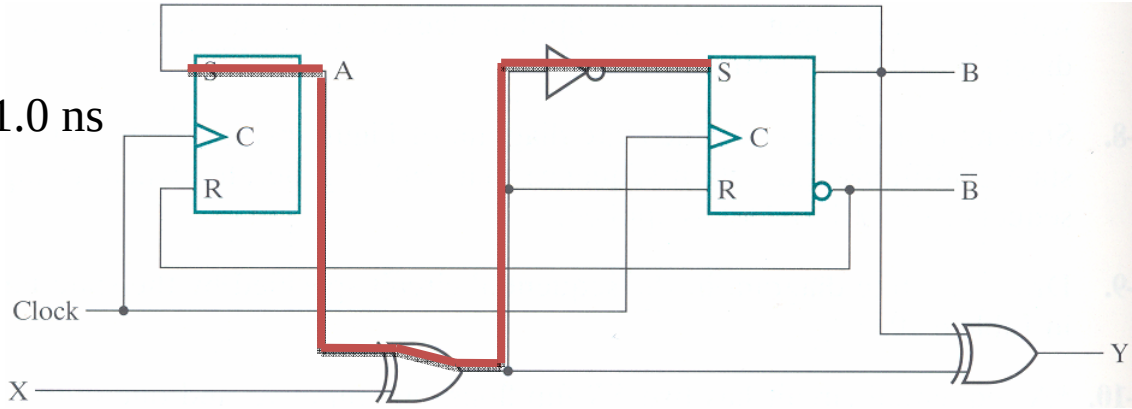
(e) Determine the maximum frequency of operation of the circuit in megahertz (MHz).

<Ans.>

(c) $t_{delay} = t_{pdFF} + t_{pdXOR} + t_{pdXOR}$
$= 6.0$ ns



(d) $t_{delay} = t_{pdFF} + t_{pdXOR} + t_{pdINV} + t_{sFF}$
$= 2.0$ ns $+ 2.0$ ns $+ 0.5$ ns $+ 1.0$ ns
$= 5.5$ ns



(e) Maximum frequency $= 1 / t_{delay\_max} = 1 / 6.0$ ns $= 166.67$ MHz

5. A Universal Serial Bus (USB) communication link requires a circuit that produces the sequence 00000001. You are to design a synchronous sequential circuit that starts producing this sequence for input E = 1. Once the sequence starts, it completes. If E = 1, during the last output in the sequence, the sequence repeats. Otherwise, if E = 0, the output remains constant at 1.

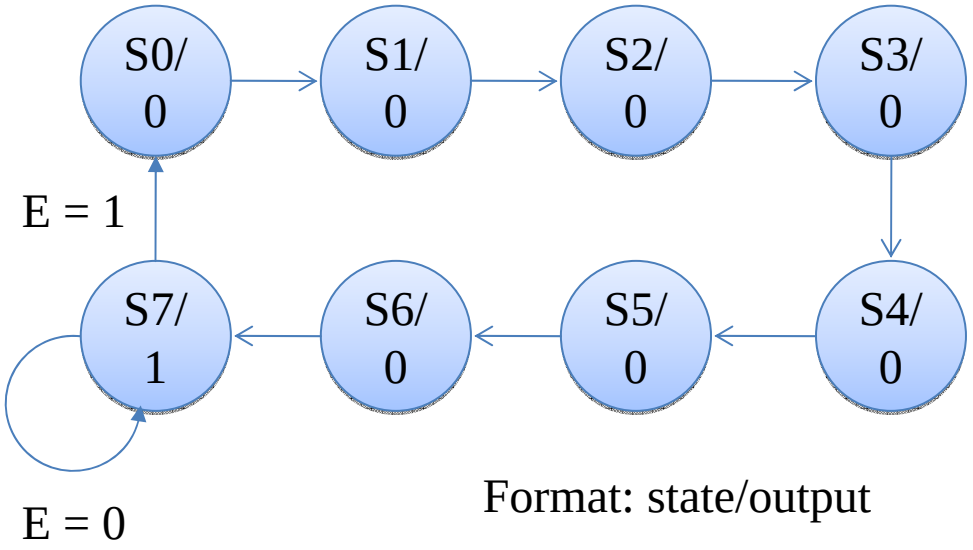
(a) Draw the Moore state diagram for the circuit.

(b) Find the state table and make a state assignment.

(c) Design the circuit using D flip-flops and logic gates. A reset should be include to place the circuit in the appropriate initial state at which E is examined to determine if the sequence or constant 1's is to be produced.

<Ans.>

(a)



Format: state/output

(b)因為有0~7共8個states，所以用$D_2D_1D_0$ 3 bits 表示。

Present state	Next state For input		Output
$D_2D_1D_0$	E = 0	E = 1	Z
0 0 0	0 0 1		0
0 0 1	0 1 0		0
0 1 0	0 1 1		0
0 1 1	1 0 0		0
1 0 0	1 0 1		0
1 0 1	1 1 0		0
1 1 0	1 1 1		0
1 1 1	1 1 1	0 0 0	1

5.

(c) Design the circuit using D flip-flops and logic gates. A reset should be include to place the circuit in the appropriate initial state at which E is examined to determine if the sequence or constant 1's is to be produced.

Present state	Next state For input		Output
$D_2D_1D_0$	E = 0	E = 1	Z
0 0 0	0 0 1		0
0 0 1	0 1 0		0
0 1 0	0 1 1		0
0 1 1	1 0 0		0
1 0 0	1 0 1		0
1 0 1	1 1 0		0
1 1 0	1 1 1		0
1 1 1	1 1 1	0 0 0	1

<Ans.>

(c) 根據 (b)

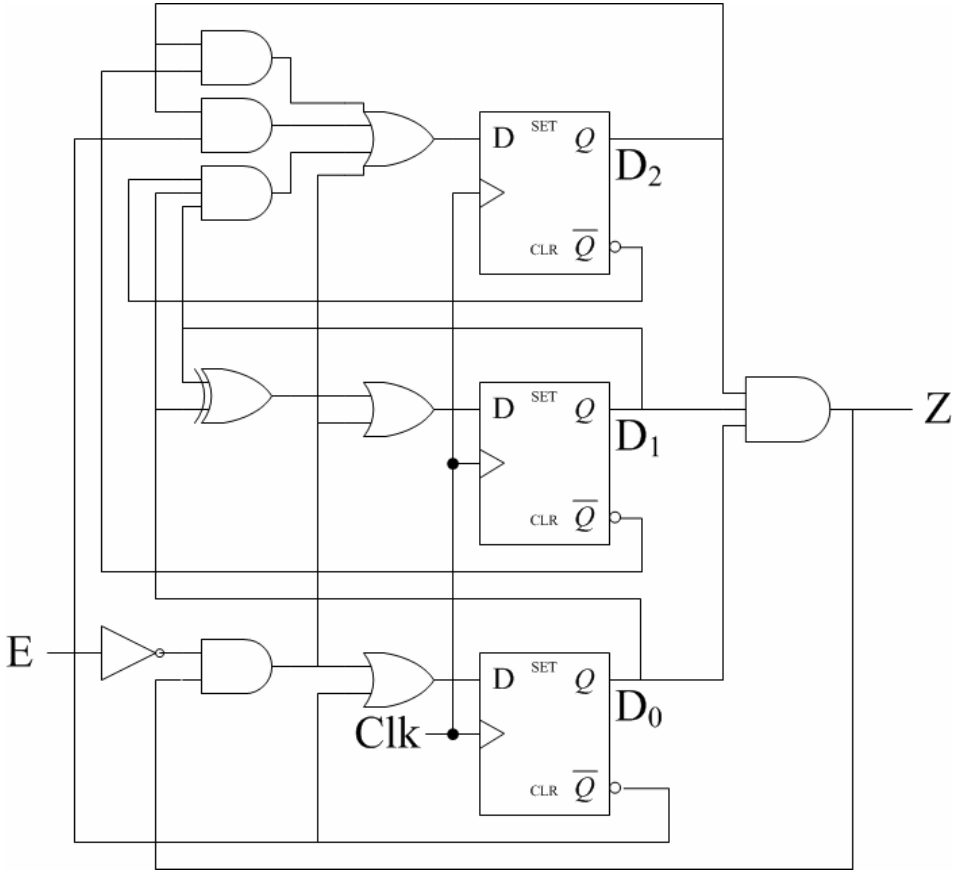
$Z = D_2D_1D_0$

$D_2^+ = D_2D_1' + D_2D_0' + D_2'D_1D_0 + D_2D_1D_0E$

$D_1^+ = D_1 \oplus D_0 + D_2D_1D_0E$

$D_0^+ = D_0' + D_2D_1D_0E$

題目要求reset的作用是讓state初始化成，看E等於多少決定要產生00000001還是一直是1，這跟state 7的行為完全相同，所以將reset接到每個D flip-flop的set。



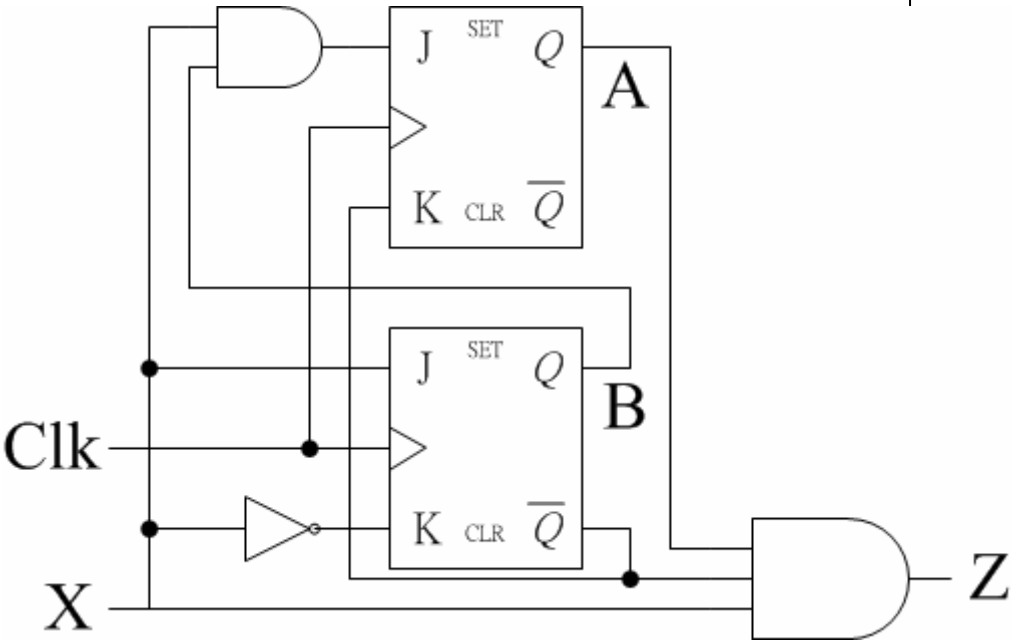
6. Find the logic diagram for the circuit having the state table given in table. Use J-K flip-flops.

<Ans.>

先寫出右圖的 flip-flop inputs
再寫出 input output equations

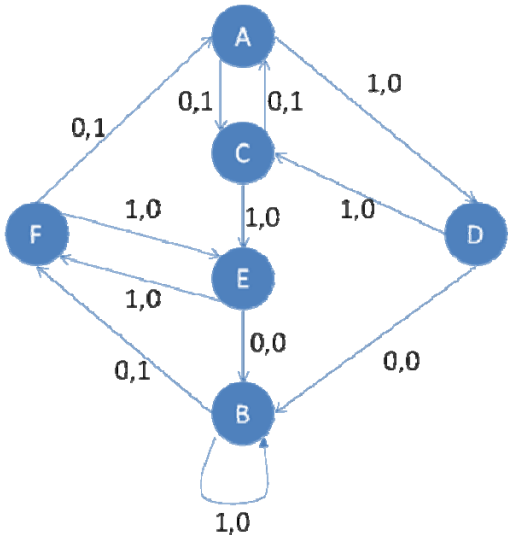
$J_A = BX$
$K_A = B'$
$J_B = X$
$K_B = X'$
$Z = AB'X$

Present state		Input	Next state		Output	Flip-Flop Inputs			
A	B	X	A^+	B^+	Z	J_A	K_A	J_B	K_B
0	0	0	0	0	0	0	X	0	X
0	0	1	0	1	0	0	X	1	X
0	1	0	0	0	0	0	X	X	1
0	1	1	1	1	0	1	X	X	0
1	1	0	1	0	0	X	0	X	1
1	1	1	1	1	0	X	0	X	0
1	0	0	0	0	0	X	1	0	X
1	0	1	0	1	1	X	1	1	X



補充題 1：State Reduction

化簡下列state diagram，求出化簡後的state table



<Ans.>

Step 0. 根據右圖列出 state table

Step 1. I/O behavior 不同者打X

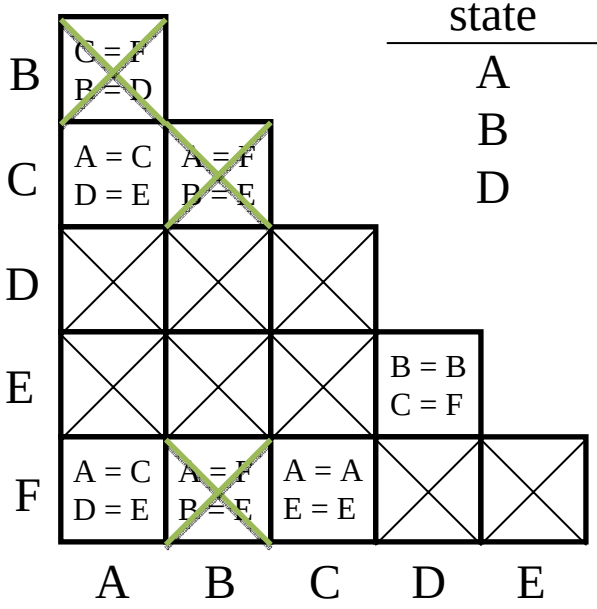
Step 2. 列出 next state 關係

Step 3. 持續檢查因既有的 X 而不可能相同者打 X

round 1. 綠色 X

round 2. 發現沒有再打 X => A = C = F, D = E

Present state	Next state I = 0	Next state I = 1	Output I = 0	Output I = 1
A	C	D	1	0
B	F	B	1	0
C	A	E	1	0
D	B	C	0	0
E	B	F	0	0
F	A	E	1	0



Present state	Next state I = 0	Next state I = 1	Output I = 0	Output I = 1
A	A	D	1	0
B	A	B	1	0
D	B	A	0	0

補充題 2：State Assignment

Given the following state diagram, select a good state assignment. Show your assignment in a state map and justify your answer in terms of the state assignment guidelines.

Present state	Next state I = 0	Next state I = 1	Output I = 0	Output I = 1
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	d	0	1
e	a	d	0	1

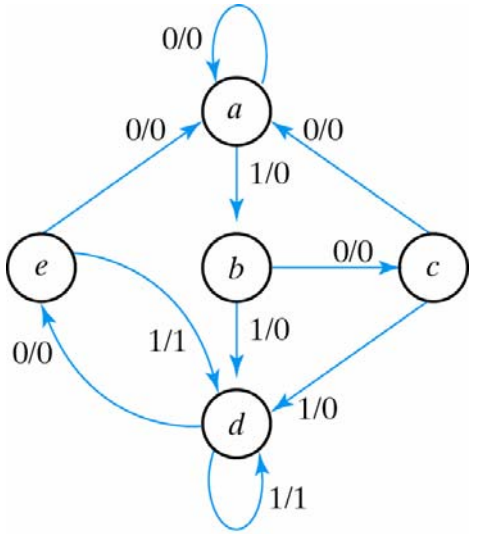


Fig. 5-23 Reduced State Diagram

Highest: states that share a common next state

(b, c, d, e) (a, c, e)

Medium: states that share a common ancestor state

(a, b) (c, d) (a, d) (d, e) (a, d) => **(a, b)** (a, d) × **2** (c, d) (d, e)

Lowest: states that have common output behavior

(a, b, c, d, e) (a, b, c) (d, e)

* 紅色底線表可符合之條件

* 答案非唯一

Q_2 \ Q_1Q_0	00	01	11	10
0	a	d		
1	c	e	b	