Department of Computer Science, National Chengchi University

Digital Systems Midterm Examination, 4/16/2003

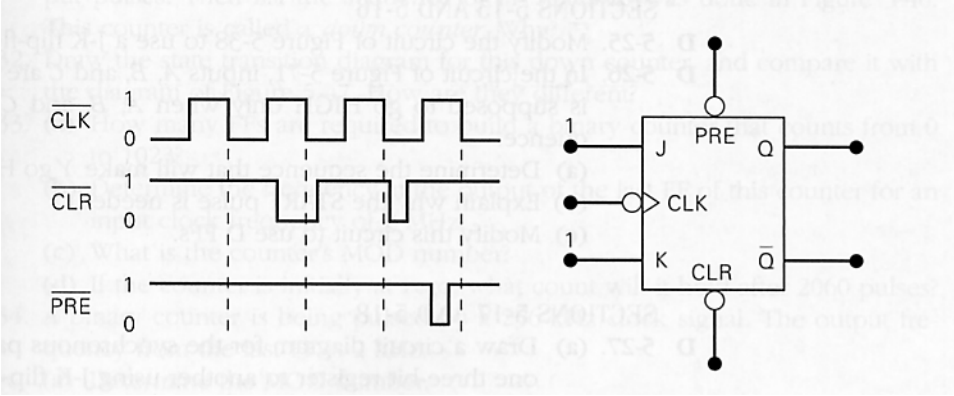
1. True or False (20%)
   (a) Logic expressions in a sum-of-products form are simpler than their product-of-sums counterparts.
   (b) An exclusive OR gate can have only two inputs.
   (c) A J-K flip-flop can be used as an S-C flip-flop, but not vice versa.
   (d) CMOS ICs usually have a lower f_{Max} (maximum clocking frequency) than the TTL counterparts.
   (e) 74ACT series are both pin- and electrically-compatible with TTL.
   (f) Floating input is not allowed in CMOS IC.
   (g) A D latch is in its transparent mode when EN=1.
   (h) Synchronous data transfer requires less circuitry than asynchronous transfer.
   (i) A MOD-4 counter requires 4 J-K flip-flops.
   (j) CMOS ICs should not be used together with TTL ICs because they have different logic-level voltage ranges.
2. (a) Prove that x'+xy=x'+y. Compare the number of basic gates used. (4%)
   (b) Show how an AND gate can be implemented using only NOR gates. Write down the corresponding Boolean expressions. (6%)
3. (a) Simplify the following expressions using Boolean algebra. (6%)
   X = A'BC' + A'BC + ABC + AB'C' + AB'C
   Y= (B+C')(B'+C) + (A'+ B + C')'
   Z = A(C+D)'+A'CD'+AB'C'+A'B'CD+ACD'
   (b) Verify your results in part (a) using Karnaugh maps. (4%)
4. The excess-3 code obtained by adding 3 to the BCD code. (a) Build the truth table for excess-3 code. (3%) (b) Obtain the SOP form of the excess-3 code and use Karnaugh map to simplify the logic equation (Note: be aware of the don't care condition). (5%) (c) Draw the circuit diagram using conventional gate symbols. (2%)
5. (a) Draw the internal circuit of a negative-going-edge-triggered J-K flip-flop and identify the three basic components. (4%)
   (b) Describe how to detect the negative going edge of a pulse. (3%)
   (c) Explain how the FF works when J=K=1. (assuming that Q_{before}=0) (3%)
6. (a) Perform the following operations in the 2's complement system. Use 6 bits (including the sign bit) for each number (6%):
   (1) Add +18 to +14 (2) Add +14 to –17 (3) Subtract +13 from –10 (4) Add 17 to –17
   (b) Repeat (4) for sign-magnitude system. What can you conclude from this result? (4%)
7. (a) BCD addition: Design a combinational circuit to detect when the sum of two digits is

greater than 9 and needs correction. What correction is required? (b) BCD subtraction:

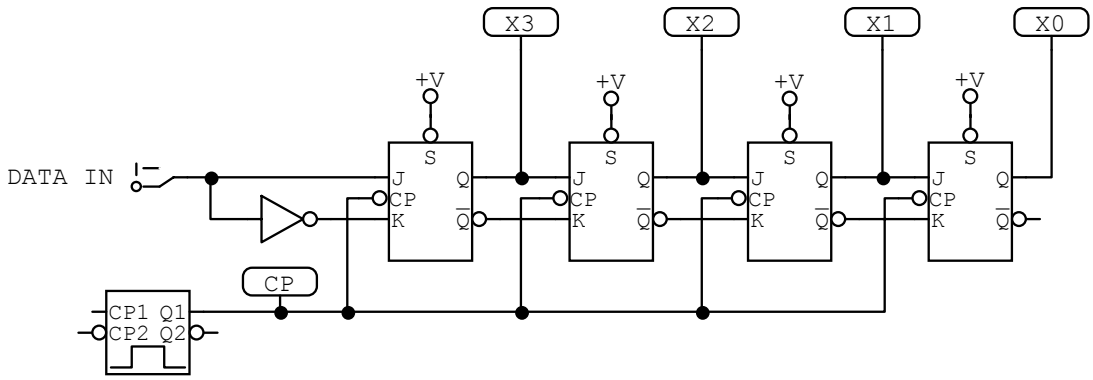
8. One method to detect the overflow situation for an adder that operates in a 2's complement system is described as follows:
   - □ Examine the sign bits of the two number being added
   - □ Examine the sign bit of the result.
   - □ Overflow occurs whenever the numbers being added are both positive and the sign bit of the result is 1 or when the numbers are both negative and the sign bit of the result is 0.

   Suppose the two numbers to be added are $x_3x_2x_1x_0$, $y_3y_2y_1y_0$ and the sum bits are $s_3s_2s_1s_0$, design the overflow detection circuit. (6%)

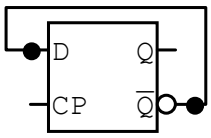
9. (a) Determine the Q waveform for the FF in the following figure, assuming that Q=0 initially.(4%)



10. (a) Shown below is the diagram of a four-bit shift register. Modify the design so that it becomes a *recirculating* shift register that keeps the binary information circulating through the register as clock pulses are applied. Verify your design by listing the states of the registers from its initial state at 1011 (X_3=1, X_2=0,X_1=1,X_0=1) to the eighth shift pulse. (6%)



(b) Explain the function of the circuit shown below (assuming that Q=0 initially). (4%)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Q
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Q