Department of Computer Science, National Chengchi University

Digital Systems Midterm Examination

1. **[Logic Gates]** (a) Show how an XOR gate can be used as an INVERTER. (3%) (b) Then show to construct an XNOR gate using XOR gates. (2%)
2. **[Universality of NOR gate]** Why is the NOR gate universal? Explain with Boolean expressions and the corresponding circuit diagrams. (6%)
3. **[Gray code and combinational circuit design]** (a) What is the key property of Gray codes? (2%) (b) Convert 010101 (gray) to its binary code equivalent. (3%) (c) Design a 3-bit gray-to-binary converter using only basic AND, OR, NOT gates. (9%)
4. **[Boolean Theorem]** (a) Prove x+x'y=x+y without using truth table. (5%)
5. **[SOP to POS]** The SOP form of a two-variable logic function can be expressed as: $f(x,y) = \alpha_0 \bar{x}\bar{y} + \alpha_1 \bar{x}y + \alpha_2 x\bar{y} + \alpha_3 xy$ while the POS of a two-variable logic function can be expressed as $g(x,y) = (\bar{x}+\bar{y})^{\beta_0}(\bar{x}+y)^{\beta_1}(x+\bar{y})^{\beta_2}(x+y)^{\beta_3}$, $\alpha_i, \beta_i \in \{0,1\}$.

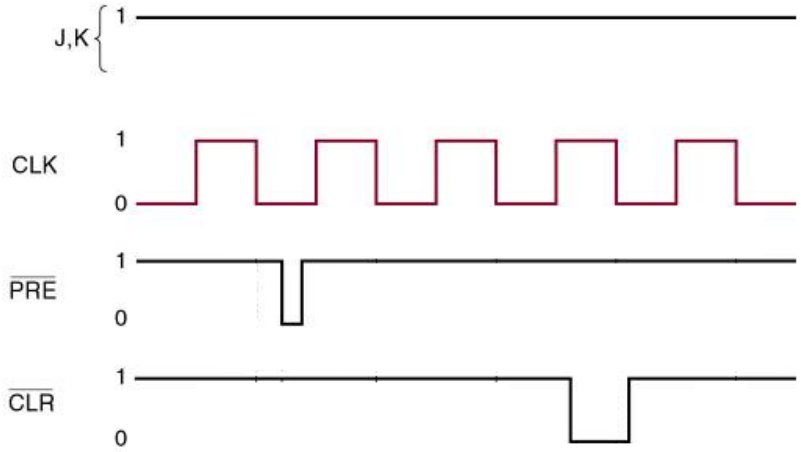
   Suppose we have an expression in the sum-of-products format, suggest a systematic way to convert it into product-of-sums format. Use h(x,y)= xy + x'y' as an example to illustrate the steps. (10%) [Hint: DeMorgan theorem]
6. **[Combinational Circuit Design by Inspection]** You are asked to design a *comparator* that takes two four-bit signed binary numbers $x_3x_2x_1x_0$ and $y_3y_2y_1y_0$ (represented in *2's complement*) and determine whether they are equal and, if not, which one is larger. There are three outputs, defined as follows: (10%)
   - M=1 only if the two input numbers are equal.
   - N=1 only if $x_3x_2x_1x_0$ is greater than $y_3y_2y_1y_0$
   - P=1 only if $y_3y_2y_1y_0$ is greater than $x_3x_2x_1x_0$

   Design the logic circuitry for this comparator. (Note: This circuit has eight inputs and three outputs and is therefore much too complex to handle using the truth-table approach.)
7. **[J-K Flip Flop]** (a) Draw the internal circuit of a negative-going-edge-triggered J-K flip-flop and identify the three basic components. (4%)

   (b) Describe how to detect the positive and negative going edge of a pulse. (3%)

   (c) Explain how the FF works when J=K=1. (assuming $Q_{initial}$=1) (3%)

8. **[Timing Diagram]** For a PGT J-K FF shown below, draw the output Q if Q is initially set to 1. (5%)



9. **[Overflow Detection]** Suppose we want to add two **k**-bit numbers: $\mathbf{x_{k-1}...x_0}$ and $\mathbf{y_{k-1}...y_0}$. The sum is $\mathbf{s_{k-1}...s_0}$. Design the logic circuit for detecting the overflow condition. (5%)
10. **[Synchronous vs. Asynchronous Counter]** (a) Design a MOD-12 ripple counter using J-K flip flops and basic logic gates. (b) Design a MOD-12 synchronous up counter using J-K flip flops and basic logic gates.(10%)
11. **[Synchronous Counter Design]** (a) Fill in the blanks in the following J-K excitation table. (2%)

Transition at Output	Present State	Next State	J	K
0→0	0	0		
0→1	0	1		
1→0	1	0		
1→1	1	1		

(b) Use the above table to design a synchronous counter with the following counting sequence: 0→1→3→5→7→2→4→6, and repeat. You should write down the complete design procedure and draw the final implementation using J-K flip-flops. (10%)

12. **[HDL]** (a) HDL is the abbreviation of _____ (3%) ?
(b) Rewrite the following code for a NOR latch in AHDL. (5%)