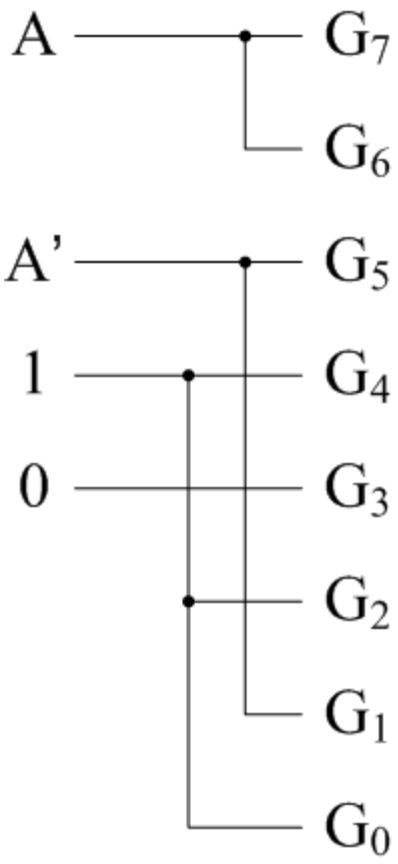
邏輯設計 Hw#4
Answer

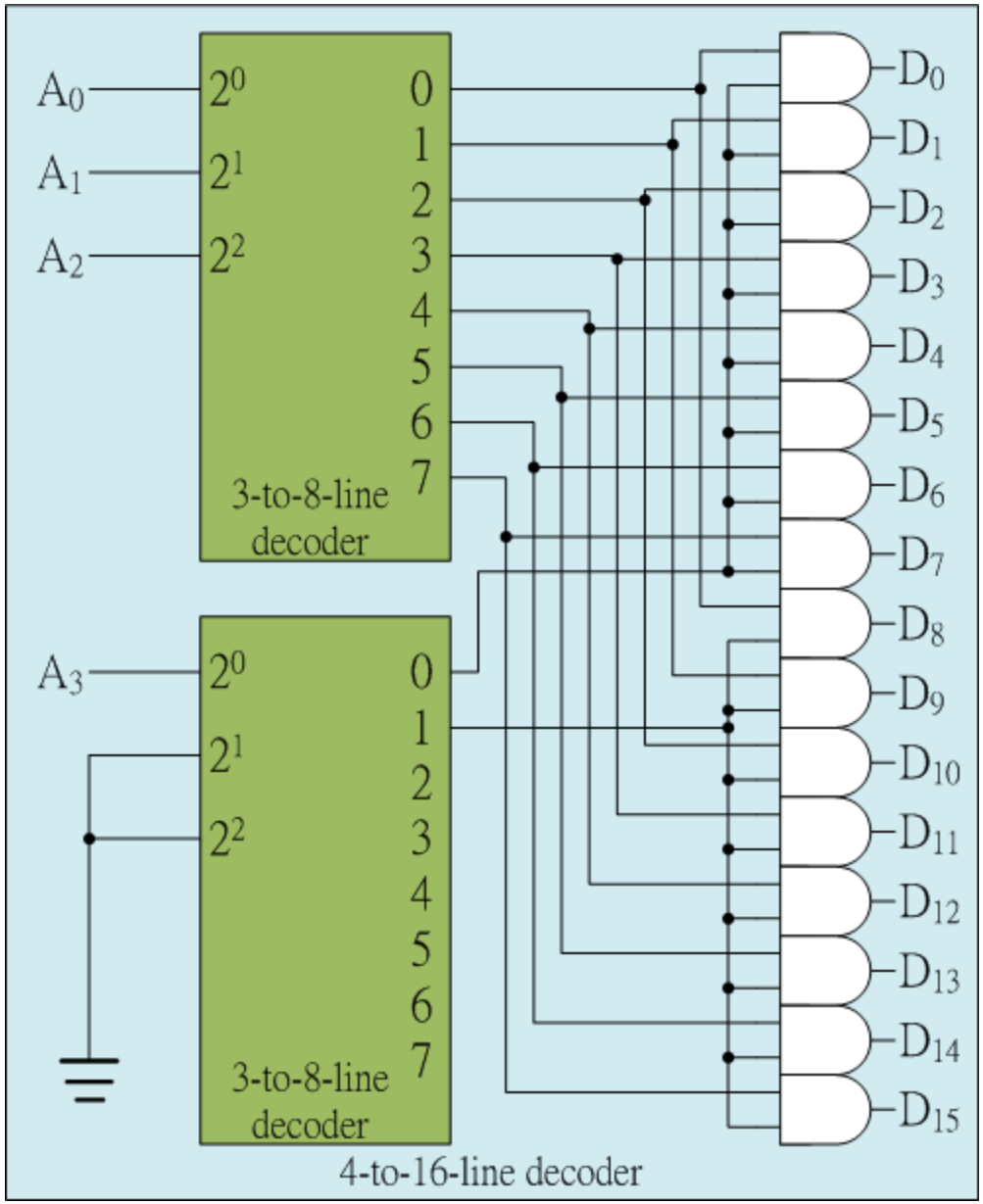
1. Draw an implementation diagram for a rudimentary vector function G = (G_7, G_6, G_5, G_4, G_3, G_2, G_1, G_0) = (A, A, A', 1, 0, 1, A', 1) using inputs 1, 0, A, and A'.

<Ans>



2. Design a 4-to-16-line decoder using two 3-to-8-line decoders and 16 2-input AND gates.

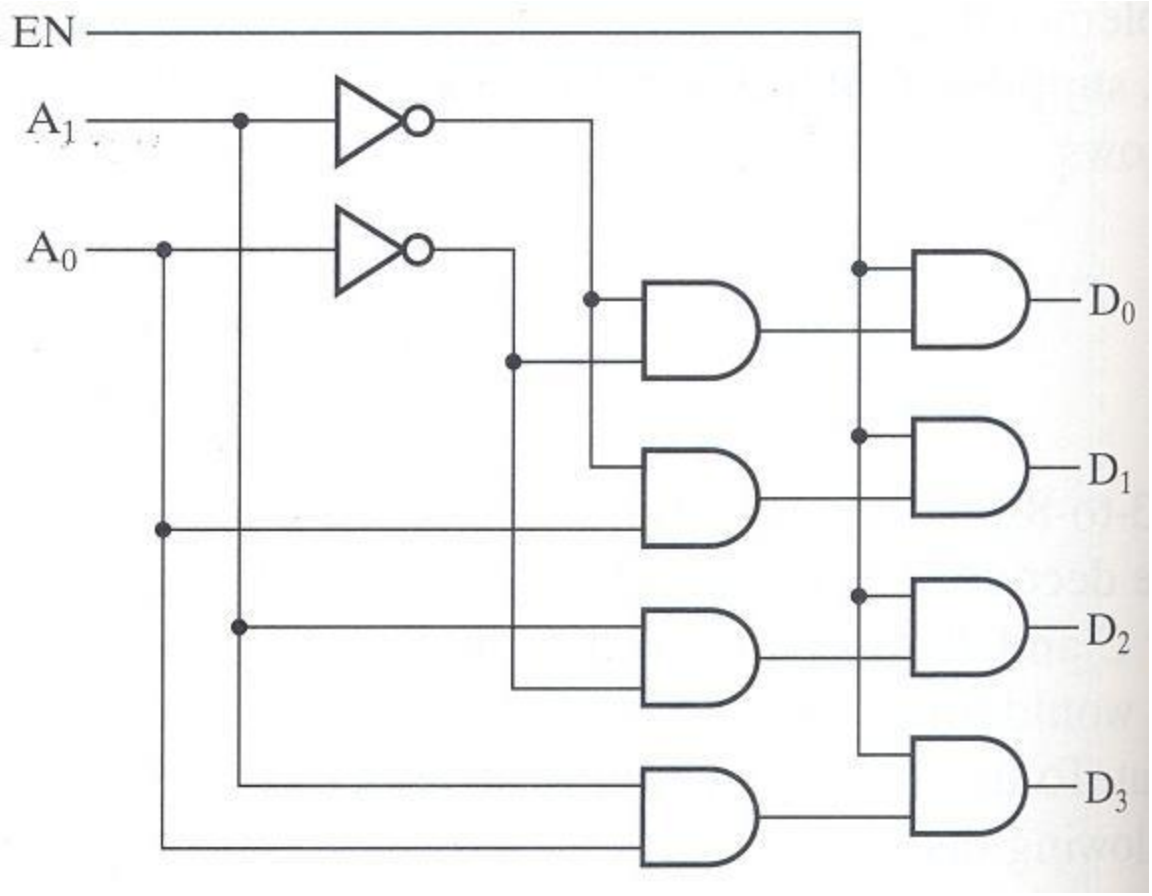
<Ans>



其實用2個3-to-8-line decoders有點多餘，以1-to-2-line decoder便可勝任第2個3-to-8-line decoder的工作。

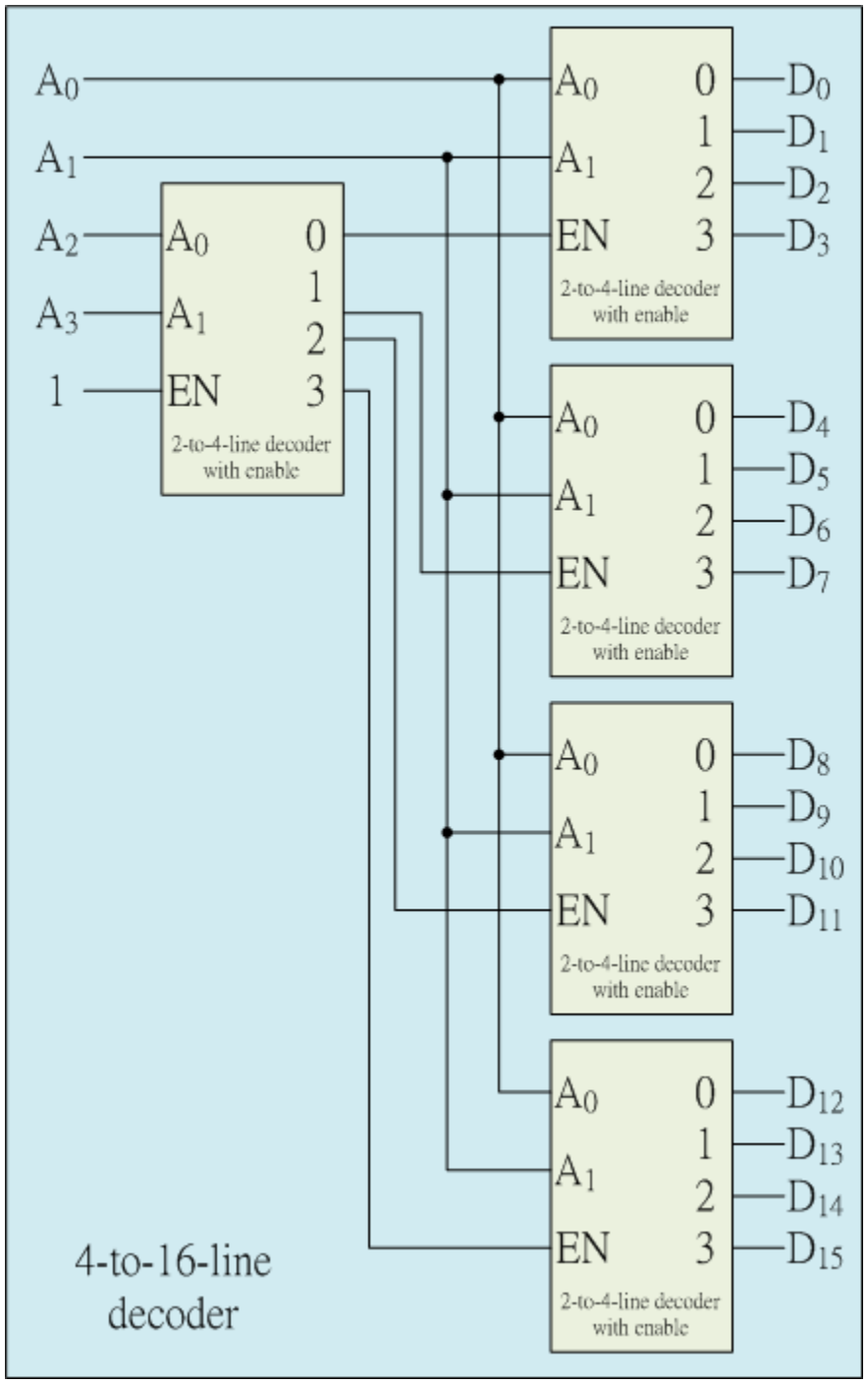
3. Design a 4-to-16-line decoder with enable using five 2-to-4-line decoders with enables as shown in figure.

EN	A_1	A_0	D_0	D_1	D_2	D_3
0	X	X	0	0	0	0
1	0	0	1	0	0	0
1	0	1	0	1	0	0
1	1	0	0	0	1	0
1	1	1	0	0	0	1



<Ans>

A_3A_2	A_1A_0	哪個output爲1
0 0	0 0	D_0
0 0	0 1	D_1
0 0	1 0	D_2
0 0	1 1	D_3
0 1	0 0	D_4
0 1	0 1	D_5
0 1	1 0	D_6
0 1	1 1	D_7
1 0	0 0	D_8
1 0	0 1	D_9
1 0	1 0	D_{10}
1 0	1 1	D_{11}
1 1	0 0	D_{12}
1 1	0 1	D_{13}
1 1	1 0	D_{14}
1 1	1 1	D_{15}



4. Derive the truth table of a Decimal-to-binary priority encoder.

<Ans> 9 is the highest priority.

Decimal Inputs										Binary Outputs				
9	8	7	6	5	4	3	2	1	0	A_3	A_2	A_1	A_0	V
0	0	0	0	0	0	0	0	0	0	X	X	X	X	0
0	0	0	0	0	0	0	0	0	1	0	0	0	0	1
0	0	0	0	0	0	0	0	1	X	0	0	0	1	1
0	0	0	0	0	0	0	1	X	X	0	0	1	0	1
0	0	0	0	0	0	1	X	X	X	0	0	1	1	1
0	0	0	0	0	1	X	X	X	X	0	1	0	0	1
0	0	0	0	1	X	X	X	X	X	0	1	0	1	1
0	0	0	1	X	X	X	X	X	X	0	1	1	0	1
0	0	1	X	X	X	X	X	X	X	0	1	1	1	1
0	1	X	X	X	X	X	X	X	X	1	0	0	0	1
1	X	X	X	X	X	X	X	X	X	1	0	0	1	1

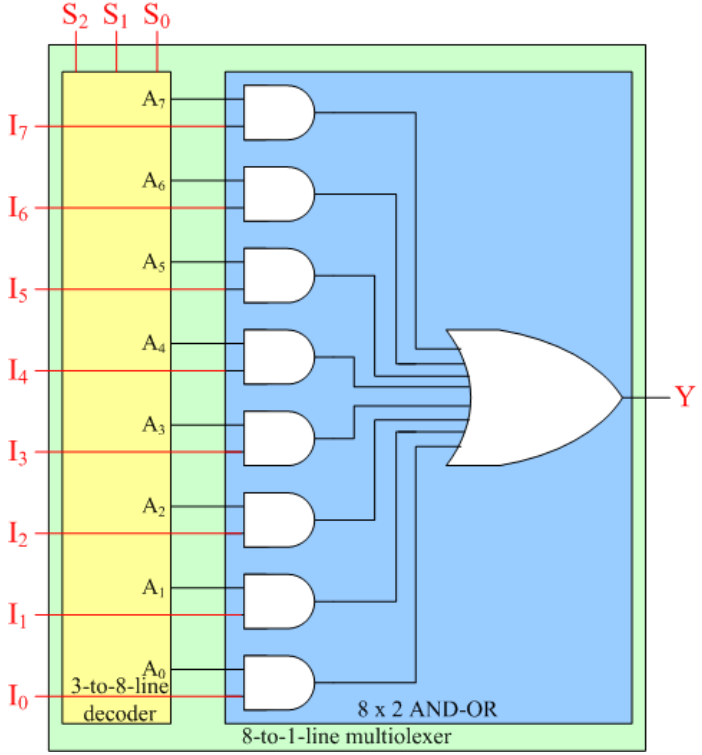
5. (a) Design an 8-to-1-line multiplexer using a 3-to-8-line decoder and an 8 × 2 AND-OR.

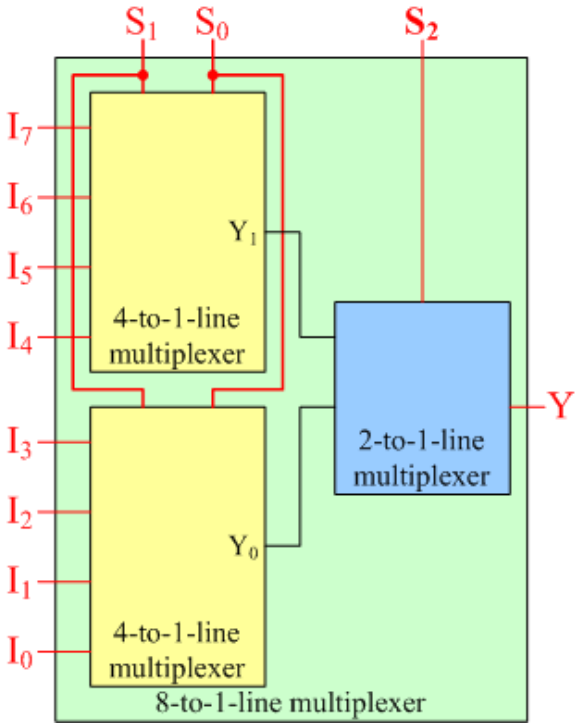
(b) Repeat part (a), using two 4-to-1-line multiplexers and one 2-to-1-line multiplexers.

<Ans>

(a) 將選擇訊號$S_2S_1S_0$輸入3-to-8-line decoder，再將decoder輸出的A_7~A_0跟Input I_7~I_0分別AND在一起決定是否讓I_i通過送到OR gate，左圖。

(b) 將選擇訊號S_1S_0餵給兩個4-to-1-line multiplexers，自分成兩組的I_7~I_4、I_3~I_0中選出兩個中間值Y_1、Y_0，最後2-to-1-line multiplexer再利用選擇訊號S_2決定是哪一個是真正要輸出的，右圖。





6. A combinational circuit is specified by the following three Boolean functions:

$F_1(A, B, C) = \Sigma m(0,3,4)$

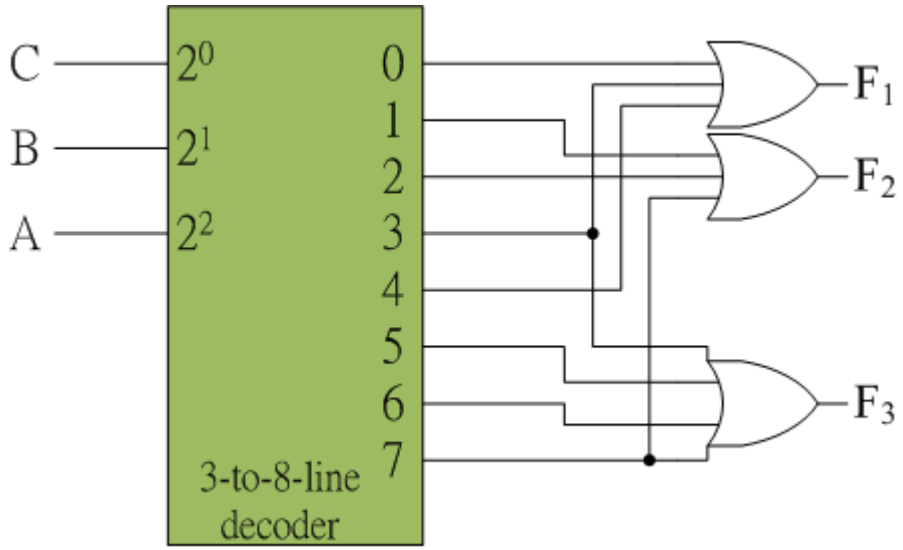
$F_2(A, B, C) = \Sigma m(1,2,7)$

$F_3(A, B, C) = \Pi M(0,1,2,4)$

Implement the circuit with a decoder and external OR gates.

<Ans>

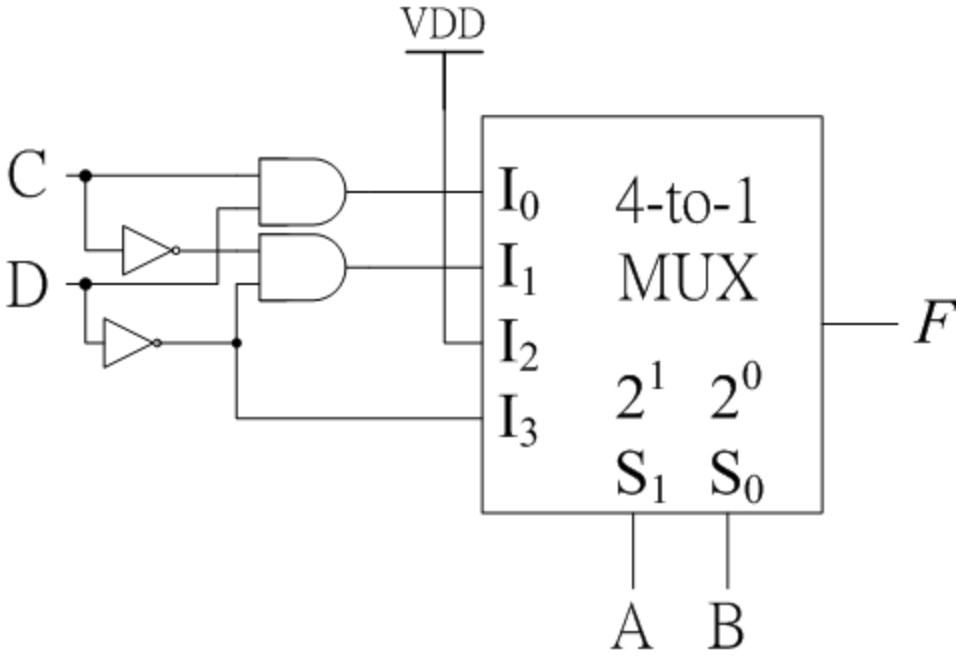
$F_3(A, B, C) = \Pi M(0,1,2,4) = \Sigma m(3, 5, 6, 7)$



7. Implement the Boolean function F(A,B,C,D) = Σm(3,4,8,9,10,11,12,14) with a 4-to-1-line multiplexer and external gates. Connect inputs A and B to the selection lines. The input requirements for the four data lines will be a function of the variables C and D. The values of these variables are obtained by expressing F as a function of C and D for each of the cases when AB = 00, 01, 10, and 11. These functions must be implemented with external gates.

<Ans>

AB	CD	F	CD與F的關係
0 0	0 0	0	F = CD
0 0	0 1	0	
0 0	1 0	0	
0 0	1 1	1	
0 1	0 0	1	F = C'D'
0 1	0 1	0	
0 1	1 0	0	
0 1	1 1	0	
1 0	0 0	1	F = 1
1 0	0 1	1	
1 0	1 0	1	
1 0	1 1	1	
1 1	0 0	1	F = C'D' + CD' = D'
1 1	0 1	0	
1 1	1 0	1	
1 1	1 1	0	



8. Tabulate the truth table for an 8 × 4 ROM that implements the following four Boolean functions:

$A(X, Y, Z) = \Sigma m(0,1,2,6,7)$

$B(X, Y, Z) = \Sigma m(2,3,4,5,6)$

$C(X, Y, Z) = \Sigma m(2,6)$

$D(X, Y, Z) = \Sigma m(1,2,3,5,6,7)$

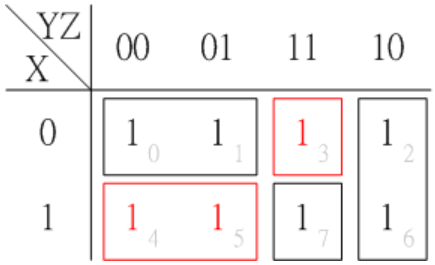
<Ans>

Inputs			Outputs			
X	Y	Z	A	B	C	D
0	0	0	1	0	0	0
0	0	1	1	0	0	1
0	1	0	1	1	1	1
0	1	1	0	1	0	1
1	0	0	0	1	0	0
1	0	1	0	1	0	1
1	1	0	1	1	1	1
1	1	1	1	0	0	1

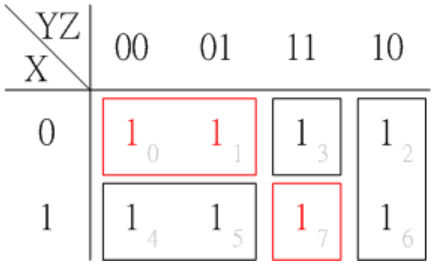
9. Obtain the PLA programming table for the four Boolean functions listed in Problem 8. Minimize the number of product terms. Be sure to attempt to share product terms between functions that are not prime implicants of individual functions and to consider the use of complemented (C) outputs.

<Ans>

A A'



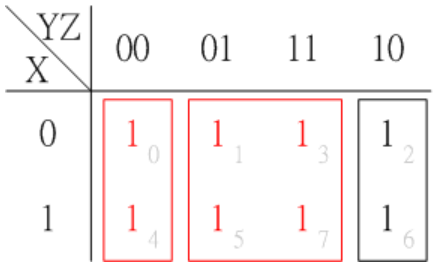
B B'



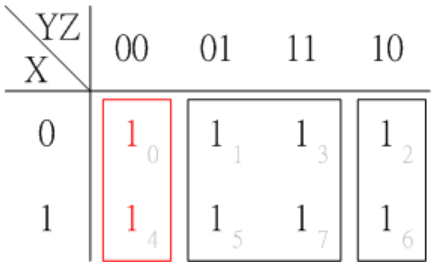
$A = X'Y' + XYZ + YZ'$ $B = XY' + X'YZ + YZ'$

$A' = XY' + X'YZ$ $B' = X'Y' + XYZ$

C C'



D D'



$C = YZ'$ $D = Z + YZ'$

$C' = Y'Z' + Z$ $D' = Y'Z'$

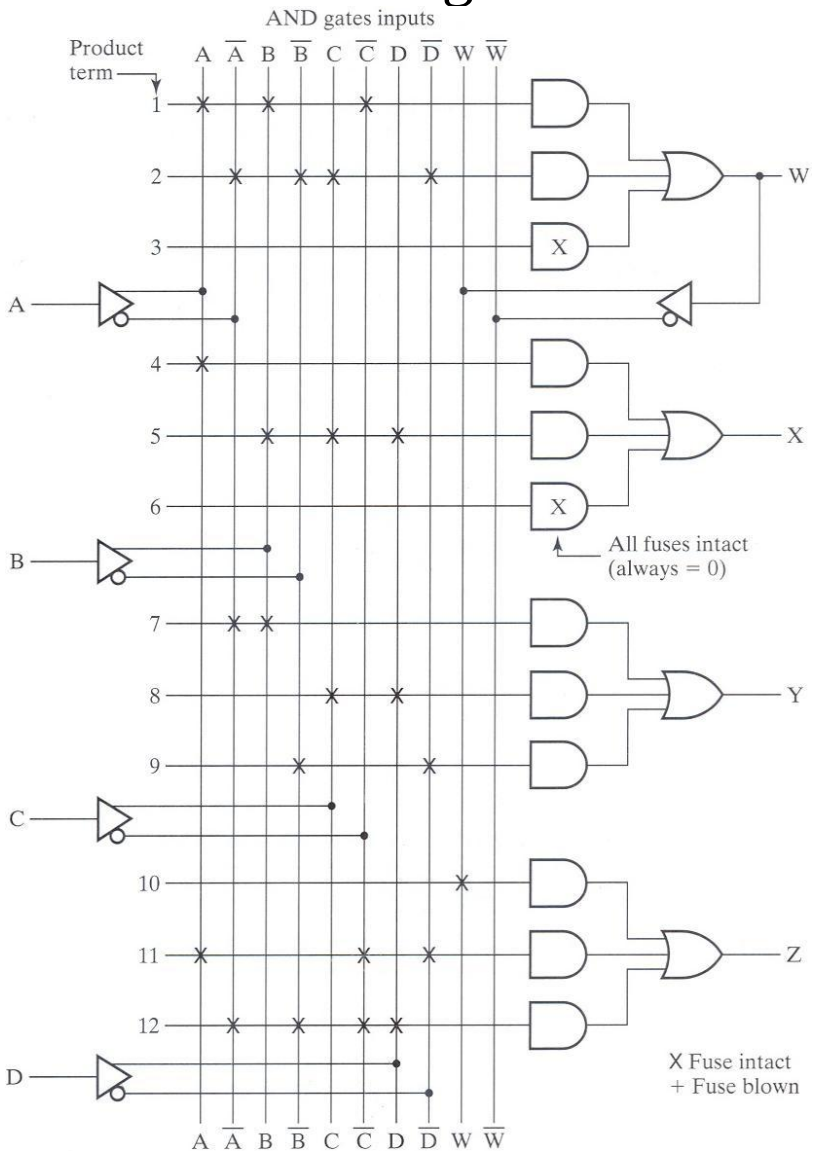
選擇 (A, B', C, D), (A', B, C, D), (A, B', C, D'), 或者 (A', B, C, D') 都只需要 4 product terms。
以選擇 (A, B', C, D) 爲例，需要 X'Y', XYZ, YZ', Z。

Ans:

Product Terms	Inputs X Y Z	Outputs A B'C D
1. X'Y'	0 0 –	1 1 – –
2. XYZ	1 1 1	1 1 – –
3. YZ'	– 1 0	1 – 1 –
4. Z	– – 1	– – – 1

10. The following is the truth table of a three-input, four-output combinational circuit. Obtain the PAL programming table for the circuit, and mark the fuses to be blown in a PAL diagram similar to the one shown in figure.

Inputs			Outputs			
X	Y	Z	A	B	C	D
0	0	0	0	1	0	0
0	0	1	1	1	1	1
0	1	0	1	0	1	1
0	1	1	0	1	0	1
1	0	0	1	0	1	0
1	0	1	0	0	0	1
1	1	0	1	1	1	0
1	1	1	0	1	1	1



A = XZ’ + X’Y’Z + YZ’

B = XY + X’Y’ + YZ

C = XY + XZ’ + X’Y’Z + YZ’

= XY + A

D = X’Y + Z

Ans:

Product Terms	Inputs X	Y	Z	A
1. XZ’	1	–	0	–
2. X’Y’Z	0	0	1	–
3. YZ’	–	1	0	–
4. XY	1	1	–	–
5. X’Y’	0	0	–	–
6. YZ	–	1	1	–
7. XY	1	1	–	–
8. A	–	–	–	1
9.	–	–	–	–
10. X’Y	0	1	–	–
11. Z	–	–	1	–
12.	–	–	–	–