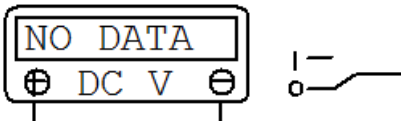
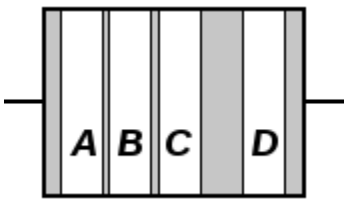
Digital Systems Lab Final Exam
Spring 2014 (6/11/2014)

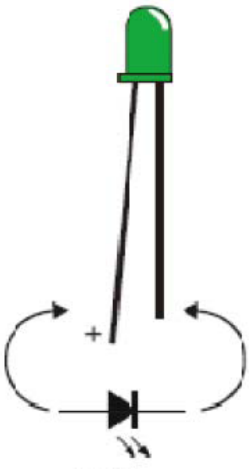
1. **[Terminology]** (10%)
   (a) HDL (b) LCD (c) DSP (d) TTL (e) LED
2. **[Tech Trend]** Name the world's second largest ICT trade show held from 6/3/-6/7/2014 in Taipei. (5%)
3. **[Lab Affairs]**
   (a) What is the password for accessing the course website? (5%)
   (b) Name the partners in your group. (5%)
   (c) How many times did we conduct the experiments this semester? Which of the following are <u>not</u> included in our experiments? `1-of-8 decoder, octal-to-binary encoder, 8 line to 3 line priority encoder, 4 bit comparator, 3 bit * 2 bit multiplier, 1-bit full adder, 4 bit even parity generator.` (8%)
   (d) Name the bonus experiment. (2%)
4. **[Software]** (a) What is the software used for circuit simulation in our class? (2%) (b) What symbol is used to indicate digital simulation mode? What is used to indicate analog mode? (4%) (c) Identify the following components: (4%)

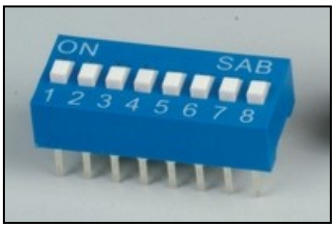


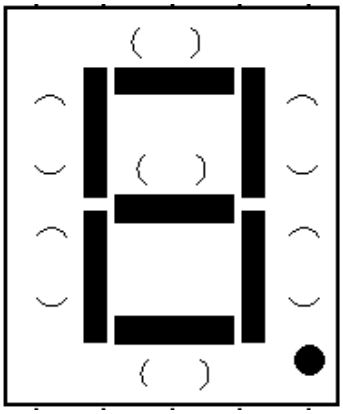
5. **[Resistor]** (a) What do bands A-D represent? (b) Name the color bands of a 210 Ω resistor with 10% tolerance. (c) Why do we usually connect a small resistor when using a diode? (10%)



6. **[Basic Components]** Name the components shown below and fill in the blanks. (10%)







7. **[Trouble shooting]** (a) A technician wires the output from a BCD counter to the inputs of the decoder shown below. He applies pulses to the counter at a very slow rate and observed the LED display, which is shown below, as the counter counts up from 0000 to 1001. Examine the observed sequence carefully and try to predict the most probable fault. *(Hint: Look at the common properties of the incorrect patterns (2,4,5,9). Then look at the common properties of the correct patterns. Which segments are not used in these correct patterns?)* (5%)

COUNT	0	1	2	3	4	5	6	7	8	9
Observed display	0	1	2	3	4	5	6	7	8	9
Expected display	0	1	2	3	4	5	6	7	8	9

(b) Repeat (a) when the observed sequence is as follows: (5%)

COUNT	0	1	2	3	4	5	6	7	8	9
Observed display	0	7	2	3	4	5	6	7	8	9

8. **[Subtractor]** Design a full subtractor. (Input: A, B, BOR_{in}, Output: D, BOR_{out} . Please write down the complete process.) (10%)

9. **[Basic Gates]** Match the Pairs by connecting lines (5%)

7404	AND
7486	OR
7400	NOT
7408	NAND
7432	XOR

10. **[Encoder]** (a) Construct the truth table for an 8x3 encoder. (b) Derive the logic expression of Q_2,Q_1 and Q_0. (10%)

$A_0A_1A_2A_3A_4A_5A_6A_7$	$Q_2Q_1Q_0$
1 0 0 0 0 0 0 0	
0 1 0 0 0 0 0 0	
0 0 1 0 0 0 0 0	
0 0 0 1 0 0 0 0	
0 0 0 0 1 0 0 0	
0 0 0 0 0 1 0 0	
0 0 0 0 0 0 1 0	
0 0 0 0 0 0 0 1	