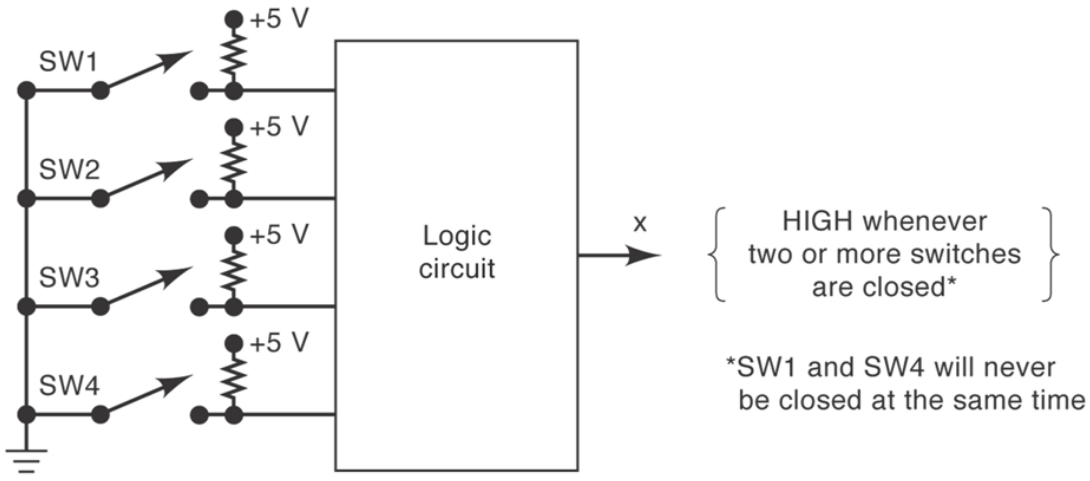
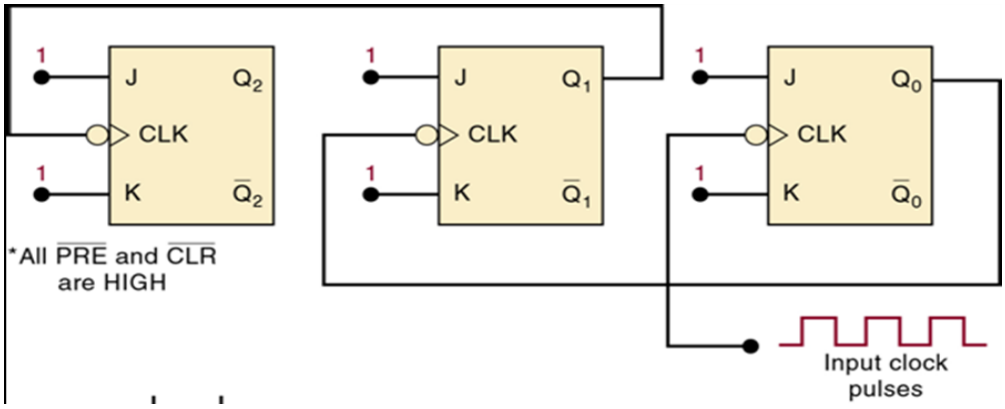
Department of Computer Science, National Chengchi University

Digital Systems Midterm Examination, 4/18/2012

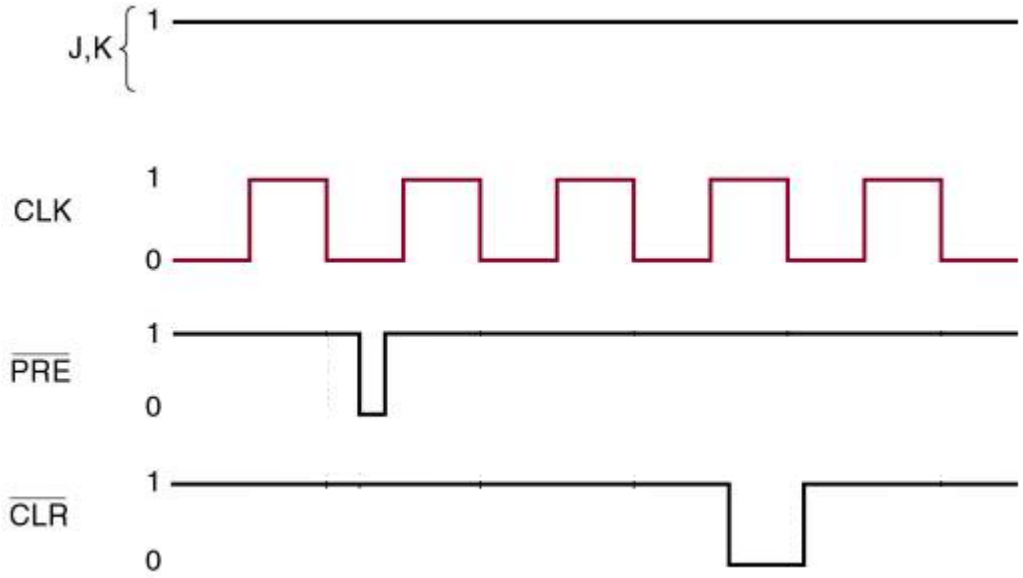
1. **[General Knowledge]** (a) Name two of the major computer expos in the world (4%) (b) What does the '3C' in 3C products stand for? (3%) (c) What is the name of the circuit simulator used in this course? (3%)
2. **[Universality of NOR/NAND gates]** Why are NOR/NAND gates universal? Explain with Boolean expressions and the corresponding circuit diagrams. (10%)
3. **[Gray code]** (a) What is the key property of Gray codes? (2%) (b) Convert 011101 (gray) to its binary code equivalent. (3%)
4. **[Boolean Theorem]** (a) Prove x+x'y=x+y without using truth table. (5%)
5. **[Sum-of-Products Form]** The SOP form of a two-variable logic function can be expressed as : $f(x,y) = \alpha_0 \bar{x}\bar{y} + \alpha_1 \bar{x}y + \alpha_2 x\bar{y} + \alpha_3 xy$
   (a) How many different functions can be generated for the two-variable case? (3%)
   (b) How about the N-variable case? (2%)
6. **[Combinational Circuit Design]** The following figure shows four switches that are part of the control circuitry in a copy machine. The switches are at various points along the path of the copy paper and as the paper passes over a switch, the switch closes. It is impossible for switches SW1 and SW4 to be closed at the same time. (a) Design the logic circuit to produce a HIGH for whenever two or more switches are closed at the same time. (Use K map and take advantage of the don't care condition.) (8%) (b) Draw the circuit diagram using conventional gate symbols. (2%)



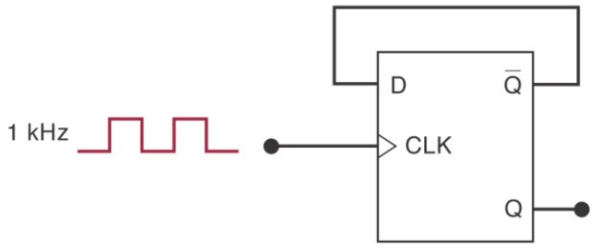
7. **[J-K Flip Flop]** (a) Draw the internal circuit of a negative-going-edge-triggered J-K flip-flop and identify the three basic components. (4%)
   (b) Describe how to detect the positive and negative going edge of a pulse. (3%)
   (c) Explain how the FF works when J=K=1. (assuming Q_{before}=1) (3%)
8. **[MOD 8 Down Counter]** (a) Modify the following circuit to construct a MOD-8 down counter. (4%) (b) Illustrate its function by starting all FFs in the 1 state and draw the various output FF waveforms. (6%)



9. **[Timing Diagram]** For a NGT J-K FF shown below, draw the output Q if Q is initially set to 1. (5%)



10. **[D Flip-Flop]** An edge-triggered D flip-flop can be made to operate in the toggle mode by connecting it as show in the following figure. Assume that Q=0 initially, determine the Q waveform. (5%)



11. [**Sign Integers**] (a) What is meant by the operation: 'sign extension'? Illustrate with examples. (b) Show that sign extension will not change the value of the number. (c) What is sign-magnitude representation? Explain and illustrate with an example. (d) Name two potential problems with the 'sign-magnitude' representation for signed integers. (10%)

12. [**Half Adder/Full Adder**] (a) Design the logic circuit for half adder. (2%)(b) Use two half adders and an 'or' gate to construct a full adder. (3%)

13. **[BCD Adder]** Build a single-digit BCD adder using two four-bit adders (74HC283) and a correction-detector circuit. Show all necessary steps. (10%)