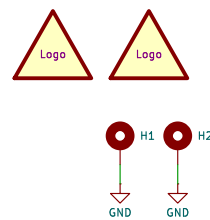


The schematic diagram illustrates the power supply circuit for the STM32F103C8T6 microcontroller. It includes a 5V regulator (U5, 1117-3.3) and a 3V3 regulator (U6, 1117-3.3). The circuit features a series of decoupling capacitors (C7, C8, C9, C10, C11-C20, C21-C26) and two LEDs (LED1, LED2) connected to the 3V3 supply. The ground is connected to GND and GND A.

Pinout diagram of the EPM3128ATC100 (U3) showing connections to various components:

- Power Supply:**
 - +3V3 (Pin 3)
 - GND (Pin 11, 26, 33, 43, 53, 59, 65, 74, 78, 95, 98, 38, 86)
- Control Signals:**
 - TDI (Pin 4)
 - YM_A0 (Pin 9)
 - YM_A1 (Pin 10)
 - YM_CS (Pin 12)
 - YM_SMP2 (Pin 13)
 - YM_SMP1 (Pin 14)
 - TMS (Pin 16)
 - YM_DATA (Pin 17)
 - YM_DCLK (Pin 18)
 - CLK14 (Pin 19)
 - A0 (Pin 20)
 - A1 (Pin 21)
 - A2 (Pin 23)
 - A3 (Pin 25)
 - TORQGE (Pin 29)
 - A7 (Pin 30)
 - A6 (Pin 31)
 - A5 (Pin 32)
 - A4 (Pin 35)
 - A9 (Pin 36)
 - RS1 (Pin 40)
 - IORQ (Pin 41)
 - M1 (Pin 44)
 - A8 (Pin 45)
- General Purpose I/O:**
 - I/O Pins: 1, 2, 5, 6, 7, 8, 11, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49
- Power and Ground:**
 - VCCIO (Pins 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49)
 - VCCINT (Pin 39)
 - GNDINT (Pin 38)
- Other Connections:**
 - TCK (Pin 62)
 - LED2 (Pin 69)
 - LED1 (Pin 72)
 - TDO (Pin 73)
 - DAC_STD (Pin 87)
 - CLK2B8 (Pin 89)
 - CFG4 (Pin 93)
 - CFG3 (Pin 94)
 - CFG0 (Pin 96)
 - CFG1 (Pin 97)
 - CFG2 (Pin 98)
 - DAC_DAT (Pin 99)
 - DAC_LRCK (Pin 99)
 - DAC_BCK (Pin 100)

The diagram illustrates a 5-bit digital-to-analog converter (DAC) circuit. It is powered by a +5V supply and connected to ground (GND). The circuit consists of a resistor ladder with resistors R15, R16, R17, R18, and R19, each labeled with a value of 10k. A switch, labeled SW1 and SW_DIP_x05, is connected to the output of the ladder. The output is connected to a 5-bit digital input (CFG0 to CFG4) which is also connected to a 5-bit digital output (1 to 5).



The schematic diagram shows the P1307 component with two sets of connections:

- J3 Connections:**
 - S:** Connected to GND_A.
 - R:** Connected to SND_R.
 - RN:** Connected to SND_R.
 - T:** Connected to SND_L.
 - TN:** Connected to SND_L.
- J4 Connections:**
 - 1:** Connected to SND_R.
 - 2:** Connected to GND_A.
 - 3:** Connected to GND_A.
 - 4:** Connected to SND_L.

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