

The schematic diagram illustrates the test circuit for the 5V_PRG pin. It features two op-amp buffers, U5 and U6, which provide clean +5V and +3V3 signals. A series of 100nF capacitors (C11-C20) are used for decoupling. A 100uF/16V electrolytic capacitor (C21) is connected to the +5V line. Another set of 100nF capacitors (C22-C25) and a 100uF/16V electrolytic capacitor (C26) are connected to the +3V3 line. A 1k resistor (R20) is connected to the +3V3 line. The 5V_PRG pin (J5) is connected to the +5V line. The circuit is powered by a +5V and a +3V3 source.

Pinout diagram of the EPM3128ATC100 (U3) showing connections to various components. The diagram includes a central chip with pins 1-49 on the left and 50-100 on the right. Pin 3 is connected to +3V3. Pins 18, 34, 51, 66, 82, 39, and 91 are connected to VCCIO or VCCINT. Pins 11, 26, 33, 43, 53, 59, 65, 74, 78, 95, 38, and 86 are connected to GND. Various pins are connected to components like TDI, TMS, LED2, LED1, TDO, DAC_STD, CLK2B, CFG4, CFG3, CFG0, CFG1, CFG2, DAC_DAT, DAC_LRCK, and DAC_BCK. The diagram also shows connections to U1 (74VHC04), U2 (74VHC04), and U4 (74VHC04).

Rev: B