CA Final Project Report

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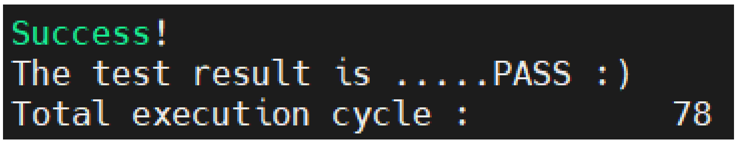
一、Cycle數
default

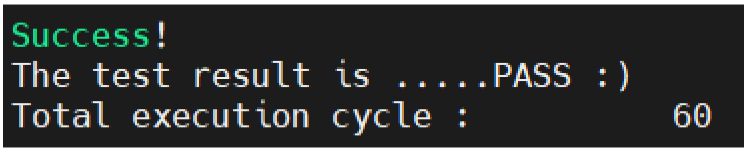
Without Cache	With Cache	Speed up
78	60	1.3
453	324	1.4
307	289	1.06
1359	427	3.18

I0 with default test pattern
without cache



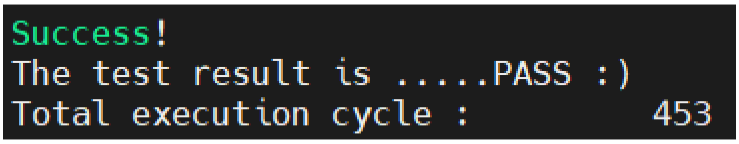
```
Success!
The test result is .....PASS :)
Total execution cycle :          78
```

with cache



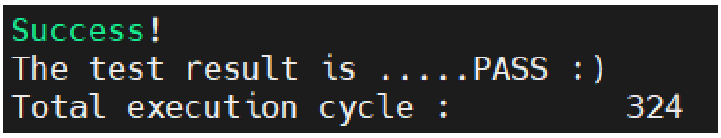
```
Success!
The test result is .....PASS :)
Total execution cycle :          60
```

I1 with default test pattern
without cache



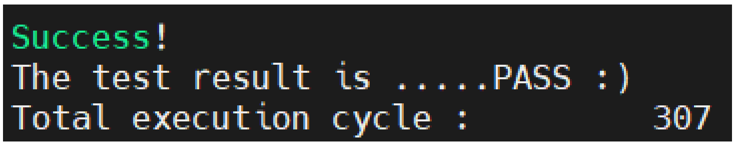
```
Success!
The test result is .....PASS :)
Total execution cycle :         453
```

with cache



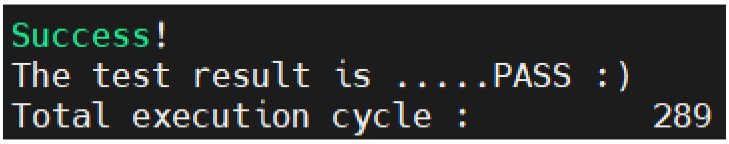
```
Success!
The test result is .....PASS :)
Total execution cycle :         324
```

I2 with default test pattern
without cache



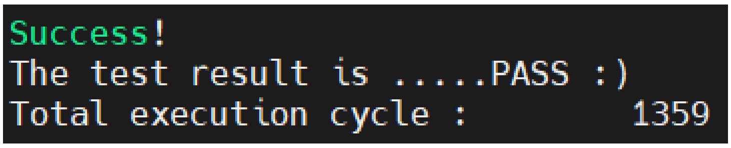
```
Success!
The test result is .....PASS :)
Total execution cycle :         307
```

with cache



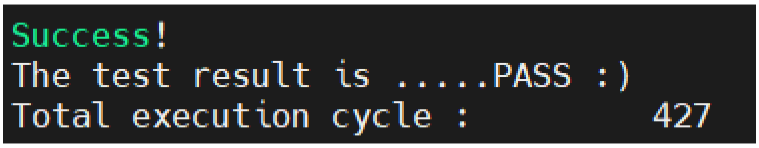
```
Success!
The test result is .....PASS :)
Total execution cycle :          289
```

I3 with default test pattern
without cache



```
Success!
The test result is .....PASS :)
Total execution cycle :         1359
```

with cache



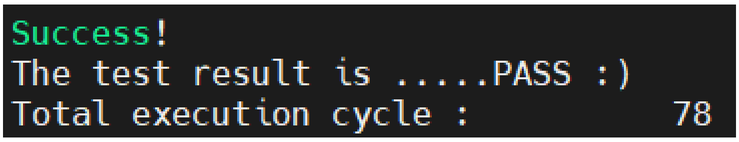
```
Success!
The test result is .....PASS :)
Total execution cycle :          427
```

testcase調整

Pattern	testcase	cycle(without cache)	with cache
I0	a=9,b=6,c=5,d=7	78	60
I1	n=8	693	498
I2	n=70	421	388

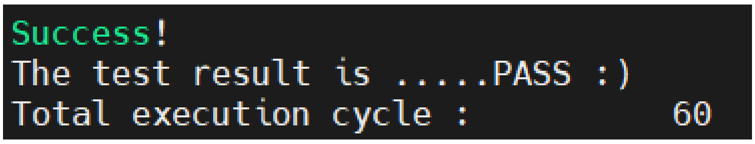
I3	n = 8
	v = [6, 4, 7, 9, 3, 2, 0, 1]
		1923	584

I0 with changed test pattern
without cache



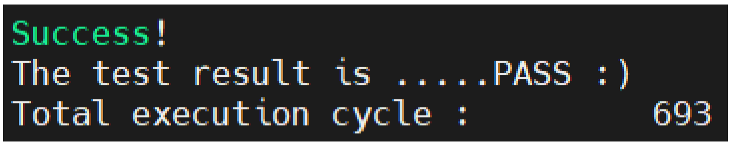
```
Success!
The test result is .....PASS :)
Total execution cycle :           78
```

with cache



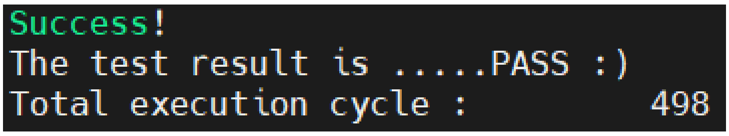
```
Success!
The test result is .....PASS :)
Total execution cycle :           60
```

I1 with changed test pattern
without cache



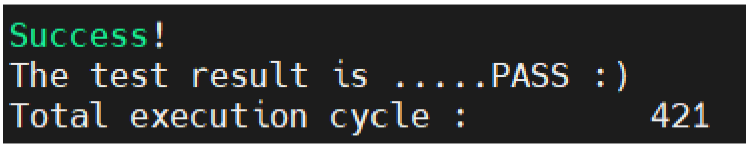
```
Success!
The test result is .....PASS :)
Total execution cycle :         693
```

with cache



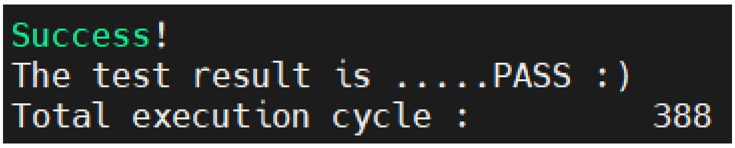
```
Success!
The test result is .....PASS :)
Total execution cycle :         498
```

I2 with changed test pattern
without cache



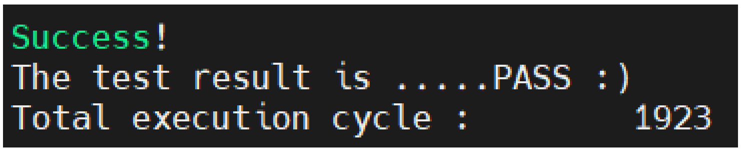
```
Success!
The test result is .....PASS :)
Total execution cycle :         421
```

with cache



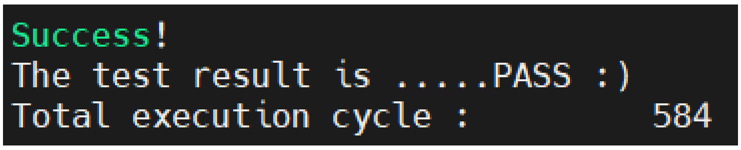
```
Success!
The test result is .....PASS :)
Total execution cycle :         388
```

I3 with changed test pattern
without cache



```
Success!
The test result is .....PASS :)
Total execution cycle :        1923
```

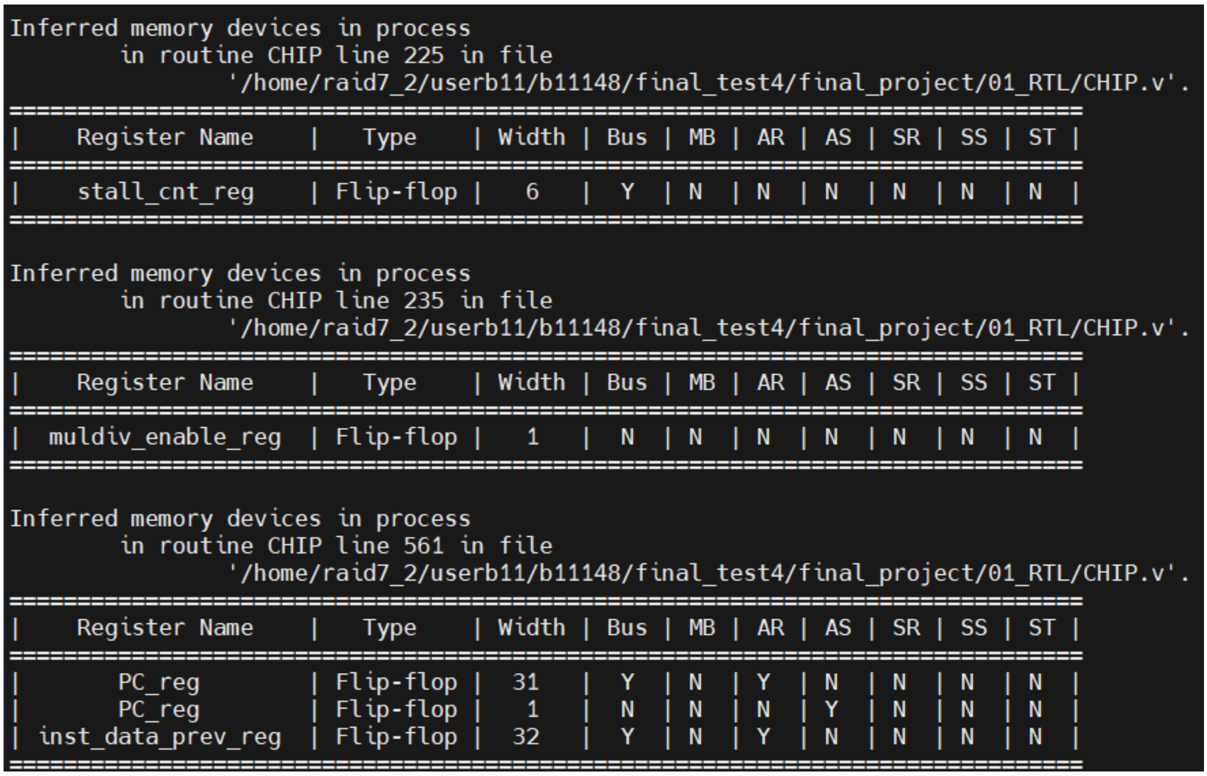
with cache



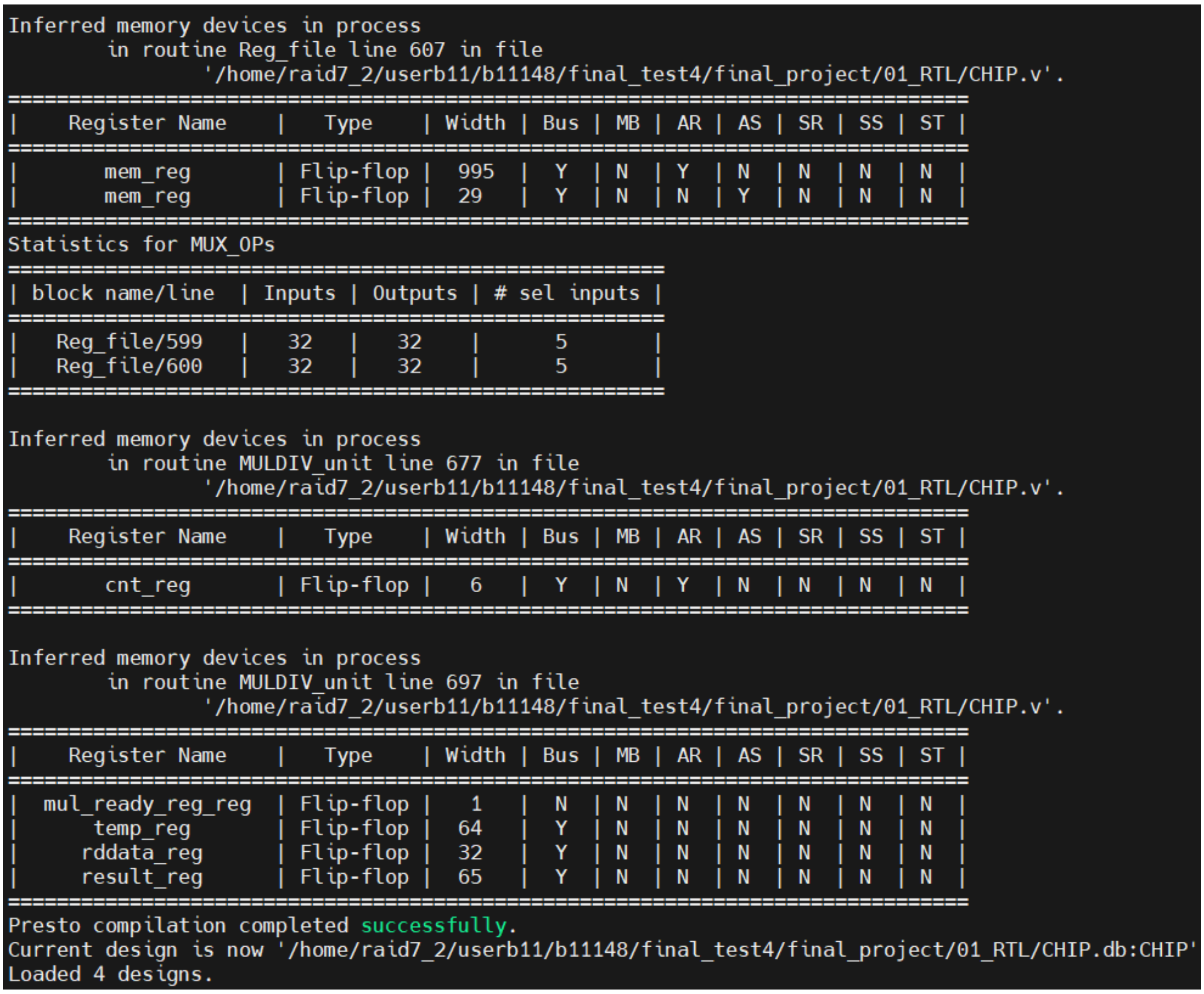
```
Success!
The test result is .....PASS :)
Total execution cycle :         584
```

二、Register Table

without cache

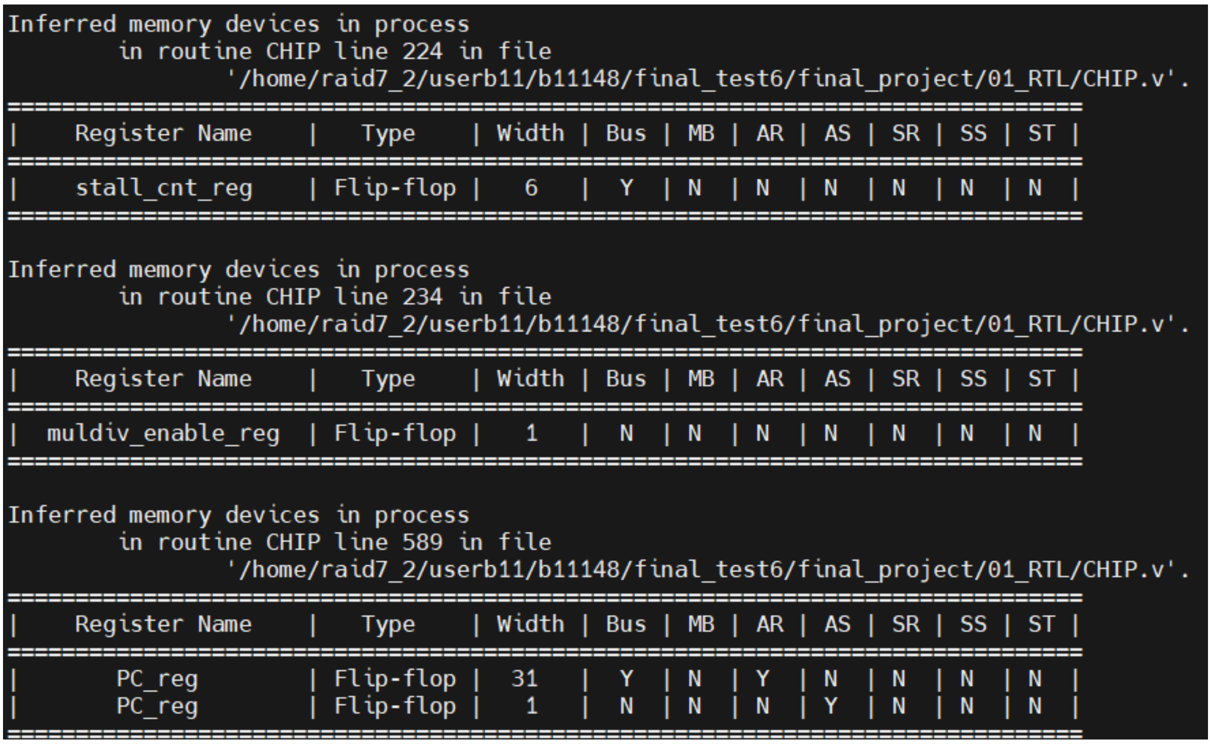


```
Inferred memory devices in process
        in routine CHIP line 225 in file
                '/home/raid7_2/userb11/b11148/final_test4/final_project/01_RTL/CHIP.v'.
===============================================================================
|    Register Name    |   Type    | Width | Bus | MB | AR | AS | SR | SS | ST |
===============================================================================
|    stall_cnt_reg    | Flip-flop |   6   |  Y  | N  | N  | N  | N  | N  | N  |
===============================================================================

Inferred memory devices in process
        in routine CHIP line 235 in file
                '/home/raid7_2/userb11/b11148/final_test4/final_project/01_RTL/CHIP.v'.
===============================================================================
|    Register Name    |   Type    | Width | Bus | MB | AR | AS | SR | SS | ST |
===============================================================================
|  muldiv_enable_reg  | Flip-flop |   1   |  N  | N  | N  | N  | N  | N  | N  |
===============================================================================

Inferred memory devices in process
        in routine CHIP line 561 in file
                '/home/raid7_2/userb11/b11148/final_test4/final_project/01_RTL/CHIP.v'.
===============================================================================
|    Register Name    |   Type    | Width | Bus | MB | AR | AS | SR | SS | ST |
===============================================================================
|       PC_reg        | Flip-flop |  31   |  Y  | N  | Y  | N  | N  | N  | N  |
|       PC_reg        | Flip-flop |   1   |  N  | N  | N  | Y  | N  | N  | N  |
| inst_data_prev_reg  | Flip-flop |  32   |  Y  | N  | Y  | N  | N  | N  | N  |
===============================================================================
```

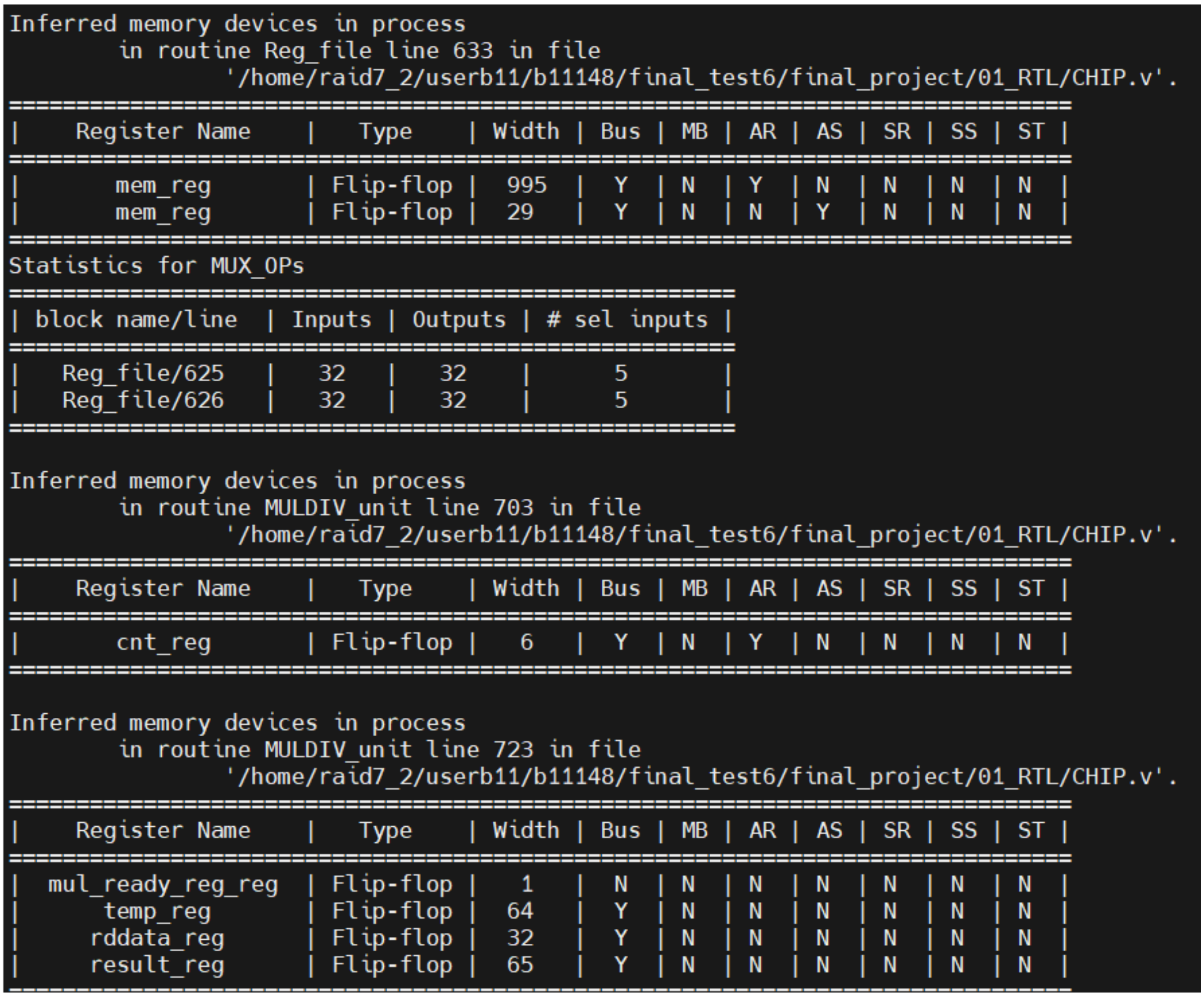


```
Inferred memory devices in process
        in routine Reg_file line 607 in file
                '/home/raid7_2/userb11/b11148/final_test4/final_project/01_RTL/CHIP.v'.
===============================================================================
|    Register Name    |   Type    | Width | Bus | MB | AR | AS | SR | SS | ST |
===============================================================================
|       mem_reg       | Flip-flop |  995  |  Y  | N  | Y  | N  | N  | N  | N  |
|       mem_reg       | Flip-flop |  29   |  Y  | N  | N  | Y  | N  | N  | N  |
===============================================================================
Statistics for MUX_OPs
======================================================
| block name/line  | Inputs | Outputs | # sel inputs |
======================================================
|   Reg_file/599   |   32   |   32    |      5       |
|   Reg_file/600   |   32   |   32    |      5       |
======================================================

Inferred memory devices in process
        in routine MULDIV_unit line 677 in file
                '/home/raid7_2/userb11/b11148/final_test4/final_project/01_RTL/CHIP.v'.
===============================================================================
|    Register Name    |   Type    | Width | Bus | MB | AR | AS | SR | SS | ST |
===============================================================================
|       cnt_reg       | Flip-flop |   6   |  Y  | N  | Y  | N  | N  | N  | N  |
===============================================================================

Inferred memory devices in process
        in routine MULDIV_unit line 697 in file
                '/home/raid7_2/userb11/b11148/final_test4/final_project/01_RTL/CHIP.v'.
===============================================================================
|    Register Name    |   Type    | Width | Bus | MB | AR | AS | SR | SS | ST |
===============================================================================
|  mul_ready_reg_reg  | Flip-flop |   1   |  N  | N  | N  | N  | N  | N  | N  |
|      temp_reg       | Flip-flop |  64   |  Y  | N  | N  | N  | N  | N  | N  |
|     rddata_reg      | Flip-flop |  32   |  Y  | N  | N  | N  | N  | N  | N  |
|     result_reg      | Flip-flop |  65   |  Y  | N  | N  | N  | N  | N  | N  |
===============================================================================
Presto compilation completed successfully.
Current design is now '/home/raid7_2/userb11/b11148/final_test4/final_project/01_RTL/CHIP.db:CHIP'
Loaded 4 designs.
```

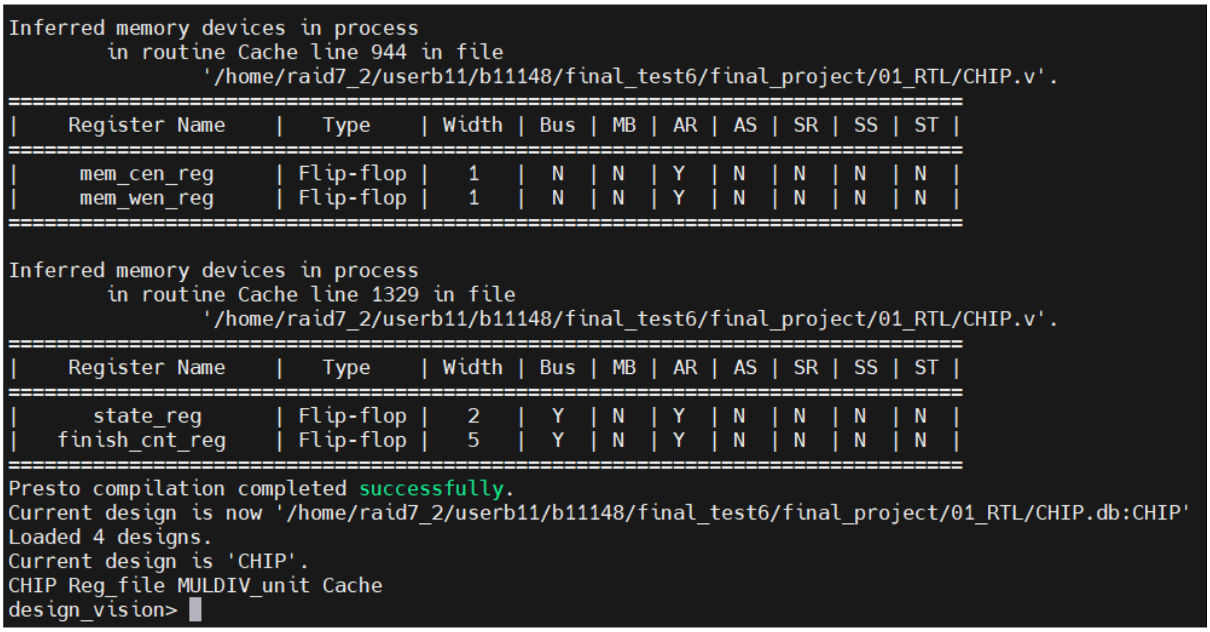
with cache



```
Inferred memory devices in process
        in routine CHIP line 224 in file
                '/home/raid7_2/userb11/b11148/final_test6/final_project/01_RTL/CHIP.v'.
===============================================================================
|    Register Name    |   Type    | Width | Bus | MB | AR | AS | SR | SS | ST |
===============================================================================
|    stall_cnt_reg    | Flip-flop |   6   |  Y  | N  | N  | N  | N  | N  | N  |
===============================================================================

Inferred memory devices in process
        in routine CHIP line 234 in file
                '/home/raid7_2/userb11/b11148/final_test6/final_project/01_RTL/CHIP.v'.
===============================================================================
|    Register Name    |   Type    | Width | Bus | MB | AR | AS | SR | SS | ST |
===============================================================================
|  muldiv_enable_reg  | Flip-flop |   1   |  N  | N  | N  | N  | N  | N  | N  |
===============================================================================

Inferred memory devices in process
        in routine CHIP line 589 in file
                '/home/raid7_2/userb11/b11148/final_test6/final_project/01_RTL/CHIP.v'.
===============================================================================
|    Register Name    |   Type    | Width | Bus | MB | AR | AS | SR | SS | ST |
===============================================================================
|       PC_reg        | Flip-flop |  31   |  Y  | N  | Y  | N  | N  | N  | N  |
|       PC_reg        | Flip-flop |   1   |  N  | N  | N  | Y  | N  | N  | N  |
===============================================================================
```



```
Inferred memory devices in process
        in routine Reg_file line 633 in file
                '/home/raid7_2/userb11/b11148/final_test6/final_project/01_RTL/CHIP.v'.
===============================================================================
|    Register Name    |   Type    | Width | Bus | MB | AR | AS | SR | SS | ST |
===============================================================================
|       mem_reg       | Flip-flop |  995  |  Y  | N  | Y  | N  | N  | N  | N  |
|       mem_reg       | Flip-flop |  29   |  Y  | N  | N  | Y  | N  | N  | N  |
===============================================================================
Statistics for MUX_OPs
======================================================
| block name/line  | Inputs | Outputs | # sel inputs |
======================================================
|   Reg_file/625   |   32   |   32    |      5       |
|   Reg_file/626   |   32   |   32    |      5       |
======================================================

Inferred memory devices in process
        in routine MULDIV_unit line 703 in file
                '/home/raid7_2/userb11/b11148/final_test6/final_project/01_RTL/CHIP.v'.
===============================================================================
|    Register Name    |   Type    | Width | Bus | MB | AR | AS | SR | SS | ST |
===============================================================================
|       cnt_reg       | Flip-flop |   6   |  Y  | N  | Y  | N  | N  | N  | N  |
===============================================================================

Inferred memory devices in process
        in routine MULDIV_unit line 723 in file
                '/home/raid7_2/userb11/b11148/final_test6/final_project/01_RTL/CHIP.v'.
===============================================================================
|    Register Name    |   Type    | Width | Bus | MB | AR | AS | SR | SS | ST |
===============================================================================
|  mul_ready_reg_reg  | Flip-flop |   1   |  N  | N  | N  | N  | N  | N  | N  |
|      temp_reg       | Flip-flop |  64   |  Y  | N  | N  | N  | N  | N  | N  |
|     rddata_reg      | Flip-flop |  32   |  Y  | N  | N  | N  | N  | N  | N  |
|     result_reg      | Flip-flop |  65   |  Y  | N  | N  | N  | N  | N  | N  |
```

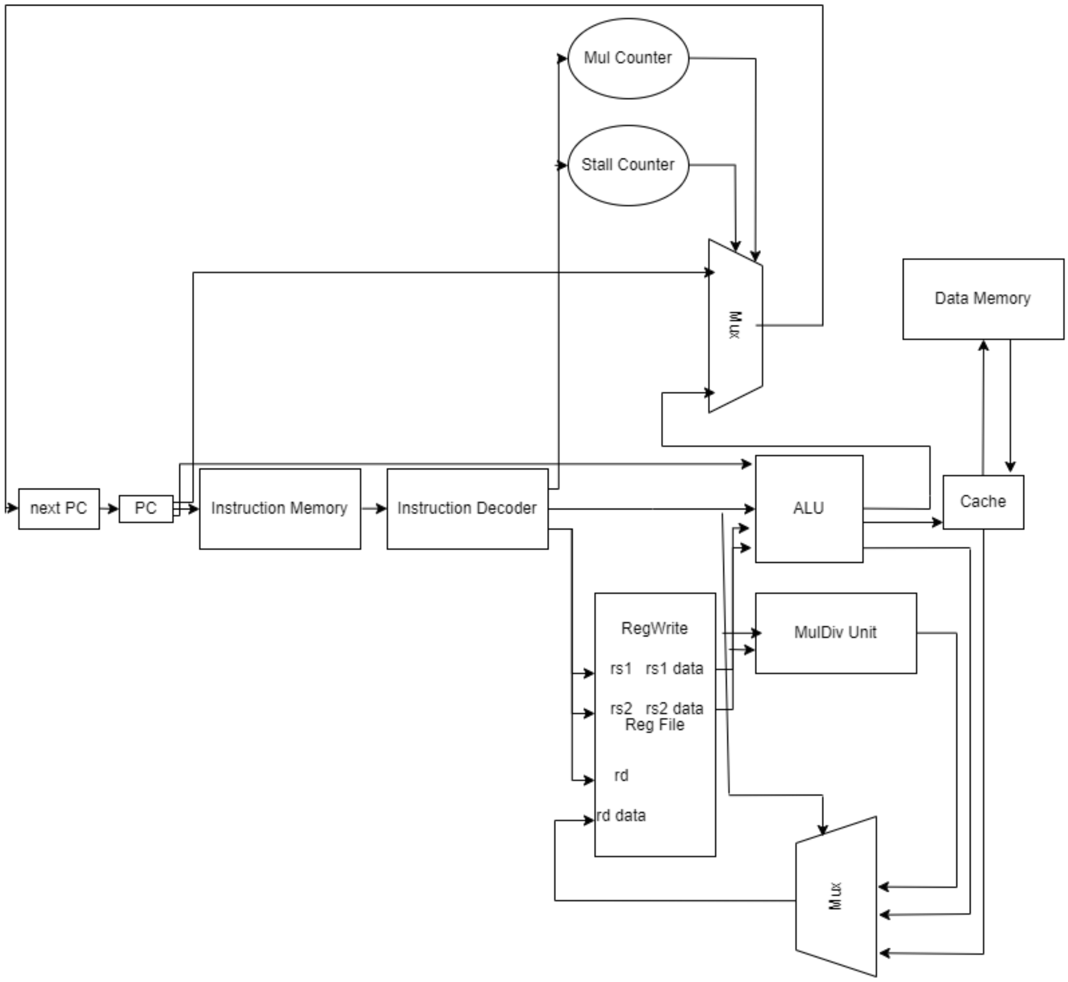


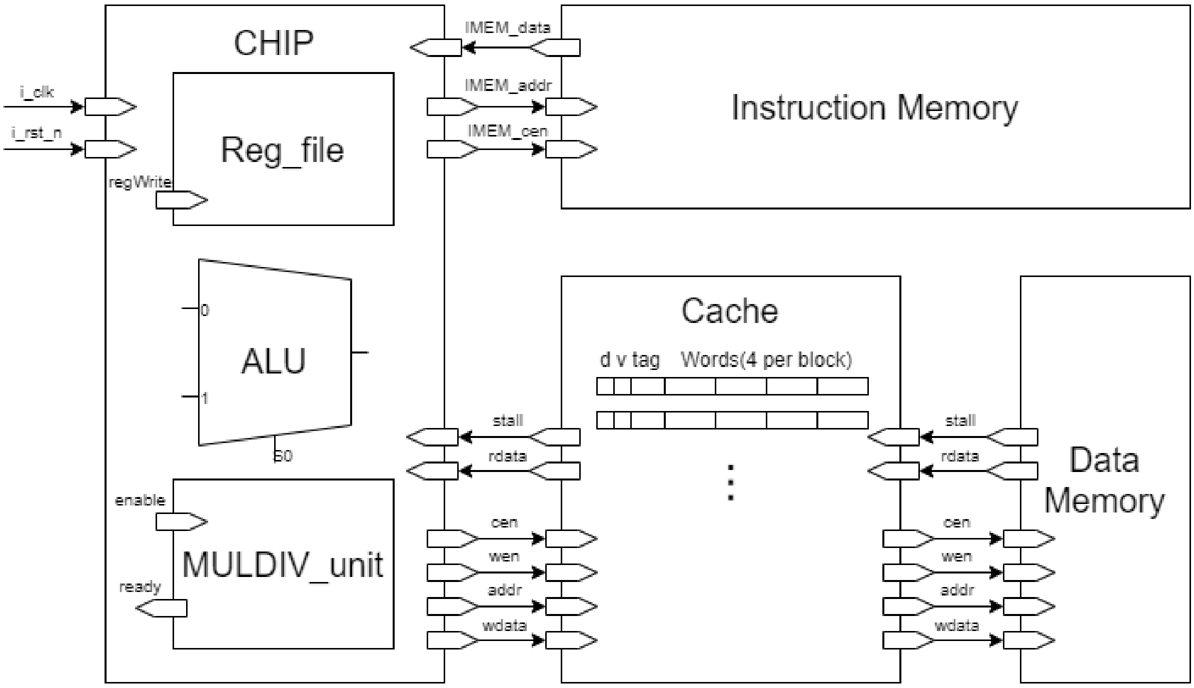
```
Inferred memory devices in process
        in routine Cache line 944 in file
                '/home/raid7_2/userb11/b11148/final_test6/final_project/01_RTL/CHIP.v'.
===============================================================================
|    Register Name    |   Type    | Width | Bus | MB | AR | AS | SR | SS | ST |
===============================================================================
|     mem_cen_reg     | Flip-flop |   1   |  N  | N  | Y  | N  | N  | N  | N  |
|     mem_wen_reg     | Flip-flop |   1   |  N  | N  | Y  | N  | N  | N  | N  |
===============================================================================

Inferred memory devices in process
        in routine Cache line 1329 in file
                '/home/raid7_2/userb11/b11148/final_test6/final_project/01_RTL/CHIP.v'.
===============================================================================
|    Register Name    |   Type    | Width | Bus | MB | AR | AS | SR | SS | ST |
===============================================================================
|      state_reg      | Flip-flop |   2   |  Y  | N  | Y  | N  | N  | N  | N  |
|   finish_cnt_reg    | Flip-flop |   5   |  Y  | N  | Y  | N  | N  | N  | N  |
===============================================================================
Presto compilation completed successfully.
Current design is now '/home/raid7_2/userb11/b11148/final_test6/final_project/01_RTL/CHIP.db:CHIP'
Loaded 4 designs.
Current design is 'CHIP'.
CHIP Reg_file MULDIV_unit Cache
design_vision>
```

三、問題回答

Work description

Q1：Draw the block diagram of your CPU architecture





Q2：Describe how you design the data path of instructions not referred in the lecture slides (jal, jalr, auipc, …)

A2：基本上就是參考Green Card上面定義的方式，個別寫法為：
各個immmediate都會初始化為0
JAL：下一個要輸入PC的值設定為signed(PC)加上其對應的signed(immediate)，並將要寫入reg file的rd data設定為PC+4
JALR：下一個要輸入PC的值設定為來自reg file的signed(rs1 data)加上其對應的signed(immediate)，並將要寫入reg file的rd data設定為PC+4
AUIPC：擷取來自instruction中Most Significant的12位並放到immediate中的Most Significant的12位，並將要寫入reg file的rd data設定為PC+immediate

Q3：Describe how you handle multi-cycle instructions (mul, div …)
A3：本次final project只有要處理mul的指令。mul指令的部分，在收到mul的指令後，設定一個允許muldiv_unit運作的訊號(muldiv_enable)為high，並把從reg file取得的資料丟進muldiv_unit進行32次移位與運算，並在運算完成後傳輸一個告知chip說他算完的訊號 (muldiv_ready)pull high。chip在收到這個訊號後會將允許寫入reg file的訊號pull high，並將運算結果存入reg file中。

Q4：Describe your observation
A4：1.有加cache可以使運行cycle數下降，尤其是在I3這種有大量存取指令表現差異尤為明顯。
2.要傳輸給memory.v的cen與wen訊號最多只能pull high一個cycle
3.一個reg只能在同一個always block裡面指定他的值，否則該reg會不知道要接收來自哪裡的值並在read verilog時出現error。
4.memory裡面有一大段是沒有被設計的，並且i_offset一定得使用，否則傳遞

address給memory時會出錯。

5. cache如果模仿memory.v裡對data在無使用時設定為z的話會出現tri-state buffer，因此不應這樣設定。(還是其實有其他理由我們也不確定)

6. memory裡面的delay是人為設定而非物理限制，因此理論上將cache設計為 fully associative與write back+write allocate可以發揮最大的cache優勢。

四、Cache design

Q1：Briefly describe your cache architecture

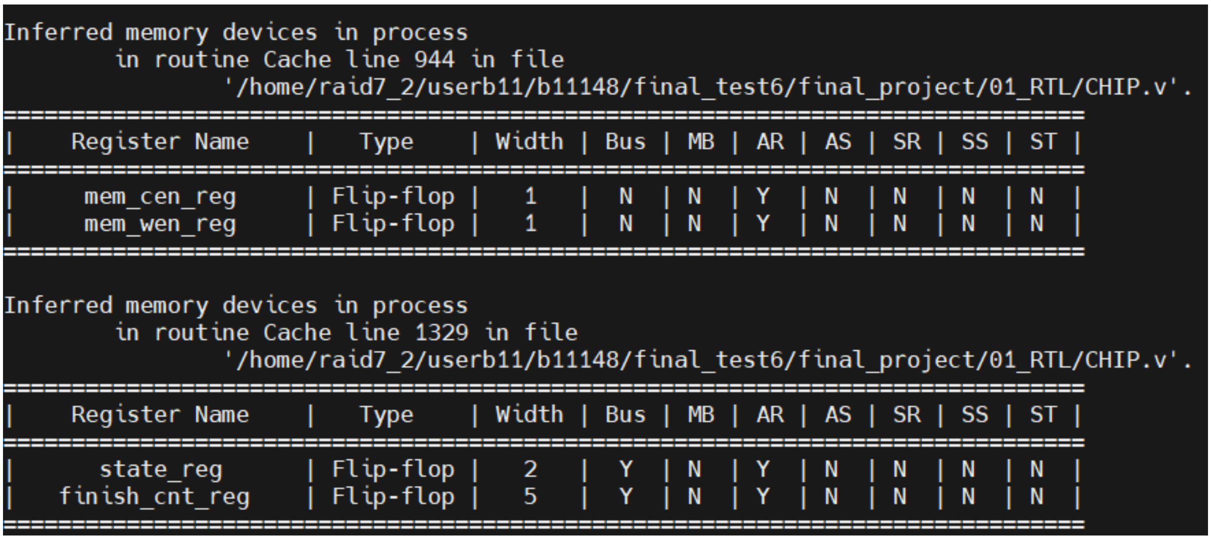
A1：我們選擇做write back, fully associative的cache，且因為cache連接到memory傳輸資料的線有128 bit (4 word)，因此我們選擇做4 words per block的cache。
在cache中有INITIAL, WRITE_BACK, ALLO, FINISH四個state，在idle或讀寫有hit的狀態都會在INITIAL state處理，並在1個cycle就完成讀寫及回傳資料給CHIP。若結果為miss，則會判斷cache是否滿了：如果還沒滿，就進入ALLO(allocate) state，將要讀/寫的資料先從data memory存到cache，如果是要寫則在cache修改，並將dirty bit標記為1；如果cache滿了，則要先進入WRITE_BACK state，將原本block中的資料(若為dirty)寫回memory，再進入ALLO state執行上述的動作。最後，為了確保data memory中資料是正確的，在instruction為ecall時cache會進入FINISH state，將所有dirty bit = 1的block寫回memory，再回傳finish的訊號給CHIP，並結束運作。

Q2：Describe how your cache improves time performance

A2：已在上方Cycle數的表格中列出。

Q3：Cache的大小

A3：由於我們cache不是由clock去trigger，因此不會在read_verilog時顯示。我們cache部分儲存資料大小為(32(bits per word)*4(words per block)+28(tag bits)+1(valid bit)+1(dirty bit))*18(# of blocks)=2844 bits，其他read_verilog有出現的部分如下：



```
Inferred memory devices in process
        in routine Cache line 944 in file
                '/home/raid7_2/userb11/b11148/final_test6/final_project/01_RTL/CHIP.v'.
===============================================================================
|    Register Name    |   Type    | Width | Bus | MB | AR | AS | SR | SS | ST |
===============================================================================
|     mem_cen_reg     | Flip-flop |   1   |  N  | N  | Y  | N  | N  | N  | N  |
|     mem_wen_reg     | Flip-flop |   1   |  N  | N  | Y  | N  | N  | N  | N  |
===============================================================================

Inferred memory devices in process
        in routine Cache line 1329 in file
                '/home/raid7_2/userb11/b11148/final_test6/final_project/01_RTL/CHIP.v'.
===============================================================================
|    Register Name    |   Type    | Width | Bus | MB | AR | AS | SR | SS | ST |
===============================================================================
|      state_reg      | Flip-flop |   2   |  Y  | N  | Y  | N  | N  | N  | N  |
|   finish_cnt_reg    | Flip-flop |   5   |  Y  | N  | Y  | N  | N  | N  | N  |
===============================================================================
```

五、List a work distribution table

連子力、李承彥：各50% (CHIP及cache皆為一起寫)