

# Team09 Lab1 Report

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## 1. File Structure

team09\_lab1

| - team09\_lab1\_report.pdf

| - src/

| - Top.sv

| - DE2\_115/

| - DE2\_115.qsf

| - DE2\_115.sdc

| - DE2\_115.sv

| - Debounce.sv

| - LFSR.sv

| - SevenHexDecoder.sv

## 2. System Architecture

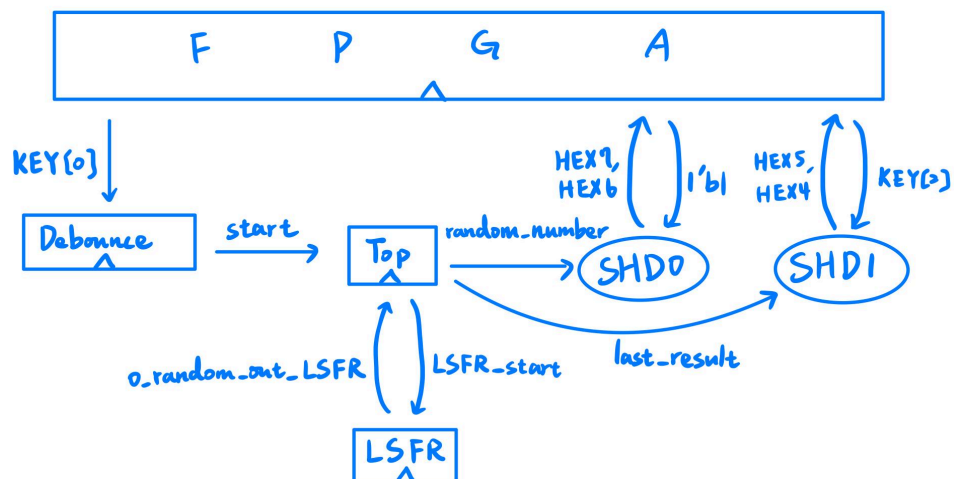
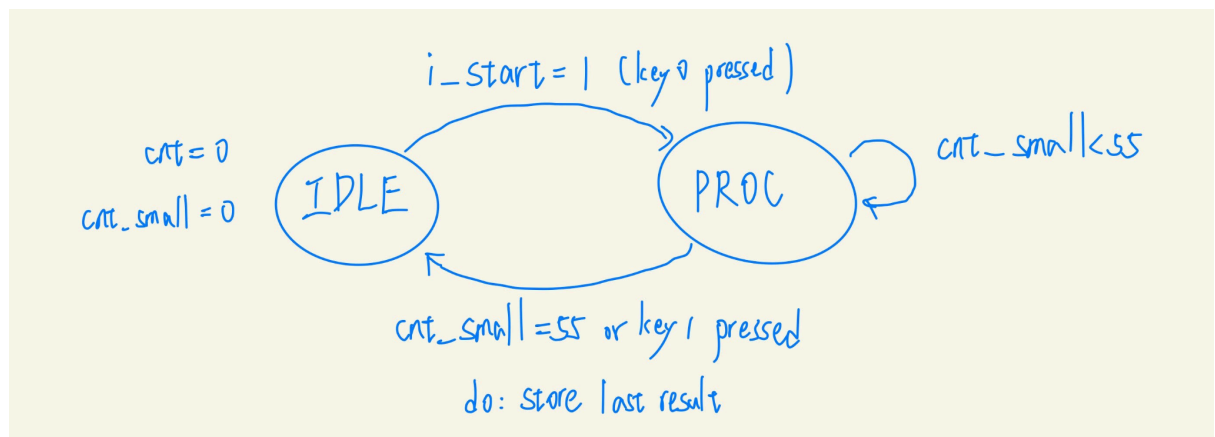


Figure 1: System Architecture (SHD: Seven Hex Decoder)

### 3. Hardware Scheduling

#### a. FSM



#### b. Algorithm

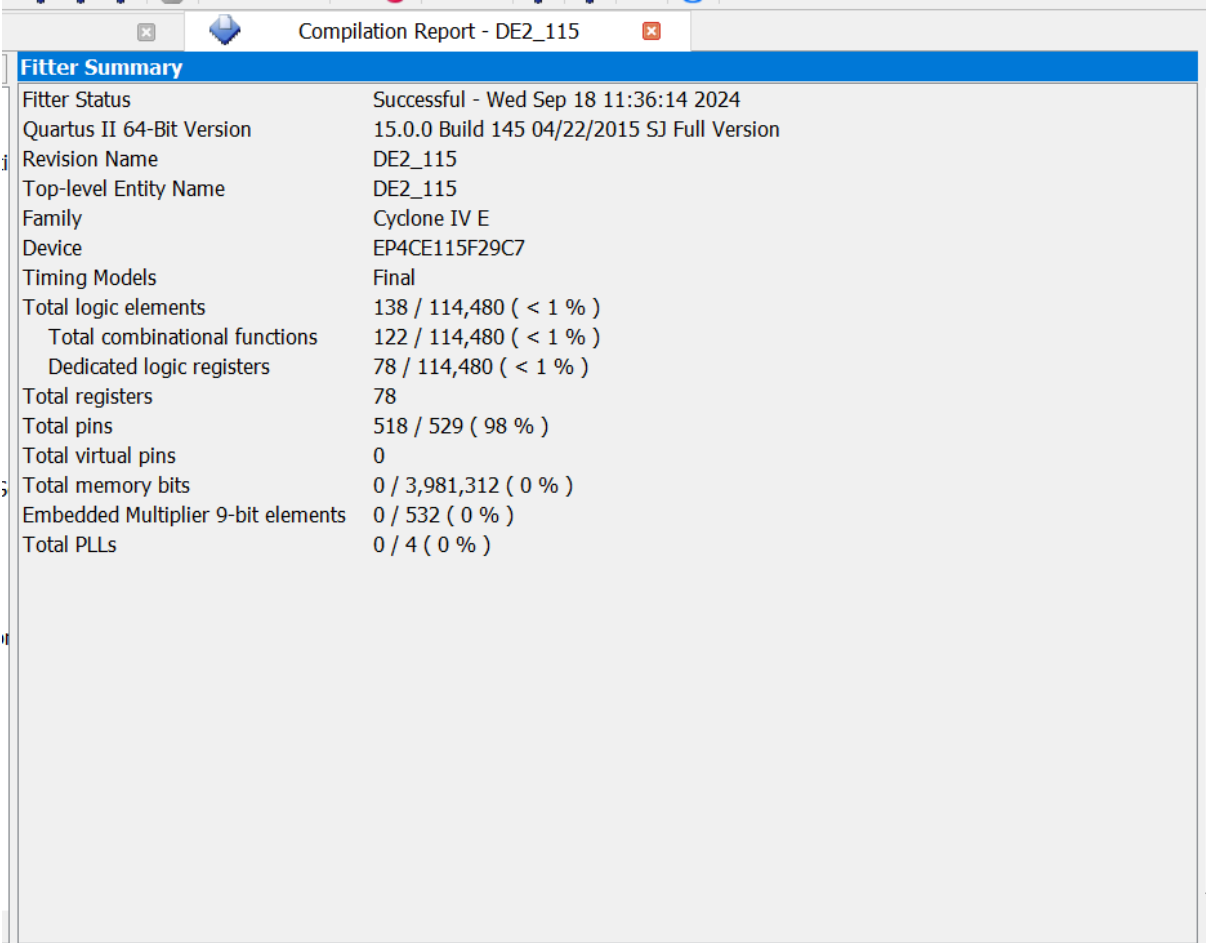
##### i. LFSR

We use two 16-bit vectors *random\_number* and *random\_seed* to generate random numbers. For each clock, *random\_seed* does LFSR one time, and if input *LFSR\_start* is 1, *random\_number* also does LFSR one time. (If *random\_number* is 16'b0, *random\_number*  $\leq$  *random\_seed*. If *random\_seed* is 16'b0, set *random\_seed* to be a non-zero value.) And the output is the first four bits of *random\_number*.

##### ii. Record last result

We update the last result upon entering the next number generating iteration. The history will show on the LED if the button is pressed.

#### 4. Fitter Summary 截圖



Fitter Summary	
Fitter Status	Successful - Wed Sep 18 11:36:14 2024
Quartus II 64-Bit Version	15.0.0 Build 145 04/22/2015 SJ Full Version
Revision Name	DE2_115
Top-level Entity Name	DE2_115
Family	Cyclone IV E
Device	EP4CE115F29C7
Timing Models	Final
Total logic elements	138 / 114,480 ( < 1 % )
Total combinational functions	122 / 114,480 ( < 1 % )
Dedicated logic registers	78 / 114,480 ( < 1 % )
Total registers	78
Total pins	518 / 529 ( 98 % )
Total virtual pins	0
Total memory bits	0 / 3,981,312 ( 0 % )
Embedded Multiplier 9-bit elements	0 / 532 ( 0 % )
Total PLLs	0 / 4 ( 0 % )

#### 5. Timing Analyzer 截圖

	Property	Setup	Hold
1	Illegal Clocks	0	0
2	Unconstrained Clocks	0	0
3	Unconstrained Input Ports	3	3
4	Unconstrained Input Port Paths	94	94
5	Unconstrained Output Ports	24	24
6	Unconstrained Output Port Paths	93	93

## 6. 遇到的問題與解決辦法

- a. 如果 LFSR 出現零的話會無法生成其他數字  
多設一個variable random\_seed, random\_seed也會做LFSR, 他等於0的時候會被賦予一個特定數值, 而random\_number == 0 的時候會跟 random\_seed取值, 增加隨機性。
- b. 生成的序列感覺不夠隨機  
把random\_number開大一點(16 bit), 增加他循環的長度, 實際output只取他的最後4位。

## 7. 心得

以前寫verilog都只是在電腦上模擬。這是第一次用FPGA, 能讓自己的verilog有實際硬體成果很開心。除此之外也有試著寫一點testbench, 有成功藉此找到錯誤, 好玩!