

# Team09 Lab3 Report

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## 1. File Structure

team09\_lab3

| - team09\_lab3\_report.pdf

| - src/

    | - DE2\_115/

        | - DE2\_115.sv

        | - Debounce.sv

        | - SevenHexDecoder.sv

    | - Altpll/

        | - Altpll.v

    | - AudDSP.sv

    | - AudPlayer.sv

    | - AudRecorder.sv

    | - AudPlayer.sv

    | - I2cInitializer.sv

    | - Top.sv

## 2. System Architecture

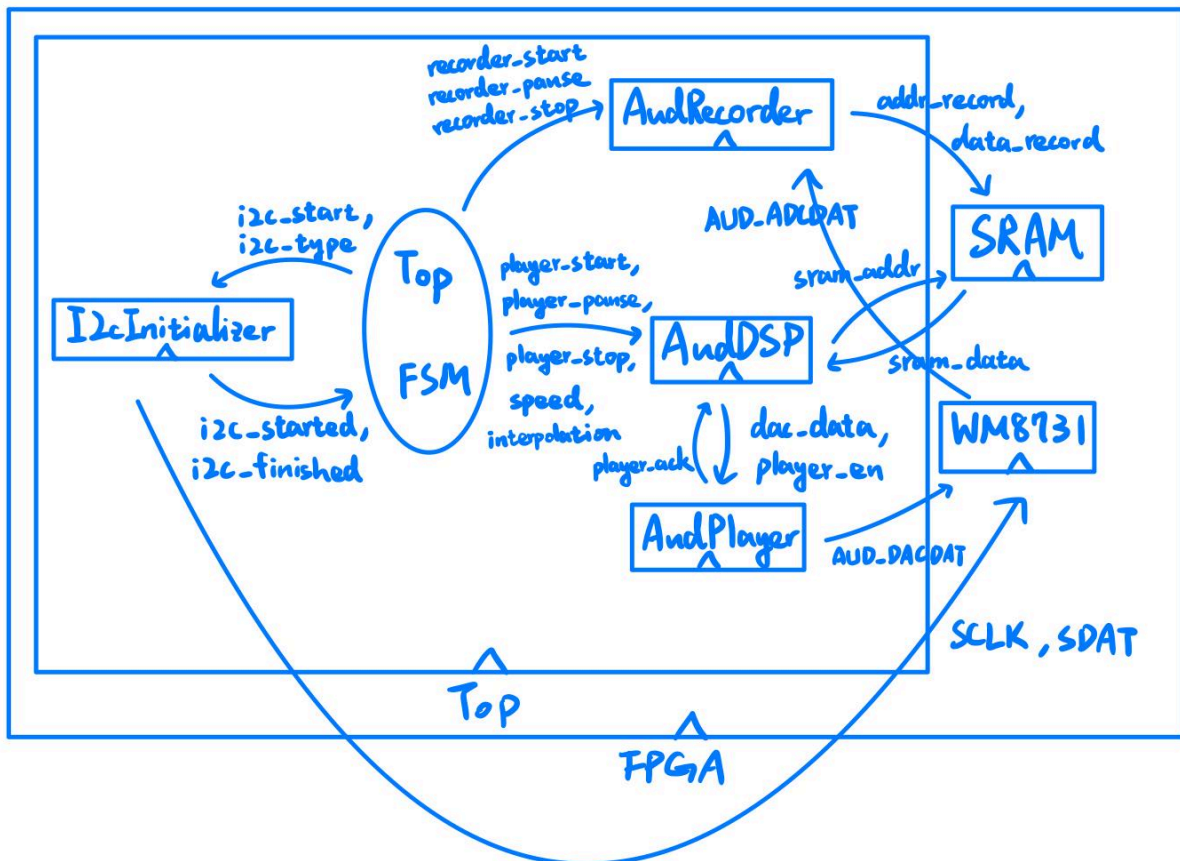


Figure 1: System Architecture

3. Hardware Scheduling

a. FSM

i. Top

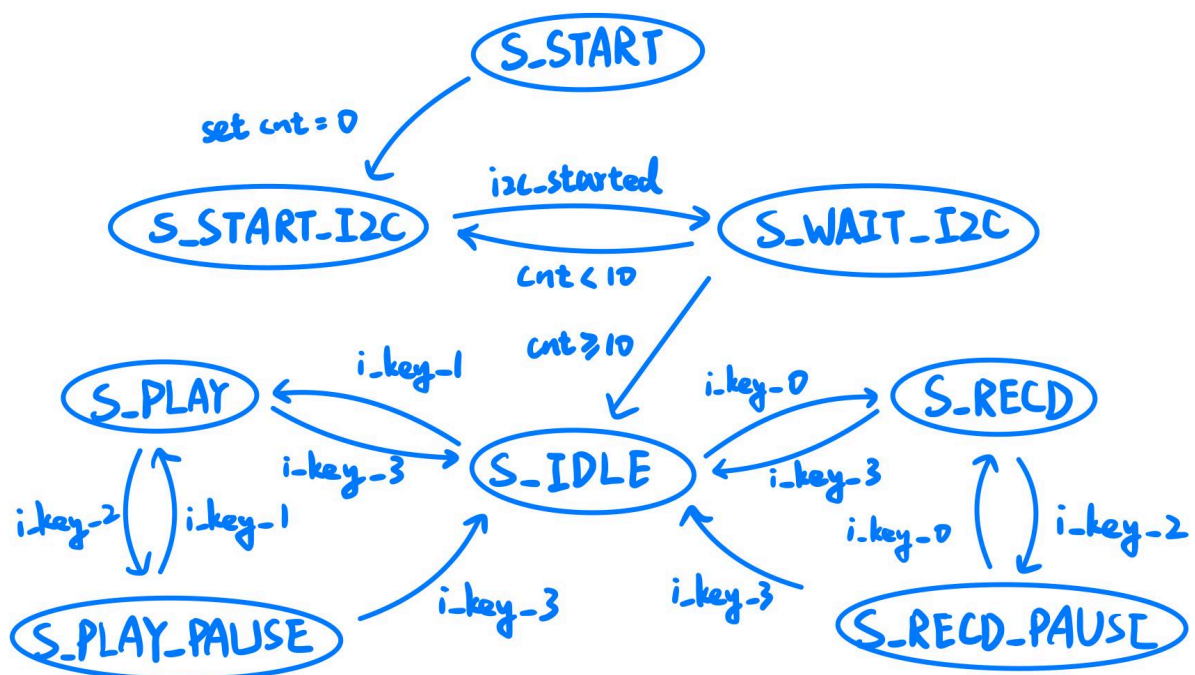


Figure 2: FSM of Top.

ii. I2cInitializer

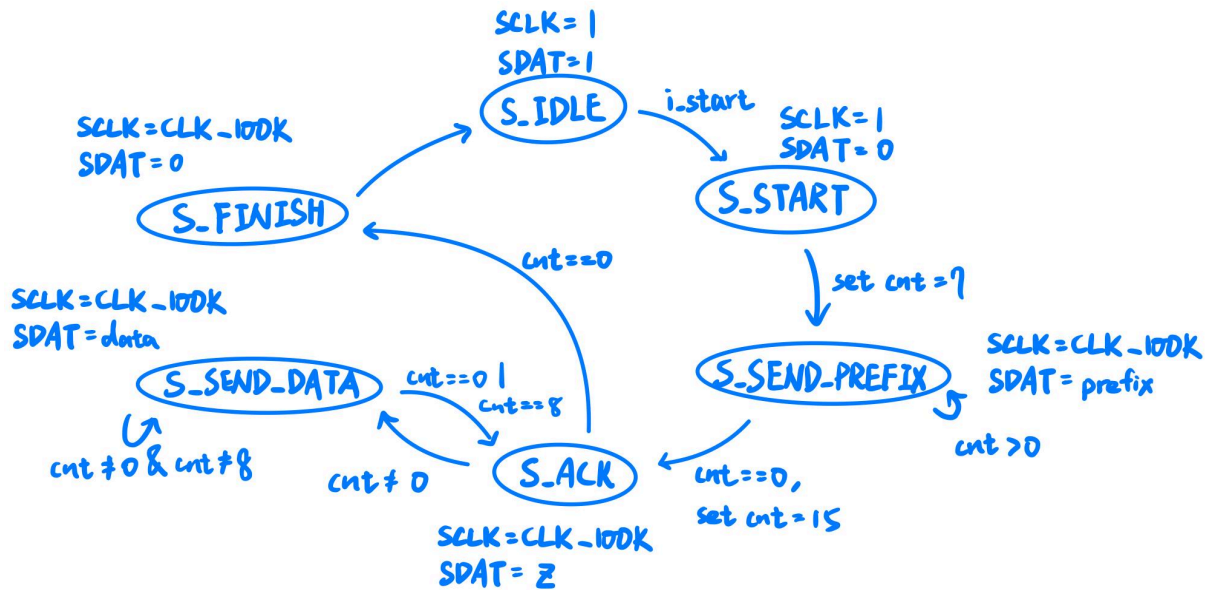


Figure 2: FSM of I2cInitializer.

iii. AudRecorder

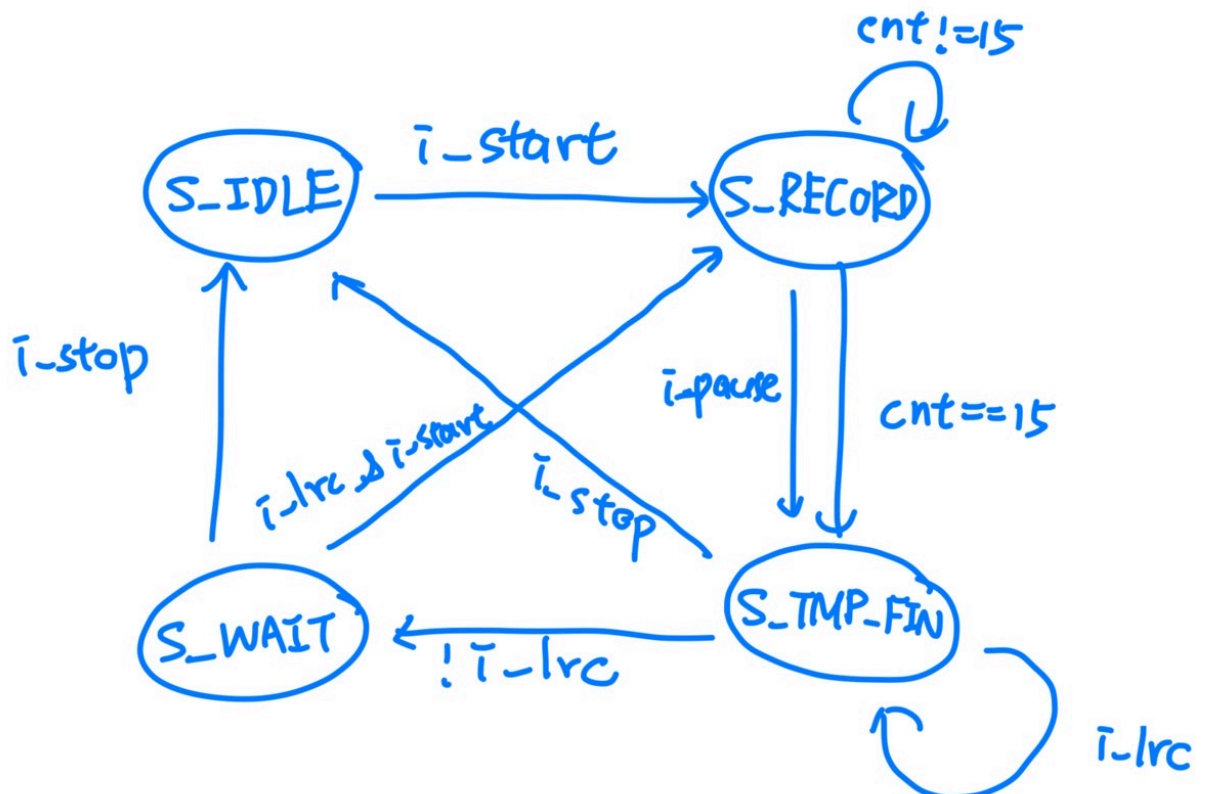


Figure 4: FSM of AudRecorder.

IDLE: set output data and SRAM address to 0 and wait for  $i\_start$  to start recording.

RECORD: record input data for 16 cycles

TMP\_FIN: temporarily pause and wait for the next i\_LRC to be the opposite channel and go to WAIT.

WAIT: wait for the next i\_LRC signal to be the desired channel and start recording

PAUSE: pause the recording, and keep the same SRAM address

iv. AudDSP

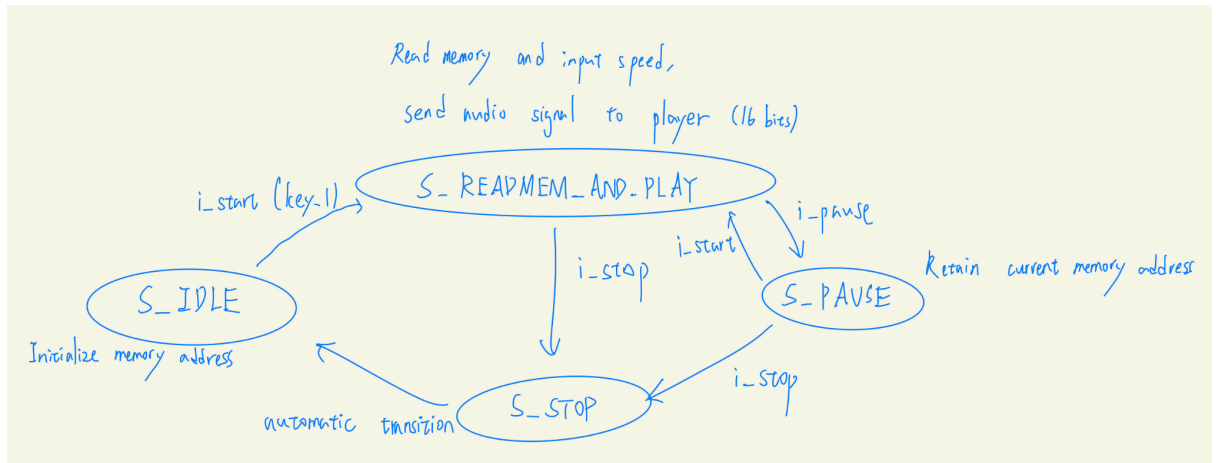
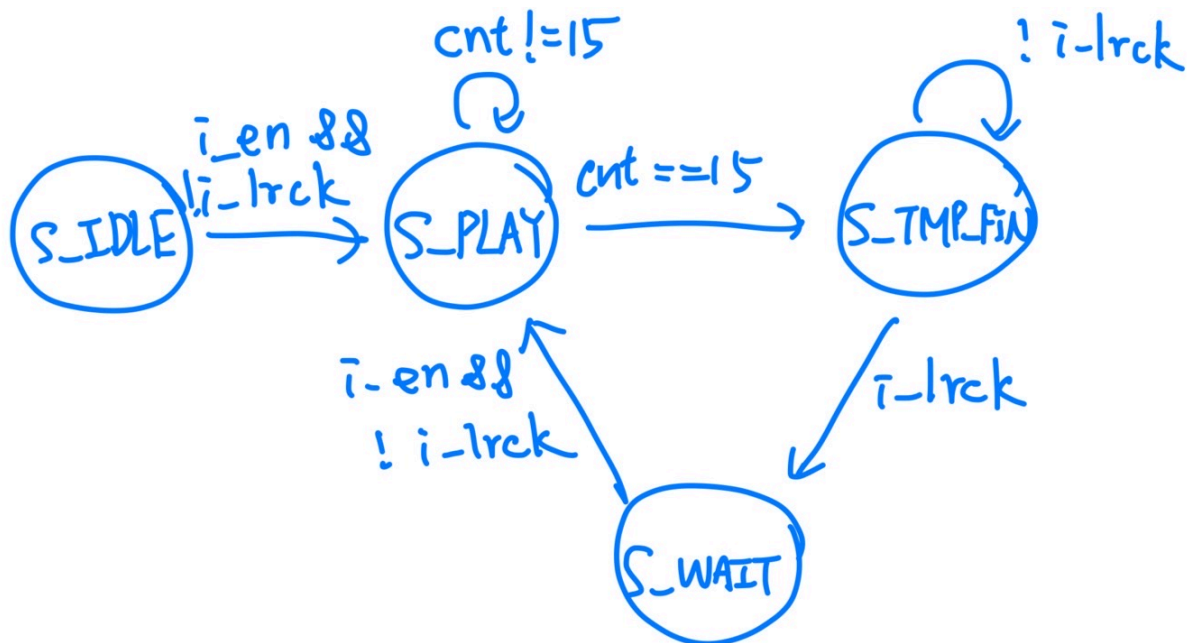


Figure 5: FSM of AudDSP

v. AudPlayer



IDLE, WAIT: wait for  $i_{en}$  and  $i_{LRC}$  to start playing and load data before switching to wait

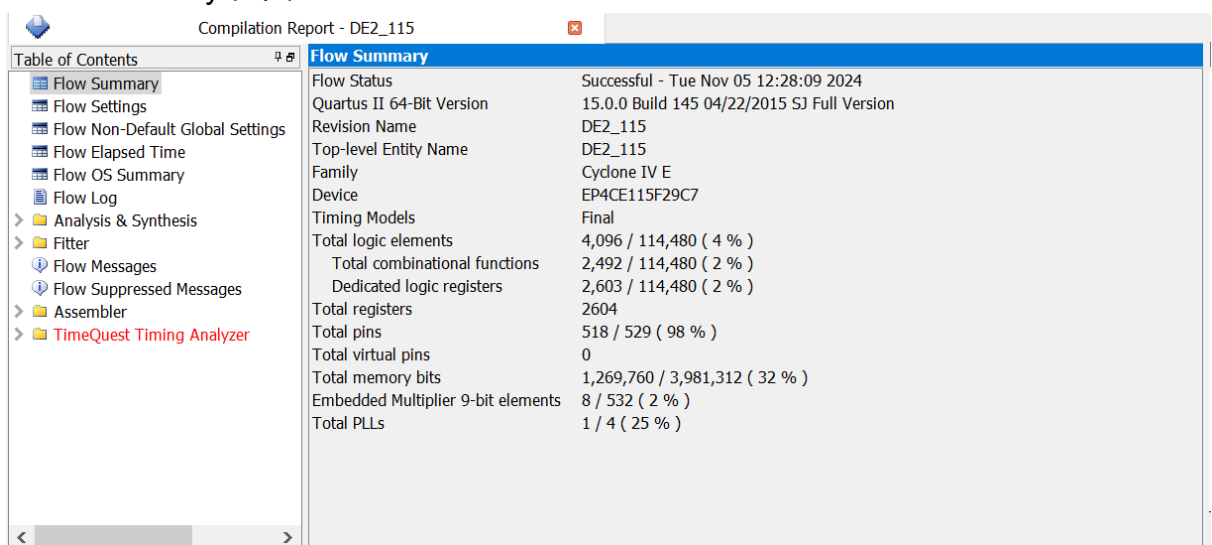
PLAY: load input data and transfer the data into I2S format

TMP\_FIN: finish the transfer of the current data and wait for the  $i_{lrc}$  signal to change.

#### b. DSP functions

- i. play speed determination: A table is established to be looked up when a speed signal is sent from DE2\_115.sv -> Top.sv -> AudDSP.sv, which will then control the speed of the update of sram address and thus present the effect of playing music with different speed.
- ii. interpolation method: Based on the input interpolation decision signal, different interpolation methods will be activated when playing music with slower speed. A counter will decide when to get a new audio signal and the weight of different data to form a linear combination of audio signals. 1/2, 1/4, 1/8 play speed are easily attained by shifting the combined signals, while 1/3 play speed is achieved by an approximated division. 1/5, 1/6, 1/7 play speed are using similar methods of 1/4, 1/8, 1/8 respectively and the reasons will be discussed later.
- iii. communicate with player: Since signal are sent on specific moments according to I2S protocol, DSP needs to control when to enable and send right signals to the player. This is achieved by following DACLRCK and requesting for memory data right after the opposite edge of DACLRCK.

#### 4. Fitter Summary 截圖



Compilation Report - DE2_115		
Flow Summary		
Flow Status	Successful - Tue Nov 05 12:28:09 2024	
Quartus II 64-Bit Version	15.0.0 Build 145 04/22/2015 SJ Full Version	
Revision Name	DE2_115	
Top-level Entity Name	DE2_115	
Family	Cyclone IV E	
Device	EP4CE115F29C7	
Timing Models	Final	
Total logic elements	4,096 / 114,480 ( 4 % )	
Total combinational functions	2,492 / 114,480 ( 2 % )	
Dedicated logic registers	2,603 / 114,480 ( 2 % )	
Total registers	2604	
Total pins	518 / 529 ( 98 % )	
Total virtual pins	0	
Total memory bits	1,269,760 / 3,981,312 ( 32 % )	
Embedded Multiplier 9-bit elements	8 / 532 ( 2 % )	
Total PLLs	1 / 4 ( 25 % )	

## 5. Timing Analyzer截圖

Table of Contents

- Summary
- Parallel Compilation
- SDC File List
- Clocks
- Slow 1200mV 85C Model
  - Fmax Summary
  - Timing Closure Recomm
  - Setup Summary
  - Hold Summary
  - Recovery Summary
  - Removal Summary
  - Minimum Pulse Width Sun
- Worst-Case Timing Paths
  - Setup: 'pll0|altpll\_0|sd:
  - Setup: 'AUD\_BCLK'
  - Setup: 'altera\_reserved
  - Setup: 'pll0|altpll\_0|sd:
  - Hold: 'pll0|altpll\_0|sd1
  - Hold: 'AUD\_BCLK'
  - Hold: 'altera reserved

### Timing Closure Recommendations

Summary [hide details]

This design contains failing setup paths with a worst-case slack of -7.470 ns. Run [Report Timing Closure Recommendations](#) for recommendations on how to dose setup timing. For recommendations for any particular path, click the appropriate link in the table below.

Top Failing Paths [hide details]

Slack	From	To	Recommendations
1 -7.470	Top:top0 AudPlayer:player0 cnt[2]	sl_d_slnaltap:aut...ligger_in_reg[49]	<a href="#">Report recommendations for this path</a>
2 -7.455	Top:top0 AudPlayer:player0 cnt[2]	sl_d_slnaltap:aut..._data_in_reg[49]	<a href="#">Report recommendations for this path</a>
3 -7.341	Top:top0 AudPlayer:player0 cnt[3]	sl_d_slnaltap:aut...ligger_in_reg[49]	<a href="#">Report recommendations for this path</a>
4 -7.326	Top:top0 AudPlayer:player0 cnt[2]	sl_d_slnaltap:aut...ligger_in_reg[49]	<a href="#">Report recommendations for this path</a>
5 -7.326	Top:top0 AudPlayer:player0 cnt[3]	sl_d_slnaltap:aut..._data_in_reg[49]	<a href="#">Report recommendations for this path</a>

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  - Recovery Summary
  - Removal Summary
  - Minimum Pulse Width Sun
- Worst-Case Timing Paths
  - Setup: 'pll0|altpll\_0|sd:
  - Setup: 'AUD\_BCLK'
  - Setup: 'altera\_reserved
  - Setup: 'pll0|altpll\_0|sd:
  - Hold: 'pll0|altpll\_0|sd1
  - Hold: 'AUD\_BCLK'
  - Hold: 'altera reserved

### Slow 1200mV 85C Model Setup Summary

	Clock	Slack	End Point TNS
1	pll0 altpll_0 sd1 pll7 clk[0]	-7.470	-1209.491
2	AUD_BCLK	-5.565	-111.552
3	altera_reserved_tck	43.371	0.000
4	pll0 altpll_0 sd1 pll7 clk[1]	79.634	0.000

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  - Recovery Summary
  - Removal Summary
  - Minimum Pulse Width Sun
- Worst-Case Timing Paths
  - Setup: 'pll0|altpll\_0|sd:
  - Setup: 'AUD\_BCLK'
  - Setup: 'altera\_reserved
  - Setup: 'pll0|altpll\_0|sd:
  - Hold: 'pll0|altpll\_0|sd1
  - Hold: 'AUD\_BCLK'
  - Hold: 'altera reserved

### Slow 1200mV 85C Model Hold Summary

	Clock	Slack	End Point TNS
1	pll0 altpll_0 sd1 pll7 clk[0]	-0.361	-1.976
2	AUD_BCLK	0.189	0.000
3	altera_reserved_tck	0.403	0.000
4	pll0 altpll_0 sd1 pll7 clk[1]	0.404	0.000



Table of Contents		Slow 1200mV 85C Model Setup: 'pll0 altpll_0 sd1 pll7 clk[0]'			
SDC File List		Slack	From Node	To Node	
Clocks					
Slow 1200mV 85C Model					
Fmax Summary					
Timing Closure Recomm					
Setup Summary					
Hold Summary					
Recovery Summary					
Removal Summary					
Minimum Pulse Width Sum					
Worst-Case Timing Paths					
Setup: 'pll0 altpll_0 sd1 pll7 clk[0]'					
Setup: 'AUD_BCLK'					
Setup: 'altera_reserved_					
Setup: 'pll0 altpll_0 sd1 pll7 clk[0]'					
Hold: 'pll0 altpll_0 sd1 pll7 clk[0]'					
Hold: 'AUD_BCLK'					
Hold: 'altera_reserved_					
Hold: 'pll0 altpll_0 sd1 pll7 clk[0]'					
Recovery: 'altera_resen					

Table of Contents		Slow 1200mV 85C Model Setup: 'AUD_BCLK'			
SDC File List		Slack	From Node	To Node	
Clocks					
Slow 1200mV 85C Model					
Fmax Summary					
Timing Closure Recomm					
Setup Summary					
Hold Summary					
Recovery Summary					
Removal Summary					
Minimum Pulse Width Sum					
Worst-Case Timing Paths					
Setup: 'pll0 altpll_0 sd1 pll7 clk[0]'					
Setup: 'AUD_BCLK'					
Setup: 'altera_reserved_					
Setup: 'pll0 altpll_0 sd1 pll7 clk[0]'					
Hold: 'pll0 altpll_0 sd1 pll7 clk[0]'					
Hold: 'AUD_BCLK'					
Hold: 'altera_reserved_					
Hold: 'pll0 altpll_0 sd1 pll7 clk[0]'					
Recovery: 'altera_resen					

Table of Contents		Slow 1200mV 85C Model Hold: 'pll0 altpll_0 sd1 pll7 clk[0]'			
SDC File List		Slack	From Node	To Node	
Clocks					
Slow 1200mV 85C Model					
Fmax Summary					
Timing Closure Recomm					
Setup Summary					
Hold Summary					
Recovery Summary					
Removal Summary					
Minimum Pulse Width Sum					
Worst-Case Timing Paths					
Setup: 'pll0 altpll_0 sd1 pll7 clk[0]'					
Setup: 'AUD_BCLK'					
Setup: 'altera_reserved_					
Setup: 'pll0 altpll_0 sd1 pll7 clk[0]'					
Hold: 'pll0 altpll_0 sd1 pll7 clk[0]'					
Hold: 'AUD_BCLK'					
Hold: 'altera_reserved_					
Hold: 'pll0 altpll_0 sd1 pll7 clk[0]'					
Recovery: 'altera_resen					

Slow 1200mV 0C Model Setup Summary			
	Clock	Slack	End Point TNS
1	pll0 altpll_0 sd1 pll7 clk[0]	-6.687	-1076.431
2	AUD_BCLK	-5.189	-106.369
3	altera_reserved_tck	44.046	0.000
4	pll0 altpll_0 sd1 pll7 clk[1]	79.917	0.000

Slow 1200mV 0C Model Hold Summary			
	Clock	Slack	End Point TNS
1	pll0 altpll_0 sd1 pll7 clk[0]	-0.343	-1.797
2	AUD_BCLK	0.192	0.000
3	altera_reserved_tck	0.354	0.000
4	pll0 altpll_0 sd1 pll7 clk[1]	0.356	0.000

Slow 1200mV 0C Model Setup: 'pll0 altpll_0 sd1 pll7 clk[0]'				
	Slack	From Node	To Node	
1	-6.687	Top:top0 AudPlayer:player0 cnt[2]	sld_signaltap:auto_signaltap_0 acq_trigger_in_reg[49]	AU
2	-6.664	Top:top0 AudPlayer:player0 cnt[2]	sld_signaltap:auto_signaltap_0 acq_data_in_reg[49]	AU
3	-6.571	Top:top0 AudPlayer:player0 cnt[3]	sld_signaltap:auto_signaltap_0 acq_trigger_in_reg[49]	AU
4	-6.548	Top:top0 AudPlayer:player0 cnt[3]	sld_signaltap:auto_signaltap_0 acq_data_in_reg[49]	AU
5	-6.471	Top:top0 AudPlayer:player0 dac_data[5]	sld_signaltap:auto_signaltap_0 acq_trigger_in_reg[49]	AU
6	-6.448	Top:top0 AudPlayer:player0 dac_data[5]	sld_signaltap:auto_signaltap_0 acq_data_in_reg[49]	AU
7	-6.374	Top:top0 AudPlayer:player0 dac_data[1]	sld_signaltap:auto_signaltap_0 acq_trigger_in_reg[49]	AU
8	-6.363	Top:top0 AudPlayer:player0 dac_data[4]	sld_signaltap:auto_signaltap_0 acq_trigger_in_reg[49]	AU
9	-6.356	Top:top0 AudPlayer:player0 dac_data[13]	sld_signaltap:auto_signaltap_0 acq_trigger_in_reg[49]	AU
10	-6.351	Top:top0 AudPlayer:player0 dac_data[1]	sld_signaltap:auto_signaltap_0 acq_data_in_reg[49]	AU
11	-6.343	Top:top0 AudPlayer:player0 dac_data[9]	sld_signaltap:auto_signaltap_0 acq_trigger_in_reg[49]	AU
12	-6.340	Top:top0 AudPlayer:player0 dac_data[4]	sld_signaltap:auto_signaltap_0 acq_data_in_reg[49]	AU
13	-6.335	Top:top0 AudPlayer:player0 dac_data[2]	sld_signaltap:auto_signaltap_0 acq_trigger_in_reg[49]	AU
14	-6.333	Top:top0 AudPlayer:player0 dac_data[13]	sld_signaltap:auto_signaltap_0 acq_data_in_reg[49]	AU
15	-6.320	Top:top0 AudPlayer:player0 dac_data[9]	sld_signaltap:auto_signaltap_0 acq_data_in_reg[49]	AU
16	-6.313	Top:top0 AudPlayer:player0 dac_data[2]	sld_signaltap:auto_signaltap_0 acq_data_in_reg[49]	AU
17	-6.311	Top:top0 AudPlayer:player0 dac_data[3]	sld_signaltap:auto_signaltap_0 acq_trigger_in_reg[49]	AU
18	-6.289	Top:top0 AudPlayer:player0 dac_data[3]	sld_signaltap:auto_signaltap_0 acq_data_in_reg[49]	AU
19	-6.273	Top:top0 AudPlayer:player0 dac_data[0]	sld_signaltap:auto_signaltap_0 acq_trigger_in_reg[49]	AU



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Flow Messages

Flow Suppressed Messages

Assembler

TimeQuest Timing Analyzer

- Summary
- Parallel Compilation
- SDC File List
- Clocks
- Slow 1200mV 85C Model
- Slow 1200mV 0C Model
  - Fmax Summary
  - Setup Summary
  - Hold Summary
  - Recovery Summary
  - Removal Summary
  - Minimum Pulse Width Sum
  - Worst-Case Timing Paths
    - Setup: 'pll0|altpll\_0|sd:
    - Setup: 'AUD\_BCLK'
    - Setup: 'altera\_reserved

Slack

From Node

To Node

1

-5.189

Top:top0|state\_r.S\_RECD

Top:top0|AudRecorder:recorder0|state.S\_WAIT

2

-5.161

Top:top0|state\_r.S\_RECD

Top:top0|AudRecorder:recorder0|state.S\_PAUSE

3

-5.139

Top:top0|state\_r.S\_RECD

Top:top0|AudRecorder:recorder0|state.S\_RECORD

4

-4.850

Debounce:deb3|neg\_r

Top:top0|AudRecorder:recorder0|state.S\_WAIT

5

-4.848

Debounce:deb3|neg\_r

Top:top0|AudRecorder:recorder0|state.S\_PAUSE

6

-4.834

Debounce:deb3|neg\_r

Top:top0|AudRecorder:recorder0|state.S\_RECORD

7

-4.772

Top:top0|state\_r.S\_RECD

Top:top0|AudRecorder:recorder0|state.S\_TMP\_FIN

8

-4.712

Top:top0|state\_r.S\_RECD

Top:top0|AudRecorder:recorder0|state.S\_IDLE

9

-4.698

Debounce:deb3|neg\_r

Top:top0|AudRecorder:recorder0|state.S\_TMP\_FIN

10

-4.683

Debounce:deb3|neg\_r

Top:top0|AudRecorder:recorder0|state.S\_IDLE

11

-4.679

Debounce:deb2|neg\_r

Top:top0|AudRecorder:recorder0|state.S\_WAIT

12

-4.651

Debounce:deb2|neg\_r

Top:top0|AudRecorder:recorder0|state.S\_PAUSE

13

-4.593

Debounce:deb2|neg\_r

Top:top0|AudRecorder:recorder0|state.S\_RECORD

14

-4.570

Top:top0|state\_r.S\_RECD\_PAUSE

Top:top0|AudRecorder:recorder0|state.S\_WAIT

15

-4.568

Top:top0|state\_r.S\_RECD\_PAUSE

Top:top0|AudRecorder:recorder0|state.S\_PAUSE

16

-4.554

Top:top0|state\_r.S\_RECD\_PAUSE

Top:top0|AudRecorder:recorder0|state.S\_RECORD

17

-4.418

Top:top0|state\_r.S\_RECD\_PAUSE

Top:top0|AudRecorder:recorder0|state.S\_TMP\_FIN

18

-4.403

Top:top0|state\_r.S\_RECD\_PAUSE

Top:top0|AudRecorder:recorder0|state.S\_IDLE

19

-4.262

Debounce:deb2|neg\_r

Top:top0|AudRecorder:recorder0|state.S\_TMP\_FIN

Table of Contents		Slow 1200mV 0C Model Hold: 'pll0 altpll_0 sd1 pll7 clk[0]'			
		Slack	From Node		To
Parallel Compilation		1	-0.343	pll0 altpll_0 sd1 pll7 clk[1]	sld_signaltap:auto_signaltap_0 ao
SDC File List		2	-0.340	pll0 altpll_0 sd1 pll7 clk[1]	sld_signaltap:auto_signaltap_0 ao
Clocks		3	-0.312	pll0 altpll_0 sd1 pll7 clk[2]	sld_signaltap:auto_signaltap_0 ao
Slow 1200mV 85C Model		4	-0.309	pll0 altpll_0 sd1 pll7 clk[2]	sld_signaltap:auto_signaltap_0 ao
Slow 1200mV 0C Model		5	-0.300	pll0 altpll_0 sd1 pll7 clk[0]	sld_signaltap:auto_signaltap_0 ao
Fmax Summary		6	-0.285	pll0 altpll_0 sd1 pll7 clk[1]	sld_signaltap:auto_signaltap_0 ao
Setup Summary		7	-0.282	pll0 altpll_0 sd1 pll7 clk[1]	sld_signaltap:auto_signaltap_0 ao
Hold Summary		8	-0.193	pll0 altpll_0 sd1 pll7 clk[0]	sld_signaltap:auto_signaltap_0 ao
Recovery Summary		9	0.256	sld_signaltap:auto_signaltap_0 sl...body acq_data_in_pipe_reg[3][121]	sld_signaltap:auto_signaltap_0 sl...
Removal Summary		10	0.276	sld_signaltap:auto_signaltap_0 sl...body acq_data_in_pipe_reg[3][82]	sld_signaltap:auto_signaltap_0 sl...
Minimum Pulse Width Summary		11	0.331	sld_signaltap:auto_signaltap_0 sl...body acq_data_in_pipe_reg[3][59]	sld_signaltap:auto_signaltap_0 sl...
Worst-Case Timing Paths		12	0.335	sld_signaltap:auto_signaltap_0 sl...p_body acq_data_in_pipe_reg[3][2]	sld_signaltap:auto_signaltap_0 sl...
Setup: 'pll0 altpll_0 sd1 pll7 clk[0]'		13	0.336	sld_signaltap:auto_signaltap_0 sl...body acq_data_in_pipe_reg[3][123]	sld_signaltap:auto_signaltap_0 sl...
Setup: 'AUD_BCLK'		14	0.337	sld_signaltap:auto_signaltap_0 sl...p_body acq_data_in_pipe_reg[3][1]	sld_signaltap:auto_signaltap_0 sl...
Setup: 'altera_reserved_tck'		15	0.338	sld_signaltap:auto_signaltap_0 sl...body acq_data_in_pipe_reg[3][147]	sld_signaltap:auto_signaltap_0 sl...
Setup: 'pll0 altpll_0 sd1 pll7 clk[0]'		16	0.340	sld_signaltap:auto_signaltap_0 sl...body acq_data_in_pipe_reg[3][118]	sld_signaltap:auto_signaltap_0 sl...
Hold: 'pll0 altpll_0 sd1 pll7 clk[0]'		17	0.341	sld_signaltap:auto_signaltap_0 sl...body acq_data_in_pipe_reg[3][126]	sld_signaltap:auto_signaltap_0 sl...
Hold: 'AUD_BCLK'		18	0.341	sld_signaltap:auto_signaltap_0 sl...body acq_data_in_pipe_reg[3][116]	sld_signaltap:auto_signaltap_0 sl...
Hold: 'altera_reserved_tck'		19	0.343	sld_signaltap:auto_signaltap_0 sl...body acq_data_in_pipe_reg[3][154]	sld_signaltap:auto_signaltap_0 sl...
Hold: 'pll0 altpll_0 sd1 pll7 clk[0]'		20	0.343	sld_signaltap:auto_signaltap_0 sl...body acq_data_in_pipe_reg[3][154]	sld_signaltap:auto_signaltap_0 sl...

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Recovery: 'altera\_reserved\_tck'

Removal: 'altera\_reserved\_tck'

Minimum Pulse Width: 'altera\_reserved\_tck'

Minimum Pulse Width: 'altera\_reserved\_tck'

Minimum Pulse Width: 'altera\_reserved\_tck'

Minimum Pulse Width: 'altera\_reserved\_tck'

Minimum Pulse Width: 'altera\_reserved\_tck'

Minimum Pulse Width: 'altera\_reserved\_tck'

Datasheet Report

Metastability Summary

Fast 1200mV 0C Model

- Setup Summary
- Hold Summary
- Recovery Summary
- Removal Summary
- Minimum Pulse Width Summary
- Worst-Case Timing Paths
- Datasheet Report
- Metastability Summary

	Clock	Slack	End Point TNS
1	pll0 altpll_0 sd1 pll7 clk[0]	-4.406	-780.698
2	AUD_BCLK	-2.237	-48.637
3	altera_reserved_tck	47.009	0.000
4	pll0 altpll_0 sd1 pll7 clk[1]	81.425	0.000

Fast 1200mV OC Model Hold Summary			
	Clock	Slack	End Point TNS
1	AUD_BCLK	-0.645	-1.161
2	pll0 altpll_0 sd1 pll7 clk[0]	-0.195	-1.040
3	pll0 altpll_0 sd1 pll7 clk[1]	0.155	0.000
4	altera_reserved_tck	0.181	0.000

Fast 1200mV OC Model Setup: 'pll0 altpll_0 sd1 pll7 clk[0]'				
	Slack	From Node	To Node	
1	-4.406	Top:top0 AudPlayer:player0 cnt[2]	sld_signaltap:auto_signaltap_0 acq_data_in_reg[49]	AU
2	-4.395	Top:top0 AudPlayer:player0 cnt[2]	sld_signaltap:auto_signaltap_0 acq_trigger_in_reg[49]	AU
3	-4.335	Top:top0 AudPlayer:player0 cnt[3]	sld_signaltap:auto_signaltap_0 acq_data_in_reg[49]	AU
4	-4.324	Top:top0 AudPlayer:player0 cnt[3]	sld_signaltap:auto_signaltap_0 acq_trigger_in_reg[49]	AU
5	-4.279	Top:top0 AudPlayer:player0 dac_data[5]	sld_signaltap:auto_signaltap_0 acq_data_in_reg[49]	AU
6	-4.268	Top:top0 AudPlayer:player0 dac_data[5]	sld_signaltap:auto_signaltap_0 acq_trigger_in_reg[49]	AU
7	-4.244	Top:top0 AudPlayer:player0 dac_data[1]	sld_signaltap:auto_signaltap_0 acq_data_in_reg[49]	AU
8	-4.234	Top:top0 AudPlayer:player0 dac_data[13]	sld_signaltap:auto_signaltap_0 acq_data_in_reg[49]	AU
9	-4.233	Top:top0 AudPlayer:player0 dac_data[1]	sld_signaltap:auto_signaltap_0 acq_trigger_in_reg[49]	AU
10	-4.232	Top:top0 AudPlayer:player0 dac_data[2]	sld_signaltap:auto_signaltap_0 acq_data_in_reg[49]	AU
11	-4.230	Top:top0 AudPlayer:player0 dac_data[3]	sld_signaltap:auto_signaltap_0 acq_data_in_reg[49]	AU
12	-4.223	Top:top0 AudPlayer:player0 dac_data[13]	sld_signaltap:auto_signaltap_0 acq_trigger_in_reg[49]	AU
13	-4.221	Top:top0 AudPlayer:player0 dac_data[2]	sld_signaltap:auto_signaltap_0 acq_trigger_in_reg[49]	AU
14	-4.219	Top:top0 AudPlayer:player0 dac_data[9]	sld_signaltap:auto_signaltap_0 acq_data_in_reg[49]	AU
15	-4.219	Top:top0 AudPlayer:player0 dac_data[3]	sld_signaltap:auto_signaltap_0 acq_trigger_in_reg[49]	AU
16	-4.210	Top:top0 AudPlayer:player0 dac_data[4]	sld_signaltap:auto_signaltap_0 acq_data_in_reg[49]	AU
17	-4.208	Top:top0 AudPlayer:player0 dac_data[9]	sld_signaltap:auto_signaltap_0 acq_trigger_in_reg[49]	AU
18	-4.199	Top:top0 AudPlayer:player0 dac_data[4]	sld_signaltap:auto_signaltap_0 acq_trigger_in_reg[49]	AU
19	-4.180	Top:top0 AudPlayer:player0 dac_data[0]	sld_signaltap:auto_signaltap_0 acq_data_in_reg[49]	AU

Fast 1200mV OC Model Setup: 'AUD_BCLK'			
	Slack	From Node	To Node
1	-2.237	Top:top0 state_r.S_RECDD	Top:top0 AudRecorder:recorder0 state.S_RECORD
2	-2.229	Top:top0 state_r.S_RECDD	Top:top0 AudRecorder:recorder0 state.S_WAIT
3	-2.215	Top:top0 state_r.S_RECDD	Top:top0 AudRecorder:recorder0 state.S_PAUSE
4	-2.126	Debounce:deb3 neg_r	Top:top0 AudRecorder:recorder0 state.S_IDLE
5	-2.121	Debounce:deb3 neg_r	Top:top0 AudRecorder:recorder0 state.S_TMP_FIN
6	-2.106	Top:top0 state_r.S_RECDD	Top:top0 AudRecorder:recorder0 state.S_TMP_FIN
7	-2.057	Top:top0 state_r.S_RECDD	Top:top0 AudRecorder:recorder0 state.S_IDLE
8	-2.037	Debounce:deb3 neg_r	Top:top0 AudRecorder:recorder0 state.S_RECORD
9	-2.029	Debounce:deb3 neg_r	Top:top0 AudRecorder:recorder0 state.S_WAIT
10	-2.015	Debounce:deb3 neg_r	Top:top0 AudRecorder:recorder0 state.S_PAUSE
11	-1.980	Top:top0 state_r.S_RECDD_PAUSE	Top:top0 AudRecorder:recorder0 state.S_IDLE
12	-1.975	Top:top0 state_r.S_RECDD_PAUSE	Top:top0 AudRecorder:recorder0 state.S_TMP_FIN
13	-1.963	Top:top0 AudDSP:dsp0 o_player_en_r	Top:top0 AudPlayer:player0 state.S_PLAY
14	-1.928	Debounce:deb2 neg_r	Top:top0 AudRecorder:recorder0 state.S_RECORD
15	-1.920	Debounce:deb2 neg_r	Top:top0 AudRecorder:recorder0 state.S_WAIT
16	-1.916	Top:top0 AudDSP:dsp0 o_processed_data_r[9]	Top:top0 AudPlayer:player0 dac_data[9]
17	-1.910	Top:top0 AudDSP:dsp0 o_processed_data_r[4]	Top:top0 AudPlayer:player0 dac_data[4]
18	-1.906	Debounce:deb2 neg_r	Top:top0 AudRecorder:recorder0 state.S_PAUSE
19	-1.899	Top:top0 AudDSP:dsp0 o_processed_data_r[11]	Top:top0 AudPlayer:player0 dac_data[11]

Table of Contents		Fast 1200mV OC Model Hold: 'AUD_BCLK'		
<ul style="list-style-type: none"> <li>Minimum Pulse Width:</li> <li>Minimum Pulse Width:</li> <li>Minimum Pulse Width:</li> <li>Minimum Pulse Width:</li> <li>Datasheet Report</li> <li>Metastability Summary</li> <li>Fast 1200mV OC Model <ul style="list-style-type: none"> <li>Setup Summary</li> <li>Hold Summary</li> <li>Recovery Summary</li> <li>Removal Summary</li> <li>Minimum Pulse Width Summary</li> </ul> </li> <li>Worst-Case Timing Paths <ul style="list-style-type: none"> <li>Setup: 'pll0 altpll_0 sd1</li> <li>Setup: 'AUD_BCLK'</li> <li>Setup: 'altera_reserved_</li> <li>Setup: 'pll0 altpll_0 sd1</li> <li>Hold: 'AUD_BCLK'</li> <li>Hold: 'pll0 altpll_0 sd1</li> <li>Hold: 'pll0 altpll_0 sd1</li> </ul> </li> </ul>		Slack	From Node	To Node
	1	-0.645	Debounce:deb0 neg_r	Top:top0 AudRecorder:recorder0 state.S_IDLE
	2	-0.250	Top:top0 state_r.S_REC_D_PAUSE	Top:top0 AudRecorder:recorder0 state.S_TMP_FIN
	3	-0.226	Debounce:deb2 neg_r	Top:top0 AudRecorder:recorder0 state.S_IDLE
	4	-0.215	Top:top0 state_r.S_REC_D_PAUSE	Top:top0 AudRecorder:recorder0 state.S_IDLE
	5	-0.127	Top:top0 state_r.S_REC_D_PAUSE	Top:top0 AudRecorder:recorder0 state.S_RECORD
	6	-0.125	Debounce:deb2 neg_r	Top:top0 AudRecorder:recorder0 state.S_TMP_FIN
	7	-0.109	Debounce:deb3 neg_r	Top:top0 AudRecorder:recorder0 state.S_IDLE
	8	-0.075	Top:top0 state_r.S_REC_D_PAUSE	Top:top0 AudRecorder:recorder0 state.S_WAIT
	9	-0.075	Debounce:deb0 neg_r	Top:top0 AudRecorder:recorder0 state.S_TMP_FIN
	10	-0.064	Top:top0 state_r.S_REC_D_PAUSE	Top:top0 AudRecorder:recorder0 state.S_PAUSE
	11	-0.002	Debounce:deb2 neg_r	Top:top0 AudRecorder:recorder0 state.S_RECORD
	12	0.048	Debounce:deb0 neg_r	Top:top0 AudRecorder:recorder0 state.S_RECORD
	13	0.050	Debounce:deb2 neg_r	Top:top0 AudRecorder:recorder0 state.S_WAIT
	14	0.061	Debounce:deb2 neg_r	Top:top0 AudRecorder:recorder0 state.S_PAUSE
	15	0.100	Debounce:deb0 neg_r	Top:top0 AudRecorder:recorder0 state.S_WAIT
	16	0.111	Debounce:deb0 neg_r	Top:top0 AudRecorder:recorder0 state.S_PAUSE
	17	0.143	Top:top0 state_r.S_REC_D	Top:top0 AudRecorder:recorder0 state.S_TMP_FIN
	18	0.168	Top:top0 state_r.S_REC_D	Top:top0 AudRecorder:recorder0 state.S_IDLE
	19	0.266	Top:top0 state_r.S_REC_D	Top:top0 AudRecorder:recorder0 state.S_RECORD

Table of Contents		Fast 1200mV OC Model Hold: 'pll0 altpll_0 sd1 pll7 clk[0]'		
<ul style="list-style-type: none"> <li>Setup Summary</li> <li>Hold Summary</li> <li>Recovery Summary</li> <li>Removal Summary</li> <li>Minimum Pulse Width Summary</li> <li>Worst-Case Timing Paths <ul style="list-style-type: none"> <li>Setup: 'pll0 altpll_0 sd1</li> <li>Setup: 'AUD_BCLK'</li> <li>Setup: 'altera_reserved_</li> <li>Setup: 'pll0 altpll_0 sd1</li> <li>Hold: 'AUD_BCLK'</li> <li>Hold: 'pll0 altpll_0 sd1</li> <li>Hold: 'altera_reserved_</li> <li>Recovery: 'altera_reserved_</li> <li>Removal: 'altera_reserved_</li> <li>Minimum Pulse Width:</li> <li>Minimum Pulse Width:</li> <li>Minimum Pulse Width:</li> <li>Minimum Pulse Width:</li> </ul> </li> </ul>		Slack	From Node	To Node
	1	-0.195	pll0 altpll_0 sd1 pll7 clk[2]	sld_signaltap:auto_signaltap_0 ao
	2	-0.194	pll0 altpll_0 sd1 pll7 clk[2]	sld_signaltap:auto_signaltap_0 ao
	3	-0.185	pll0 altpll_0 sd1 pll7 clk[0]	sld_signaltap:auto_signaltap_0 ao
	4	-0.169	pll0 altpll_0 sd1 pll7 clk[1]	sld_signaltap:auto_signaltap_0 ao
	5	-0.168	pll0 altpll_0 sd1 pll7 clk[1]	sld_signaltap:auto_signaltap_0 ao
	6	-0.129	pll0 altpll_0 sd1 pll7 clk[0]	sld_signaltap:auto_signaltap_0 ao
	7	-0.128	pll0 altpll_0 sd1 pll7 clk[1]	sld_signaltap:auto_signaltap_0 ao
	8	-0.126	pll0 altpll_0 sd1 pll7 clk[1]	sld_signaltap:auto_signaltap_0 ao
	9	0.078	sld_signaltap:auto_signaltap_0 sl...body acq_data_in_pipe_reg[3][121]	sld_signaltap:auto_signaltap_0 sl...
	10	0.097	sld_signaltap:auto_signaltap_0 sl...body acq_data_in_pipe_reg[3][82]	sld_signaltap:auto_signaltap_0 sl...
	11	0.127	sld_signaltap:auto_signaltap_0 sl...body acq_data_in_pipe_reg[3][59]	sld_signaltap:auto_signaltap_0 sl...
	12	0.127	sld_signaltap:auto_signaltap_0 sl...body acq_data_in_pipe_reg[3][147]	sld_signaltap:auto_signaltap_0 sl...
	13	0.128	sld_signaltap:auto_signaltap_0 sl...p_body acq_data_in_pipe_reg[3][1]	sld_signaltap:auto_signaltap_0 sl...
	14	0.132	sld_signaltap:auto_signaltap_0 sl...body acq_data_in_pipe_reg[3][123]	sld_signaltap:auto_signaltap_0 sl...
	15	0.133	sld_signaltap:auto_signaltap_0 sl...body acq_data_in_pipe_reg[3][126]	sld_signaltap:auto_signaltap_0 sl...
	16	0.133	sld_signaltap:auto_signaltap_0 sl...body acq_data_in_pipe_reg[3][116]	sld_signaltap:auto_signaltap_0 sl...
	17	0.134	sld_signaltap:auto_signaltap_0 sl...p_body acq_data_in_pipe_reg[3][2]	sld_signaltap:auto_signaltap_0 sl...
	18	0.136	sld_signaltap:auto_signaltap_0 sl...body acq_data_in_pipe_reg[3][154]	sld_signaltap:auto_signaltap_0 sl...
	19	0.137	sld_signaltap:auto_signaltap_0 sl...body acq_data_in_pipe_reg[3][107]	sld_signaltap:auto_signaltap_0 sl...



- c. 錄音與播放秒數:可隨播放速度變化, 於Top.sv內處理
- d. 倒帶播放:將錄製內容倒著播放出來, 會從錄製結束的位置開始往回播放, 避免播出雜音

## 8. 心得

這次的lab雖然不像上次有演算法的部分需要理解一下, 但因為開始需要在實作上與FPGA板上其他晶片溝通, 因此處理protocol的部分花了不少時間。除此之外, 因為整體系統逐漸擴大, 因此在分工時需要更詳細討論各部分的溝通方式, 也同時滿足各protocol的要求。這次最大的收穫之一應該是debug工具的使用, 可以了解FPGA上面訊號的正確性, 不再只是自己寫tb猜訊號的正確性, 為之後final project增加一大利多。