Team09 Lab1 Report

b11901003 方嘉麟
b11901091 鄭淳芸
b11901148 李承彥

1. File Structure

```
team09_lab1
| - team09_lab1_report.pdf
| - src/
    | - Top.sv
    | - DE2_115/
        | - DE2_115.qsf
        | - DE2_115.sdc
        | - DE2_115.sv
        | - Debounce.sv
        | - LFSR.sv
        | - SevenHexDecoder.sv
```

2. System Architecture

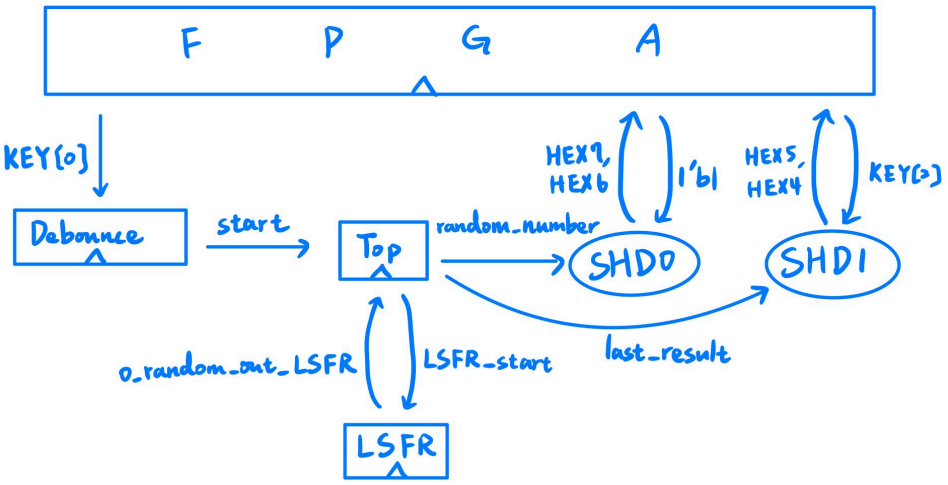
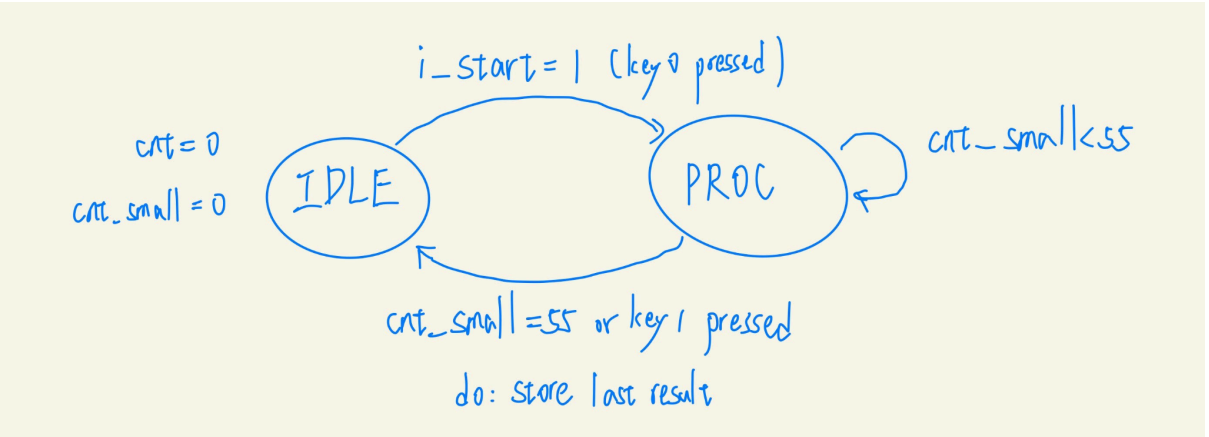


Figure 1: System Architecture (SHD: Seven Hex Decoder)

3. Hardware Scheduling
   a. FSM



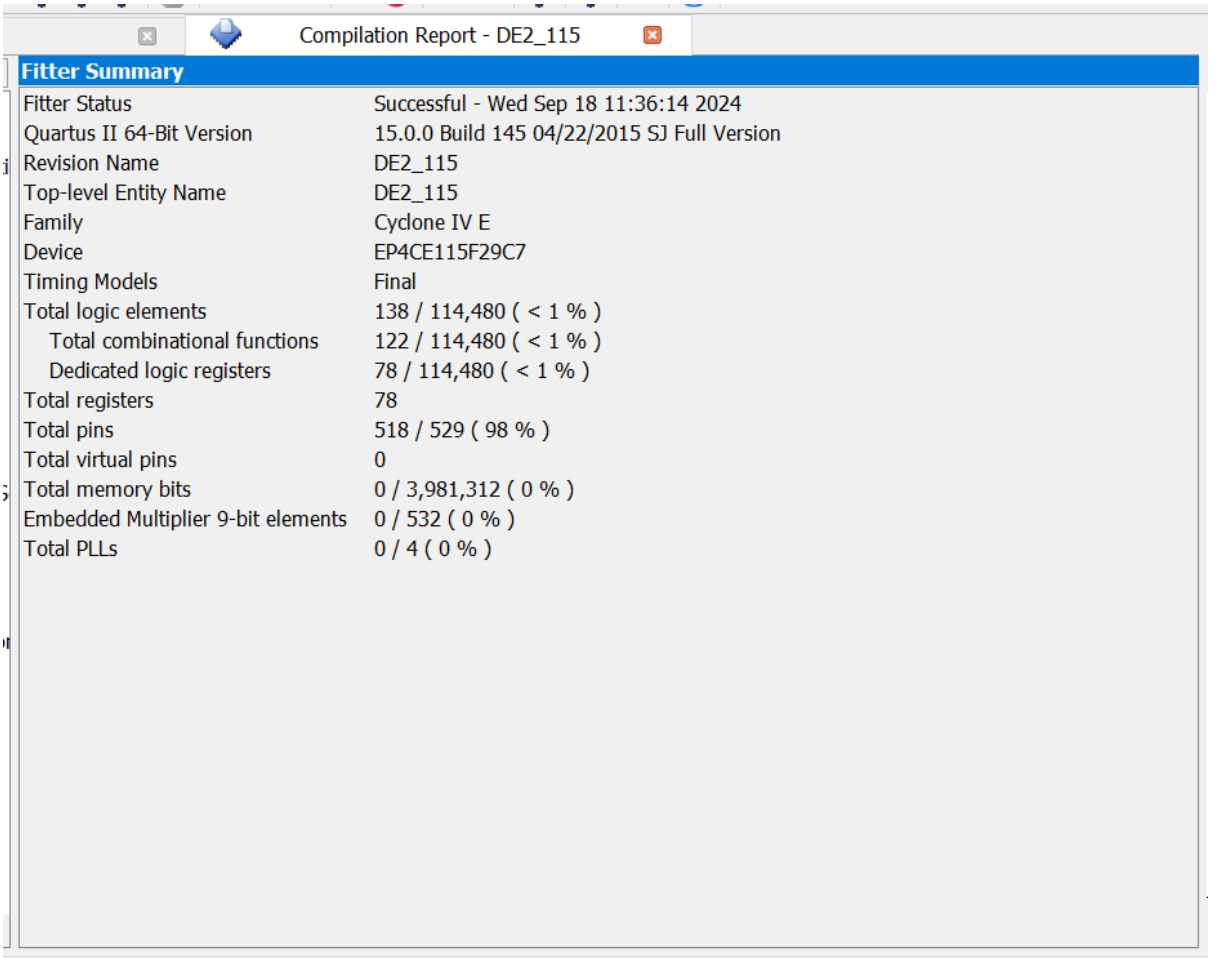
   b. Algorithm
      i. LFSR

         We use two 16-bit vectors *random_number* and *random_seed* to generate random numbers. For each clock, *random_seed* does LFSR one time, and if input *LFSR_start* is 1, *random_number* also does LFSR one time. (If *random_number* is 16'b0, *random_number* <= *random_seed.* If *random_seed* is 16'b0, set *random_seed* to be a non-zero value.) And the output is the first four bits of *random_number*.

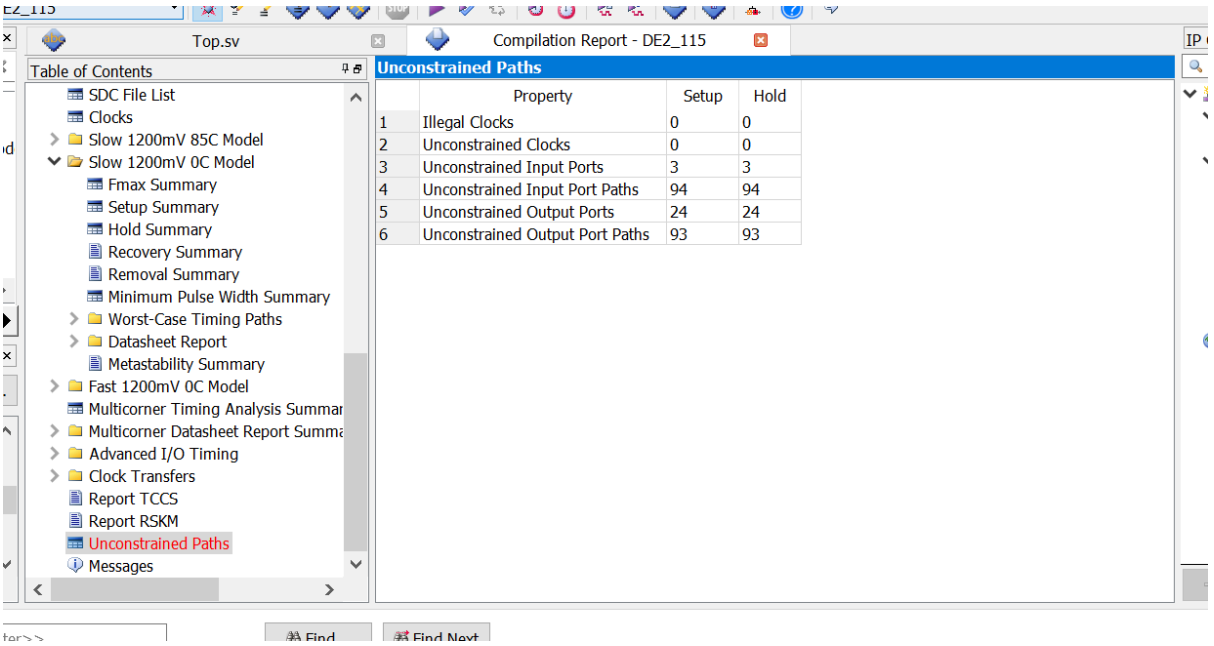
      ii. Record last result

         We update the last result upon entering the next number generating iteration. The history will show on the LED if the button is pressed.

4. Fitter Summary 截圖



5. Timing Analyzer截圖



6. 遇到的問題與解決辦法
    a. 如果 LFSR 出現零的話會無法生成其他數字
    多設一個variable random_seed，random_seed也會做LFSR，他等於0的時候會被賦予一個特定數值，而random_number == 0 的時候會跟random_seed取值，增加隨機性。
    b. 生成的序列感覺不夠隨機
    把random_number開大一點(16 bit)，增加他循環的長度，實際output只取他的最後4位。

7. 心得
    以前寫verilog都只是在電腦上模擬。這是第一次用FPGA，能讓自己的verilog有實際硬體成果很開心。除此之外也有試著寫一點testbench，有成功藉此找到錯誤，好玩!