Team09 Final Report

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1. File Structure

```
└── team09_final/
    ├── team09_final_report.pdf
    ├── team09_final_presentation.pdf
    ├── src/
    │   ├── Sdram_Control/
    │   │   ├── command.v
    │   │   ├── control_interface.v
    │   │   ├── sdr_data_path.v
    │   │   ├── Sdram_Control.v
    │   │   ├── Sdram_Params.h
    │   │   ├── Sdram_RD_FIFO.qip
    │   │   ├── Sdram_RD_FIFO.v
    │   │   ├── Sdram_WR_FIFO.qip
    │   │   └── Sdram_WR_FIFO.v
    │   ├── v/
    │   │   ├── Algorithm/
    │   │   │   ├── moveNum.sv
    │   │   │   ├── moveZero.sv
    │   │   │   ├── solver.sv
    │   │   │   ├── solver.py
    │   │   │   └── gif.py
    │   │   ├── Block_Movement2Motor.sv
    │   │   ├── CCD_Capture.v
    │   │   ├── gray_sort.sv
    │   │   ├── I2C_CCD_Config.v
    │   │   ├── I2C_Controller.v
    │   │   ├── Line_Buffer.bsf
    │   │   ├── Line_Buffer.qip
    │   │   ├── Line_Buffer1.v
    │   │   ├── Motor_Control.sv
    │   │   ├── RAW2RGB.v
    │   │   ├── Read_VGA_RGB.sv
    │   │   ├── Read_VGA.sv
    │   │   ├── Reset_Delay.v
    │   │   ├── RGB_sort.sv
    │   │   ├── sdram_pll.bsf
    │   │   ├── sdram_pll.ppf
    │   │   ├── sdram_pll.qip
    │   │   ├── sdram_pll.v
    │   │   ├── SEG_LUT_8.v
    │   │   ├── SEG_LUT_.v
    │   │   ├── Top_Control.sv
```

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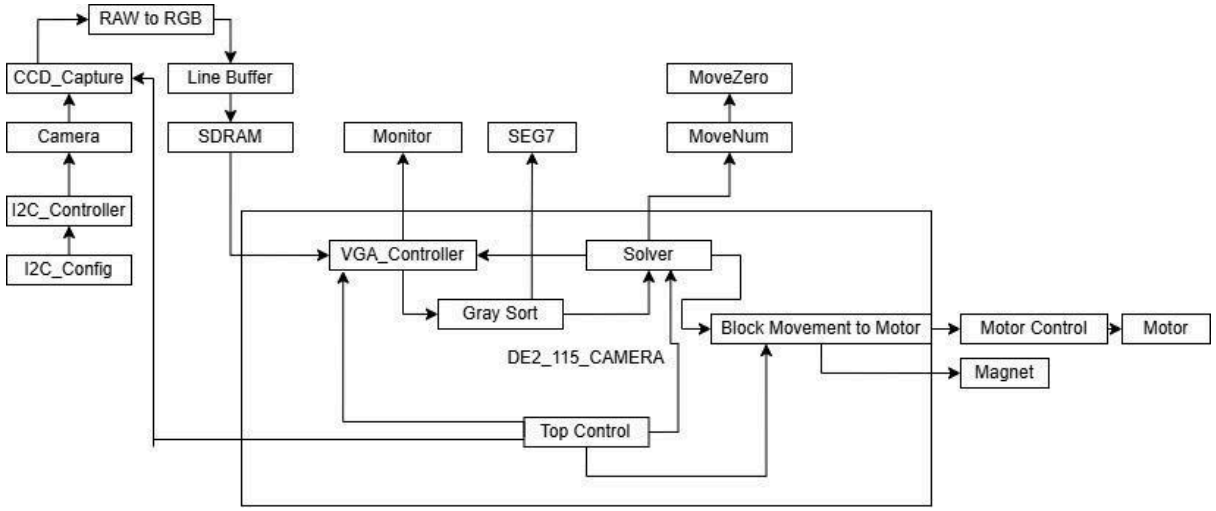
│   │   ├── VGA_Controller_rec.sv
│   │   ├── VGA_Controller.sv
│   │   ├── vga_pll.bsf
│   │   └── vga_pll.ppf
│   ├── DE2_115_CAMERA_assignment_defaults.qdf
│   ├── DE2_115_CAMERA.pin
│   ├── DE2_115_CAMERA.qpf
│   ├── DE2_115_CAMERA.qsf
│   ├── DE2_115_CAMERA.sof
│   ├── DE2_115_CAMERA.sv
│   ├── DE2_115_D5M_VGA.sdc
│   ├── Debounce.sv
│   ├── PLLJ_PLLSPE_INFO.txt
│   └── VGA_param.h
```

2. System Architecture



3. Algorithm
   a. Klotski

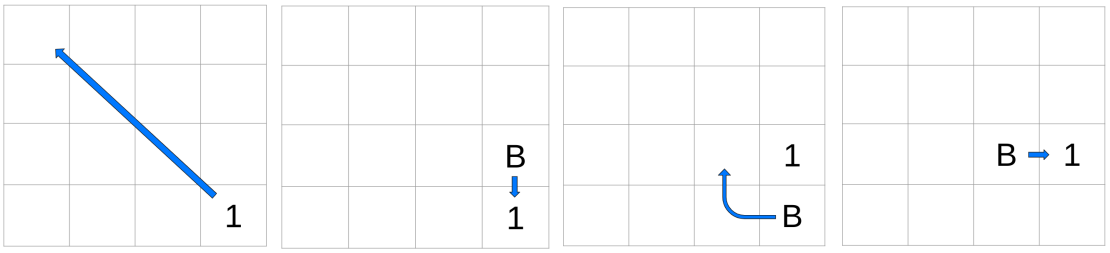
      We use the bottom-up method to solve Klotski. First, we design a module *MoveZero* to move blank to the target position. Then we design a module *MoveNum* to move the target number to the target position by reusing *MoveZero*. Finally, we design the top module *Solver* to solve the Klotski by reusing *MoveNum*.

      i. MoveZero

      The blank has 4 directions to move. To avoid the blank destroying the blocks already sorted, we freeze those blocks to avoid moving them.

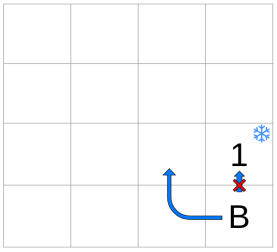
      ii. MoveNum

      Reuse *MoveZero* to move the target number to the target position. Our idea is repeating to put the blank next to the target number and between the number's position and the target position, then switch the blank and the number, until the number arrives at the target position, as shown in the following figure.

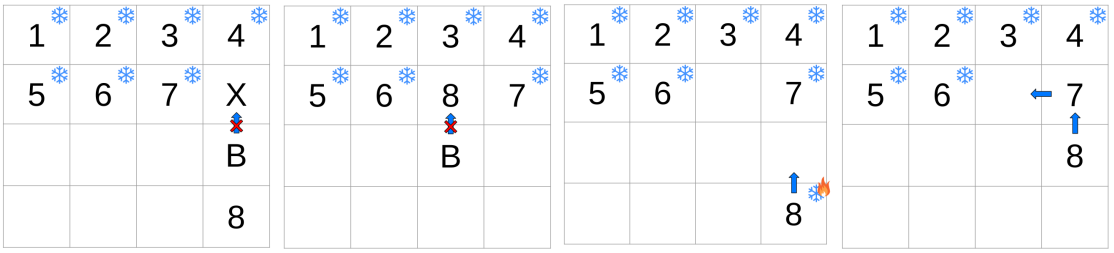


But there exist some issues:

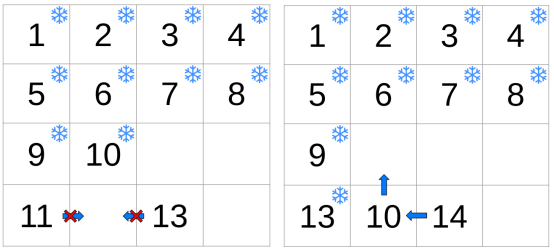
(1) When the blank is moving next to the number, the blank may directly go through the target number. Therefore, we freeze the target number until the blank is next to the number. As shown in below.



(2) Once some numbers are already sorted, other blocks may be hindered. Take the following figure as an example, 8 can not go to its correct position. Therefore, we don't move 7 to its correct position until 8 follows 7. But this yields another issue: 8 may be captured between 5 and 7 unluckily, so we finally decide to move 8 to the lower right corner, then move 7 and 8 to their positions after 8 follows 8.



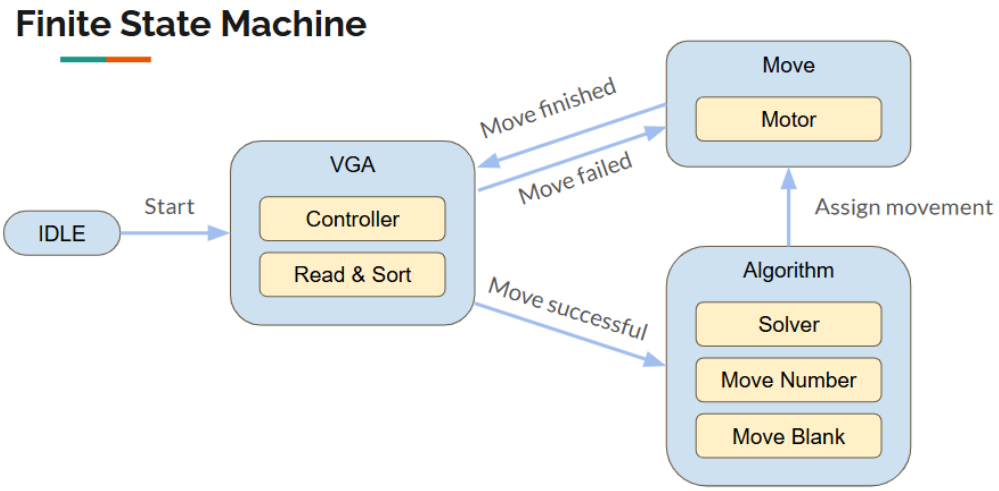
(3) After sorting 1~8, we found that the lower two rows are to narrow to sort the following numbers, so we change to sort columns by columns as follows.



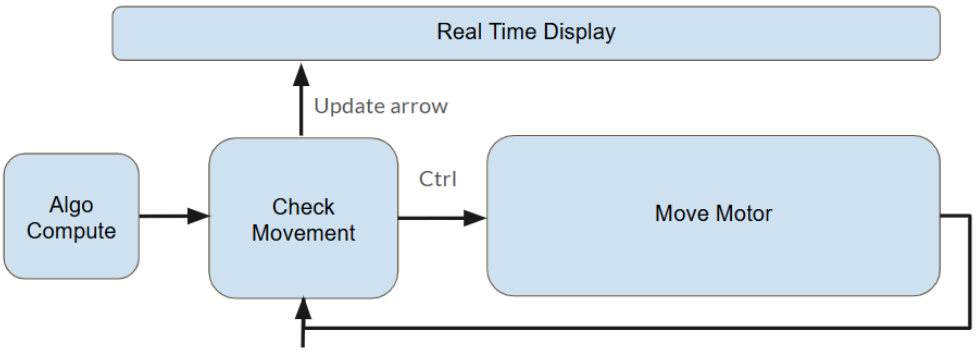
iii. Solver

Solver is the top module of the Klotski algorithm. It reuses the module *MoveNum* to solve the problem.

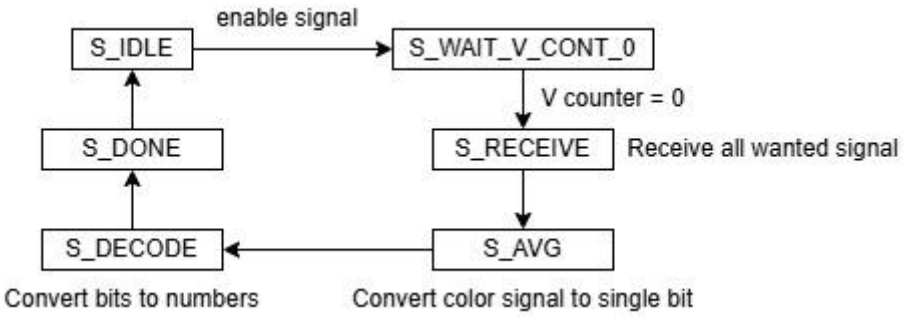
4. Hardware Scheduling
   a. Entire Workflow



b. Time Scheduling

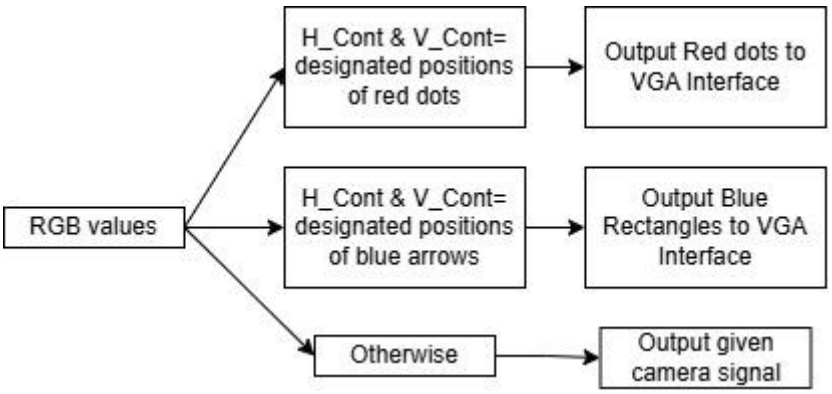


c. Gray Sort



S_IDLE：Wait enable signal from top control unit to start processing RGB values from VGA Controller
S_WAIT_V_CONT_0：Wait V_Cont of VGA to return to 0；otherwise, you'll get wrong averaged RGB values
S_RECEIVE：Start collecting RGB values sent from VGA Controller
VGA Controller
S_AVG：We select green values as our approach of differentiating between black and white by setting a certain threshold. Values above the threshold will be set to one and others will be set to zero.
S_DECODE：Convert 0,1s from the last step to numbers（of the klotski blocks）
S_DONE： Tell the top control unit that it has finished decoding.

d. VGA Controller

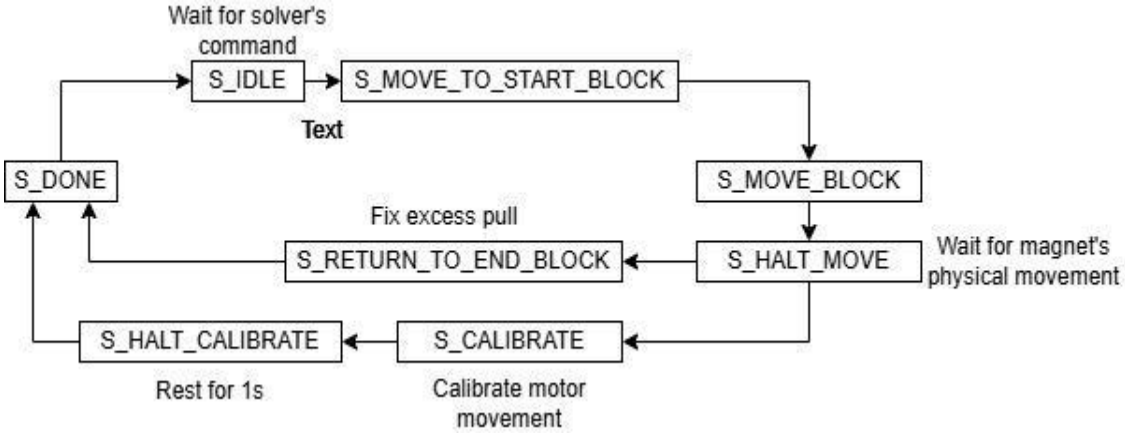


Output RGB values to VGA interface. The values are decided by

i. whether it is a sampling point for later number recognition(red dots)
ii. whether it is on the path of desired moved klotski blocks.

If the above 2 conditions are not met, the controller outputs values received from the camera.

e. Block_Movement2Motor and Relay



S_IDLE: Wait for solver to finish calculation; receive starting block and destination block

S_MOVE_TO_START_BLOCK：Plan a route to the starting block based on the previous few steps. Move the electromagnet to the starting block. Send values to the motor control unit.

S_MOVE_BLOCK: Use the relay (we use the *normal open* mode to connect the electromagnet) to control the electromagnet to move a klotski block. Send values to the motor control unit. The electromagnet is moved excessively to avoid stucking the klotski block in half way.

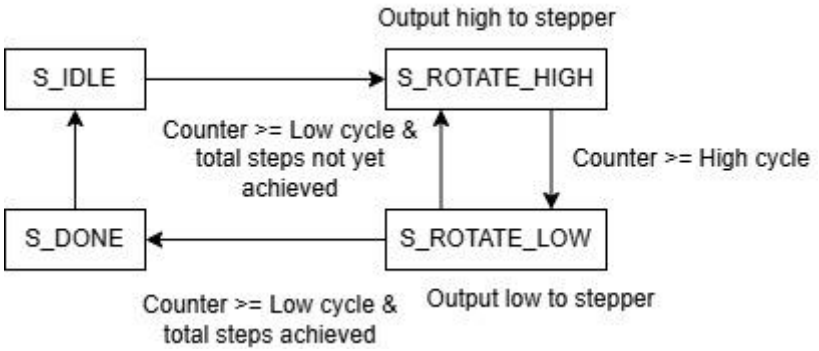
S_HALT_MOVE: Wait for the klotski block's physical movement.

S_RETURN_TO_END_BLOCK: Return to the destination block.

S_CALIBRATE: Return to the starting point of the entire motor control unit to calibrate the non-ideal movements of the motor.

S_HALT_CALIBRATE: Let the motor take a rest.

f. Motor



S_IDLE: Receive movement values from Block_Movement2Motor.
S_ROTATE_HIGH & S_ROTATE_LOW: Send simulated PWM signals to stepper drivers.

5. Fitter Summary

Fitter Summary	
Fitter Status	Successful - Fri Dec 27 20:24:39 2024
Quartus II 64-Bit Version	15.0.0 Build 145 04/22/2015 SJ Full Version
Revision Name	DE2_115_CAMERA
Top-level Entity Name	DE2_115_CAMERA
Family	Cyclone IV E
Device	EP4CE115F29C7
Timing Models	Final
Total logic elements	6,014 / 114,480 (5 %)
Total combinational functions	5,004 / 114,480 (4 %)
Dedicated logic registers	3,209 / 114,480 (3 %)
Total registers	3209
Total pins	433 / 529 (82 %)
Total virtual pins	0
Total memory bits	892,984 / 3,981,312 (22 %)
Embedded Multiplier 9-bit elements	0 / 532 (0 %)
Total PLLs	1 / 4 (25 %)

5. Timing Analyzer

Slow 1200mV 85C Model Recovery Summary			
	Clock	Slack	End Point TNS
1	u6|altpll_component|auto_generated|pll1|clk[4]	-4.191	-4424.968
2	u6|altpll_component|auto_generated|pll1|clk[0]	3.118	0.000
3	CLOCK2_50	13.000	0.000
4	altera_reserved_tck	47.944	0.000

Slow 1200mV 85C Model Recovery: 'u6|altpll_component|auto_generated|pll1|clk[4]'

	Slack	From Node	To Node	Launch Clock	Latch Clock
1	-4.191	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|Motor_Control:x_motor|state_r.S_IDLE	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
2	-4.191	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|Motor_Control:x_motor|cnt_r[8]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
3	-4.191	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|Motor_Control:x_motor|cnt_r[9]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
4	-4.191	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|Motor_Control:x_motor|cnt_r[10]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
5	-4.191	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|Motor_Control:x_motor|cnt_r[11]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
6	-4.191	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|Motor_Control:x_motor|cnt_r[12]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
7	-4.191	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|Motor_Control:x_motor|cnt_r[13]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
8	-4.191	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|Mo..._motor|state_r.S_ROTATE_HIGH	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
9	-4.191	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|Mo...x_motor|state_r.S_ROTATE_LOW	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
10	-4.191	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|Motor_Control:x_motor|cnt_r[19]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
11	-4.191	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|Mot...ontrol:x_motor|state_r.S_DONE	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
12	-4.191	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|Motor_Control:x_motor|step_control_r	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
13	-4.190	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|Motor_Control:x_motor|cnt_r[14]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
14	-4.190	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|Motor_Control:x_motor|cnt_r[17]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
15	-4.190	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|Motor...ontrol:x_motor|total_steps_r[4]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
16	-4.190	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|Motor...ntrol:x_motor|total_steps_r[13]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
17	-4.190	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|Motor...ntrol:x_motor|total_steps_r[14]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
18	-4.190	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|Motor...ntrol:x_motor|total_steps_r[30]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
19	-4.187	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|calibrate_move_x_cnt_r[0]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
20	-4.187	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|calibrate_move_y_cnt_r[0]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
21	-4.187	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|return_to_end_block_y_cnt_r[0]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
22	-4.187	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|finish_calibrate_r	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
23	-4.186	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|finish_move_block_r	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
24	-4.186	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|state_r.S_HALT_MOVE	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
25	-4.186	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|state_r.S_RETURN_TO_END_BLOCK	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]

Slow 1200mV 85C Model Recovery: 'u6|altpll_component|auto_generated|pll1|clk[4]'

	Slack	From Node	To Node	Launch Clock	Latch Clock
25	-4.186	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|state_r.S_RETURN_TO_END_BLOCK	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
26	-4.186	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|current_y_pos_r[2]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
27	-4.186	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|current_y_pos_r[3]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
28	-4.186	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|current_y_pos_r[4]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
29	-4.186	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|current_y_pos_r[6]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
30	-4.186	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|current_y_pos_r[7]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
31	-4.186	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|current_y_pos_r[8]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
32	-4.186	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|current_y_pos_r[9]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
33	-4.186	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|current_y_pos_r[10]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
34	-4.186	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|current_y_pos_r[12]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
35	-4.186	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|current_y_pos_r[31]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
36	-4.186	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|to_motor_y_total_steps_r[1]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
37	-4.186	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|Motor...ontrol:y_motor|total_steps_r[1]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
38	-4.186	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|to_motor_y_total_steps_r[2]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
39	-4.186	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|to_motor_y_total_steps_r[4]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
40	-4.186	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|Motor...ontrol:y_motor|total_steps_r[4]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
41	-4.186	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|to_motor_y_total_steps_r[5]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
42	-4.186	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|to_motor_y_total_steps_r[7]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
43	-4.186	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|Motor...ntrol:y_motor|total_steps_r[14]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
44	-4.186	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|Motor...ntrol:y_motor|total_steps_r[30]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
45	-4.186	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|calibrate_cnt_r[0]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
46	-4.186	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|calibrate_cnt_r[1]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
47	-4.186	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|calibrate_cnt_r[2]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
48	-4.186	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|calibrate_cnt_r[3]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
49	-4.186	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|calibrate_cnt_r[4]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]

Slow 1200mV 85C Model Recovery: 'u6|altpll_component|auto_generated|pll1|clk[4]'

	Slack	From Node	To Node	Launch Clock	Latch Clock
49	-4.186	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|calibrate_cnt_r[4]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
50	-4.186	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|state_r.S_CALIBRATE	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
51	-4.186	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|state_r.S_HALT_CALIBRATE	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
52	-4.186	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|state_r.S_DONE	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
53	-4.186	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|Motor_Control:y_motor|direction_r	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
54	-4.185	Reset_Delay:u2|oRST_2	Solver:solver|klotski_r[0][3][3]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
55	-4.185	Reset_Delay:u2|oRST_2	Top_Control:top_control|klotski_r[2][0][3]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
56	-4.185	Reset_Delay:u2|oRST_2	Solver:solver|klotski_r[1][3][3]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
57	-4.185	Reset_Delay:u2|oRST_2	Solver:solver|MoveNum:moveNum|M...ero:moveZero|klotski_r[1][3][3]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
58	-4.185	Reset_Delay:u2|oRST_2	Read_VGA_Grey:read_vga|block_Red_value_r[4][4][1]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
59	-4.185	Reset_Delay:u2|oRST_2	Read_VGA_Grey:read_vga|block_Red_value_r[4][4][2]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
60	-4.185	Reset_Delay:u2|oRST_2	Read_VGA_Grey:read_vga|block_Red_value_r[4][4][3]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
61	-4.185	Reset_Delay:u2|oRST_2	Read_VGA_Grey:read_vga|block_Red_value_r[4][4][0]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
62	-4.185	Reset_Delay:u2|oRST_2	Solver:solver|MoveNum:moveNum|M...ero:moveZero|klotski_r[1][2][3]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
63	-4.185	Reset_Delay:u2|oRST_2	Solver:solver|MoveNum:moveNum|M...ero:moveZero|klotski_r[3][0][3]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
64	-4.185	Reset_Delay:u2|oRST_2	Read_VGA_Grey:read_vga|block_Red_value_r[4][2][0]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
65	-4.185	Reset_Delay:u2|oRST_2	Solver:solver|MoveNum:moveNum|M...ero:moveZero|klotski_r[1][3][2]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
66	-4.185	Reset_Delay:u2|oRST_2	Solver:solver|MoveNum:moveNum|M...ero:moveZero|klotski_r[1][2][2]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
67	-4.185	Reset_Delay:u2|oRST_2	Solver:solver|MoveNum:moveNum|M...ero:moveZero|klotski_r[3][0][2]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
68	-4.185	Reset_Delay:u2|oRST_2	Top_Control:top_control|klotski_r[1][1][2]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
69	-4.185	Reset_Delay:u2|oRST_2	Solver:solver|klotski_r[0][0][1]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
70	-4.185	Reset_Delay:u2|oRST_2	Solver:solver|MoveNum:moveNum|M...ero:moveZero|klotski_r[3][0][1]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
71	-4.185	Reset_Delay:u2|oRST_2	Solver:solver|MoveNum:moveNum|M...ero:moveZero|klotski_r[1][3][1]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
72	-4.185	Reset_Delay:u2|oRST_2	Solver:solver|MoveNum:moveNum|M...ero:moveZero|klotski_r[1][2][1]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
73	-4.185	Reset_Delay:u2|oRST_2	Top_Control:top_control|klotski_r[1][1][1]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]

Slow 1200mV 85C Model Recovery: 'u6|altpll_component|auto_generated|pll1|clk[4]'

	Slack	From Node	To Node	Launch Clock	Latch Clock
73	-4.185	Reset_Delay:u2|oRST_2	Top_Control:top_control|klotski_r[1][1][1]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
74	-4.185	Reset_Delay:u2|oRST_2	Solver:solver|MoveNum:moveNum|M...ero:moveZero|klotski_r[3][0][0]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
75	-4.185	Reset_Delay:u2|oRST_2	Solver:solver|MoveNum:moveNum|M...ero:moveZero|klotski_r[1][2][0]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
76	-4.185	Reset_Delay:u2|oRST_2	Solver:solver|MoveNum:moveNum|M...ero:moveZero|klotski_r[1][3][0]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
77	-4.185	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|state_r.S_MOVE_TO_START_BLOCK	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
78	-4.185	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|finish_return_to_end_block_r	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
79	-4.185	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|move_to_start_x_cnt_r[0]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
80	-4.185	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|Motor...ontrol:x_motor|total_steps_r[7]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
81	-4.185	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|Motor...ontrol:x_motor|total_steps_r[8]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
82	-4.185	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|Motor...ntrol:x_motor|total_steps_r[12]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
83	-4.185	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|Motor...ontrol:y_motor|total_steps_r[2]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
84	-4.185	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|Motor...ontrol:y_motor|total_steps_r[5]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
85	-4.185	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|Motor...ontrol:y_motor|total_steps_r[6]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
86	-4.185	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|Motor...ontrol:y_motor|total_steps_r[7]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
87	-4.185	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|Motor...ontrol:y_motor|total_steps_r[9]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
88	-4.185	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|Motor...ntrol:y_motor|total_steps_r[10]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
89	-4.185	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|Motor...ntrol:y_motor|total_steps_r[11]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
90	-4.185	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|Motor...ntrol:y_motor|total_steps_r[12]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
91	-4.185	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|Motor...ntrol:y_motor|total_steps_r[13]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
92	-4.185	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|move_to_start_y_cnt_r[0]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
93	-4.185	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|finish_move_to_start_r	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
94	-4.185	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|state_r.S_MOVE_BLOCK	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
95	-4.185	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|halt_calibrate_cnt_r[8]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
96	-4.185	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|halt_calibrate_cnt_r[9]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
97	-4.185	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|halt_calibrate_cnt_r[10]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
98	-4.185	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|halt_calibrate_cnt_r[11]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
99	-4.185	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|halt_calibrate_cnt_r[12]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
100	-4.185	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|halt_calibrate_cnt_r[13]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]

Slow 1200mV 0C Model Recovery Summary

	Clock	Slack	End Point TNS
1	u6|altpll_component|auto_generated|pll1|clk[4]	-3.421	-3545.596
2	u6|altpll_component|auto_generated|pll1|clk[0]	3.901	0.000
3	CLOCK2_50	13.687	0.000
4	altera_reserved_tck	48.249	0.000

Slow 1200mV 0C Model Recovery: 'u6|altpll_component|auto_generated|pll1|clk[4]'

	Slack	From Node	To Node	Launch Clock	Latch Clock
1	-3.421	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|Motor_Control:x_motor|state_r.S_IDLE	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
2	-3.421	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|Motor...ontrol:x_motor|total_steps_r[7]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
3	-3.421	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|Motor...ontrol:x_motor|total_steps_r[8]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
4	-3.421	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|Motor...ntrol:x_motor|total_steps_r[12]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
5	-3.421	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|Mo..._motor|state_r.S_ROTATE_HIGH	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
6	-3.421	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|Mo...x_motor|state_r.S_ROTATE_LOW	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
7	-3.421	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|Motor_Control:x_motor|cnt_r[19]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
8	-3.421	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|Mot...ontrol:x_motor|state_r.S_DONE	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
9	-3.421	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|Motor_Control:x_motor|step_control_r	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
10	-3.420	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|state_r.S_RETURN_TO_END_BLOCK	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
11	-3.420	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|Motor_Control:x_motor|cnt_r[8]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
12	-3.420	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|Motor_Control:x_motor|cnt_r[9]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
13	-3.420	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|Motor_Control:x_motor|cnt_r[10]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
14	-3.420	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|Motor_Control:x_motor|cnt_r[11]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
15	-3.420	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|Motor_Control:x_motor|cnt_r[12]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
16	-3.420	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|Motor_Control:x_motor|cnt_r[13]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
17	-3.420	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|Motor_Control:x_motor|cnt_r[14]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
18	-3.420	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|Motor_Control:x_motor|cnt_r[17]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
19	-3.420	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|Motor...ontrol:x_motor|total_steps_r[4]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
20	-3.420	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|Motor...ntrol:x_motor|total_steps_r[13]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
21	-3.420	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|Motor...ntrol:x_motor|total_steps_r[14]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
22	-3.420	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|Motor...ntrol:x_motor|total_steps_r[30]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
23	-3.420	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|current_y_pos_r[2]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
24	-3.420	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|current_y_pos_r[3]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
25	-3.420	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|current_y_pos_r[4]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]

Slow 1200mV 0C Model Recovery: 'u6|altpll_component|auto_generated|pll1|clk[4]'

	Slack	From Node	To Node	Launch Clock	Latch Clock
25	-3.420	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|current_y_pos_r[4]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
26	-3.420	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|current_y_pos_r[6]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
27	-3.420	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|current_y_pos_r[7]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
28	-3.420	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|current_y_pos_r[8]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
29	-3.420	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|current_y_pos_r[9]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
30	-3.420	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|current_y_pos_r[10]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
31	-3.420	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|current_y_pos_r[12]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
32	-3.420	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|state_r.S_CALIBRATE	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
33	-3.420	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|state_r.S_HALT_CALIBRATE	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
34	-3.420	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|state_r.S_DONE	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
35	-3.419	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|calibrate_move_x_cnt_r[0]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
36	-3.419	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|current_y_pos_r[31]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
37	-3.419	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|calibrate_move_y_cnt_r[0]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
38	-3.419	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|to_motor_y_total_steps_r[1]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
39	-3.419	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|to_motor_y_total_steps_r[2]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
40	-3.419	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|to_motor_y_total_steps_r[4]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
41	-3.419	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|to_motor_y_total_steps_r[5]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
42	-3.419	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|to_motor_y_total_steps_r[7]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
43	-3.419	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|return_to_end_block_y_cnt_r[0]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
44	-3.419	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|finish_calibrate_r	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
45	-3.418	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|Motor...ontrol:y_motor|total_steps_r[1]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
46	-3.418	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|Motor...ontrol:y_motor|total_steps_r[4]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
47	-3.418	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|Motor...ntrol:y_motor|total_steps_r[14]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
48	-3.418	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|Motor...ntrol:y_motor|total_steps_r[30]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
49	-3.418	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|Motor_Control:y_motor|direction_r	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]

Slow 1200mV 0C Model Recovery: 'u6|altpll_component|auto_generated|pll1|clk[4]'

	Slack	From Node	To Node	Launch Clock	Latch Clock
49	-3.418	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|Motor_Control:y_motor|direction_r	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
50	-3.417	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|finish_move_block_r	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
51	-3.417	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|state_r.S_HALT_MOVE	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
52	-3.417	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|state_r.S_MOVE_BLOCK	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
53	-3.417	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|calibrate_cnt_r[0]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
54	-3.417	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|calibrate_cnt_r[1]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
55	-3.417	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|calibrate_cnt_r[2]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
56	-3.417	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|calibrate_cnt_r[3]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
57	-3.417	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|calibrate_cnt_r[4]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
58	-3.417	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|magnet_r	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
59	-3.416	Reset_Delay:u2|oRST_2	Read_VGA_Grey:read_vga|block_Red_value_r[5][7][1]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
60	-3.416	Reset_Delay:u2|oRST_2	Read_VGA_Grey:read_vga|block_Red_value_r[5][7][2]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
61	-3.416	Reset_Delay:u2|oRST_2	Read_VGA_Grey:read_vga|block_Red_value_r[5][7][3]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
62	-3.416	Reset_Delay:u2|oRST_2	Top_Control:top_control|klotski_r[0][2][0]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
63	-3.416	Reset_Delay:u2|oRST_2	Top_Control:top_control|klotski_r[2][0][3]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
64	-3.416	Reset_Delay:u2|oRST_2	Read_VGA_Grey:read_vga|block_Red_value_r[2][2][2]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
65	-3.416	Reset_Delay:u2|oRST_2	Read_VGA_Grey:read_vga|block_Red_value_r[2][2][1]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
66	-3.416	Reset_Delay:u2|oRST_2	Read_VGA_Grey:read_vga|block_Red_value_r[2][2][3]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
67	-3.416	Reset_Delay:u2|oRST_2	Top_Control:top_control|klotski_r[1][1][3]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
68	-3.416	Reset_Delay:u2|oRST_2	Solver:solver|MoveNum:moveNum|M...ero:moveZero|klotski_r[1][2][3]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
69	-3.416	Reset_Delay:u2|oRST_2	Solver:solver|MoveNum:moveNum|M...ero:moveZero|klotski_r[3][0][3]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
70	-3.416	Reset_Delay:u2|oRST_2	Read_VGA_Grey:read_vga|block_Red_value_r[4][1][1]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
71	-3.416	Reset_Delay:u2|oRST_2	Read_VGA_Grey:read_vga|block_Red_value_r[4][1][2]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
72	-3.416	Reset_Delay:u2|oRST_2	Read_VGA_Grey:read_vga|block_Red_value_r[4][1][3]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
73	-3.416	Reset_Delay:u2|oRST_2	Read_VGA_Grey:read_vga|block_Red_value_r[4][1][0]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]

Slow 1200mV 0C Model Recovery: 'u6|altpll_component|auto_generated|pll1|clk[4]'

	Slack	From Node	To Node	Launch Clock	Latch Clock
73	-3.416	Reset_Delay:u2|oRST_2	Read_VGA_Grey:read_vga|block_Red_value_r[4][1][0]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
74	-3.416	Reset_Delay:u2|oRST_2	Read_VGA_Grey:read_vga|block_Red_value_r[2][1][1]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
75	-3.416	Reset_Delay:u2|oRST_2	Read_VGA_Grey:read_vga|block_Red_value_r[2][1][2]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
76	-3.416	Reset_Delay:u2|oRST_2	Read_VGA_Grey:read_vga|block_Red_value_r[4][2][0]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
77	-3.416	Reset_Delay:u2|oRST_2	Read_VGA_Grey:read_vga|block_Red_value_r[2][1][3]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
78	-3.416	Reset_Delay:u2|oRST_2	Read_VGA_Grey:read_vga|block_Red_value_r[2][1][0]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
79	-3.416	Reset_Delay:u2|oRST_2	Solver:solver|MoveNum:moveNum|M...ero:moveZero|klotski_r[1][2][2]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
80	-3.416	Reset_Delay:u2|oRST_2	Solver:solver|MoveNum:moveNum|M...ero:moveZero|klotski_r[3][0][2]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
81	-3.416	Reset_Delay:u2|oRST_2	Top_Control:top_control|klotski_r[1][1][2]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
82	-3.416	Reset_Delay:u2|oRST_2	Top_Control:top_control|klotski_r[1][2][2]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
83	-3.416	Reset_Delay:u2|oRST_2	Top_Control:top_control|klotski_r[3][3][1]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
84	-3.416	Reset_Delay:u2|oRST_2	Top_Control:top_control|klotski_r[1][3][1]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
85	-3.416	Reset_Delay:u2|oRST_2	Solver:solver|MoveNum:moveNum|M...ero:moveZero|klotski_r[3][0][1]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
86	-3.416	Reset_Delay:u2|oRST_2	Solver:solver|MoveNum:moveNum|M...ero:moveZero|klotski_r[1][2][1]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
87	-3.416	Reset_Delay:u2|oRST_2	Top_Control:top_control|klotski_r[0][1][1]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
88	-3.416	Reset_Delay:u2|oRST_2	Top_Control:top_control|klotski_r[1][1][1]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
89	-3.416	Reset_Delay:u2|oRST_2	Solver:solver|MoveNum:moveNum|M...ero:moveZero|klotski_r[3][0][0]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
90	-3.416	Reset_Delay:u2|oRST_2	Top_Control:top_control|klotski_r[1][2][0]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
91	-3.416	Reset_Delay:u2|oRST_2	Top_Control:top_control|klotski_r[2][2][0]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
92	-3.416	Reset_Delay:u2|oRST_2	Solver:solver|MoveNum:moveNum|M...ero:moveZero|klotski_r[1][2][0]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
93	-3.416	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|state_r.S_MOVE_TO_START_BLOCK	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
94	-3.416	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|halt_move_cnt_r[1]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
95	-3.416	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|halt_move_cnt_r[2]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
96	-3.416	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|halt_move_cnt_r[3]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
97	-3.416	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|halt_move_cnt_r[4]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]

98	-3.416	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|halt_move_cnt_r[5]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
99	-3.416	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|halt_move_cnt_r[6]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
100	-3.416	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|halt_move_cnt_r[7]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]

Fast 1200mV 0C Model Recovery Summary

	Clock	Slack	End Point TNS
1	u6|altpll_component|auto_generated|pll1|clk[4]	-1.129	-1092.872
2	u6|altpll_component|auto_generated|pll1|clk[0]	6.278	0.000
3	CLOCK2_50	16.319	0.000
4	altera_reserved_tck	49.289	0.000

Fast 1200mV 0C Model Recovery: 'u6|altpll_component|auto_generated|pll1|clk[4]'

	Slack	From Node	To Node	Launch Clock	Latch Clock
1	-1.129	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|Motor_Control:x_motor|state_r.S_IDLE	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
2	-1.129	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|Motor_Control:x_motor|cnt_r[8]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
3	-1.129	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|Motor_Control:x_motor|cnt_r[9]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
4	-1.129	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|Motor_Control:x_motor|cnt_r[10]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
5	-1.129	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|Motor_Control:x_motor|cnt_r[11]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
6	-1.129	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|Motor_Control:x_motor|cnt_r[12]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
7	-1.129	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|Motor_Control:x_motor|cnt_r[13]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
8	-1.129	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|Motor_Control:x_motor|cnt_r[14]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
9	-1.129	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|Motor_Control:x_motor|cnt_r[17]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
10	-1.129	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|Motor...ontrol:x_motor|total_steps_r[4]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
11	-1.129	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|Motor...ntrol:x_motor|total_steps_r[13]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
12	-1.129	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|Motor...ntrol:x_motor|total_steps_r[14]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
13	-1.129	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|Motor...ntrol:x_motor|total_steps_r[30]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
14	-1.129	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|Mo..._motor|state_r.S_ROTATE_HIGH	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
15	-1.129	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|Mo...x_motor|state_r.S_ROTATE_LOW	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
16	-1.129	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|Motor_Control:x_motor|cnt_r[19]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
17	-1.129	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|Mot...ontrol:x_motor|state_r.S_DONE	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
18	-1.129	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|Motor_Control:x_motor|step_control_r	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
19	-1.128	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|state_r.S_RETURN_TO_END_BLOCK	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
20	-1.128	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|Motor...ontrol:x_motor|total_steps_r[7]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
21	-1.128	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|Motor...ontrol:x_motor|total_steps_r[8]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
22	-1.128	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|Motor...ntrol:x_motor|total_steps_r[12]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
23	-1.128	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|current_y_pos_r[2]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
24	-1.128	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|current_y_pos_r[3]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
25	-1.128	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|current_y_pos_r[4]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]

Fast 1200mV 0C Model Recovery: 'u6|altpll_component|auto_generated|pll1|clk[4]'

	Slack	From Node	To Node	Launch Clock	Latch Clock
25	-1.128	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|current_y_pos_r[4]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
26	-1.128	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|current_y_pos_r[6]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
27	-1.128	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|current_y_pos_r[7]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
28	-1.128	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|current_y_pos_r[8]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
29	-1.128	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|current_y_pos_r[9]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
30	-1.128	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|current_y_pos_r[10]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
31	-1.128	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|current_y_pos_r[12]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
32	-1.128	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|state_r.S_CALIBRATE	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
33	-1.128	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|state_r.S_HALT_CALIBRATE	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
34	-1.128	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|state_r.S_DONE	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
35	-1.127	Reset_Delay:u2|oRST_2	Read_VGA_Grey:read_vga|block_Red_value_r[5][7][1]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
36	-1.127	Reset_Delay:u2|oRST_2	Read_VGA_Grey:read_vga|block_Red_value_r[5][7][2]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
37	-1.127	Reset_Delay:u2|oRST_2	Read_VGA_Grey:read_vga|block_Red_value_r[5][7][3]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
38	-1.127	Reset_Delay:u2|oRST_2	Read_VGA_Grey:read_vga|block_Red_value_r[2][1][1]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
39	-1.127	Reset_Delay:u2|oRST_2	Read_VGA_Grey:read_vga|block_Red_value_r[2][1][2]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
40	-1.127	Reset_Delay:u2|oRST_2	Read_VGA_Grey:read_vga|block_Red_value_r[2][1][3]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
41	-1.127	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|state_r.S_MOVE_TO_START_BLOCK	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
42	-1.127	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|halt_move_cnt_r[1]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
43	-1.127	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|halt_move_cnt_r[2]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
44	-1.127	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|halt_move_cnt_r[3]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
45	-1.127	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|halt_move_cnt_r[4]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
46	-1.127	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|halt_move_cnt_r[5]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
47	-1.127	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|halt_move_cnt_r[6]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
48	-1.127	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|halt_move_cnt_r[7]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
49	-1.127	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|halt_move_cnt_r[8]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]

Fast 1200mV 0C Model Recovery: 'u6|altpll_component|auto_generated|pll1|clk[4]'

	Slack	From Node	To Node	Launch Clock	Latch Clock
49	-1.127	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|halt_move_cnt_r[8]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
50	-1.127	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|halt_move_cnt_r[9]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
51	-1.127	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|halt_move_cnt_r[10]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
52	-1.127	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|halt_move_cnt_r[11]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
53	-1.127	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|halt_move_cnt_r[12]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
54	-1.127	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|halt_move_cnt_r[13]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
55	-1.127	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|halt_move_cnt_r[14]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
56	-1.127	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|halt_move_cnt_r[15]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
57	-1.127	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|finish_move_block_r	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
58	-1.127	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|state_r.S_HALT_MOVE	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
59	-1.127	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|finish_return_to_end_block_r	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
60	-1.127	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|calibrate_move_x_cnt_r[0]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
61	-1.127	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|move_to_start_x_cnt_r[0]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
62	-1.127	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|current_y_pos_r[31]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
63	-1.127	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|calibrate_move_y_cnt_r[0]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
64	-1.127	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|to_motor_y_total_steps_r[1]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
65	-1.127	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|Motor...ontrol:y_motor|total_steps_r[1]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
66	-1.127	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|to_motor_y_total_steps_r[2]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
67	-1.127	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|Motor...ontrol:y_motor|total_steps_r[2]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
68	-1.127	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|to_motor_y_total_steps_r[4]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
69	-1.127	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|Motor...ontrol:y_motor|total_steps_r[4]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
70	-1.127	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|to_motor_y_total_steps_r[5]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
71	-1.127	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|Motor...ontrol:y_motor|total_steps_r[5]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
72	-1.127	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|Motor...ontrol:y_motor|total_steps_r[6]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
73	-1.127	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|to_motor_y_total_steps_r[7]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]

Fast 1200mV 0C Model Recovery: 'u6|altpll_component|auto_generated|pll1|clk[4]'

	Slack	From Node	To Node	Launch Clock	Latch Clock
73	-1.127	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|to_motor_y_total_steps_r[7]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
74	-1.127	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|Motor...ontrol:y_motor|total_steps_r[7]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
75	-1.127	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|Motor...ontrol:y_motor|total_steps_r[9]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
76	-1.127	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|Motor...ntrol:y_motor|total_steps_r[10]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
77	-1.127	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|Motor...ntrol:y_motor|total_steps_r[11]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
78	-1.127	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|Motor...ntrol:y_motor|total_steps_r[12]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
79	-1.127	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|Motor...ntrol:y_motor|total_steps_r[13]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
80	-1.127	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|Motor...ntrol:y_motor|total_steps_r[14]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
81	-1.127	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|Motor...ntrol:y_motor|total_steps_r[30]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
82	-1.127	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|return_to_end_block_y_cnt_r[0]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
83	-1.127	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|move_to_start_y_cnt_r[0]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
84	-1.127	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|finish_move_to_start_r	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
85	-1.127	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|calibrate_cnt_r[0]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
86	-1.127	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|calibrate_cnt_r[1]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
87	-1.127	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|calibrate_cnt_r[2]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
88	-1.127	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|calibrate_cnt_r[3]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
89	-1.127	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|calibrate_cnt_r[4]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
90	-1.127	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|finish_calibrate_r	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
91	-1.127	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|halt_calibrate_cnt_r[8]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
92	-1.127	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|halt_calibrate_cnt_r[9]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
93	-1.127	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|halt_calibrate_cnt_r[10]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
94	-1.127	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|halt_calibrate_cnt_r[11]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
95	-1.127	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|halt_calibrate_cnt_r[12]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
96	-1.127	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|halt_calibrate_cnt_r[13]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
97	-1.127	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|halt_calibrate_cnt_r[14]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
98	-1.127	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|halt_calibrate_cnt_r[15]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
99	-1.127	Reset_Delay:u2|oRST_2	Block_Movement2Motor:bm2m|Motor_Control:y_motor|direction_r	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]
100	-1.126	Reset_Delay:u2|oRST_2	Solver:solver|MoveNum:moveNum|M...ero:moveZero|klotski_r[3][1][0]	CLOCK2_50	u6|altpll_component|auto_generated|pll1|clk[4]

Multicorner Timing Analysis Summary

	Clock	Setup	Hold	Recovery	Removal	Minimum Pulse Width
1	Worst-case Slack	1.540	0.149	-4.191	0.488	4.685
1	CLOCK2_50	14.438	0.181	13.000	1.173	9.271
2	CLOCK3_50	N/A	N/A	N/A	N/A	16.000
3	CLOCK_50	N/A	N/A	N/A	N/A	16.000
4	altera_reserved_tck	43.247	0.162	47.944	0.488	49.283
5	u6|altpll_component|auto_generated|pll1|clk[0]	1.540	0.149	3.118	2.718	4.685
6	u6|altpll_component|auto_generated|pll1|clk[4]	7.716	0.168	-4.191	2.702	12.185
2	Design-wide TNS	0.0	0.0	-4424.968	0.0	0.0
1	CLOCK2_50	0.000	0.000	0.000	0.000	0.000
2	CLOCK3_50	N/A	N/A	N/A	N/A	0.000
3	CLOCK_50	N/A	N/A	N/A	N/A	0.000
4	altera_reserved_tck	0.000	0.000	0.000	0.000	0.000
5	u6|altpll_component|auto_generated|pll1|clk[0]	0.000	0.000	0.000	0.000	0.000
6	u6|altpll_component|auto_generated|pll1|clk[4]	0.000	0.000	-4424.968	0.000	0.000

Unconstrained Paths

	Property	Setup	Hold
1	Illegal Clocks	0	0
2	Unconstrained Clocks	3	3
3	Unconstrained Input Ports	65	65
4	Unconstrained Input Port Paths	410	410
5	Unconstrained Output Ports	136	136
6	Unconstrained Output Port Paths	1190	1190

6. Problems Encountered and Solutions
   a. Color Recognition
      i. Problem: RGB values are highly affected by ambient lighting.
      Solution: Use relative RGB values for comparison and parallelize the sorting process. Implement bitonic sorting, which requires only 10 cycles to sort 16 values. By sharing hardware, only six distinct stages are needed. This allows simultaneous sorting of the RGB channels or a pipelined approach where different colors are sorted one cycle apart, using the same hardware.

      ii. Problem: Sorting relative RGB values is still significantly affected by lighting.
      Solution: Use binary-coded block colors by dividing the blocks into four quadrants painted black and white, making color recognition more definitive.

      iii. Problem: Ambient brightness affects black-and-white binary recognition.
      Solution: Dynamically adjust the camera's exposure time.

      iv. Problem: Using red values for black-and-white segmentation is unstable.
      Solution: Since the TRDB-D5M camera employs a Bayer pattern to mimic human photoreceptor sensitivity, it is more responsive to green. Thus, green values are used for recognition. Four points within the same block are averaged, and if the average exceeds a threshold, the block is identified as white. This method uses shifting and adding to reduce the number of required register bits.

   b. Klotski Movement
      i. Problem: Klotski blocks occasionally fail to move smoothly, causing incorrect block movements.
      Solution: Use the camera for real-time block position recognition. Coordinate the top control unit with the algorithm, camera, and motor path calculation modules to compensate for any failed block movements.

   c. Motor, Relay, and Camera Setup
      i. Problem: Camera image distortion occurs when connected to the FPGA GPIO via long wires.
      Solution: Change the FPGA placement to shorten the connection length.

ii. Problem: Residual magnetism in electromagnets after power-off affects previously moved Klotski blocks during movement.
Solution: Plan the electromagnet's movement path to avoid previously moved empty spaces.

iii. Problem: Motor vibrations or abnormal operations.
Solution: Adjust the motor reference voltage and replace the driver module wires with more stable multi-core wires.

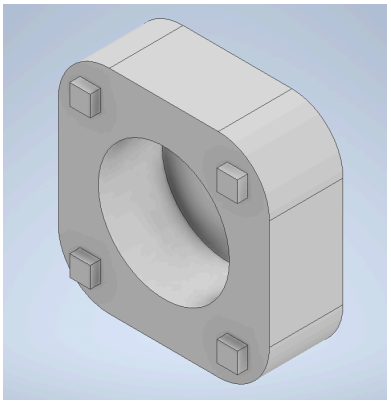
iv. Problem: Relay fails to switch properly.
Solution: Ensure the relay's driving voltage matches its signal voltage to enable proper switching.

v. Problem: Prolonged Klotski solving causes the driver module to overheat.
Solution: Use external physical cooling methods.

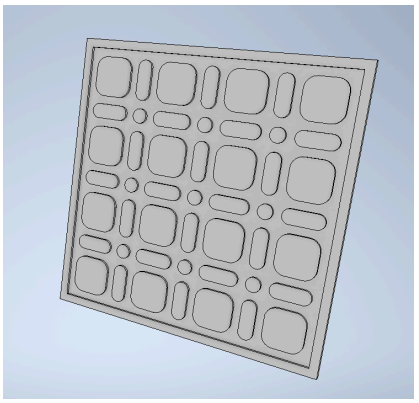
vi. Problem: Excessive resistance in the slider track.
Solution: Use eccentric nuts to adjust the distance between the rollers.

d. Klotski方塊與移動平面設計
   i. Problem: Cubes are prone to rotate while moving
   Solution: Add rails to the plate and make the cubes move along the rail

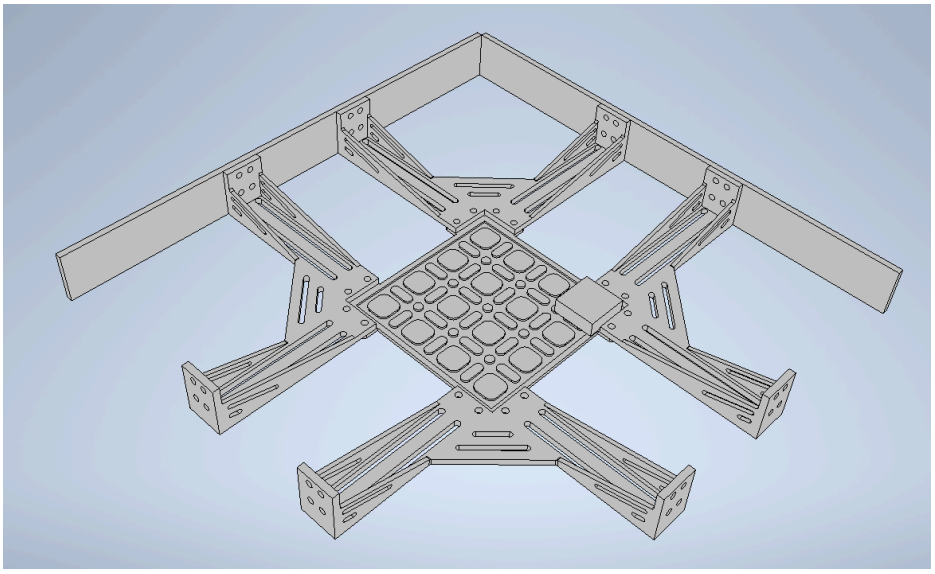
   ii. Cubes are easily stuck with each other
   Solution: Round the corners and rails



Cad illustration of a cube



Cad illustration of the rail



Cad illustration of the support Structure

7. 心得

我們覺得這個題目比原本想像中的難，從方塊移動、辨識顏色、馬達移動、到最後的移動監測，每個步驟都需要注意很多細節。我們覺得最難的地方是這整個系統沒有人為操作，所以我們要設計讓他能夠自我監測，並做出調整。每次按下按鈕後都要開始祈禱，我們甚至在吃飯時看到旁邊的月曆寫著12/27宜祭祀，所以我們 demo 當天早上就去買了一包乖乖，最後 demo 時也超級順利。真的超級謝謝隊友們的合作！！