NEC

MOS INTEGRATED CIRCUIT

μPD4990A

SERIAL I/O CALENDAR & CLOCK
CMOS LSI

The μPD4990A is a CMOS LSI developed to input/output calendar & clock data serially to/from the micro computer.

The crystal frequency is 32.768 kHz and the data items included are time, minute, second, year, month, day, and week.

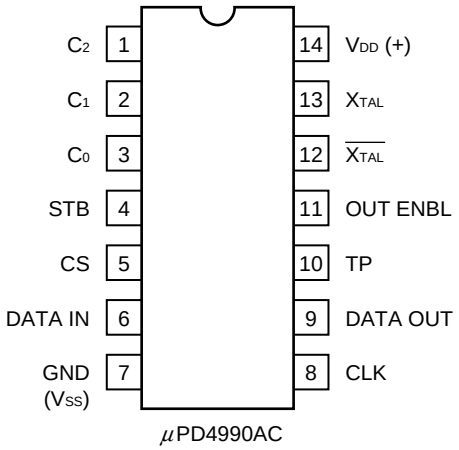
FEATURES

- Built-in counters for time (hour, minute, and second) and date (year, month, day, and week)
- Leap years are adjusted automatically.
- Data is represented in BCD notation (except months in hexadecimal notation) and input/output serially.
- Commands can be set by inputting serial data.
- Selective timing pulses (TPs) are 64 Hz, 256 Hz, 2 048 Hz, and 4 096 Hz and selective output intervals are 1, 10, 30, and 60 seconds.

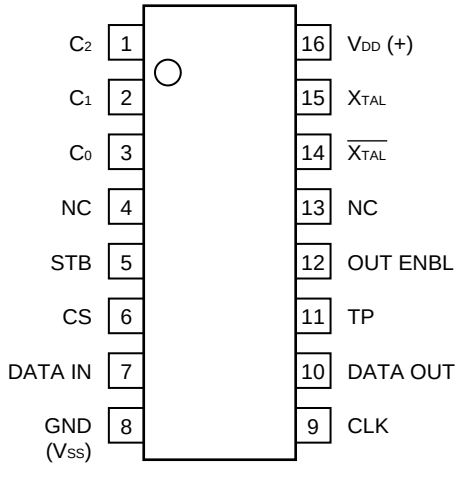
ORDERING INFORMATION

PART No.	PACKAGE
μPD4990AC	14-pin plastic DIP (300 mil)
μPD4990AG	16-pin plastic SOP (300 mil)

CONNECTION DIAGRAM (Top View)



μPD4990AC



μPD4990AG

NC: NO CONNECTION

Document No. IC-1755 (1st edition)
Date Published March 1997 P
Printed in Japan

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	$V_{DD} - V_{SS}$	–0.5 to 7.0	V
Input Voltage	V_{IN}	V_{SS} –0.3 to V_{DD} +0.3	V
Operating Temperature Range	T_{opt}	–40 to +85	°C
Storage Temperature Range	T_{stg}	–65 to +125	°C
Output Terminal Voltage	V_{OUT}	–0.5 to 7.0	V

ELECTRICAL CHARACTERISTICS (f = 32.768 kHz, $C_G = C_D$ = 20 pF, C_I = 20 kΩ, T_a = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Operating Voltage	$V_{DD} - V_{SS}$	2.00		5.50	V	
Current Consumption	I_{DD}		8	20	μA	$V_{DD} - V_{SS}$ = 3.60 V
				100	μA	$V_{DD} - V_{SS}$ = 5.50 V
Low Level Output Voltage	V_{OL}			0.4*	V	$V_{DD} - V_{SS}$ = 2.0 to 5.5 V I_{OL} = 500 μA
CLK Input Frequency	f_{CLK}	DC		500	kHz	$V_{DD} - V_{SS}$ = 2.0 V, Duty 50 %
Input Leakage Current	I_{IN}			±1	μA	$V_{DD} - V_{SS}$ = 5.50 V
High Level Input Voltage	V_{IH}	0.7 V_{DD}		V_{DD}	V	
Low Level Input Voltage	V_{IL}	V_{SS}		0.3 V_{DD}	V	

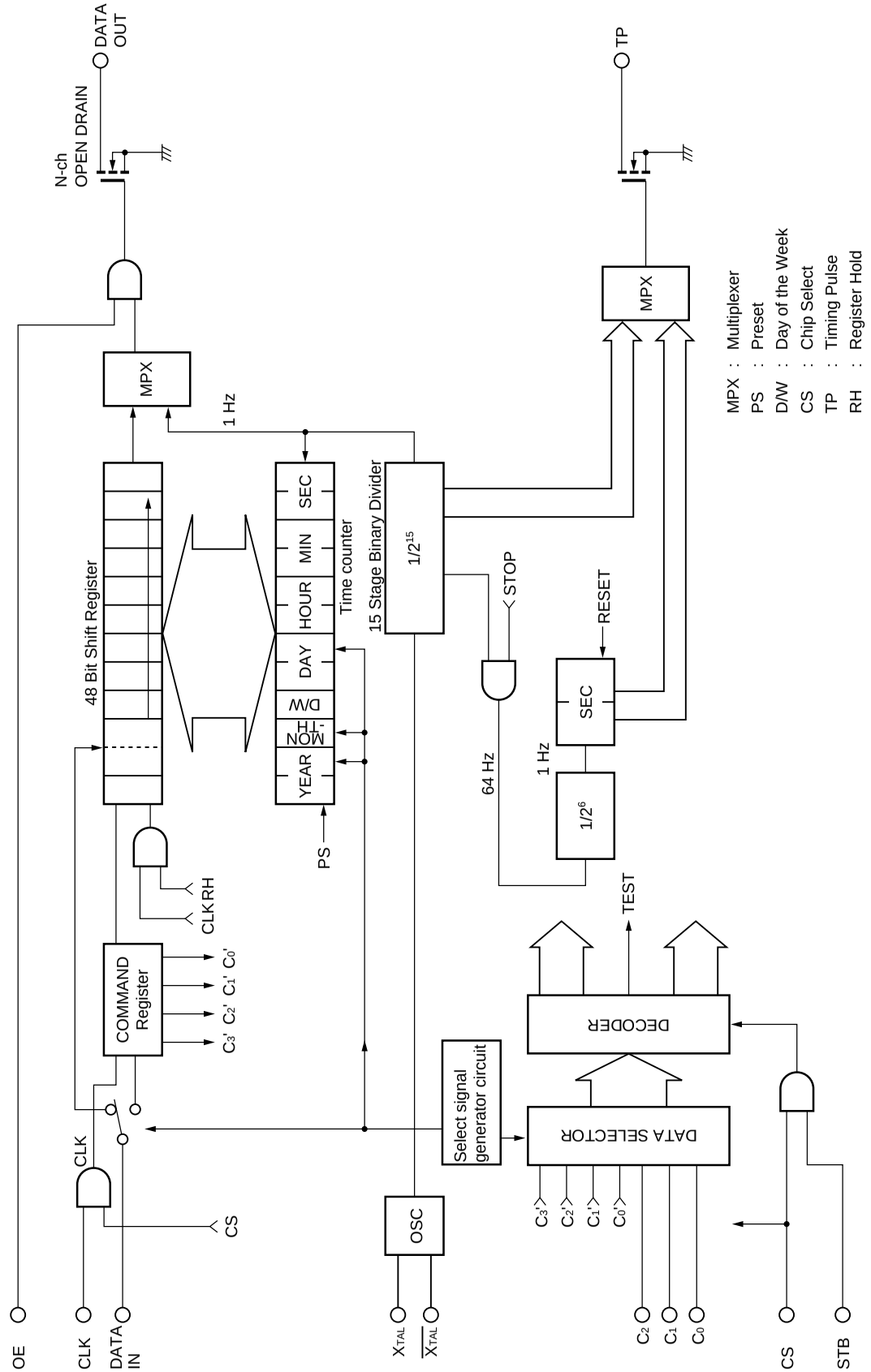
* TP and DATA OUT are N-channel open drain output.

A.C. ELECTRICAL CHARACTERISTICS (f = 32.768 kHz, $V_{DD} - V_{SS}$ = 2.0 V, T_a = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
$C_{0\ to\ 2}$, CS – STB Set-up Time	t_{SU}	1			μs	
STB Pulse Width	t_{STB}	1			μs	
$C_{0\ to\ 2}$, CS – STB Hold Time	t_{HLD}	1			μs	
STB LATCH Delay Time	t_{d1}			1**	μs	except Time Read mode
CLK-DATA OUT Delay time	$t_{d(c-o)}$			1	μs	R_L = 33 kΩ, C_L = 15 pF
DATA IN Set-up Time	t_{DSU}	1			μs	
DATA IN Hold Time	t_{DHLD}	1			μs	

** **Note:** When a function mode is Time Read mode (other than Test mode), STB LATCH delay time is 20 μs MAX. (t_{d2}).

BLOCK DIAGRAM



FUNCTION SPECIFICATIONS

- Crystal frequency (X tal osc.).
  - 32.768 kHz

- Data

  Data types are: second, minute, day, week, month, and year.
  Leap years, 31-day months, and months with 30 or less days are adjusted automatically.
  A 24-hour system is used and last two digits of Gregorian year are indicated.
  It is assumed that leap years are expressed by multiples of 4.

- Data format

  Data is represented in BCD notation. Only months are represented in hexadecimal notation.

- Data input-output and Clock

  Data is input/output synchronously with reference to the external clocks input from the CLK pin using the serial input/output system. (See Fig. 1.)

- Timing pulse output

  Three frequencies, 64 Hz, 256 Hz, and 2 048 Hz, can be set with C_0, C_1 and C_2 pins.
  Using serial data input command, selective timing pulses (TPs) are 64 Hz, 256 Hz, 2 048 Hz, and 4 096 Hz and selective output intervals are 1, 10, 30, and 60 seconds.

- Function mode selection

  A function mode can be selected by the inputs from C_0, C_1, and C_2. Also a function mode can be selected through serial data input. ($C_0 = C_1 = C_2 = V_{DD}$)
  Each command is latched with STB (strobe).

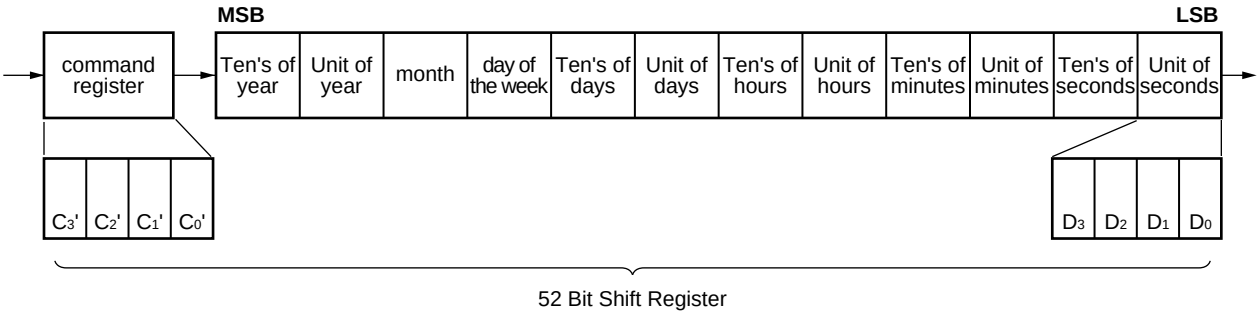
- Chip select

  Connecting the CS pin to the ground level inhibits CLK and STB inputs.

- Data output inhibition

  Connecting the OUT ENBL pin to the ground level sets the DATA OUT pin at high impedance.

Figure 1.



* DATA of 52 Bit Shift Register appears on DATA OUT terminal from LSB of second.

TERMINALS

- Input terminals
  - DATA IN — Data input of 40-/52-bit shift register
  - CLK — Shift clock input of 40-/52-bit shift register
  - C_0, C_1, C_2 — Command input (3 bit)
  - STB — Strobe input
  - CS — Chip select input (Prohibits CLK & STB)
  - OUT ENBL — Output control input (Makes the DATA OUT high impedance by inputting low level).

- Output terminals (N-channel Open Drain)
  - DATA OUT — Data output of 40-/52-bit shift register
  - TP — Timing pulse output

- Oscillation terminals
  - X_{TAL} — Oscillation inverter input (OSC IN)
  - $\overline{X_{TAL}}$ — Oscillation inverter output (OSC OUT)

- Power supply terminals
  - V_{DD} — Plus power supply
  - GND (V_{SS}) — Common line

COMMAND SPECIFICATIONS

○ Commands input from C_0, C_1, and C_2 pins (1 ...H, 0 ...L)
Shift register 40 bit (The year function is ineffective.)
(Operates as the existing μPD1990AC in other than test mode)

C_2	C_1	C_0	FUNCTION	
0	0	0	Register Hold	DATA OUT = 1 Hz
0	0	1	Register Shift	DATA OUT = [LSB] = 0 or 1
0	1	0	Time Set & Counter Hold	DATA OUT = [LSB] = 0 or 1
0	1	1	Time Read	DATA OUT = 1 Hz
1	0	0	TP = 64 Hz	
1	0	1	TP = 256 Hz	
1	1	0	TP = 2 048 Hz	
1	1	1	Serial command transfer mode	

* The test mode is cancelled by [C2, C1, C0] = [0, 0, 0] to [1, 1, 0].

○ Serial data commands
Set [C_2, C_1, C_0] = [1, 1, 1] at all time.
Shift register 52 bit (The year function is effective.)

C_3'	C_2'	C_1'	C_0'	FUNCTION	
0	0	0	0	Register Hold	DATA OUT = 1 Hz
0	0	0	1	Register Shift	DATA OUT = [LSB] = 0 or 1
0	0	1	0	Time Set & Counter Hold	DATA OUT = [LSB] = 0 or 1
0	0	1	1	Time Read	DATA OUT = 1 Hz
0	1	0	0	TP = 64 Hz	
0	1	0	1	TP = 256 Hz	
0	1	1	0	TP = 2 048 Hz	
0	1	1	1	TP = 4 096 Hz	
1	0	0	0	TP = 1 s interval set (counter reset & start)	
1	0	0	1	TP = 10 s interval set (counter reset & start)	
1	0	1	0	TP = 30 s interval set (counter reset & start)	
1	0	1	1	TP = 60 s interval set (counter reset & start)	
1	1	0	0	Interval Output Flag Reset	
1	1	0	1	Interval Timer Clock Run	
1	1	1	0	Interval Timer Clock Stop	
1	1	1	1	TEST MODE SET	

When serial data commands are used, C_0, C_1, and C_2 pins should be connected V_{DD} pin.

- Command input
  (1) 3-bit binary code input: C_2, C_1, C_0
  (2) 4-bit serial transfer command input: C_3', C_2', C_1', C_0'

- Number of commands

	C_2, C_1, C_0	C'_3, C'_2, C'_1, C'_0
Register control	4	4
TP select	3	8
TP control	0	3
Test mode set	1	1

- Commands (C_3', C_2', C_1', C_0' commands are made effective only when [C_2, C_1, C_0] = [1, 1, 1].)
  (1) Register control [C_2, C_1, C_0] / [C_3', C_2', C_1', C_0']
  - **Register Hold Mode** [0, 0, 0] / [0, 0, 0, 0]
    [C_2, C_1, C_0]
    The 40-bit shift register is held. The year function is ineffective.
    [C_3', C_2', C_1', C_0']
    The 48-bit shift register is held.
    The command register is not held.
    * The DATA OUT output frequency is 1 Hz.
  - **Register Shift Mode** [0, 0, 1] / [0, 0, 0, 1]
    [C_2, C_1, C_0]
    The 40-bit shift register data can be shifted. The year function is ineffective.
    [C_3', C_2', C_1', C_0']
    Data in 52-bit shift registers (including command registers) can be shifted. For command register, data can be always shifted using the serial command transfer mode.
    * The DATA OUT output is LSB data from the shift register.
  - **Time Set and Counter Hold Mode** [0, 1, 0] / [0, 0, 1, 0]
    [C_2, C_1, C_0]
    Data is transferred from the 40-bit shift register to the time counter. The year function is ineffective.
    [C_3', C_2', C_1', C_0']
    Data is transferred from the 48-bit shift register to the time counter.
    * This command is used to reset the last 10-15 of 15 Stage Binary Divider and holds the time counter.
      15 Stage Binary Divider resetting and time counter release are executed by the following:
      [C2, C1, C0] = [0, 0, 0] [0, 0, 1] [0, 1, 1] [C3', C2', C1', C0'] = [0, 0, 0, 0] [0, 0, 0, 1] [0, 0, 1, 1]
      The time setting accuracy is ±15.625 ms.
      The DATA OUT pin outputs LSB data (0 or 1) from the shift register.
      After this command is executed, the 40-/48-bit shift register is held and data cannot be shifted.
  - **Time Read Mode** [0, 1, 1] / [0, 0, 1, 1]
    [C_2, C_1, C_0]
    Data is transferred from the time-counter to the 40-bit shift register. The year function is ineffective.
    [C_3', C_2', C_1', C_0']
    Data is transferred from the time counter to the 48-bit shift register.
    * The DATA OUT pin output is a 1 Hz frequency.
      After this command is executed, the 40-/48-bit shift register is held and data cannot be shifted.

(2) TP selection and control [C_2, C_1, C_0] / [C_3', C_2', C_1', C_0']

- **TP = 64 Hz** Set Mode [1, 0, 0] / [0, 1, 0, 0]
  64 Hz (50 % duty) is output to the TP pin.
  [C_2, C_1, C_0]: The year function is ineffective and the interval timer stops.
- **TP = 256 Hz** Set Mode [1, 0, 1] / [0, 1, 0, 1]
  256 Hz (50 % duty) is output to the TP pin.
  [C_2, C_1, C_0]: The year function is ineffective and the interval timer stops.
- **TP = 2 048 Hz** Set Mode [1, 1, 0] / [0, 1, 1, 0]
  2 048 Hz (50 % duty) is output to the TP pin.
  [C_2, C_1, C_0]: The year function is ineffective and the interval timer stops.

Modes permitted only for serial commands [C_3', C_2', C_1', C_0']

- **TP = 4 098 Hz** Set Mode [0, 1, 1, 1]
  4 098 Hz (50 % duty) is output to the TP pin. The interval timer stops.
- **TP = 1-second** Interval Set Mode (counter reset & start) [1, 0, 0, 0]
  A 1-second interval signal is output to the TP pin.
- **TP = 10-second** Interval Set Mode (counter reset & start) [1, 0, 0, 1]
  A 10-second interval signal is output to the TP pin.
- **TP = 30-second** Interval Set Mode (counter reset & start) [1, 0, 1, 0]
  A 30-second interval signal is output to the TP pin.
- **TP = 60-second** Interval Set Mode (counter reset & start) [1, 0, 1, 1]
  A 60-second interval signal is output to the TP pin.
- **Interval Output Flag Reset** [1, 1, 0, 0]
  The interval signal output to the TP pin is reset.
  The interval timer counter continue the operation.
- **Interval Timer Clock Run** [1, 1, 0, 1]
  The timer for outputting interval signals is reset then started.
- **Interval Timer Clock Stop** [1, 1, 1, 0]
  The timer for outputting interval signals stops.
  The output status does not change.

(3) Serial command transfer mode setting
Set [C_2, C_1, C_0] = [1, 1, 1]

(4) Test mode setting
Set [C_2, C_1, C_0] = [1, 1, 1] [C_3', C_2', C_1', C_0'] = [1, 1, 1, 1]

- 3-bit parallel command setting mode [C_2, C_1, C_0]
  The year function is ineffective when commands are input through C_2, C_1, and C_0 pins.
  Generally, February involves 28 days. The 29th day can be set optionally. The next day of the February 29th can be set the March 1st automatically. The interval timer is in the halt state.
  * The test mode is cancelled by [C_2, C_1, C_0] = [0, 0, 0] to [1, 1, 0].
- Serial command transfer mode [C_3', C_2', C_1', C_0']
  If a strobe signal is input with C_2, C_1, and C_0 pins set at the V_{DD} level ([1, 1, 1]), the contents of the serial command register ([C_3', C_2', C_1', C_0']) are received as a command; the year function is effective.
  * The test mode is cancelled by [C_3', C_2', C_1', C_0']
    = [0, 0, 0]
    = [0, 1, 0, 0] to [1, 1, 1, 0]

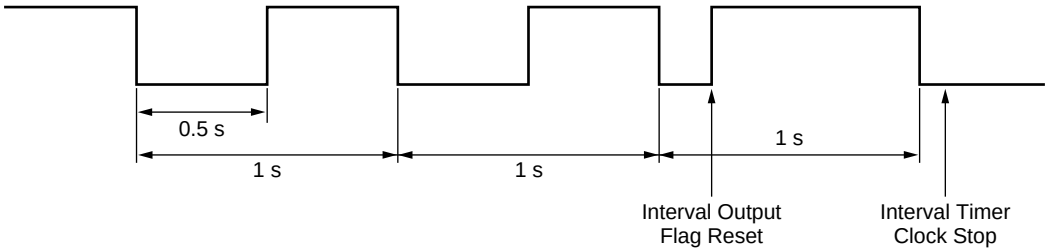
  In this mode, the serial command register is not held with the Register Hold command. Accordingly, the serial command can be executed irrespective of the mode if the CS pin is active.
  The year function is effective in the serial command transfer mode.

○ Interval output function

An interrupt signal can be output by selecting an output from TP.

Interrupt signals are output repeatedly at specified intervals until their output is suppressed by a command.

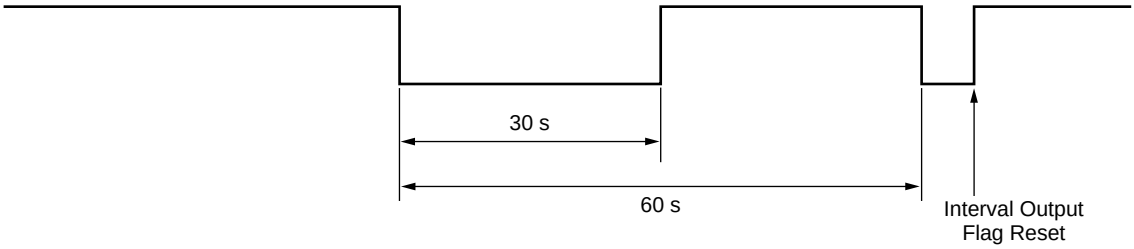
Only output flags can be reset to operate the timer continuously.



Interval of 1 second

The interval signal waveform is rectangular (50 % duty) if not reset.

The interval timer is independent of the Timer Counter, so it is not affected by the resetting of the current time timer.



The interval timer accuracy is ±15.625 ms.

* The interval timer counter is reset by [1, 0, 0, 0] through [1, 0, 1, 1].

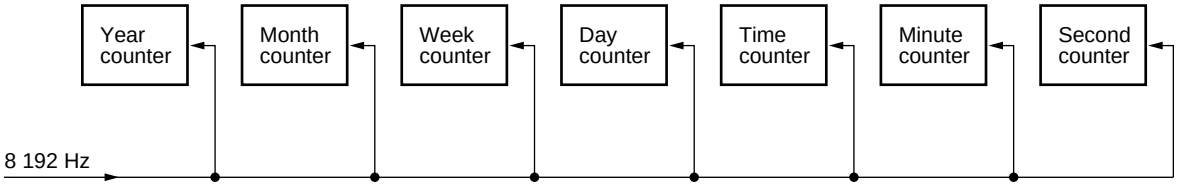
○ Test mode

In the test mode, data is output to the DATA OUT pin regardless of whether data has been input to OUT ENBL.

There are two different test modes depending on the OUT ENBL data.

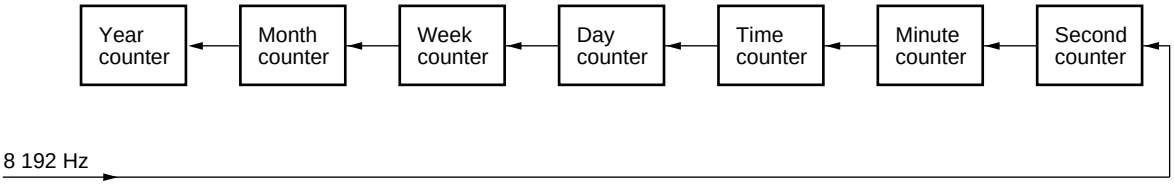
(1) Test mode 1 (OUT ENBL = 0)

8 192 Hz signals are set parallel in the counters for year, month, week, day, time, minute, and second. There is no carry from these counters.



(2) Test mode 2 (OUT ENBL = 1)

A 8 192 Hz signal is input to the second counter instead of the 1 Hz signal. There is carry from counters.



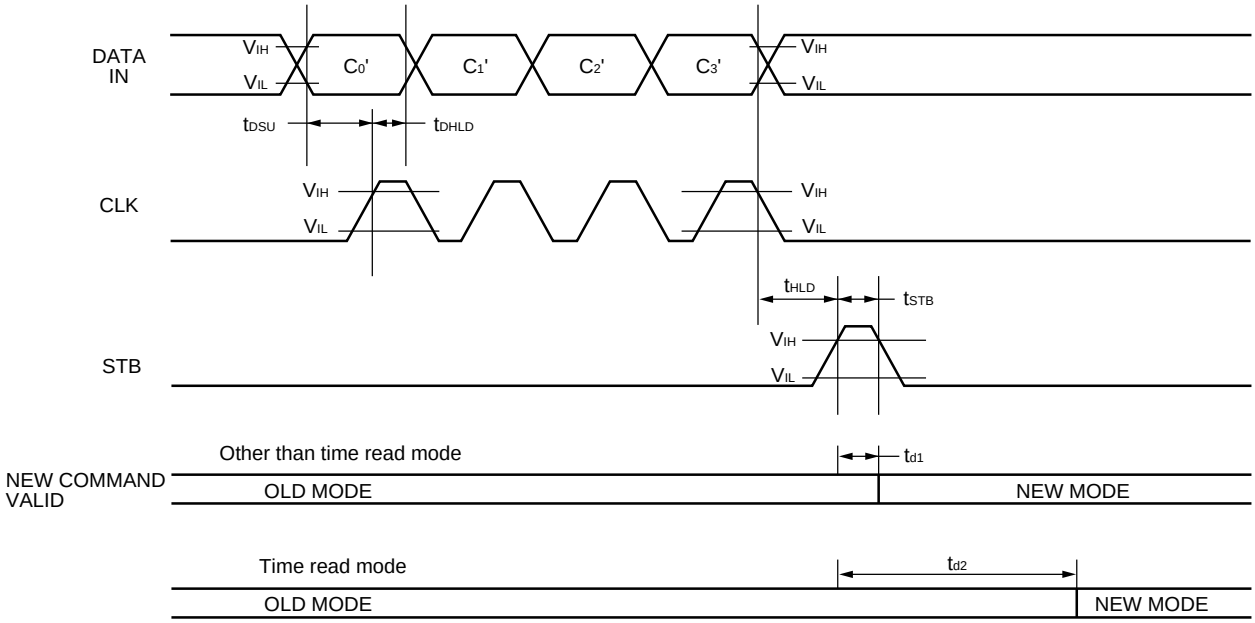
Outputs from DATA OUT and TP OUT pins in different function modes are listed below.

MODE	DATA OUT	TP	Others	
REGISTER HOLD	1 Hz	64 Hz	By this command, TEST MODE is released.	
REGISTER SHIFT	LSB of shift register	32 Hz	Test mode	8 192 Hz input to time counter
TIME SET	LSB of shift register	L Level		
TIME READ	1 Hz	32 Hz		8 192 Hz input to time counter

When the REGISTER HOLD command cancels the test mode, 64 Hz is output to the TP pin.

TIMING DIAGRAM FOR SETTING COMMANDS (C_0', C_1', C_2', C_3')

Figure 2.



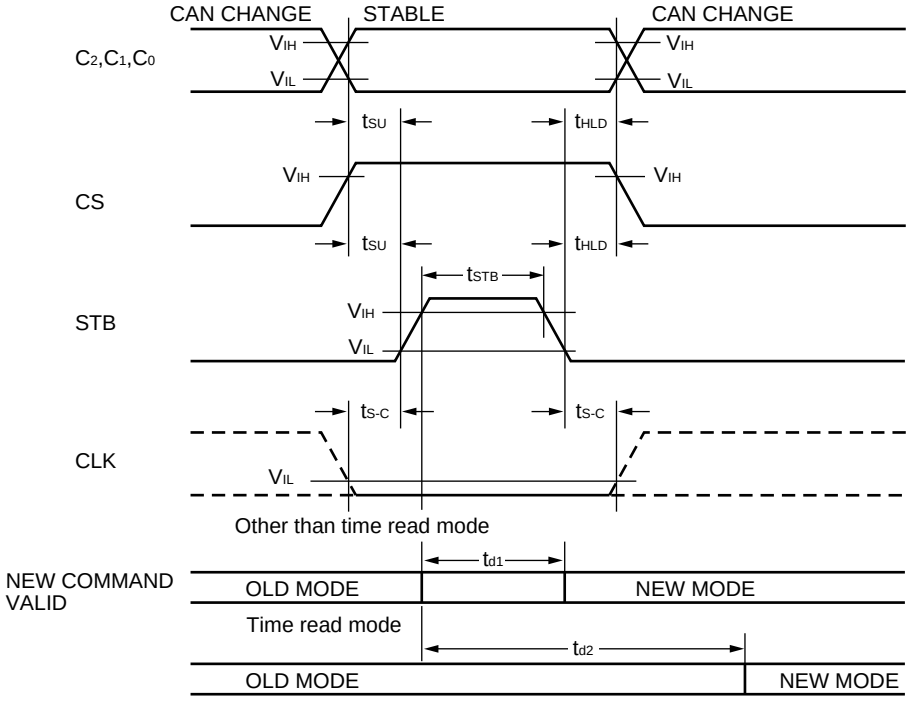
$V_{DD} - V_{SS}$ = 2.0 V

t_{DSU} = 1 μs MIN.
t_{DHLD} = 1 μs MIN.
t_{HLD} = 1 μs MIN.
t_{STB} = 1 μs MIN.
t_{d1} = 1 μs MAX. (Other than time read mode)
t_{d2} = 20 μs MAX. (Time read mode)

Note: Command (C_2, C_1, C_0) is set to (1, 1, 1)
CS = "H"
A mode is latched by STB and held until another mode in the same group is set.

TIMING DIAGRAM FOR SETTING COMMANDS (C_0, C_1, C_2)

Figure 3.



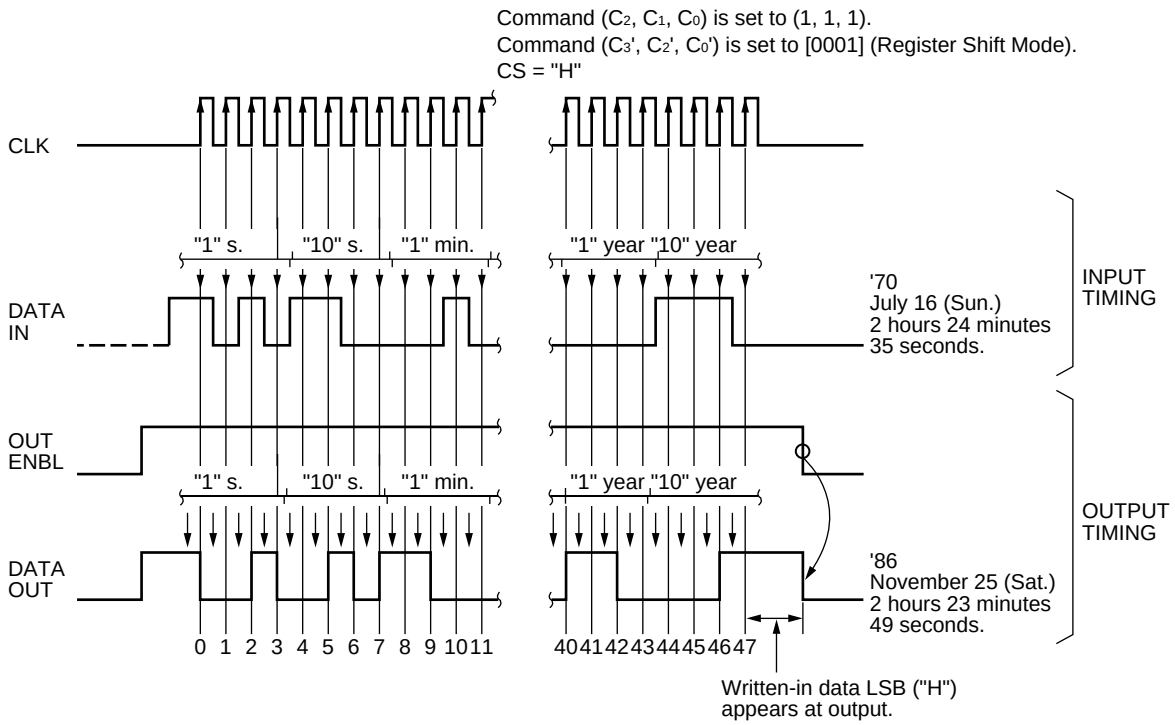
$V_{DD} - V_{SS}$ = 2.0 V

t_{SU} = 1 μs MIN.
t_{HLD} = 1 μs MIN.
t_{STB} = 1 μs MIN.
t_{d1} = 1 μs MAX. (Other than time read mode)
t_{d2} = 20 μs MAX. (Time read mode)
t_{S-C} = 1 μs MIN.

Note: A mode is latched by STB and held until another mode in the same group is set.

DATA INPUT/OUTPUT TIMING DIAGRAM

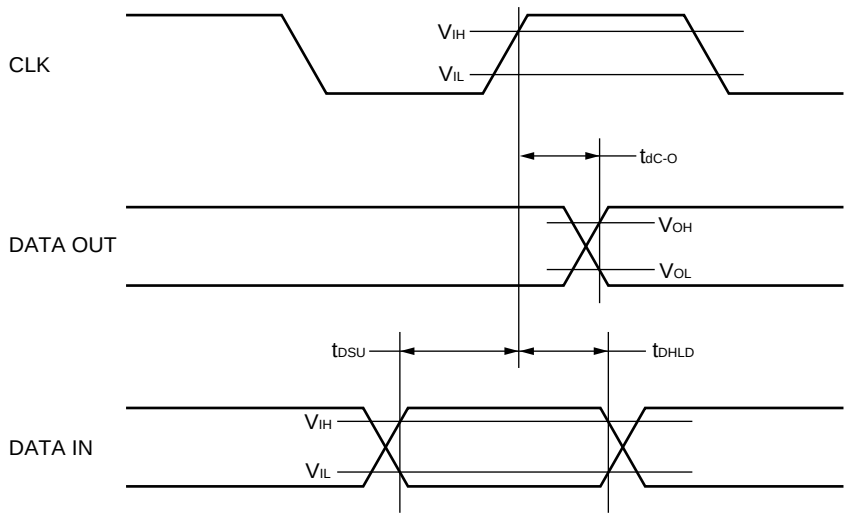
Figure 4.



Note: Reading-in timing of CPU (Trailing edge of CLK).

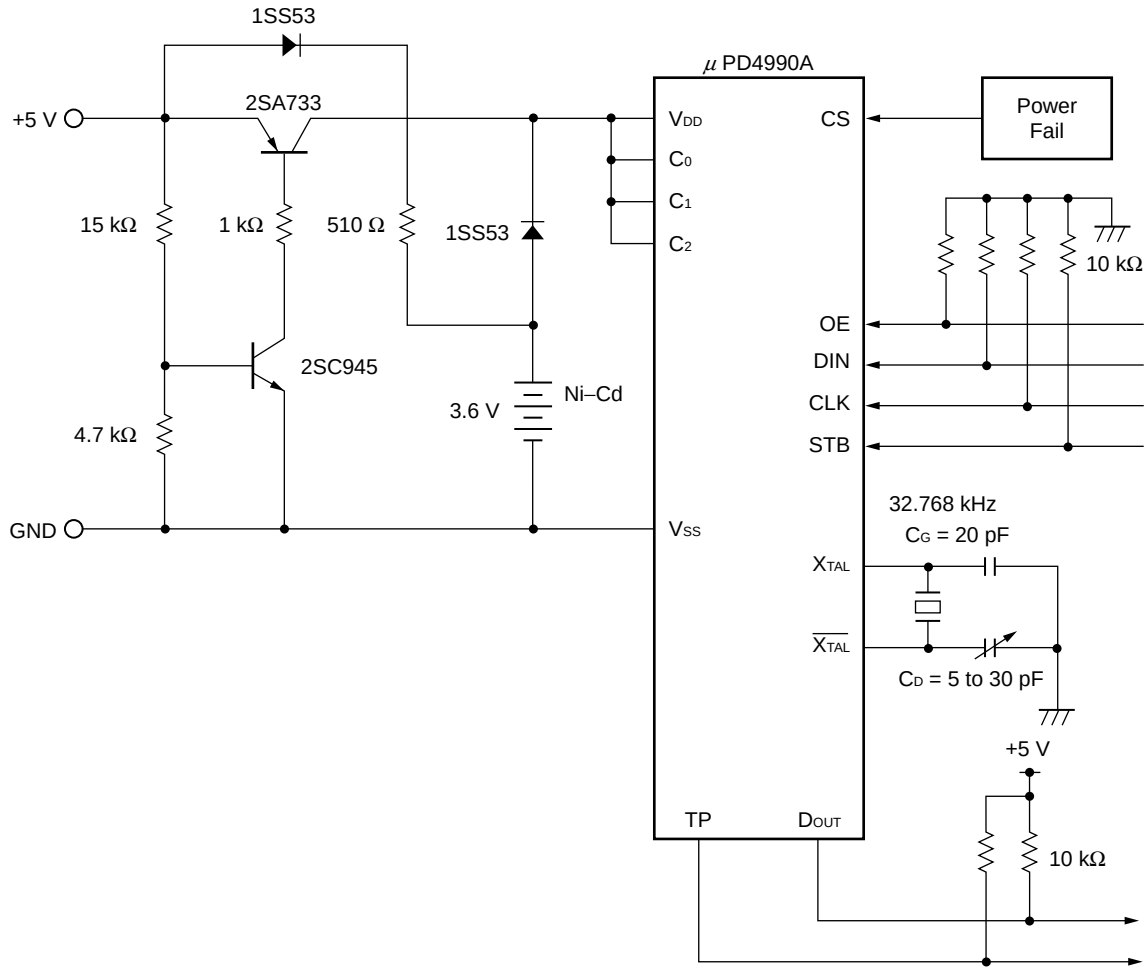
TIMING DIAGRAM OF DATA INPUT AND OUTPUT

Figure 5.

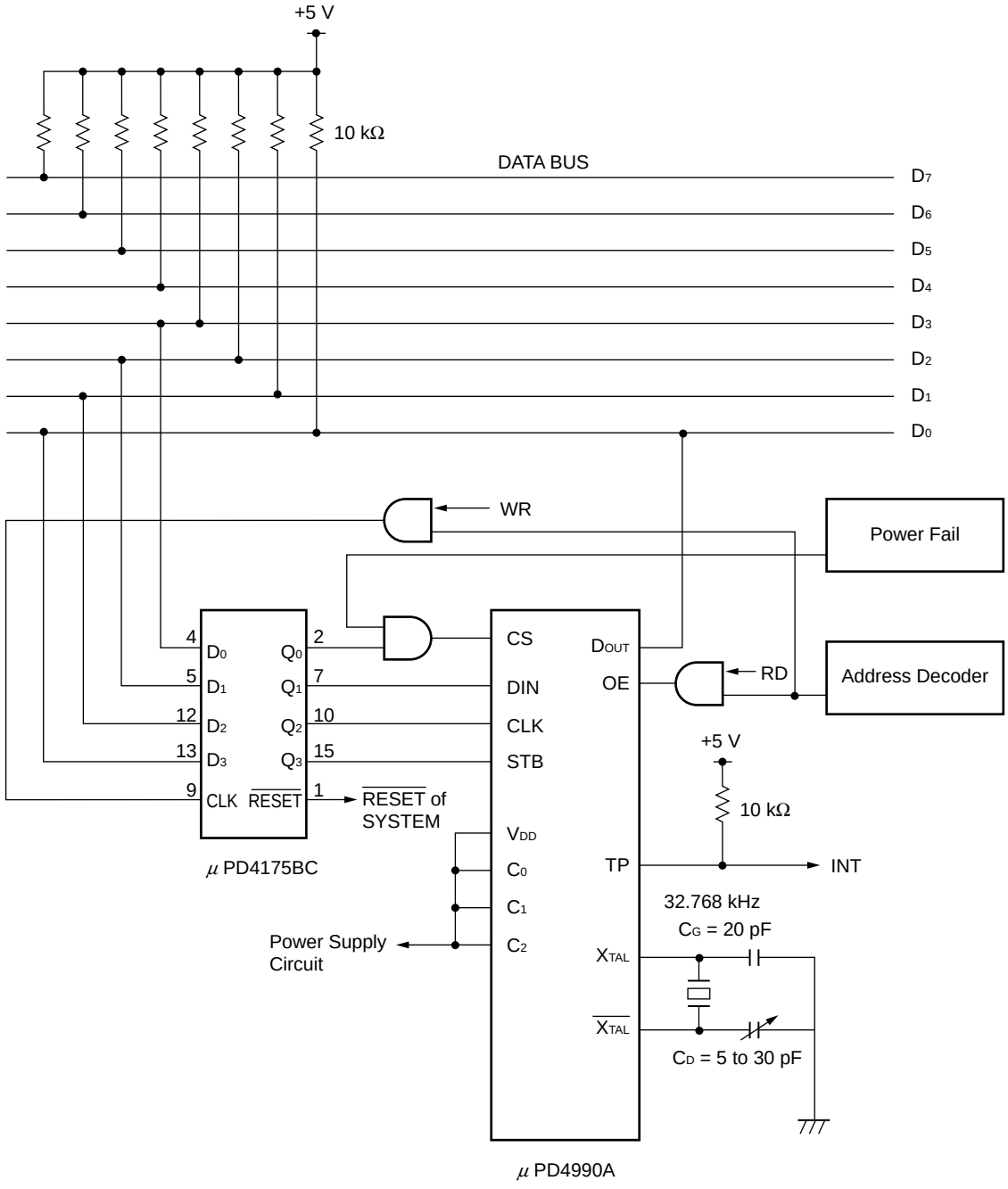


t_{dC-O} : 1 μs MAX. (R_L = 33 kΩ, C_L = 25 pF)
t_{DSU} : 1 μs MIN.
t_{DHLD} : 1 μs MIN.

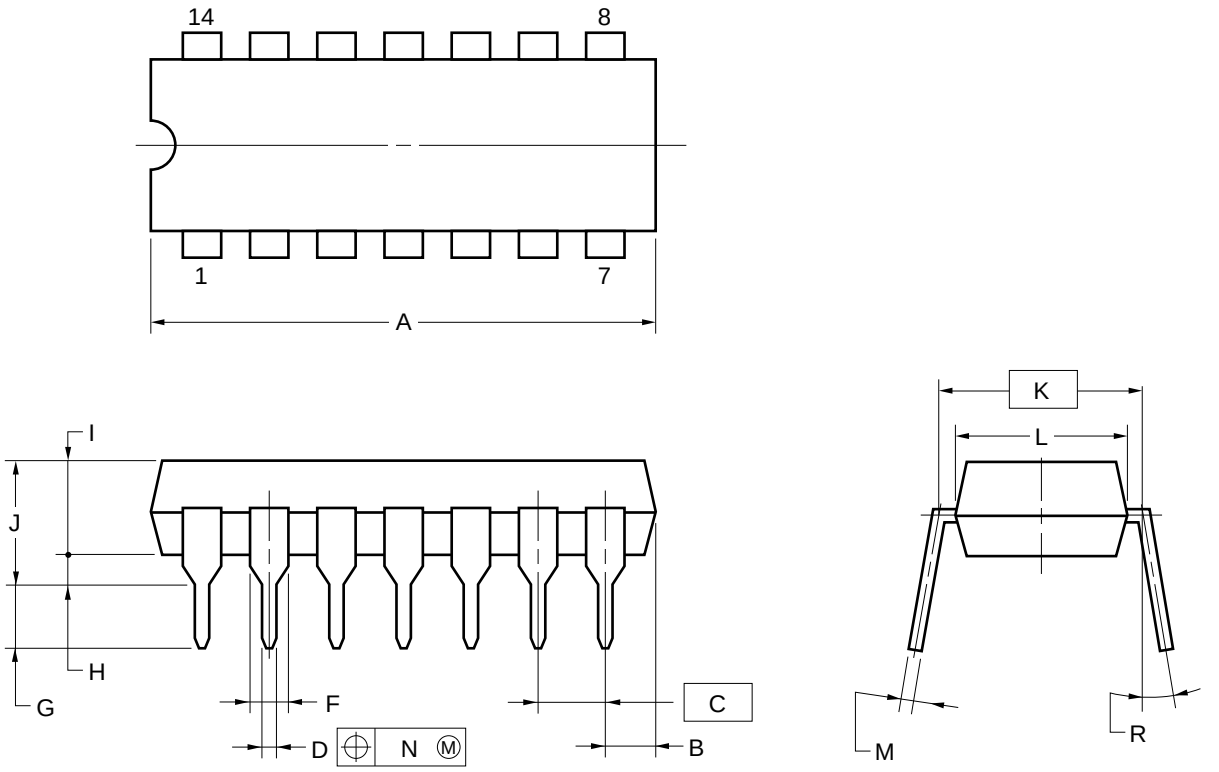
POWER SUPPLY CIRCUIT



APPLICATION



14PIN PLASTIC DIP (300 mil)



NOTES

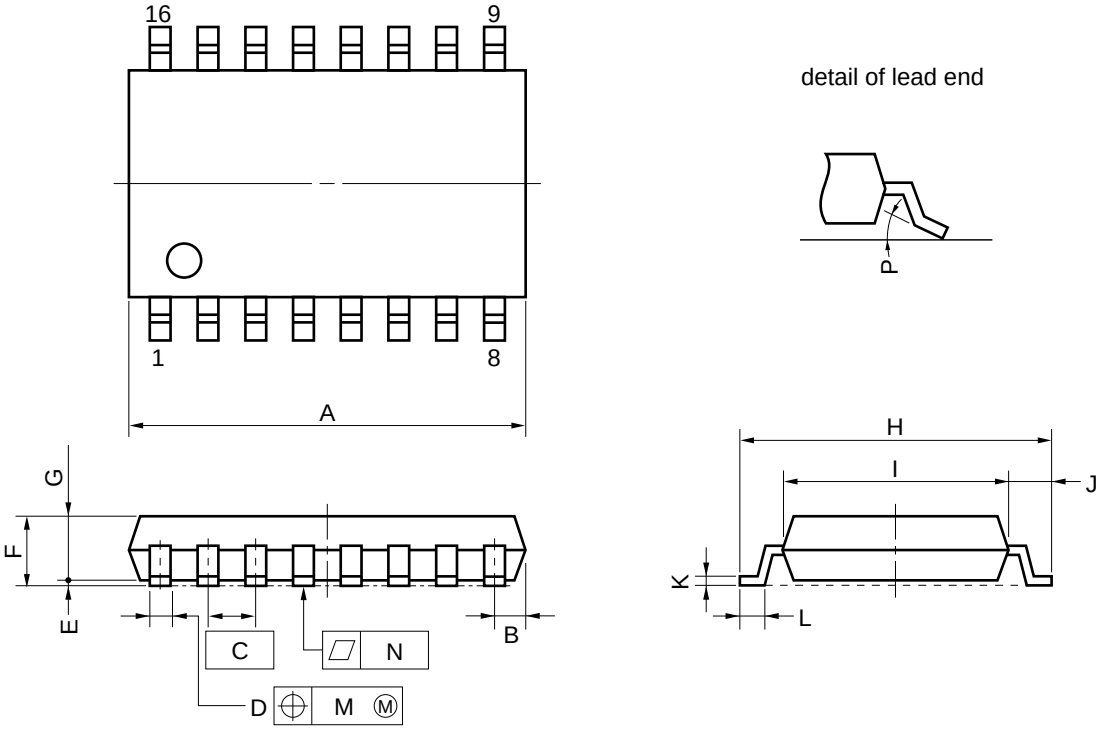
1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	20.32 MAX.	0.800 MAX.
B	2.54 MAX.	0.100 MAX.
C	2.54 (T.P.)	0.100 (T.P.)
D	0.50 ± 0.10	$0.020^{+0.004}_{-0.005}$
F	1.2 MIN.	0.047 MIN.
G	3.5 ± 0.3	0.138 ± 0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	7.62 (T.P.)	0.300 (T.P.)
L	6.4	0.252
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.25	0.01
R	0~15°	0~15°

P14C-100-300A,C-1

16 PIN PLASTIC SOP (300 mil)



NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	10.46 MAX.	0.412 MAX.
B	0.78 MAX.	0.031 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.40^{+0.10}_{-0.05}$	$0.016^{+0.004}_{-0.003}$
E	0.1±0.1	0.004±0.004
F	1.8 MAX.	0.071 MAX.
G	1.55	0.061
H	7.7±0.3	0.303±0.012
I	5.6	0.220
J	1.1	0.043
K	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$
L	0.6±0.2	$0.024^{+0.008}_{-0.009}$
M	0.12	0.005
N	0.10	0.004
P	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$

P16GM-50-300B-4

[MEMO]

[MEMO]

M4 96.5