Mod #	Group	New Style Name	Old Style Name	Description	Pin 01	Pin 02	Pin 03	Pin 04	Pin 05	Pin 06	Pin 07	Pin 08	Pin 09	Pin 10	Pin 11	Pin 12	Die Row
1001		Their orgin reality	old otyle Hame	Continuity Structure (10um wide metal line between all pads)	short	short	short	short	short	short	short	short	short	short	short	short	1
1002				Alignment Structure (metal lines surrounding all pads by 1.0um)			1			-	metal						1
				n-chan field oxide FETs poly1 gate						1							1
1003	1			poly1 gate w/l = 100/0.14	substrate	drain / source	gate	source / drain	gate	drain / source							1
				poly1 gate w/l = 1000/0.17	substrate		······································					drain / source	gate	source / drain	gate	drain / source	-
				n-chan field oxide FETs metal1 gate													1
1004	1			metal1 gate w/l = 1000/0.24	substrate	drain/ source	gate 1	drain 1	gate 2	drain 2							1
				metal1 gate w/l = 1000/0.27	substrate		***************************************		***************************************			source	gate 1	drain 1	gate 2	drain 2	-
	2			n+ resistor 320.73 / 12.8 : 25.06 sq	n+ res				n+ res	substrate							1
1005	2			n-well resistor 24.505 / 24.87 : 0.99 sq			n-well res	n-well res		substrate							1 .
1005	2			p+ resistor 320.67 / 12.8 : 25.05 sq							p+ res	n-well			p+ res		1
	2			p+ resistor - 4 terminal measurement 40.01/0.14 : 285.79 sq							force I		meas V	meas V		force I	-
	2			n+ high voltage resistor 320.67 / 12.8 : 25.06 sq	hv n+ res				hv n+ res	substrate							T
1006	2			deep n-well resistor 24.505 / 22.545 : 1.09 sq			deep n-well res	deep n-well res		substrate							1
1000	2			p+ resistor 320.67 / 12.8 : 25.05 sq							hv p+ res	n-well			hv p+ res		1 '
				p+ resistor - 4 terminal measurement 40.01/0.14 : 285.79 sq							force I		meas V	meas V		force I	
	5			n-chan gate oxide capacitor, no source/drain: large area -THIN OX													T
1012	5			Area = 4267.2 um2, perimeter = 1029.8 um, poly over field=1281.3 um2	substrate	gate	substrate	gate	substrate	gate							1
1012	5			p-chan gate oxide capacitor, no source/drain: large area] '
	J			Area = 4203.5 um2, perimeter = 1055.9 um, poly over field=1369.7 um2							n-well	gate	n-well	gate	n-well	gate	1
	2			n+ resistor 12.44 / 311.105 : 25.0 sq	n+ res	substrate			n+ res								
				n+ resistor - 4 terminal measurement 42.55/0.14: 303.9 sq		substrate	n+ res	n+ res									
1014				ultra long poly 1 line													1
	2			0.15/1650.48, 0.28 um space over n_ diff lines							n+ diff	poly comb	poly serp	poly serp			
	-			0.13/1566.17, 0.3 um space over field								poly comb		poly serp	poly serp		
				0.1/1955.46, 0.245 um space over field								poly comb			poly serp	poly serp	
1016				VPP_25fF, Poly/M4 Shield, M1-M3 fingers; m=275	c0	c1									Top Shield	Psub	1
1017				VPP_25fF, Ll/M4 Shield, M1-M3 fingers; m=275	c0	c1									Top Shield	Psub	1
1018				340fF 2X Nhvnatives, 4X XCMVPP's, M3-M4 fingers, M5-shield, m=132	G	S/D/Bulk										Psub	1
1021				VPP_100fF, Poly/M4 Shield, M1-M3 fingers; m=132	c0	c1									Top Shield	Psub	1
1022				VPP_100fF, M4 Shield, M1-M3 fingers; m=132	c0	c1									Top Shield	Psub	1
1023				description is missing													1
				ultra long n+ diff line integrity test;													
	2			1354.5 squares long ; 0.29 um line, 0.3 um space	substrate	n+ serp	n+ serp	n+ serp									
	_			1354.5 squares long ; 0.29 um line, 0.3 um space	substrate	n+ serp		n+ serp	n+ serp								
1026				1354.5 squares long ; 0.29 um line, 0.30 um space	substrate	n+ serp			n+ serp	n+ serp							1
				ultra long p+ diff line integrity test;													
	2			1354.5 squares long ; 0.29 um line, 0.30 um space				<u> </u>			n-well	p+ serp	p+ serp	p+ serp			
	_			1354.5 squares long ; 0.29 um line, 0.3 um space							n-well	p+ serp			p+ serp	p+ serp	
				1354.5 squares long; 0.29 um line, 0.3 um space							n-well	p+ serp		p+ serp	p+ serp		—
				n+/n-well field FET w/ poly 1 gate													
	1			n+ / n-well w/l = 26 x 40 / 0.32 (diff to nwell 0.32, poly to diff 0.05)	substrate	n-well	gate	n+									
1030				n+ / n-well w/l = (6.56*210) / 0.32 (N+ diff to nwell 0.32, poly to diff 0.05) with NWM corner rounding	substrate	n-well			gate	n+							1
	١.			p+/p-well field FET w/ poly 1 gate				ļ									
	1			p+/p-well wll = 26 x 40 / 0.18 (diff to pwell 0.18, poly to diff 0.05)				ļ		-	n-well	substrate	gate	p+		1	
		-	+	p+/p-well w/l = 24 x 40 / 0.15 (diff to pwell 0.15, poly to diff 0.05)						+	n-well	substrate		-	gate	p+	+
1037	3			M1-LI1-poly contacts: mcon/licon = 0.17/0.17 um M1 sq = 4668.5													
1037	3			contact string (8740 contacts; 0.73 sq/ct RSGP)	string	string	string	string	string	string			-17	-17			1
	3	-	+	M2 to M1 via: 0.15um (3240 vias) M2 sq = 3060 nested poly 1 on diff						+	string	string	string	string	string	string	+
				nested poly 1 on diff p1 w = 0.15um, s = 0.25um res l/w = 23.595 / 0.15			1	ļ		-						ļ	
	2			p1 w = 0.15um, s = 0.25um res I/w = 23.595 / 0.15 p1 w = 0.15um, s = 0.25um res I/w = 25.595 / 0.15	V-meas	force - I	V-meas	force - I				-				-	
1040	ļ			p1 w = 0.15um, s = 0.25um res l/w = 25.595 / 0.15 isolated poly 1 on diff		force - I		force - I	V-meas	V-meas						-	- 1
	2			p1 w = 0.15um res I/w = 23.595 / 0.15				ļ			sense 2	force I		force I		-	
	²			p1 w = 0.15um res l/w = 23.595 / 0.15 p1 w = 0.15um res l/w = 23.595 / 0.15				ļ			sense z	force I		force I		1	
1062		-	+	p1 w = 0.15um res w = 23.595 / 0.15 VPP 12fF 3.6x3.6		0		1		+		TOFCE I		TOFCE I	sense 2	sense 1 Psub	+
1062		+	+	VPP_12fF 3.6x3.6 VPP mis 12fF	A	B	1/-	Vn	Verse	Veed		+		-	-	PSUD	1 1
1063		 	+		stub	load	Vp	Vn Vn	Vpwr	Vgnd		-			1	-	$+$ 1
4070	١.,			p-chan field oxide FETs poly1 gate						1		-		-		-	
1070	1	1		poly1 gate w/l = 1000/0.17, diff spacing = 0.27	n-well	drain / source	gate	source / drain	gate	drain / source		1				1	1
1072		 	+	poly1 gate w/l = 1000/0.14, diff spacing = 0.24	n-well	04		1		+		drain / source	gate	source / drain	gate	drain / source	+
	l			VPP_12fF, M3-Shield; m=891 VPP_50fF, M3-Shield; m=275	C0	C1 C1		<u> </u>		+		1		-	MET-3 MET-3	Psub Psub	1
																	1
1072				VPP_100fF, M3-Shield; m=275	CO	CI									MET-3	Psub	1

Mod#	Group	New Style Name	Old Style Name	Description	Pin 01	Pin 02	Pin 03	Pin 04	Pin 05	Pin 06	Pin 07	Pin 08	Pin 09	Pin 10	Pin 11	Pin 12	Die Row
MUU #		New Style Name	Olu Style Name	M1-L11-N+ contacts: mcon/licon1 = 0.17/0.17 um	FIIIVI	FIII VZ	FIII US	FIII 04	FIII UJ	FIII 00	FIIIV	FIII 00	FIII US	FIII IV		FIII 12	Die Kow
	3			contact string (6384 contacts; 0.88 sg/ct RSN)	string	string	string	string	string	substrate							
1076				M1-L11-P+ contacts: mcon/licon1 = 0.17/0.17 um	Sully	Sully	Sully	Sully	Sully	Substrate				+			1
	3			contact string (6992 contacts; 0.88 sq/ct RSP)		······································	<u></u>				string	string	string	string	string	n-well	
			_	HV M1-LI1-N+ contacts: mcon/licon1 = 0.17/0.17 um	_		 		+	-	Sully	Stillig	Stillig	Sully	String	II-Well	+
	3			contact string (6384 contacts; 0.88 sq/ct RSN) m1 sq = 3734.808	string	string	string	string	string	substrate							
1077		-		HV M1-L11-P+ contacts: mcon/licon1 = 0.17/0.17 um	Sung	Sung	Sung	String	Suring	Substrate							1
	3			contact string (6992 contacts; 0.88 sq/ct RSP) m1 sq = 3410.04			<u></u>								42.	n-well	
4070				VPP mis 50fF: M3 shield	24.4	lead	1/-	- 1/-	- Verre	1/	string	string	string	string	string		+
1079 1081		1		XCMVPP2 over NHVNATIVE10x4	stub Psub/S/D/B	load	Vp	Vn	Vpwr	Vgnd	stub_t	load_t	Vp_t	Vn_t	Vpwr	Vgnd	1
1081					PSUD/S/D/B	Gate										Psub/S/D/B	1
	3			M1-LI1 contacts: mcon = 0.17 um			<u></u>		_			ļ					
				contact string (3600 contacts; 0.88 sq/ct RSLIW)	string	string	string	string	string	string							
1082				LI sheet resistance and electrical linewidth			<u></u>										1
	3			2.6 X 452.785 Line			<u></u>				Force 1	Force 2	Sense 1		Sense 2		
				0.17 X 426.04		- 01					Force 1	Force 2		Sense 1		Sense 2	+
1083				VPP_1fF, M3-Shield; m=7436	C0	C1									MET-3	Psub	1
1085				VPP_1fF, LI Shield, M1/M2 fingers; m=7436	C0	C1										Psub	1
1086				VPP_mis 1fF; LI shield, M1/M2 fingers	stub	load	Vp	Vn	Vpwr	Vgnd	1	l					1
				VPP_mis 1fF; LI shield, M1/M2 fingers							stub_t	load_t	Vp_t	Vn_t	Vpwr	Vgnd	
1087				XCMVPP2 over PHV5x4	S/D/B	Gate	4			1	1				 	Psub	1
				M2-M1-L11-N+ stacked via on mcon on licon1;			4	1									
	3			M2 = 0.45 um, via = 0.15 um, mcon/licon = 0.17/0.17 um			<u>4</u>										
1089	ļ	ļ		string (6992 contacts; 0.904 sq/ct RSN)	string	string	string	string	string	substrate		 	_	<u> </u>	ļ	<u> </u>	- 1
	_			M2-M1-LI1-P+ stacked via on mcon on licon1;		1	4										
	3			M2 = 0.45 um, via = 0.15 um, mcon/licon = 0.17/0.17 um string (6992 contacts; 0.904 sq/ct RSP)			<u></u>								-1		
	_						4				string	string	string	string	string	n-well	+
	3			LI1-poly contacts: licon1 = 0.17 um (generic)			<u> </u>		_								
				string (8360 contacts; 0.73 sq/ct RSGP, 0.73 sq/ct RSLIW)	string	string	string	string	string	string							
1092				M1-Li contact Kelvin, M1/Li width=0.47/0.28 um			<u></u>										1
	3			0.17um mcon Kelvin: .05 LI enclosure			<u></u>				metal 1 Vs	metal 1 lf	LI 1 If		LI Vs		
				0.17um mcon Kelvin:01 LI enclosure									LI Vs	metal 1 If	LI If	metal 1 Vs	
			phighvt	phighvt; w/l=0.64/0.15; licon resistance; n_licons=2,304; contact-gate=0.055u			<u> </u>				G/S/B (vpwr=1.8V)			r0	r1		
			phighvt	phighvt; w/l=0.64/0.15; licon resistance; n_licons=4,608; contact-gate=0.055u			<u> </u>				G/S/B (vpwr=1.8V)			r0		r2	
			phighvt	phighvt; w/l=0.64/0.15; licon resistance; n_licons=2,304; contact-gate=0.050u			<u> </u>				G/S/B (vpwr=1.8V)	r0	r1				
1093			phighvt	phighvt; w/l=0.64/0.15; licon resistance; n_licons=4,608; contact-gate=0.050u			<u> </u>				G/S/B (vpwr=1.8V)	r0		r2			1
			nshort	nshort; w/l=0.64/0.15; licon resistance; n_licons=4,608; contact-gate=0.055u			r0	r1		G/S/B (vgnd=0V)							
			nshort	nshort; w/l=0.64/0.15; licon resistance; n_licons=4,608; contact-gate=0.055u			On		r2	G/S/B (vgnd=0V)							
			nshort	nshort; w/l=0.64/0.15; licon resistance; n_licons=4,608; contact-gate=0.050u	r0	r1	<u> </u>			G/S/B (vgnd=0V)							
			nshort	nshort; w/l=0.64/0.15; licon resistance; n_licons=4,608; contact-gate=0.050u	r0		r2			G/S/B (vgnd=0V)							
	3			LI1-n+ diffusion contacts: licon1 = 0.17 um (generic)			<u> </u>					ļ					
1094				string (6992 cts 0.88 sq/ct RSN, 0.73 sq.ct RSLIW)	string	string	string	string	string	substrate		ļ					1
	3			LI1-p+ diffusion contacts: licon1 = 0.17 um (generic)			<u></u>										
	-			string (6992 cts 0.88 sq/ct RSP, 0.73 sq/ct RSLIW)							string	string	string	string	string	n-well	
	5			n-chan gate oxide capacitor: field-edge intensive			4					ļ					
1137	ļ			FOM w/s = 0.14/0.27, Active Area = 722.4 um2, FOX Perimeter = 10353.6 um	substrate	gate	substrate	gate	substrate	gate		ļ					1
	5			p-chan gate oxide capacitor: field-edge intensive								ļ	1			1	
				FOM w/s = 0.14/0.27, Active Area = 1657.8 um2, FOX Perimeter = 23760 um			4				n-well	gate	n-well	gate	n-well	gate	
				NMOS contacted pitch FETs: lower half with prox. bars on diff. (0.28 um space)													
				0.42/20 NMOS	substrate	gate	drain	source									
				7/8 NMOS	substrate	gate	4	drain	source								
1141	4			7/0.15 NMOS	substrate	gate			drain	source			gate				1
				PLACE IN CENTER, CORNER OF RETICLE													
				w/l = 0.15/9.15 um electrical linewidth: upper half		Force 1					Sense 2	Sense 1	Force 2				
				10x10 Van der P.		Sense 1	4							Sense 2	Force 1	Force 2	
1174				VPP_50fF, LI Shield, M1/M2/M3 fingers; m=275	C0	C1										Psub	1
1175				VPP_100fF, LI Shield, M1/M2/M3 fingers; m=132	C0	C1										Psub	1
1178				VPP_mis_50fF; LI shield, M1/M2/M3 fingers	stub	load	Vp	Vn	Vpwr	Vgnd							1
11/0				VPP_mis 100fF; LI shield, M1/M2/M3 fingers							stub_t	load_t	Vp_t	Vn_t	Vpwr	Vgnd	_ '
1182				VPP_12fF, LI Shield, M1/M2/3 fingers; m=891	C0	C1										Psub	1
1183				VPP_mis 12fF; LI shield, M1/M2/M3 fingers	stub	load	Vp	Vn	Vpwr	Vgnd							Т.
	I			VPP_mis 12fF; LI shield, M1/M2/M3 fingers			A	1	1	1	stub t	load t	Vp t	Vn t	Vpwr	Vgnd	1
1183	l .																
1184				VPP_100fF, Poly-M5 Shield, Ll/M1/M2/M3/M4 fingers; m=132	C0	C1	1								MET-5	Psub	1

Mod #	Group	New Style Name	Old Style Name	Description	Pin 01	Pin 02	Pin 03	Pin 04	Pin 05	Pin 06	Pin 07	Pin 08	Pin 09	Pin 10	Pin 11	Pin 12	Die Row
1186				VPP_100fF, LI-M5 Shield, M1/M2/M3/M4 fingers; m=132	C0	C1									MET-5	Psub	1
1187				VPP_50fF, LI-M5 Shield, M1/M2/M3 fingers; m=275	C0	C1									MET-3	Psub	1
1188				VPP_12fF, xcmvpp4p4x4p6_fltpolym3shield, PYfloat-M3 Shield, Ll/M1/M2 fingers; m=486	C0	C1	botshield	topshield								Psub	1
				VPP_12fF, xcmvpp4p4x4p6_polym5shield, PY-M5 Shield, LI/M1/M2/M3/M4 fingers; m=405							C0	C1			topshield	Psub	<u> </u>
1189				VPP_50fF, xcmvpp6p86p1_polym5shield, PY-M5 Shield, LI/M1/M2/M3/M4 fingers; m=150	C0	C1		topshield								Psub	- 1
				VPP_50fF, xcmvpp8p6x7p9_tpolym5shield, PYfloat-M5 Shield, Ll/M1/M2/M3/M4 fingers; m=125							C0	C1			topshield	Psub	+
1206				PiS Capacitor in N-Well, C = 30.5pF per device						ļ	ļ						4
				w/l = 5/0.5, m=1650 (C=18.5fF per finger) PIS resistor in nwell L/W = 20/5	sub sub	less.	L:-L			body	gate						+
		•		PiS resistor in riwell LW = 40/5	sub	low	high low	high	gate gate								
		-		PiS resistor not in nwell. L/W = 20//5	sub		IOW	- Iligii	gate	low	high				+		
1213		=		PiS resistor not in nwell L/W = 40/5	sub	·		-	gate	IUW	low	high					- 4
1213				PiS capacitor in nwell, W/L = 40/40, n = 2, C = 23.7 pF	sub				gate		1011	nigii	S/D	gate			-1 `
		•		PiS capacitor in nwell, W/L = 40/0.5, n = 50, C = 7.4 pF	sub	•		-	-	-	†	-		gate	S/D		-
		•		PiS capacitor in nwell, W/L = 40/0.33, n = 66, C = 6.5 pF	sub						-			gate		S/D	-
	6			AF Cell (WNIv/LNIv,WNmx/LNmx,Wfuse/Lfuse)				i	i	i i	İ			J			†
				Vpp: metal connection							1						"
				Vpp_res: connection through 513.5 Ohm resistor													
1240				N+ diffusion w/l = 0.29/1.275,													4
				2nd resistor terminals shorted by Metal3													
				2x2 (4/.15,4/.37,4/.48) AF Array: Cell Ver. 1.B	sub		WL2 gate	WL1 gate	HV gate	Vpp_res		Vpp			Source 1	Source 2	
				2x2 (4/.15,4/.37,4/.48) AF Array: Cell Ver. 2	sub	Vpp_res	WL2 gate	WL1 gate	HV gate		Vpp		Source 1	Source 2			
	6			AF Cell (WNIv/LNIv,WNmx/LNmx,Wfuse/Lfuse)							ļ						_
				2x2 (4/.15,4/.37,4/.48) AF Array: Cell Ver. 2						1							
				Vpp: metal connection													
1242				Vpp_res: connection through N+ diff resistor													4
				extra N+ diffusion w/l = 0.29/1.275 (513 Ohm) resistor terminals shorted by Metal3													
				N+ diffusion w/l = 0.29/3.825, 1.54 kOhm	sub		WL2 gate	WL1 gate	HV gate	Vpp_res	ļ	Vpp			Source 1	Source 2	
				N+ diffusion w/l = 0.29/3.625, 1.34 KOMM N+ diffusion w/l = 0.29/2.550, 1.03 KOMM	sub	Vpp_res	WL2 gate	WL1 gate	HV gate	vpp_res	Vpp	Vpp	Source 1	Source 2	Source I	Source 2	
	6			AF Cell (WNIv/LNIv,WNmx/LNmx Wfuse/Lfuse)	300	VPP_103	WLZ gate	WET gate	11V gate		- трр		Gource 1	OULIUS Z			+
	ľ			2x2 (4/.15,4/.37,4/.48) AF Array: Cell Ver. 2 Breakout													-
				Vpp: metal connection													
1243				Vpp_res: connection through N+ diff resistor													4
				extra N+ diffusion w/l = 0.29/1.275 (513 Ohm)													
				resistor terminals shorted by Metal3						AF body	1	AF body			AF body	AF body	
				N+ diffusion w/l = 0.29/2.550, 1.03 kOhm	sub	Vpp_res	WL2 gate	WL1 gate	HV gate	WL1 / S1	Vpp	WL1 / S2	Source 1	Source 2	WL2 / S1	WL2 / S2	"
1248				missing description													4
				M1 sheet resistance and electrical linewidth													
	2			2.595 x 435.255 Line	Force 1	Force 2	Sense 1			Sense 2							
1375				0.18 X 443.965 Line	Force 1	Force 2		Sense 1	Sense 2								- 1
				M2 sheet resistance and electrical width							ļ						
	2			2.6 X 457.2 Line 0.24 X 417.46 Line							Force 1 Force 1	Force 2	Sense 1		Sense 2	Sense 2	
				lateral PNP BJT (pnppar) (Ae=0.68x0.68um2) Local Mismatch 1-1	Psub	B1	E1	E2	B2		FOICE I	Force 2		Sense 1		Serise 2	+
1668	8			lateral PNP BJT (prippar) (Ae=0.68x0.68um2) Local Mismatch 8-1	C-B-Psub	DI			DZ		ļ			E8	E1		- 1
1690	 			Matching Poly Resistors	O-D-F SUU			1	 	 	 	 	1	EU	E1	 	+
1030	-			W/L = 1/57.925, spacing = 0.48; proximity resistors	IF	V2		V1	+	+	<u> </u>	<u> </u>	1			<u> </u>	4
				W/L = 0.68/12.42, spacing = 0.48; proximity resistors				 	IF	V2	V1						1 1
				W/L = 1.0/12.42, spacing = 0.48; proximity resistors					T	T		V1	V2	If			1
1691				Matching Poly Resistors				1	1	1				1			1
1				W/L = 1/65, spacing = 0.48; proximity resistors	V1		V2	IF									1 .
				W/L = 0.68/65, spacing = 0.48; proximity resistors				IF	V2		V1						7 1
				W/L = 0.68/57.925, spacing = 0.48; proximity resistors								V1		V2	IF		1
1692				Matching Poly Resistors													
				W/L = 1/57.925, spacing = 0.48; proximity resistors	IF	V0	IS2	V2		V1	IS1						1
				W/L = 0.68/12.42, spacing = 0.48; proximity resistors							IS1	V1	V2	IS2	V0	IF	
1693				Matching Poly Resistors													
				W/L = 5/50.3, spacing = 0.48; proximity resistors	V1		V2	IF									1
				W/L = 1/20, spacing = 0.48; proximity resistors				IF	V1	V2							٦ '
				W/L = 2/10, spacing = 0.48; proximity resistors							V1	V2	IF			1	4
				Cell Vss contact			17				ļ						
1700	6			string (9014 cts; 3.22 sq/ct RSN; 1.68 sq/ct RSM1)			string	poly	substrate	string	ļ		ļ			ļ	- 1
				Kelvin contact (u-test)	met1 {diff}	met1	diff	-	substrate	-						-	-
		l .	1	[(u-test)	{αm}			1		1		1	1	1		1	

Mod#	Group	New Style Name	Old Style Name	Description	Pin 01	Pin 02	Pin 03	Pin 04	Pin 05	Pin 06	Pin 07	Pin 08	Pin 09	Pin 10	Pin 11	Pin 12	Die Row
				Cell L1/p+ cross-couple contact		1				1		1					
1701	6			string (32256 cts; 0.48 sq/ct RSP; 1.84 sq/ct RSLI)			string	poly	n-well	string							1
1/01	ь			Kelvin contact	LI1	LI1	diff		n-well	1							1 1 1
				(u-test)	{diff}												
				Cell Vcc contact													
1702	6			string (7968 cts; 3.22 sq/ct RSP; 3.92 sq/ct RSM1)			string	poly	n-well	string							
1702	"			Kelvin contact	met1	diff	diff		n-well								. '
				(u-test)	{met1}												
				Cell L1/n+ cross-couple contact													
1703	6			string (32256 cts; 0.56 sq/ct RSN; 1.84 sq/ct RSLI)			string	poly	substrate	string							- 1
				Kelvin contact (micropad)	LI1 {diff}	LI1	diff		substrate	ļ							-
				L1/n+ bit line contact	{OIT}												+
				string (10080 mcons / 10080 licons; 3.92 sg/mcon RSM1; 1.25 sg/mcon RSLI; 1.24 sg/licon RSN)			string	poly	substrate	string							-
1705	6			Kelvin contact	met1	met1	diff	poly	substrate	July							1
				(micropad)	{diff}				Cuboudio								1
1709	6			LI to LI / LICON to LICON bridging test structure (15232 cells)	serp			comb	serp								1
1726				Ultra long local interconnect 1 line integrity test; ~81600 squares; 9520 cells	serp	met1		comb				met1		comb		serp	1
				Cell LI1-poly string													
1743	6			"long" side: 5200 cts	serp		poly	substrate	p-well	n-well	p-well	n-well	poly	substrate		serp	1
				"short" side: 5200 cts		serp	poly	substrate	p-well	n-well	p-well	n-well	poly	substrate	serp		
				6T SRAM cell FETs													
1744	6			NPD long landing pad side: 0.21/0.15			Psub	G	S	D				Nwell		Psub	. 1
	"			NPASS long landing pad side: 0.14/0.15	S	D	Psub	G				D2		Nwell		Psub	
				PPU long landing pad side: 0.14/0.15			Psub				G		S	Nwell	D	Psub	
				s8te2et_s1744_npass_c;	src	drn	dm2	gate	vpwell	<u> </u>					vnwell		
1745				s8te2et_s1745_npd_a;				gate	vpwell	dm1	dm2	src	14	1.0	vnwell		. 1
	_			s8te2et_s1745_ppu_a;				gate	vpwell				dm1	drn2	vnwell	src	
	6			6T SRAM N-channel gap and endcap													-
				integrity structure (for cell FET leakage measurement)													
1756		npass	special nfet pass	NPASS: 2240 FETs						Psub	G	S			D	Psub	
1730		npd	Special_IIIet_pass	NPD: 3360 FETs, 1680 gaps						Psub	G1	S	G2	D	U	Psub	1 '
		npass		NPASS: 2240 FETs	G	S	····		D	Psub	- 01		02			Psub	•
		npd		NPD: 3360 FETs, 1680 gaps	G1	Š	G2	D		Psub	-					Psub	1
	6			6T SRAM P-channel gap and endcap integrity structure (for cell FET leakage measurement)	-	-				1,000	1						<u> </u>
1758		ppu		PPU: 12320 FETs, 6160 gaps	G1		G2							S	D	Nwell	- 1
				M1 / M2 step coverage/bridging over cell topo.													
1760	6			M1: 0.14um ~16210m	m1 serp			m1 comb						m1 comb		m1 serp	1
				M2: 0.14um ~22395 um		m2 serp	m2 comb						m2 comb		m2 serp		
				Memory cell poly bridging structure 20880 NMOS; 20880 PMOS; 31320 gaps						l .							١.
1773	6			20880 NMOS; 20880 PMOS; 31320 gaps PMOS W/L = 0.15/0.14; NMOS W/L = 0.21/0.15			WL1	WL2	substrate	n-well	NO PAD	NO PAD	NO PAD	NO PAD	NO PAD	NO PAD	1
			nfet	fet mismatch nfet w/ sep sb; w=1.000; i=0.500;	S	G	D1	D1		-		+			-	R	+
			nfet	fet mismatch nfet w/ sep sb ; w=1.000; i=0.500; fet mismatch nfet w/ sep sb ; w=3.000; i=0.150;	5	G	l l	- VI	D1	D2	 	+			1	B	1
2602			nfet	fet mismatch met w/ sep sb; w=0.000; 1=0.130; fet mismatch nfet w/ sep sb; w=0.420; I=0.150;	S	G				DE.	D1	D2				B	2
			nfet	fet mismatch nfet w/ sep sb; w=0.420; I=0.150;	Š	G						- 52	D1	D2		В	1
			pfet	fet mismatch pfet w/ sep sb; w=1.000; l=0.500;	S	G	D1	D1	1		İ	1				В	
2605			pfet	fet mismatch pfet w/ sep sb; w=3.000; l=0.150;	S	G			D1	D2	1					В	٠,
2605			pfet	fet mismatch pfet w/ sep sb; w=0.420; I=0.150;	S	G					D1	D2				В	1 2
			pfet	fet mismatch pfet w/ sep sb; w=0.420; I=0.150;	S	G							D1	D2		В	1
			lowytnfet	fet mismatch LowVtnfet w/ sep sb; w=7.000; I=0.250;	S	G	D1	D1								В	
2607			lowytnfet	fet mismatch LowVtnfet w/ sep sb; w=7.000; I=0.150;	S	G			D1	D2						В	2
			lowytnfet	fet mismatch LowVtnfet w/ sep sb; w=3.000; l=0.250;	S	G					D1	D2	-			В	4
			lowytnfet	fet mismatch LowVtnfet w/ sep sb; w=3.000; l=0.150;	S	G							D1	D2		В	
			lowytnfet	fet mismatch LowVtnfet w/ sep sb; w=0.420; l=1.000;	S	G	D1	D1	L			+	-	-	-	В	4
2608		-	lowytnfet lowytnfet	fet mismatch LowVtnfet w/ sep sb; w=0.420; l=0.180; fet mismatch LowVtnfet w/ sep sb; w=0.420; l=0.150;	S	G			D1	D2	D1	D2	-	-	 	B B	2
	-		lowytntet lowytnfet	fet mismatch LowVtnfet w/ sep sb; w=0.420; l=0.150; fet mismatch LowVtnfet w/ sep sb; w=0.420; l=0.150;	5	G					D1	UZ.	D1	D2	-	B	1
	 		highytpfet	fet mismatch High/Vtpfet w/ sep sb; w=0.420, i=0.130; fet mismatch High/Vtpfet w/ sep sb; w=1.000; i=0.500;		G	D1	D1		1	+	+		D2	1	B	+
			highytpfet	fet mismatch HighVtpfet w/ sep sb; w=1.000; i=0.150; fet mismatch HighVtpfet w/ sep sb; w=3.000; i=0.150;	S	G	DI DI	1 01	D1	D2	 	+	<u> </u>	1	1	B	1
2611			highytpfet	fet mismatch HighVtpfet w/ sep sb; w=0.420; l=0.150;	9	G		<u> </u>	- DI	- UZ	D1	D2			1	R	2
			highytpfet	fet mismatch HighVtpfet w/ sep sb; w=0.420; l=0.150;	S	G					- DI	D2	D1	D2		B	1
			J	1								-			·		

Mod#	Group	New Style Name		Description	Pin 01	Pin 02	Pin 03	Pin 04	Pin 05	Pin 06	Pin 07	Pin 08	Pin 09	Pin 10	Pin 11	Pin 12	Die Row
				fet mismatch NTVNativenfet w/ sep sb; w=4.000; I=0.500;	S	G	D1	D1								В	
2612				fet mismatch NTVNativenfet w/ sep sb; w=0.420; I=0.800;	S	G			D1	D2						В	2
				fet mismatch NTVNativenfet w/ sep sb; w=10.000; I=0.500;	S	G					D1	D2				В	
				fet mismatch NTVNativenfet w/ sep sb; w=1.000; I=0.600;	S	G							D1	D2		В	
			high voltage nfet	fet mismatch HVnfet w/ sep sb; w=0.420; I=0.500;	S	G	D1	D1	—							В	
2618			high voltage nfet	fet mismatch HVnfet w/ sep sb; w=0.420; I=0.500;	S	G			D1	D2	B4					B R	2
			high voltage nfet high voltage nfet	fet mismatch HVnfet w/ sep sb; w=0.420; l=0.500; fet mismatch HVnfet w/ sep sb; w=0.420; l=0.500;	5	G G			-		D1	D2	D1	D2		B	- 1
	1			fet mismatch HVpfet w/ sep sb; w=0.420; i=0.500;	S	G	D1	D1	1	1			D1	DZ.		B	
				fet mismatch HVpfet w/ sep sb; w=0.420; i=0.500;	S	G	DI	- DI	D1	D2						В	- 1
2622			high voltage pfet	fet mismatch HVpfet w/ sep sb; w=0.420; I=0.500;	S	G		1		DZ.	D1	D2				B	2
				fet mismatch HVpfet w/ sep sb; w=0.420; l=0.500;	S	G					D1	DZ.	D1	D2		B	1
				fet mismatch Nativenfet w/ sep sb; w=1.000; I=0.900;	S	G	D1	D1								B	
				fet mismatch Nativenfet w/ sep sb; w=0.700; l=0.900;	S	G			D1	D2						B	1 .
2624				fet mismatch Nativenfet w/ sep sb : w=0.420: I=0.900:	S	G			1	1	D1	D2				В	2
				fet mismatch Nativenfet w/ sep sb; w=0.420; I=0.900;	Š	Ğ					,	- 52	D1	D2		В	1
			lowytpfet	fet mismatch LowVtpfet w/ sep sb; w=1.000; I=0.500;	S	G	D1	D1		İ						В	
			lowytpfet	fet mismatch LowVtpfet w/ sep sb; w=0.420; I=0.350;	S	G		<u> </u>	D1	D2						B	1 .
2627			lowytpfet	fet mismatch LowVtpfet w/ sep sb; w=0.420; l=0.350;	S	G					D1	D2				В	1 2
			lowytpfet	fet mismatch LowVtpfet w/ sep sb; w=0.420; I=0.350;	S	G							D1	D2		В	1
0004	1		npn bjt	NPN BJT (poly formed emitter, HV NPN) m=1	Ì	Psub	С	E	В								
2634	1 1		npn bjt	NPN BJT (poly formed emitter, HV NPN) m=1 mismatch						Psub	B2	E2	E1	B1	С		. 2
				nvhv symmetric mismatch:5/2.2, m=4	S	G	D1	D2								В	
2729				nvhv symmetric mismatch:20/2.2, m=4	S	G			D1	D2						В	. 2
2129			nvhv	nvhv symmetric mismatch:5/0.7, m=4	S	G					D1	D2				В	1 ′
			nvhv	nvhv symmetric mismatch:20/0.7, m=4	S	G							D1	D2		В	
			pvhv	pvhv symmetric mismatch:5/2.16, m=4	S	G	D1	D2								В	
2758			pvhv	pvhv symmetric mismatch:20/2.16, m=4	S	G			D1	D2						В	2
2750				pvhv symmetric mismatch:5/0.66, m=4	S	G					D1	D2				В	1 1
			pvhv	pvhv symmetric mismatch:20/0.66, m=4	S	G							D1	D2		В	
				HV n-chan gate oxide capacitor, no source/drain: large area													
	5			NDfif Area = 10 x 41.11 x 10.38 = 4,267.22um2	substrate	gate	substrate	gate	substrate	gate							
3012				NDiff perimeter = 10 x 2 x (41.11+10.38) = 1,029.8um		9-1-		3		3							2
	5			HV p-chan gate oxide capacitor, no source/drain: large area													
	5			NDfff Area = 10 x 43.025 x 9.77 = 4,203.54um2 NDiff perimeter = 10 x 2 x (43.025+9.77) = 1.055.9um							n-well	gate	n-well	gate	n-well	gate	
3051	1	cap		xcmvpo3	C0	C1		1		1						Psub	2
3052	1	Cap		xcmvpp4	CO	C1		<u> </u>	1							Psub	2
3053	_			xcmvpp5													
3054					CO	C1		 	1							Psuh	2
3055		<u> </u>			C0	C1 C1										Psub Psub	2
3056			xcmvpp4p4x4p6_m1m2	xcmvpp4p4x4p6_m1m2	C0	C1										Psub	2
3057			xcmvpp4p4x4p6_m1m2 xcmvpp11p5x11p7_m1m2	xcmvpp4p4x4p6_m1m2 xcmvpp11p5x11p7_m1m2	C0	C1 C1										Psub Psub	2
3181			xcmvpp4p4x4p6_m1m2 xcmvpp11p5x11p7_m1m2 xcmvpp11p5x11p7_m1m4	xcmvpp4p4x4p6 m1m2 xcmvpp1p6x1p7 m1m2 xcmvpp1p5x1p7 m1m4	C0 C0	C1										Psub Psub Psub	2 2 2
		can var lyt	xcmvpp4p4x4p6_m1m2 xcmvpp11p5x11p7_m1m2 xcmvpp11p5x11p7_m1m4 xcmvpp6	xcmypp4p4x4p6_m1m2 xcmypp1fpx1fp7_m1m2 xcmypp1fpx1fp7_m1m4 xcmypp6	C0 C0 C0	C1 C1 C1 C1	OPFN	OPEN	OPEN	OPEN	OPEN	OPFN	OPEN	WFII	GATF1	Psub Psub	2 2 2 2
3189		cap_var_lvt	xcmvpp4p4x4p6_m1m2 xcmvpp11p5x11p7_m1m2 xcmvpp11p5x11p7_m1m4	xzmrpp15p44p6_m1m2 xzmrpp11p5x11p7_m1m2 xzmrpp11p5x11p7_m1m4 xzmrpp6 Yaractor Mismatch (xcmvvc), WILM=50.51528 Matching Pair	C0 C0 C0 C0 Psub	C1 C1 C1 C1 OPEN	OPEN OPEN	OPEN OPEN	OPEN OPEN	OPEN OPEN	OPEN OPEN	OPEN OPEN	OPEN OPEN	WELL WELL	GATE1 GATE1	Psub Psub Psub Psub GATE2	2 2 2 2 2
3189 3213	5	cap_var_lvt cap_var_hvt	xcmvpp4p4x4p6_m1m2 xcmvpp11p5x11p7_m1m2 xcmvpp11p5x11p7_m1m4 xcmvpp6 xcmvvc xcnvvc	xcmypp4p4x4p6_m1m2 xcmypp1fpx1fp7_m1m2 xcmypp1fpx1fp7_m1m4 xcmypp6	C0 C0 C0	C1 C1 C1 C1			OPEN OPEN					WELL WELL		Psub Psub Psub Psub	2 2 2 2
3213	5 5	cap_var_lvt cap_var_hvt	xcmvpp4p4x4p6_m1m2 xcmvpp11p5x11p7_m1m2 xcmvpp11p5x11p7_m1m4 xcmvpp6 xcmvvp6 xcnwvc2	xcmvpp464496_m1m2 xcmvpp1fp5x1p7_m1m2 xcmvpp1fp5x1p7_m1m4 xcmvpp6 Vareactor Missmatch (xcmvvc), WILM=50.5528 Matching Pair Vareactor Missmatch (xcmvvc2), WILM=50.5528 Matching Pair	C0 C0 C0 C0 Psub Psub	C1 C1 C1 C1 OPEN										Psub Psub Psub Psub Psub GATE2 GATE2	2 2 2 2 2 2 2 2
	5 5 5	cap_var_lvt cap_var_lvt	xcmvpp4p4x4p6_m1m2 xcmvpp11p5x11p7_m1m2 xcmvpp11p5x11p7_m1m4 xcmvpp6 xcmvp6 xcnvvc2	xamopp16p4466, m1m2 xamopp11p6x11p7, m1m2 xamopp11p6x11p7, m1m4 xamopp1 xamopp	C0 C0 C0 C0 Psub Psub A	C1 C1 C1 C1 OPEN OPEN B	OPEN	OPEN	OPEN	OPEN						Psub Psub Psub Psub Psub GATE2 GATE2	2 2 2 2 2 2 2
3213		cap_var_lvt cap_var_lvt cap_var_lvt	xcmvpp4p4x4p6_m1m2 xcmvpp11p5x11p7_m1m2 xcmvpp11p5x11p7_m1m4 xcmvpp6 xcmvp6 xcnvvc2	zcmvpp4644466, m1m2 xcmvpp116x1167, m1m2 xcmvpp16x1167, m1m4 xcmvpp6 Varactor Mismatch (xcmvxc), WLLM=50.5528 Matching Pair Varactor Mismatch (xcmvxc2), WILM=50.5528 Matching Pair VPP. 50F 7 3x7 5 VPP. 50F 7 3x7 5 VPP. m5 OIF	C0 C0 C0 C0 Psub Psub A	C1 C1 C1 C1 OPEN OPEN B	OPEN	OPEN	OPEN	OPEN	OPEN	OPEN	OPEN	WELL	GATE1	Psub Psub Psub Psub Psub GATE2 GATE2 Psub	2 2 2 2 2 2 2 2
3213		cap_var_hvt	xcmvpp4p4x4p6_m1m2 xcmvpp11p5x11p7_m1m2 xcmvpp11p5x11p7_m1m4 xcmvp6 xcmvp6 xcmvvc2	xxmmpp16p4s4g6, m1m2 xxmmpp1fp4r1p2, m1m2 xxmmpp1fp4r1p2, m1m4 xxmmpp6 xxmmpp6 xxmmp6	C0 C0 C0 C0 Psub Psub A stub	C1 C1 C1 C1 OPEN OPEN B	OPEN Vp	OPEN	OPEN	OPEN	OPEN	OPEN	OPEN	WELL	GATE1	Psub Psub Psub Psub Psub GATE2 GATE2 Psub	2 2 2 2 2 2 2 2
3213		cap_var_hvt	xcmvpp4p4x4p6_m1m2 xcmvpp11p5x11p7_m1m2 xcmvpp11p5x11p7_m1m4 xcmvpp6 xcmvvc xcmvvc2 xcmvvc2	xxmmpsfp44466_m1m2 xxmwpsfp44466_m1m2 xxmwpsfp44466_m1m2 xxmwpsfp4156x11p7_m1m2 xxmwpp8 xxmwpsfp415x1p7_m1m4 xxmwpp8 xxmwpp8 xxmwpsfp415x1p7_m1m4 xxmwpp8 xxmwpsfp415x1p7_m1m4 xxmwpp8 xxmwpsfp415x1p7_m1m4 xxxmwpsfp415x1p7_m1m4 xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx	C0 C0 C0 C0 Psub Psub A stub	C1 C1 C1 C1 OPEN OPEN B	OPEN Vp	OPEN Vn	OPEN Vpwr	OPEN	OPEN	OPEN	OPEN	WELL	GATE1	Psub Psub Psub Psub Psub GATE2 GATE2 Psub	2 2 2 2 2 2 2 2
3213 3223		cap_var_hvt cap_var_hvt cap_var_hvt	xcmwpp4p4x4p6_m1m2 xcmvpp1fp5x11p7_m1m2 xcmvpp1fp5x11p7_m1m4 xcmvpp6 xcmwc1xcmvc2 xcmwc2 xcmwc2 xcmwc2	xcmvpp464496, m1m2 xcmvpp1f6x1167, m1m2 xcmvpp1f6x1167, m1m2 xcmvpp1f6x1167, m1m4 xcmvp66 xcmvp1f6x1167, m1m4 xcmvp66 xcmvpx1f6x1167, m1m4 xcmvp66 xcmvpx16x16x16x16x16x16x16x16x16x16x16x16x16x	C0 C0 C0 C0 C0 Psub Psub A stub Psub Psub Psub Psub Psub Psub Psub	C1 C1 C1 C1 OPEN OPEN B	OPEN Vp	OPEN Vn	OPEN Vpwr	OPEN Vgnd	OPEN stub	OPEN	OPEN	WELL	GATE1 Vpwr	Psub Psub Psub Psub Psub GATE2 GATE2 Psub Vgnd	2 2 2 2 2 2 2 2
3213 3223		cap_var_hvt cap_var_hvt cap_var_hvt	xcmvpp4p4x4p6_m1m2 xcmvpp11p5x11p7_m1m2 xcmvpp11p5x11p7_m1m4 xcmvpc2 xcmvvc2 xcmvvc2 xcmvvc2 xcmvvc2 xcmvvc2 xcmvvc2 xcmvvc2 xcmvvc2	xxmmpp15p44p6, m1m2 xxmmpp11p6x11p7 m1m2 xxmmpp11p6x11p7 m1m2 xxmmpp11p6x11p7 m1m4 xxmmpp1 xxm	C0 C0 C0 C0 Psub Psub A stub Psub Psub Psub Psub Psub Psub Psub	C1 C1 C1 C1 OPEN OPEN B	OPEN Vp	OPEN Vn	OPEN Vpwr	OPEN Vgnd	OPEN stub	OPEN load	OPEN Vp	WELL	GATE1	Psub Psub Psub Psub Psub GATE2 GATE2 Psub	2 2 2 2 2 2 2 2 2
3213 3223		cap_var_hvt cap_var_hvt cap_var_hvt cap_var_hvt cap_var_hvt	xcmwpp4p4s4g6, mfm2 xcmwpp1p6x1p7, m1m2 xcmwpp1p5x1p7, m1m4 xcmwp6 xcnwvc2 xcnwvc2 xcnwvc2 xcnwvc2 xcnwvc2 xcnwvc2 xcnwvc2 xcnwvc2 xcnwvc2 xcnwvc2	xcmvpp464496, m1m2 xcmvpp1f6x1167, m1m2 xcmvpp1f6x1167, m1m2 xcmvpp1f6x1167, m1m4 xcmvp66 xcmvp1f6x1167, m1m4 xcmvp66 xcmvpx1f6x1167, m1m4 xcmvp66 xcmvpx16x16x16x16x16x16x16x16x16x16x16x16x16x	C0 C0 C0 C0 C0 Psub Psub A stub Psub Psub Psub Psub Psub Psub Psub	C1 C1 C1 C1 OPEN OPEN B	OPEN Vp	OPEN Vn	OPEN Vpwr	OPEN Vgnd	OPEN stub	OPEN load	OPEN Vp	WELL	GATE1 Vpwr	Psub Psub Psub Psub Psub GATE2 GATE2 Psub Vgnd	2 2 2 2 2 2 2 2 2
3213 3223 3316		cap_var_hvt cap_var_hvt cap_var_hvt cap_var_hvt cap_var_hvt cap_var_hvt cap_var_hvt cap_var_hvt	xcmupp464466, m1m2 xcmupp116541p7, m1m4 xcmupp116541p7, m1m4 xcmupc xcmuvc2 xcmuvc2 xcmuvc2 xcmuvc2 xcmuvc2 xcmuvc2 xcmuvc2 xcmuvc2 xcmuvc2 xcmuvc2 xcmuvc2	xxmmpp15p44p6, m1m2 xxmmpp11p6x11p7, m1m2 xxmmpp11p6x11p7, m1m2 xxmmpp11p6x11p7, m1m4 xxmmpp1 xxmmp1 xxmmpp1 x	C0 C0 C0 C0 C0 Psub Psub Psub A stub Psub Psub Psub Psub Psub Psub Psub Ps	C1 C1 C1 C1 OPEN OPEN B load	OPEN Vp GATE	OPEN Vn	OPEN Vpwr	OPEN Vgnd WELL	OPEN stub	OPEN load	OPEN Vp	WELL	GATE1 Vpwr	Psub Psub Psub Psub Psub GATE2 GATE2 Psub Vgnd	2 2 2 2 2 2 2 2 2
3213 3223	5	cap_var_hvt cap_var_hvt cap_var_hvt cap_var_hvt cap_var_hvt cap_var_hvt cap_var_hvt	xcmyp4p4s4p6, m1m2 xcmyp1tp5x1tp7, m1m4 xcmyp6 xcmyp2tp5x1tp7, m1m4 xcmyp6 xcnwvc2 xcnwc2 xcnw	xmmyp6p4466_m1m2 xmmyp1fp6x1fp7_m1m2 xmmyp1fp6x1fp7_m1m2 xmmyp1fp6x1fp7_m1m4 xmmyp6 ymmyp1fp6x1fp7_m1m4 xmmyp6 ymmyp1fp6x1fp7_m1m4 ymmyp6m6m6x16x0mwc2), WiLM=50.5528 Matching Pair Varactor Mismatch (xcnwc2), WiLM=50.5528 Matching Pair VPP 50F 7.547.5 ymmyp7_m1m2 ymmyp7_	C0 C0 C0 C0 C0 Psub Psub A stub Psub Psub Psub Psub Psub Psub Psub Ps	C1 C1 C1 C1 OPEN OPEN B load	OPEN Vp GATE	OPEN Vn WELL	OPEN Vpwr GATE	OPEN Vgnd	OPEN stub	OPEN load	Vp GATE	WELL	GATE1 Vpwr	Psub Psub Psub Psub Psub GATE2 GATE2 Psub Vgnd	2 2 2 2 2 2 2 2 2
3213 3223 3316	5	cap_var_int cap_var_int cap_var_int cap_var_int cap_var_int cap_var_int cap_var_int cap_var_int cap_var_int	xcmyp4p4s4p6, m1m2 xcmyp1tp5x1p7, m1m2 xcmyp1tp5x1p7, m1m4 xcmyp2 xcmwc2	xxmmpp1p54496, m1m2 xxmmpp1p54496, m1m2 xxmmpp1p54496, m1m2 xxmmpp1p54497, m1m2 xxmmpp1p544197, m1m4 xxmmpp6 xxmmp6	CO CO CO CO CO Psub Psub A Stub Psub Psub Psub Psub Psub Psub Psub Ps	C1 C1 C1 C1 OPEN OPEN B load	OPEN Vp GATE	OPEN Vn WELL	OPEN Vpwr GATE	OPEN Vgnd WELL	OPEN stub	OPEN load	OPEN Vp	Vn WELL	Vpwr GATE	Psub Psub Psub Psub Psub Psub GATE2 GATE2 Psub Vgnd	2 2 2 2 2 2 2 2 2 2 2
3213 3223 3316	5	cap_var_int cap_var_int cap_var_int cap_var_int cap_var_int cap_var_int cap_var_int cap_var_int cap_var_int cap_var_int cap_var_int cap_var_int cap_var_int cap_var_int cap_var_int cap_var_int cap_var_int cap_var_int cap_var_int	xcmyp4p4s4s6, m1m2 xcmyp1tp5x1p7, m1m4 xcmyp2tp5x1p7, m1m4 xcmyp2 xcmwc2	xxmmpp15p44p6, m1m2 xxmmpp1 fp6x11p7 m1m2 xxmmpp1 fp6x11p7 m1m2 xxmmpp1 fp6x11p7 m1m4 xxmmpp6 xxmmpp1 fp6x11p7 m1m4 xxmmpp6 xxmmpp1 fp6x11p7 m1m4 xxmmpp6 xxmmpc6 xxmmpc1 m1m2 m1m2 m1m2 m1m2 m1m2 m1m2 m1m2 m1	CO CO CO CO CO Psub Psub A stub Psub Psub Psub Psub Psub Psub Psub Ps	C1 C1 C1 C1 OPEN OPEN B load	OPEN Vp GATE	OPEN Vn WELL	OPEN Vpwr GATE	OPEN Vgnd WELL	OPEN stub	OPEN load	Vp GATE	WELL	GATE1 Vpwr GATE	Psub Psub Psub Psub Psub Psub GATE2 GATE2 GATE2 Psub Vgnd OPEN	2 2 2 2 2 2 2 2 2 2 2
3213 3223 3316	5	cap_var_hvt cap_var_hvt cap_v	xcmypep4s4s6, mlm2 xcmype1fs2n7, mlm2 xcmype1fs2n1p7, mlm4 xcmype1 xcmype2 xcmype3	xxmmpp16p4s466_m1m2 xxmmpp16p4s466_m1m2 xxmmpp16p4s466_m1m2 xxmmpp16p4s466_m1m2 xxmmpp16p4s466_m1m4 xxmmpp6 xxmmp6p4	CO CO CO CO CO Psub Psub A Stub Psub Psub Psub Psub Psub Psub Psub Ps	C1 C1 C1 C1 C1 C9 PEN OPEN B load WELL WELL	OPEN Vp GATE GATE	OPEN Vn WELL	OPEN Vpwr GATE	OPEN Vgnd WELL	OPEN stub	OPEN load	Vp GATE	Vn WELL	GATE1 Vpwr GATE GATE GATE nw_fing	Psub Psub Psub Psub Psub Psub GATE2 GATE2 Psub Vgnd OPEN OPEN Psub	2 2 2 2 2 2 2 2 2 2 2
3213 3223 3316 3320	5	cap_var_int cap_var_int cap_v	xcmupp4p4s4s6, m1m2 xcmupp1tp5x1p7, m1m4 xcmupp1tp5x1p7, m1m4 xcmupc xcmwc2 xcmwc2 xcmwc2 xcmwc2 xcmwc2 xcmwc2 xcmwc2 xcmwc2 xcmwc2 xcmwc	xxmmpp16p4466_m1m2 xxmmpp1 fp6x11p7_m1m2 xxmmpp1 fp6x11p7_m1m2 xxmmpp1 fp6x11p7_m1m4 xxmmpp6 xxmmp1 fp6x11p7_m1m4 xxmmpp6 xxmmp6	CO CO CO CO CO Psub Psub A stub Psub Psub Psub Psub Psub Psub Psub Ps	C1 C1 C1 C1 C1 OPEN OPEN OPEN B load WELL	OPEN Vp GATE GATE GATE	OPEN Vn WELL	OPEN Vpwr GATE GATE	OPEN Vgnd WELL	OPEN stub	OPEN load	Vp GATE	Vn WELL	GATE Vpwr GATE GATE GATE mw_ring nw_ring	Psub Psub Psub Psub Psub Psub Psub Psub	2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2
3213 3223 3316	5	cap_var_int cap_var_int cap_v	xcmyp4p4s4p6, m1m2 xcmyp1tp5x1tp7, m1m4 xcmyp2t xcmyp2tp5x1tp7, m1m4 xcmyp2 xcmvc2 xcm	xmmpp6p4s466_m1m2 xmmpp1p6s14p6_m1m2 xmmpp1p6s14p6_m1m2 xmmpp1p6s14p7_m1m2 xmmpp1p6s14p7_m1m4 xmmpp6 ymmpp1p6s14p7_m1m4 xmmpp6 ymmpp1p6s14p7_m1m4 ymmpp1p6s14p7_m1m4 ymmpp1p6s14p7_m1m5s15p8 ymmpp1p6s14p7_m1m5s15p8 ymmpp1p6s14p7_m1m5s15p8 ymmpp1p6s14p8_m1m5s15	CO CO CO CO CO Psub Psub A stub Psub Psub Psub Psub Psub Psub Psub Ps	C1 C1 C1 C1 C1 C9 PEN OPEN B load WELL WELL	OPEN Vp GATE GATE	OPEN Vn WELL	OPEN Vpwr GATE GATE	OPEN Vgnd WELL	Stub GATE GATE	OPEN load	Vp GATE	Vn WELL	GATE1 Vpwr GATE GATE Rw. jring nw. jring nw. jring nw. jring	Psub Psub Psub Psub Psub Psub Psub GATE2 GATE2 Psub Vgnd OPEN OPEN Psub Psub Psub Psub	2 2 2 2 2 2 2 2 2 2 2
3213 3223 3316 3320	5	cap_var_hvt cap_var_hvt cap_v	xcmupp4p4s4p6, m1m2 xcmupp1tp5x1p7, m1m4 xcmupp1tp5x1p7, m1m4 xcmupp xcmupp1tp5x1p7, m1m4 xcmupp xcmuvc2 xcmuv	xxmmpp1p6x4q6, m1m2 xxmmpp1p6x1p6.m1m2 xxmmpp1p6x1p7.m1m2 xxmmpp1p6x1p7.m1m2 xxmmpp1p6x1p7.m1m4 xxmmpp6 xxmmpp1p6x1p7.m1m4 xxmmpp6 xxmmp6	CO CO CO CO CO Psub Psub A stub Psub Psub Psub Psub Psub Psub Psub Ps	C1 C1 C1 C1 C1 C9 PEN OPEN B load WELL WELL	OPEN Vp GATE GATE GATE	OPEN Vn WELL	OPEN Vpwr GATE GATE	OPEN Vgnd WELL	GATE GATE GATE	OPEN load	Vp GATE	WELL Vn WELL	GATE Vpwr GATE GATE nw_ring nw_ring nw_ring nw_ring	Psub Psub Psub Psub Psub Psub Psub Psub	2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2
3213 3223 3316 3320	5	cap_var_int cap_var_int cap_v	xcmyp4p4s4p6, m1m2 xcmyp1tp5x1p7, m1m4 xcmyp2tp5x1p7, m1m4 xcmyp2 xcmwc2 xcmwc2 xcmwc2 xcmwc2 xcmwc2 xcmwc2 xcmwc2 xcmwc2 xcmwc xcmw	xmmpp16p4496, m1m2 xmmpp1 fp6x11p7 m1m2 xmmpp1 fp6x11p7 m1m2 xmmpp1 fp6x11p7 m1m2 xmmpp1 fp6x11p7 m1m4 xmmpp6	CO CO CO CO CO Psub Psub A stub Psub Psub Psub Psub Psub Psub Psub Ps	C1 C1 C1 C1 C1 CPEN OPEN OPEN B load WELL WELL r0	OPEN Vp GATE GATE GATE	OPEN Vn WELL	OPEN Vpwr GATE GATE	OPEN Vgnd WELL	Stub GATE GATE	OPEN load	Vp GATE	WELL Vn WELL WELL	GATE Vpwr GATE GATE M. ring nw_ring nw_ring nw_ring nw_ring nw_ring nw_ring	Psub Psub Psub Psub Psub Psub Psub Psub	2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2
3213 3223 3316 3320	5	cap_var_hvt cap_var_hvt cap_v	xcmyp4p4s4p6, m1m2 xcmyp1tp5x1p7, m1m4 xcmyp2tp5x1p7, m1m4 xcmyp2 xcmwc2 xcmwc2 xcmwc2 xcmwc2 xcmwc2 xcmwc2 xcmwc2 xcmwc2 xcmwc xcmw	xzmmpp1p6x4g6_m1m2 xzmmpp1p6x1p2, m1m2 xzmmpp1p6x1p2, m1m2 xzmmpp1p6x1p2, m1m2 xzmmpp1p6x1p2, m1m4 xzmmpp6 xzmmp6x1p6x1p2, m1m4 xzmmpp6 xzmmp6x1p6x1p2, m1m4 xzmmp6x xzmmp6x1p2, m2m2 xzmmp6x1p2, xzmmp6x1p2, xzmmp6x1p2, xzmmp6x1p2, xzmmp6x1p2, xzmmp6x1p2, x	CO CO CO CO CO CO CO CO CO CO CO CO CO C	C1 C1 C1 C1 C1 OPEN OPEN OPEN B load WELL WELL V-meas	OPEN Vp GATE GATE GATE	OPEN Vn WELL	OPEN VpMr GATE GATE GATE	OPEN Vgnd WELL WELL	GATE GATE GATE	OPEN load	Vp GATE	WELL Vn WELL	GATE Vpwr GATE GATE nw_ring nw_ring nw_ring nw_ring	Psub Psub Psub Psub Psub Psub Psub Psub	2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2
3213 3223 3316 3320 3350	5	cap_var_hvt cap_var_hvt cap_v	xcmyp4p4s4p6, m1m2 xcmyp1tp5x1p7, m1m4 xcmyp2tp5x1p7, m1m4 xcmyp2 xcmwc2 xcmwc2 xcmwc2 xcmwc2 xcmwc2 xcmwc2 xcmwc2 xcmwc2 xcmwc xcmw	xmmpp1p6x4p6, m1m2 xmmpp1p6x1p7 m1m2 xmmpp1p6x1p7 m1m2 xmmpp1p6x1p7 m1m2 xmmpp1p6x1p7 m1m4 xmmpp6 ymmp1p6x1p7 m1m4 ymmpp1p6x1p7 m1m4 ymmpp1p6x1p7 m1m4 ymmpp1p6x1p7 m1m4 ymmpp1p6x1p7 m1m4 ymmpp1p6x1p7 ymmpp	CO CO CO CO CO Psub Psub A stub Psub Psub Psub Psub Psub Psub Psub Ps	C1 C1 C1 C1 C1 CPEN OPEN OPEN B load WELL WELL r0	OPEN Vp GATE GATE GATE	OPEN Vn WELL	OPEN Vpwr GATE GATE	OPEN Vgnd WELL	GATE GATE GATE 10 11	OPEN load WELL WELL	OPEN Vp GATE GATE	WELL Vn WELL WELL	GATE Vpwr GATE GATE M. ring nw_ring nw_ring nw_ring nw_ring nw_ring nw_ring	Psub Psub Psub Psub Psub Psub Psub Psub	2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2
3213 3223 3316 3320	5	cap_var_hvt cap_var_hvt cap_v	xcmyp4p4s4p6, m1m2 xcmyp1tp5x1p7, m1m4 xcmyp2tp5x1p7, m1m4 xcmyp2 xcmwc2 xcmwc2 xcmwc2 xcmwc2 xcmwc2 xcmwc2 xcmwc2 xcmwc2 xcmwc xcmw	xzmmpp1p6x4g6_m1m2 xzmmpp1p6x1p2, m1m2 xzmmpp1p6x1p2, m1m2 xzmmpp1p6x1p2, m1m2 xzmmpp1p6x1p2, m1m4 xzmmpp6 xzmmp6x1p6x1p2, m1m4 xzmmpp6 xzmmp6x1p6x1p2, m1m4 xzmmp6x xzmmp6x1p2, m2m2 xzmmp6x1p2, xzmmp6x1p2, xzmmp6x1p2, xzmmp6x1p2, xzmmp6x1p2, xzmmp6x1p2, x	CO CO CO CO CO CO CO CO CO CO CO CO CO C	C1 C1 C1 C1 C1 OPEN OPEN OPEN B load WELL WELL V-meas	OPEN Vp GATE GATE GATE	OPEN Vn WELL	OPEN VpMr GATE GATE GATE	OPEN Vgnd WELL WELL	GATE GATE GATE	OPEN load	Vp GATE	WELL Vn WELL WELL	GATE Vpwr GATE GATE M. ring nw_ring nw_ring nw_ring nw_ring nw_ring nw_ring	Psub Psub Psub Psub Psub Psub Psub Psub	2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2

Mod#	Group	New Style Name	Old Style Name	Description	Pin 01	Pin 02	Pin 03	Pin 04	Pin 05	Pin 06	Pin 07	Pin 08	Pin 09	Pin 10	Pin 11	Pin 12	Die Row
				S8Q/S8P WM3 w/ dense dummy lines - 0.3 x 450 long - Pad2 - Pad5	I1	V1			V2	12							
3374				S8P RSM3_Kelvin (Width = 2.595um/ Length = 434.755um), # of squares = 167.54							I1	12	V1			V2	2
				S8P WM3 Kelvin (Width = 0.3um/ Length = 418.375um), # of squares = 1394.58						1	I1	12		V1	V2		-
				S8PIR/PF WM5 w/ dense dummy lines - 1.6 x 450 - Pad2 - Pad5:	I1	V1			V2	12							+-
3376				S8PIR/PF RSM5_Kelvin (Width = 2.4um/ Length = 353.4um)							l1	12	V1			V2	2
				S8PIR/PF WM5_Kelvin (Width = 1.6um/ Length = 223.6um)							l1	12		V1	V2		
3379		-		RSRP - 2K ohm/sq poly resistor sheet resistance: VDP RSRP - 300 ohm/sq poly resistor sheet resistance: VDP			V-meas	V-meas	force I	force I		substrate substrate	V-meas	V-meas	force I	force I	2
0.470	10			BVM3M3F	serp	comb	serp	comb	serp	comb		GGGGGGG					-
3470	10			BVM3M3T,BVM3M2							serp	comb	serp	comb	serp	metal2	2
3472	10			serpentine-0.3 micron wide RSLNM3F - 10,143 squares RSLNM3T - 10,143 squares - between each pad - s8q	flat serp	flat serp	flat serp	flat serp	flat serp	flat serp	top serp	top serp	top serp	top serp	top serp	metal2	2
				RSM3 - 1.5 x 450 long - Pad2 -7	I1	V1				 	V2	12					
3475	2			S8P RSM3 (Van der Pauw Structure 30*30um2)									I1	12	V1	V2	2
3478	3			RCVIA2,RCVIA2K - RCVIA has 16,500 vias in chain - S8Q 4125 M2 squares between each pad	chain 3300	chain 3300	chain 3300	chain 3300	chain 3300	chain end	V1	I1	V2	12			2
34/8	3			3509 M3 squares between each pad													2
3521	6			SNM module (single dut in array)	sub	nwell	unused BL / BLB	unused WL	tru	BLB	BL	bar	WL	Vcc	Vss	pwell	2
3767				s8pf M5 (w=1.6) serpentine (#sq=582.4) over field (S8PF RSLNM5)	A	serp	serp	serp	serp	В							2
	-			s8pf M5 (w=1.6) serpentine (#sq=582.4) over M4 grid (S8PF RSLNM5T) s8pf via4 (0.8x0.8) via chain (270 vias per array, 5 arrays 1350 total vias) m5 width/space 1.6	A	oboin	chain	chain	chain	В	A	serp	serp	serp	В	m4 grid	+
3768				sopt via4 (0.8x0.8) via chain (270 vias per array, 5 arrays 1350 total vias) m5 width/space 1.6 s8pf via4 (0.8x0.8) kelvin (m5 width 1.6)	A	chain	cnain	cnain	cnain	В	force a	sense a	force b	sense b			2
3770				s8p via3 (0.2x0.2) contact chain (16500 contacts)	A	chain	chain	chain	chain	В							2
3//0				s8p via3 (0.2x0.2) kelvin							force a	sense a	force b	sense b			
3782				s8p M4 (w=0.3) serp / comb over field (S8P BVM4M4) s8p M4 (w=0.3) serp / comb over M3 grid (S8P BVM4M3)	serp	comb	serp	comb	serp	comb	serp	comb	serp	comb	serp	m3 grid	2
				s8pir/pf M5 (w=1.6) serp / comb over field (S8PIR/PF BVM5M5)	serp	comb	serp	comb	serp	comb	3619	COITE	3619	COIID	зыр	iio giid	+
3789				s8pir/pf M5 (w=1.6) serp / comb over M4 grid (S8PIR/PF BVM5M4)							serp	comb	serp	comb	serp	m4 grid	2
		sky130_fd_presd_nfet_g5v0d10v5		nhvesd sym 5.40 0.600	Body	Gate	Src	Drn									_
		sky130_fd_pr_esd_nfet_g5v0d10v5		nhvesd sym 17.50 0.550	Body	Gate		Src	Drn								_
		sky130 fd pr esd nfet g5v0d10v5 sky130 fd pr esd nfet g5v0d10v5	nhvesd	nhvesd sym 19.50 0.550	Body	Gate Gate			Src	Dm Src	Dm						-
4040		sky130_fd_presd_nfet_g5v0d10v5		nhvesd sym 23.50 0.550	Body Body	Gate				Sic	Src	Dm					- 2
		sky130_fd_presd_nfet_g5v0d10v5	nhvesd	nhvesd sym 26.50 0.550	Body	Gate						Src	Dm				-
		sky130_fd_presd_nfet_g5v0d10v5		nhvesd sym 30.25 0.550	Body	Gate							Src	Dm			
		sky130 fd_pr_esd_nfet_g5v0d10v5 sky130 fd_pr_esd_nfet_g5v0d10v5	nhvesd	nhvesd asym 17.50 0.550 nhvesd asym 19.50 0.550	Body Body	Gate Gate				ļ				Src	Drn Src	Drn	
		sky130_fd_presd_pfet_g5v0d10v5		phyesd sym 14.50 0.550 (100x1080)	Body	Gate	Src	Drn							SIC	Dill	+
		sky130_fd_presd_pfet_g5v0d10v5		phyesd sym 15.50 0.550 (100x1080)	Body	Gate	- Oic	Src	Drn								-
		sky130_fd_presd_pfet_g5v0d10v5	phyesd	phyesd sym 16.50 0.550 (100x1080)	Body	Gate			Src	Dm							
4043		sky130_fd_presd_pfet_g5v0d10v5		phyesd sym 17.50 0.550 (100x1080)	Body	Gate				Src	Dm						2
		sky130_fd_presd_pfet_g5v0d10v5 sky130_fd_presd_pfet_g5v0d10v5	phvesd phvesd	phvesd sym 19.50 0.550 (100x1080) phvesd sym 21.50 0.550 (100x1080)	Body Body	Gate Gate				.	Src	Drn Src	Drn				-
		sky130 fd pr esd pfet g5v0d10v5		phyesd sym 23.50 0.550 (100x1000)	Body	Gate				 		JIC JIC	Src	Dm			-
		sky130_fd_presd_pfet_g5v0d10v5	phvesd	phvesd sym 26.50 0.550 (100x1080)	Body	Gate								Src	Drn	NC	
			nshortesd	nshortesd sym 5.40 0.180	Body	Gate	Src	Drn		ļ							
4044			nshortesd nshortesd	nshortesd sym 20.35 0.165 Inshortesd asym 20.35 0.165	Body Body	Gate Gate		Src	Drn Src	Dm							2
			nshortesd	nshortesd sym 40.31 0.165 (100x1080)	Body	Gate			- Gr	Src	Dm						1 -
			nshortesd	nshortesd asym 40.31 0.165 (100x1080)	Body	Gate					Src	Dm					
			nhvesd	nhvesd asym 21.50 0.550	Body	Gate	Src	Drn									_
			nhvesd nhvesd	nhvesd asym 23.50 0.550 nhvesd asym 26.50 0.550	Body Body	Gate Gate		Src	Drn Src	Dm							-
4045			nhvesd	nhvesd asym 30.25 0.550	Body	Gate			OIL.	Src	Dm						2
			nhvesd	nhvesd sym 30.25 1.000	Body	Gate					Src	Drn					_
			nhvesd	nhvesd asym 30.25 1.000	Body	Gate						Src	Dm				4
	ļ		nhvesd	nhvesd sym 40.31 0.550 (100x1080)	Body	Gate	Src	Drn	ļ				1				- '
			nhvesd	nhvesd sym 50.99 0.550 (100x1080) nhvesd asym 40.31 0.550 (100x1080)	Body Body	Gate Gate		Src	Drn Src	Dm	 		<u> </u>		<u> </u>		-
4046			nhvesd	nhvesd asym 50.99 0.550 (100x1080)	Body	Gate			1	Src	Dm						2
			nhvesd	nhvesd sym 50.99 1.000 (100x1080)	Body	Gate					Src	Drn					
			nhvesd	nhvesd asym 50.99 1.000 (100x1080)	Body	Gate						Src	Dm		1		+
4100	6			2T Flash EEPROM Cell Rev 2 Mini-Array FET W/Lsonos/Lnpass = 0.45/0.22/0.15	DNW	Pwell	Psub	WLS1	WL1	WLS2	WL2	SRC2	BL2	SRC1	BL1	Ring	2
		1	I	pres incomorcinguo diferezzio.10	DITT	I WOII	1 000	WEO!	1 1101	11102	1 1164	01102	I DEE	ONOT	I DE1	ı ıving	

Mod#	Group	New Style Name	Old Style Name	Description	Pin 01	Pin 02	Pin 03	Pin 04	Pin 05	Pin 06	Pin 07	Pin 08	Pin 09	Pin 10	Pin 11	Pin 12	Die Row
				SONOS Rev 2: 25/0.5	В	G	S	DNW	D								
				SONOS Rev 2: 1/0.5 SONOS Rev 2: 1/0.6	B B	G G	S	DNW		D	D D						
				SONOS Rev 2: 1/0.4	R	G		DNW				n					-
4144	4			SONOS Rev 2: 1/1	В	G	S	DNW					D				2
				SONOS Rev 2: 1,2/0.5	В	G	S	DNW						D			1
				SONOS Rev 2: 0.8/0.5	В	G	S	DNW			-				D		1 1
				SONOS Rev 2: 1/25	В	G	S	DNW								D	1
				SONOS Rev 2: 25/0.15	В	G	S	DNW	D								
				SONOS Rev 2: 2/0.15	В	G	S	DNW		D							
				SONOS Rev 2: 0.45/0.15	В	G	S	DNW			D						-
4146	4			SONOS Rev 2: 0.45/2 SONOS Rev 2: 2/2	B B	G G	S	DNW			ļ	D	D				. 2
				SONOS Rev 2: 2/2 SONOS Rev 2: 25/2	B B	G	S	DNW					U	D			-
				SONOS Rev 2: 0.45/25	B B	G		DNW						U	D		-
				SONOS Rev 2: 2/25	B	G	s s	DNW								D	-
				SONOS Rev 2: 25/0.22	В	G	S	DNW	D							_	†
				Flash Npass Rev 2: 0.45/0.17	В	G	S	DNW		D							1
				Flash Npass Rev 2: 0.45/0.15	В	G	S	DNW			D						1
4147	4			Flash Npass Rev 2: 0.45/0.13	В	G	S	DNW				D					. 2
4147	, ,			SONOS Rev 2: 0.45/0.26	В	G	S	DNW					D				.] '
l				SONOS Rev 2: 0.45/0.18	В	G	S	DNW						D			
				SONOS Rev 2: 0.45/0.22	В	G	S	DNW							D		
ļ				SONOS Rev 2: 25/25	В	Ğ	S	DNW			-	+	-	1	+	D	-
				SONOS Rev 2 w/o DNW: 25/0.5 SONOS Rev 2 w/o DNW: 1/0.5	B B	G G	8	Nwell Nwell	D	D		-					-
				SONOS Rev 2 w/o DNW: 1/0.5 SONOS Rev 2 w/o DNW: 1/0.6	B R	G	8	Nwell		<u>υ</u>	D	+	 				1
				SONOS Rev 2 w/o DNW: 1/0.4	B R	G	S	Nwell			1	D					-
4148	4			SONOS Rev 2 w/o DNW: 1/1	В	G	Š	Nwell			†	†	D				. 2
				SONOS Rev 2 w/o DNW: 1.2/0.5	В	G	S	Nwell			-			D			1
				SONOS Rev 2 w/o DNW: 0.8/0.5	В	G	S	Nwell							D		
				SONOS Rev 2 w/o DNW: 1/25	В	G	S	Nwell								D	
4149	5			SONOS Rev 2 Capacitor, Area Intensive													. 2
41.40	Ů			Area = 15,669.5, Perimeter = 770	В	S/D										G	
				2T Flash Cell Rev 2 Array, 11,264 cells							ļ						-
				FET W/Lsonos/Lnpass = 0.45/0.22/0.15 BL to SRC Leakage Structure	DNW	Pwell	Psub				ļ	WLSA	WLA	SRCA	BLA	Dia-	
4150	6			Poly Resistance of WLS and WL	DINVV	PWell	PSUD			WLB	WLSB	WLSA	WLA	SKLA	DLA	Ring	. 2
4130	0			Met1 Resistance of BL and SRC		Pwell		BLB	SRCB	WLD	WLOD	WLOA	WLA	SRCA	BLA	Ring	- 4
				BV of Poly WLS to BL	•	1 1101	······································	DED	OI OD		-	WLSA		ORON	BLA	Tally	-
				BV of Poly WL to SRC							-		WLA	SRCA			1
				2T Flash Cell Rev 2 FETs													
4151	6			Flash Npass: 0.45/0.15 w/ Breakout Licon	DNW	В	Psub		G					S	D	Ring	2
				Flash Npass: 0.45/0.15 w/ Breakout Licon	DNW	В	Psub		G			S	D			Ring	
				2T Flash Cell Rev 2 FETs													
4152	6			Flash Npass: 0.45/0.15 w/o SONOS	DNW	В	Psub		G		ļ	1		S	D	Ring	2
				Flash Npass: 0.45/0.15 w/o SONOS SONOS Rev 2 Capacitor, Perim. Intensive	DNW	В	Psub				G	S	D	1	1	Ring	+
4157	5			Area = 5967.5. Perimeter = 23870	B	S/D					 		+			G	- 2
	s8tet			s8tet_s_hvn_iso_nw_dnw_sti_2p0_esd_IP	Psub	G	P-body	S	D			+		1	NC	NC NC	+
			n20vhv1	n20vhv1 (s8tet s hvn nw dnw sti 3p0 IP): ETD, E-test	Psub	G	. 555,	1	"	s	D	1			NC NC	NC NC	
4441			n20vhviso1	n20vhviso1 (s8tet s hvn iso nw dnw sti 2p0 esd DR2 IP): ETD, E-test	Psub	G			1		1	s	D	P-body	NC NC	NC NC	2
				the site of energians and find										,	NC	NC	
	s8tet		p20vhv1	p20vhv1 (s8tet_s_hvp_pwde_stdnw_sti_1p5_2f_60um_IP_LVS)	Psub	G	N-body	S	D								
4442				s8tet_s_hvp_pwde_stdnw_sti_2p0_2f_60um_IP	Psub	G			1	S	D	1 .	_			N-body	2
				s8tet_s_hvp_pwde_stdnw_sti_1p0_2f_60um_IP_LVS	Psub	G			1			S	D	_		N-body	
	-01-1		-00 4	s8tet_s_hvp_pwde_stdnw_sti_1p5_2f_60um_s8t18_end_IP	Psub	G	NI L	1				+	-	8	D	N-body	+
	s8tet		p20vhv1	p20vhv1 (s8tet_s_hvp_pwde_stdnw_sti_1p5_2f_60um_IP_LVS)	Psub Psub	G	N-body	S	D	s	D	1				N bads	
4443				s8tet_s_hvp_pwde_stdnw_sti_2p0_2f_60um_IP s8tet_s_hvp_pwde_stdnw_sti_1p0_2f_60um_IP_LVS	Psub Psub	G G			1		۵ ا	s	D			N-body N-body	2
				satet_s_nvp_pwde_stanw_sti_1pu_zf_buum_iP_LvS satet_s_hvp_pwde_stanw_sti_1p5_zf_60um_sat18_end_IP	Psub	G			1			"	"	s	D	N-body N-body	
			n20zvtvhv1	n20zvtvhv1; w/l=30/5.5; m=2; s8defet_ccgx_hvn_nw_dnw_native_sti_2p0_nopw_L5p0_W60	Psub	G	S	D				1		<u> </u>		,	\vdash
			n20zvtvhv1	n20zvtvhv1; w/i=30/5.5; m=2; s8defet_ccgx_hvn_nw_dnw_native_sti_2p0_nopw_L5p0_W60	Psub	G	, , , , , , , , , , , , , , , , , , ,	†	S	D	t	<u> </u>	†				1
4451	s8tet		n20zvtvhv1	n20zvtvhv1; w/l=30/5.5; m=2; s8defet_ccgx_hvn_nw_dnw_native_sti_2p0_nopw_L5p0_W60	Psub	G		1	1	1	S	D					. 2
			n20zvtvhv1	n20zvtvhv1; w/l=30/5.5; m=2; s8defet_ccgx_hvn_nw_dnw_native_sti_2p0_nopw_L5p0_W60	Psub	G		<u> </u>			-	<u> </u>	S	D			1
			n20zvtvhv1	n20zvtvhv1; w/l=30/5.5; m=2; s8defet_ccgx_hvn_nw_dnw_native_sti_2p0_nopw_L5p0_W60	Psub	G									S	D	

Mod #	Group	New Style Name	Old Style Name	Description	Pin 01	Pin 02	Pin 03	Pin 04	Pin 05	Pin 06	Pin 07	Pin 08	Pin 09	Pin 10	Pin 11	Pin 12	Die Row
4530				Large MiM capacitor, CAPM on M3, 11 plates, each 40x40.	BOT plate	TOP plate	open	open	open	open	open	open	open	open	open	open	2
4030				Total A = 17600, P = 1760. Total expected capacitance 35.5 pF			·			· ·		· ·					
				Periphery-intensive MiM cap, CAPM on M3. 72 plates each 2x35.	BOT plate	TOP plate	open	open	open	open							T
4532				Total A = 5040, P = 5328. Total expected capacitance = 11.1 pF													2
4002				Area-intensive MiM cap, CAPM on M3. 5 plates each 35x35.							BOT plate	TOP plate	open	open	open	open	1 *
				Total A = 6125, P = 700. Total expected capacitance = 12.4 pF													↓
				Via-3 array, M4-M3 near CAPM (min via-3 space to CAPM)	CAPM	M4-M3	open	open	open	open							
4534				For Via Shorts, 1120 vias, each in 2x2 arrays inside holes in CAPM	(force low)	(force hi)											_ 2
				For Cap Meas, total A = 5196.8, P=5196.8. Expected cap = 11.4 pF Via-3 chain. 5754 via-3. M4-CAPM over M3 (min via enclosure)	(force hi)	(force low)					F					F 15:1	
				CAPM linewidth. L/W = 500/2.0	F	F10			Meas LO		Force Low					Force High	+
				CAPM linewidth, L/W = 500/2.0 CAPM linewidth, L/W = 400/1.0	Force HI	Force LO	Meas HI	Meas LO	Meas LO	Meas HI							-1
4536				Kelvin via-3. M4-CAPM over M3	roice ni	Poice LO	-	Meas LO		Meas ni	force A	sense A	force B	sense B			2
				CAPM sheet rho, L/W = 45/4.5				+			IOICE A	Serise A	IOICE B	Selise b	High Pin	Low Pin	-
		1		M3-M3 serp/comb structure, M3 is under CAPM at min TDR S = 1.2	Serp HI	Comb	open	open	open	open	open	Serp LO	1		Highrin	LUW FIII	+
				Total defect sensitive length = 2480 um	Odipini	Comb	ороп	open	Орен	Орен	Орен	OGIPEO					
4538				CAPM-CAPM serp/comb structure									Serp LO	Comb	Comb	Serp HI	_ 2
				Total defect sensitive length = 1005 um										(sht to 11)	(sht to 10)		
				Large MiM2 capacitor, CAP2M over M4, 11 plates, each 40x40.	BOT plate	TOP plate	open	open	open	open	open	open	open	open	open	open	+
4541				Total A = 17600. P = 1760. Total expected capacitance 35.5 pF		TO PILL		1	1	,	,						2
		i	Ì	Periphery-intensive MiM2 cap, CAP2M over M4. 72 plates each 2x35. Total A = 5040, P = 5328. Total	BOT plate	TOP plate	open	open	open	open			İ				1
4542				expected capacitance = 11.1 pF	· ·		·			· ·							2
4342				Area-intensive MiM2 capacitor, CAP2M over M4. 5 plates each 35x35.							BOT plate	TOP plate	open	open	open	open	1 1
				Total A = 6125, P = 700. Total expected capacitance = 12.4 pF													↓
				Via-4 array, M5-M4 near CAP2M (minimum via-4 space to CAP2M)	CAPM	M4-M3	open	open	open	open							
4543				For Via Shorts, 160 vias, each inside holes in CAPM	(force low)	(force hi)											3
				For cap meas, total A = 6054, P=6653. Expected cap = 13.4 pF	(force hi)	(force low)					l						
				Via-4 chain, 1392 via-4, M5-CAP2M over M4 (min via enclosure)							Force Low					Force High	+
				CAP2M linewidth, LW = 500/2.0 CAP2M linewidth, LW = 400/1.0	Force HI	Force LO	Meas HI		Meas LO	Meas HI							4
4544				CAP2M Innewidth, L/W = 400/1.0 Kelvin via-4. M5-CAP2M over M4	Force HI	Force LO		Meas LO		Meas HI	force A	sense A	force B	sense B			3
				CAP2M sheet rho 1 W = 45/4 5				_			Torce A	sense A	TOICE B	sense B	High Pin	Low Pin	-
				M4-M4 sero/comb structure. M4 is under CAP2M at min TDR S = 1.0	Serp HI	Comb	open	open	open	open	open	Serp LO	1	1	nigii Pili	LOW PIRI	+
				Total defect sensitive length = 2480 um	Odipini	Comb	ороп	open	Орен	Орен	Орен	OGIPEO					
4545				CAP2M-CAP2M serp/comb structure					_				Serp LO	Comb	Comb	Serp HI	3
				Total defect sensitive length = 1005 um									00.020	(sht to 11)	(sht to 10)	oup in	
				Large MiM capacitor, CAPM over M3, 11 plates, each 40x40.	BOT plate	TOP plate	open	open	open	open	open	open	open	open	open	open	+
4546				Same capacitor as 4530. Caps have seas of via-2's placed under M3/CAPM		TO PILL		1	1	,	,						3
				Total A = 17600, P = 1760. Total expected capacitance 35.5 pF													1 -
		i		CAPM-M3 and CAP2M-M4 capacitors, stacked on top of each other and connected together. 11 pairs of	BOT plate	TOP plate	open	open	open	open	open	open	open	open	open	open	
4548				plates, each 40x40			·			i i						·	3
				Total A = 35200, P = 3520. Total expected capacitance 71 pF	(Metal-4)	(M3/M5)											
				Large MiM capacitor, CAP2M over M4, 11 plates, each 40x40.	BOT plate	TOP plate	open	open	open	open	open	open	open	open	open	open	
4549				Same capacitor as 4531. Caps have seas of via-3's placed under M4/CAP2M													3
				Total A = 17600, P = 1760. Total expected capacitance 35.5 pF													
	7			143 stage, folded, fanout 1 inverter RO with "output"	Divided output	Output	Vss	Vdd osc	Vdd buffer / divider	Enable			Vss		Vdd buffer / divider		
5102				NMOS: 2*1.00/0.15 PMOS: 2*1.68/0.15 71 stage, folded, fanout 3 inverter RO with "output"													3
	7			NMOS: 2*1.00/0.15 PMOS: 2*1.68/0.15			Vss		Vdd buffer / divider		Divided output	Output	Vss	Vdd osc	Vdd buffer / divider	Enable	
5108c				727 inverter stages, 10 stage divider	HOLD	vowr for RO	raw out	vgnd	vpwr for buffers	divided out							3
31000	_			143 stage, folded, fanout 1 inverter RO with "output"	1												+-
5109	7		1	NMOS: 2*1.00/0.15 (low Vt) PMOS: 2*1.68/0.15	Divided output	Output	Vss	Vdd osc	Vdd buffer / divider	Enable							1
5109	7			71 stage, folded, fanout 3 inverter RO with " output"							Divided output	Output	Vss	Vdd osc	Vdd buffer / divider	Fnable	**
				NMOS: 2*1.00/0.15 (low Vt) PMOS: 2*1.68/0.15							Divided output	Output	V 55	Vuu usc	vuu bullet / ulviuet	Lilable	
5109c			1	727 inverter stages, 10 stage divider	HOLD	vpwr for RO	raw out	vgnd	vpwr for buffers	divided out							3
	7			99 stage, folded, fanout 1 inverter RO with "output"	Divided output	Output	Vss	Vdd osc	Vdd buffer / divider	Enable							
5128	ļ			NMOS: 2*1.00/0.15 (low Vt) PMOS: 2*1.68/0.35 (lowVt)							-	ļ	-				
				49 stage, folded, fanout 3 inverter RO with "output" NMOS: 2*1,00/0,15 (low Vt) PMOS: 2*1,68/0,35 (lowVt)							Divided output	Output	Vss	Vdd osc	Vdd buffer / divider	Enable	
5128c		1	1	502 inverter stages, 10 stage divider	HOLD	vowr for RO	raw out	vand	vowr for buffers	divided out	 		1	1			3
0120C		 	 	High-voltage p+ diff diode	TIOLD	VPWI IOI IO	iaw out	vgnu	-pm for build's	divided odt	<u> </u>		1				+-
		1		Area Intensive, Area: 5 * (40 * 44.9) = 8,980 um2	-						+		 	 			-
5200	5			Area Intensive, Peri: 5 * 2 * (40+44.9) = 849 um	n-well	p+ area	p+ area	p+ area	p+ area	p+ area							3
			1	Peri Intensive, Area: 225 * 20.79 um2 = 4,677.7 um2	n-well						p+ peri	p+ peri	p+ peri	p+ peri	p+ peri	p+ peri	
				Peri Intensive, Peri: 225 * 81.0 um = 18.225.0 um													

Mod#	Group	New Style Name	Old Style Name	Description	Pin 01	Pin 02	Pin 03	Pin 04	Pin 05	Pin 06	Pin 07	Pin 08	Pin 09	Pin 10	Pin 11	Pin 12	Die Row
				Periphery NMOS and PMOS FETs (for overlap capacitance)													
5203	5			NMOS: W/L = 600 * 15.645 / 0.15 = 9,387/0.15	substrate	Ngate	N gate	N S/D	N S/D	substrate							3
				PMOS: W/L = 584 * 15.045 / 0.15 = 8,786/0.15					T		P gate	P gate	P S/D	P S/D	n-well	n-well	
				HV Periphery NMOS and PMOS FETs (for overlap capacitance)													
5204	5			NMOS: W/L = 384 * 15.65 / 0.50 = 6,010/0.50	substrate	Ngate	N gate	N S/D	N S/D	substrate							3
				PMOS: W/L = 368 * 15.04 / 0.15 = 5,535/0.5					1		P gate	P gate	P S/D	P S/D	n-well	n-well	
				Low Vt n-diode; High Vt p-diode							<u> </u>	, , , , , , , , , , , , , , , , , , ,					
				N Area Intensive, Area: 2 * 40 * 44.9 = 1,796 um2 = 3,592 um2					T							·	
				N Area Intensive, Peri: 2 * 2 * (40+44.9) = 339.6 um	substrate	n+ area	n+ area										
				N Peri Intensive, Area: 3 * 57 * 39.985 * 0.52 = 3,555.5 um2				n+ peri	n+ peri	n+ peri							
5205	Z			N Peri Intensive, Peri: 3 * 57 * 2 * (39.985+0.52) = 13,852.7 um				II+ peii	II+ peli	II+ peli							3
				P Area Intensive, Area: 2 * 40 * 44.9 = 1,796 um2 = 3,592 um2							nwell	p+ area	p+ area				
				P Area Intensive, Peri: 2 * 2 * (40+44.9) = 339.6 um							1111011	p. aloa	p. aloa				
				P Peri Intensive, Area: 3 * 57 * 39.985 * 0.52 = 3,555.5 um2										p+ peri	p+ peri	p+ peri	
				P Peri Intensive, Peri: 3 * 57 * 2 * (39.985+0.52) = 13,852.7 um													_
	_			Low Vt NMOS, High Vt PMOS FETs (for overlap capacitance)						ļ							
5207	5			NMOS: W/L = 600 * 15.645 / 0.15 = 9,387/0.15	substrate	Ngate	N gate	N S/D	N S/D	substrate							3
				PMOS: W/L = 584 * 15.045 / 0.15 = 8,786/0.15							P gate	P gate	P S/D	P S/D	n-well	n-well	
				Nwell-Psub diode													
	-			Peri Intensive, Area: 30 * 1.52 * 86.425 = 3,940.9 um2	Nwell	Nwell	Psub										
5208	5			Peri Intensive, Peri: 30 * 2 * (1.52+86.425) um = 5,276.7 um Area Intensive. Area: 9 * 47.425 * 88.27 = 37.675 um2	_												3
				Area Intensive, Area: 9 * 47.425 * 88.27 = 37,675 um2 Area Intensive, Peri: 9 * 2 * (47.425+88.27) = 2.442.5 um			Psub	Nwell	Nwell	Nwell	Nwell	Nwell	Nwell	Nwell	Nwell	Nwell	
				n-diode: p-diode				1	-								_
				N Area Intensive, Area: 2 * 40 * 44.9 = 1,796 um2 = 3,592 um2										-			
				N Area Intensive, Page 2 * 40 * 44.9 = 3,952 um2 = 3,552 um2	substrate	n+ area	n+ area										
				N Peri Intensive, Area: 3 * 57 * 39.985 * 0.52 = 3,555.5 um2									-				
5209	5			N Peri Intensive, Peri: 3 * 57 * 2 * (39.985+0.52) = 13.852.7 um	substrate			n+ peri	n+ peri	n+ peri							3
				P Area Intensive. Area: 2 * 40 * 44.9 = 1.796 um2 = 3.592 um2		-											
				P Area Intensive, Peri: 2 * 2 * (40+44.9) = 339.6 um							p +area	p+ area				n-well	
				P Peri Intensive, Area: 3 * 57 * 39.985 * 0.52 = 3,555.5 um2									p+ peri	p+ peri	p+ peri	n-well	
				P Peri Intensive, Peri: 3 * 57 * 2 * (39.985+0.52) = 13,852.7 um									p. pen	p. pen	p. pen	II-WOII	
				High-voltage n+ diff diode													
				Area Intensive, Area: 5 * 1,796 um2 = 8,980 um2	substrate	n+ area	n+ area	n+ area	n+ area	n+ area							
5210	5			Area Intensive, Peri: 5 * 169.8 um = 849 um	Jubotrato	III dica	111 0100	III alca	III dica	III alea							3
				Peri Intensive, Area: 225 * 20.79 um2 = 4,677.7 um2	substrate						n+ peri	n+ peri	n+ peri	n+ peri	n+ peri	n+ peri	
				Peri Intensive, Peri: 225 * 81.0 um = 18,225.0 um							III poil	III poli	II- poii	III poil	III poil	iii puii	
5211	8			lateral PNP BJT (pnppar) (Ae=0.68x0.68um2) m=1	E	В	C-Psub										3
				lateral PNP BJT (pnppar) (Ae=0.68x0.68um2) m=1680				B	C-Psub	E							
				Deep N well-Pwell diode													
	_			Peri Intensive, Area: 26 * 1.29 * 100 = 3354 um2	Psub	D Nwell	Pwell										
5212	5			Peri Intensive, Peri: 26 * 2 * (1.29+100) um = 5,267.08 um						ļ							3
				Area Intensive, Area: 9 * 37.7 * 77.7 = 26363.61 um2 Area Intensive, Peri: 9 * 2 * (37.7+77.7) = 2077.2 um	Psub			D Nwell	Pwell	Pwell	Pwell	Pwell	Pwell	Pwell	Pwell	Pwell	
				Deep N well-Psub diode				-					-		+		_
				Peri Intensive. Area: 6 * 3 * 100 = 1800 um2		-				ļ				-			
5213	5			Peri Intensive, Area. 6 3 100 = 1000 diliz	Psub	Dnwell											3
02.0	•			Area Intensive, Area: 9 * 40.5 * 80.5 = 29342.25 um2		···							-	-			
				Area Intensive, Peri: 9 * 2 * (40.5+80.5) = 2178 um	Psub		D Nwell	D Nwell	D Nwell	D Nwell	D Nwell	D Nwell	D Nwell	D Nwell	D Nwell	D Nwell	
				Native n-diode				1	İ			1	İ	İ	1	1	
				Area Intensive. Area: 5 * 44.9 * 40 = 8980 um2		A1 P#	11.57	1	N. 179	N.F.		1	<u> </u>	<u> </u>		1	
5215	5			Area Intensive, Peri: 5 * 2 * (40 + 44.9) = 849 um	sub	Ndiff	Ndiff	Ndiff	Ndiff	Ndiff					1		3
				Peri Intensive, Area: 225 * 0.52 * 39.985 = 4678.245 um2	sub					T	Ndiff	Ndiff	Ndiff	Ndiff	Ndiff	Ndiff	
				Peri Intensive, Peri: 225 * 2 * (0.52+39.985) um = 18227.25 um	SUD						Nulli	Nulli	INGIII	INUIII	NUIII	INUIII	
				HV Native NMOS and ntv Native NMOS (for overlap capacitance)													
5217	5			Native NMOS: W/L = 384 * 15.65 / 0.50 = 6,010/0.50	substrate	gate	gate	S/D	S/D	substrate							3
				NTV native NMOS: W/L = 284 * 15.65 / 0.9 = 6010/0.50	substrate						gate	gate	S/D	S/D	substrate	substrate	
				Low Vt NMOS, High Vt PMOS FETs (for overlap capacitance)													
5219	5			NMOS: W/L = 600 * 15.645 / 0.15 = 9,387/0.15	substrate	Ngate	N gate	N S/D	N S/D	substrate		1	1	1	1	1	3
				PMOS: W/L = 584 * 15.045 / 0.15 = 8,786/0.15					1	1	P gate	P gate	P S/D	P S/D	n-well	n-well	
				· · · · · · · · · · · · · · · · · · ·	•		_		-						•		

Mod#	Group	New Style Name	Old Style Name	Description	Pin 01	Pin 02	Pin 03	Pin 04	Pin 05	Pin 06	Pin 07	Pin 08	Pin 09	Pin 10	Pin 11	Pin 12	Die Row
				Low Vt n-diode; Low Vt p-diode													
				N Area Intensive, Area: 2 * 40 * 44.9 = 1,796 um2 = 3,592 um2	substrate	n+ area	n+ area				1						
				N Area Intensive, Peri: 2 * 2 * (40+44.9) = 339.6 um	3003040	III died	111 0100										
5220	5			N Peri Intensive, Area: 3 * 57 * 39.985 * 0.52 = 3,555.5 um2 N Peri Intensive, Peri: 3 * 57 * 2 * (39.985+0.52) = 13,852.7 um				n+ peri	n+ peri	n+ peri							3
3220	"			P Area Intensive, Area: 2 * 40 * 44.9 = 1,796 um2 = 3,592 um2				-						-			
				P Area Intensive, Peri: 2 * 2 * (40+44.9) = 339.6 um							nwell	p+ area	p+ area				
				P Peri Intensive, Area: 3 * 57 * 39.985 * 0.52 = 3,555.5 um2										p+ peri	p+ peri	p+ peri	
				P Peri Intensive, Peri: 3 * 57 * 2 * (39.985+0.52) = 13,852.7 um										p. pon	p - po.:	p. pon	
5223	8		npnpar1x1	NPN BJT (npnpar 1x1) (Ae=1.0x1.0 um2) m=1 mismatch NPN BJT (npnpar 1x2) (Ae=1.0x2.0 um2) m=1 mismatch	Psub Psub-E	E1	B1	C1	C2	B2	E1	B1	C1	C2	B2		3
			npnpar1x2 npnpar1x1	NPN BJT (npnpar 1x1) (Ae=1.0x1.0 um2) m=1	Psub-E	С	В	F	+			ВІ	CI	C2	DZ.		+
5226	8		npnpar1x2	NPN BJT (npnpar 1x2) (Ae=1.0x2.0 um2) m=1	Psub		В		С с	В	F						3
OLLO	"		npnpar1x4	NPN BJT (npnpar 1x4) (Ae=1.0x4.0 um2) m=1	Psub	··· <mark>·······</mark>		-		<u>-</u>		Т с	В	E	OPEN	OPEN	
5230	8		pnppar10x	lateral PNP BJT (pnppar10X) (Ae=3.4x3.4um2) m=1	E	В	C-Psub	1	i	1	i i			1			3
5230	8		pnppar10x	lateral PNP BJT (pnppar10X) (Ae=3.4x3.4um2) mismatch				c1/c2	b1	e1	e2	b2					3
			nshort	nshort; w=0.36; l=0.15; m=2280;	b	g	d										
			nshort	nshort; w=0.39; l=0.15; m=2190;	b	9		d									
			nshort	nshort; w=0.65; l=0.15; m=1560;	b	9			d								
			nshort nshort	nshort; w=0.55; l=0.15; m=1740; nshort: w=0.64; l=0.15; m=1590;	b b	9				d	d						
5290			nshort	nshort; w=0.84; I=0.15; m=1290;	b b	9					<u>0</u>	d	-				3
			nshort	nshort; w=0.42; I=0.5; m=1680;	ь	9						u	d				••••
			nshort	nshort; w=0.6; I=0.15; m=1650;	b	n 9		-		-	+	+	+	d		-	
			nshort	nshort: w=0.82: =0.18: m=1276:	b	0									d		
			nshort	nshort; w=0.94; I=0.15; m=1170;	b	g										d	
			phighvt	phighvt; w=0.36; l=0.15; m=2280;	b	g	S										
			phighvt	phighvt; w=0.39; l=0.15; m=2190;	b	g		s									
			phighvt	phighvt; w=0.65; l=0.15; m=1560;	b	9			S								
			phighvt	phighvt; w=0.55; l=0.15; m=1740;	b b	9				S							
5291			phighvt	phighvt; w=0.64; l=0.15; m=1590; phighvt; w=0.84; l=0.15; m=1290;	b h	9					S					-	3
			phighvt phighvt	pnignvt; w=0.84; i=0.15; m=1290; phighvt; w=0.42; i=0.5; m=1680;	b b	9						S	- S	-			
			phighyt	phighvt; w=0.42; 1=0.3; n1=1000; phighvt; w=0.6; 1=0.15; m=1650;	h	9								S			
			phighyt	phighvt; w=0.82; l=0.18; m=1276;	b	g g					-				S		
			phighvt	phighvt; w=0.94; l=0.15; m=1170;	b	g										S	
				300 ohm/sq P+ POLY RESISTOR - 2 micron trench contacts oriented to current flow													
				W = 5.73, L = 2.865, sq = 0.5	V1	V2											
				W = 5.73, L = 5.73, sq = 1		V1	V2										
				W = 5.73, L = 11.46, sq =2 W = 5.73, L = 22.92, sq =4		<mark></mark>	V1	V2 V1	V2								
6200				W = 5.73, L = 114.6, sq = 20		<mark></mark>		v:	V2 V1		V2			•			3
				W = 2.85, L = 1.425, sq = 0.5		-			- V - V - V - V - V - V - V - V - V - V		V1	V2					••••
				W = 2.85, L = 2.85, sq =1		···		-			·	V1	V2				
	l			W = 2.85, L = 5.7, sq =2									V1	V2			
				W = 2.85, L = 11.4, sq =4										V1	V2	Substrate	
				300 ohm/sq P+ POLY RESISTOR - 2 micron trench contacts oriented to current flow													
				W = 1.41, L = 0.705, sq = 0.5		V1	V2										
	ļ			W = 1.41, L = 1.41, sq = 1			V1	V2						1			[
	ļ		-	W = 1.41, L = 2.82, sq = 2	-		<u> </u>	V1	V2	1			-	+	+	-	
6201	ļ			W = 1.41, L = 5.64, sq =4 W = 1.41, L = 28.2, sq =20	+				V1	V2 V1	V2			-		+	3
				W = 1.41, L = 20.2, sq = 20 W = 0.69, L = 0.345, sq = 0.5 (will not work for any routes using RRPM mask)				+		V 1	V2 V1	V2	-	-		-	
				W = 0.69, L = 0.69, sq = 1	-	-	-	1		-	- V 1	V2 V1	V2	 		<u> </u>	*****
				W = 0.69, L = 1.38, sq =2	<u> </u>			1			1	T	V1	V2		1	
	·			W = 0.69, L = 2.76, sq =4	1			1			·	1	1	V1	V2	Substrate	
				300 ohm/sq P+ POLY RESISTOR - 2 micron trench contacts oriented to current flow													
	ļ			W = 0.33, L = 0.33, sq = 1 (will not work for any routes using RRPM mask)				V1	V2								
	ļ			W = 0.33, L = 0.66, sq =2					V1	V2							
6202				W = 0.33, L = 1.32, sq =4						V1	V2						3
	ļ			W = 0.33, L = 6.6, sq =20 W = 0.69, L = 13.8, sq = 20							V1	V2 V1	V2	+		-	
				W = 0.69, L = 13.8, sq = 20 W = 2.85, L = 57.0, sq = 20								V I	V2 V1		V2	Substrate	
	_		 	300 ohm/sq P+ POLY RESISTOR - 2 micron trench contacts oriented to current flow				+					VI	+	VZ	Substrate	+
	ļ			Mismatch W = 0.33, L = 6.60, sq = 20	Common	R1	R2	+	-	-	-	-	+	+		<u> </u>	
	l			Mismatch W = 0.33, L = 1.32, sq = 4				Common	R1	R2	·	+	+	 		†	3
6203							····			-	Common	R1	R2	+			
6203				Mismatch W = 0.33, L = 0.66, sq = 2 Mismatch W = 0.33, L = 0.33, sq = 1				1	1	1	Common	KI	R2				

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Mod #	Group	New Style Name	Old Style Name	Description	Pin 01	Pin 02	Pin 03	Pin 04	Pin 05	Pin 06	Pin 07	Pin 08	Pin 09	Pin 10	Pin 11	Pin 12	Die Row
				300 ohm/sq P+ POLY RESISTOR - 2 micron trench contacts oriented to current flow													
				Mismatch W = 0.69, L = 13.8, sq = 20	Common	R1	R2										
6204				Mismatch W = 0.69, L = 2.76, sq = 4				Common	R1	R2							3
				Mismatch W = 0.69, L = 1.38, sq = 2 Mismatch W = 0.69, L = 0.69, sq = 1			<u></u>				Common	R1	R2	Common	R1	R2	
				Mismatch W = 0.69, L = 0.69, sq = 1 300 ohm/sq P+ POLY RESISTOR - 2 micron trench contacts oriented to current flow	_									Common	KI	KZ .	++
				Mismatch W = 1.41, L = 28.2, sq = 20	Common	R1	R2										-
6205				Mismatch W = 1.41, L = 13.142, sq = 4	Common			Common	R1	R2	 	-					. 3
				Mismatch W = 1.41, L = 2.82, sq = 2							Common	R1	R2				
				Mismatch W = 1.41, L = 1.41, sq = 1										Common	R1	R2	
				300 ohm/sq P+ POLY RESISTOR - 2 micron trench contacts oriented to current flow													
				Mismatch W = 2.85, L = 57.0, sq = 20	Common	R1	R2										
6206				Mismatch W = 2.85, L = 11.4, sq = 4				Common	R1	R2							. 3
				Mismatch W = 2.85, L = 5.7, sq = 2 Mismatch W = 2.85, L = 2.85, sq = 1							Common	R1	R2	Common	R1	R2	
				Mismatch W = 2.85, L = 2.85, Sq = 1 300 ohm/sq P+ POLY RESISTOR - 2 micron trench contacts oriented to current flow										Common	KI	K2	+
				Mismatch W = 5.73, L = 5.73, sq = 1	R1-Shared	R1-A	R1-B				-			•			-
6207				Mismatch W = 5.73, L = 11.46, sq = 2	Tri Ondioo			R2-Shared	R2-A	R2-B							- 3
				Mismatch W = 5.73, L = 22.92, sq = 4							R3-Shared	R3-A	R3-B				1
				Mismatch W = 5.73, L = 2.865, sq = 0.5				·			1		<u> </u>	R4-Shared	R4-A	R4-B	1
				300 ohm/sq P+ POLY RESISTOR - 2 micron trench contacts oriented to current flow													
				Mismatch W = 0.69, L = 0.345, sq = 0.5 (will not work for any routes using RRPM mask)	Common	R1	R2										
6208				Mismatch W = 1.41, L = 0.705, sq = 0.5				Common	R1	R2							3
				Mismatch W = 2.85, L = 1.425, sq = 0.5							Common	R1	R2				
				Mismatch W = 5.73, L = 114.6, sq = 20 300 ohm/sq P+ POLY RESISTOR - 2 micron trench contacts oriented to current flow										Common	R1	R2	-
				Mismatch W = 2.85, L = 11.4, 5.48 spacing	Common	R1	R2					-					-
6209				Mismatch W = 2.85, L = 11.4, 10.48 spacing	Common	NI NI	NZ	Common	R1	R2							- 3
0203				Mismatch W = 2.85, L = 11.4, 25.48 spacing			······································	Common	101	11/2	Common	R1	R2	•			
				Mismatch W = 2.85, L = 11.4, min space, no dummies										Common	R1	R2	1
				300 ohm/sq P+ POLY RESISTOR - 2 micron trench contacts oriented to current flow													
				Mismatch W = 2.85, L = 57.0, sq = 20	Common	R1	R2]
6210				Mismatch W = 2.85, L = 11.4, sq = 4				Common	R1	R2							3
				Mismatch W = 2.85, L = 5.7, sq = 2							Common	R1	R2				
				Mismatch W = 2.85, L = 2.85, sq = 1										Common	R1	R2	_
				2K ohm/sq P- POLY RESISTOR - 2 micron trench contacts oriented to current flow W = 5.73, L = 2.865, sq = 0.5	V1	V2											
				W = 5.73, L = 5.73, sq = 1	V I	V2 V1	V2										
				W = 5.73, L = 11.46, sq = 2		V I	V2 V1	V2									-
				W = 5.73, L = 22.92, sq =4				V1	V2		 						1 .
6214				W = 5.73, L = 114.6, sq =20			····		V1		V2						- 3
				W = 2.85, L = 1.425, sq =0.5							V1	V2					1
				W = 2.85, L = 2.85, sq =1								V1	V2				1
				W = 2.85, L = 5.7, sq =2									V1	V2			
				W = 2.85, L = 11.4, sq =4										V1	V2	Substrate	
				2K ohm/sq P- POLY RESISTOR - 2 micron trench contacts oriented to current flow													
				W = 1.41, L = 0.705, sq = 0.5 W = 1.41, L = 1.41, sq = 1		V1	V2 V1	V2									
				W = 1.41, L = 1.41, Sq = 1 W = 1.41, L = 2.82, sq = 2			V I	V2 V1	V2		 	-	+				-
				W = 1.41, L = 5.64, sq =4				*	V2V1	V2		-					1
6215				W = 1.41, L = 28.2, sq =20						V1	V2						- 3
				W = 0.69, L = 0.345, sq = 0.5 (may not work for routes using URPM mask)							V1	V2					1
				W = 0.69, L = 0.69, sq =1								V1	V2				1
				W = 0.69, L = 1.38, sq =2									V1	V2			1
				W = 0.69, L = 2.76, sq =4										V1	V2	Substrate	
				2K ohm/sq P- POLY RESISTOR - 2 micron trench contacts oriented to current flow							ļ						
				W= 0.33, I = 0.33, sq = 1 (may not work for routes using URPM mask)				V1	V2		 						-
6216	ļ			W= 0.33, I = 0.66, sq =2 W= 0.33, I = 1.32, sq =4				-	V1	V2 V1	V2				 	ļ	. 3
0210	ļ			W= 0.33, I = 1.32, Sq =4 W= 0.33, I = 6.6, Sq =20				+		V 1	V2 V1	V2	+		t		- "
				W= 0.69, I = 13.8, sq = 20				-			V 1	V2 V1	V2				-
				W= 2.85, I = 57.0, sq = 20				·			†	† <u>-</u>	V1		V2	Substrate	1
	İ			2K ohm/sq P- POLY RESISTOR - 2 micron trench contacts oriented to current flow				İ				İ		İ			1
	·			Mismatch W = 0.33, L = 6.60, sq = 20	Common	R1	R2	T			1	1					1
6217				Mismatch W = 0.33, L = 1.32, sq = 4				Common	R1	R2							3
				Mismatch W = 0.33, L = 0.66, sq = 2				1			Common	R1	R2		I		1
				Mismatch W = 0.33, L = 0.33, sq = 1 (may not work for routes using URPM mask)										Common	R1	R2	

Mod#	Group	New Style Name	Old Style Name	Description	Pin 01	Pin 02	Pin 03	Pin 04	Pin 05	Pin 06	Pin 07	Pin 08	Pin 09	Pin 10	Pin 11	Pin 12	Die Row
MOG #	Group	New Style Name	Old Style Name	2K ohm/sq P- POLY RESISTOR - 2 micron trench contacts oriented to current flow	PINUI	PIN UZ	PIN U3	PIN 04	PIN US	PIII V6	Pin U/	PIII VO	PIN U9	PIN 10	PIN 11	PIN 12	Die Row
				Mismatch W = 0.69, L = 13.8, sq = 20	Common	R1	R2				-						
6218				Mismatch W = 0.69, L = 13.6, sq = 20 Mismatch W = 0.69, L = 2.76, sq = 4	Common	KI	R2	Common	R1	R2				-			3
0210				Mismatch W = 0.69, L = 1.38, sq = 2				Common	KI.	RZ	Common	R1	R2				3
				Mismatch W = 0.69, L = 1.36, Sq = 2 Mismatch W = 0.69, L = 0.69, so = 1			<u> </u>				Common	KI	RZ	Common	R1	R2	
—														Common	R1	R2	
				2K ohm/sq P- POLY RESISTOR - 2 micron trench contacts oriented to current flow													
				Mismatch W = 1.41, L = 28.2, sq = 20	Common	R1	R2										
6219				Mismatch W = 1.41, L = 13.142, sq = 4				Common	R1	R2							3
				Mismatch W = 1.41, L = 2.82, sq = 2							Common	R1	R2				
				Mismatch W = 1.41, L = 1.41, sq = 1										Common	R1	R2	
				2K ohm/sq P- POLY RESISTOR - 2 micron trench contacts oriented to current flow													
				Mismatch W = 2.85, L = 57.0, sq = 20	Common	R1	R2										
6220				Mismatch W = 2.85, L = 11.4, sq = 4				Common	R1	R2							3
				Mismatch W = 2.85, L = 5.7, sq = 2							Common	R1	R2				
				Mismatch W = 2.85, L = 2.85, sq = 1										Common	R1	R2	
				2K ohm/sq P- POLY RESISTOR - 2 micron trench contacts oriented to current flow													
				Mismatch W = 5.73, L = 5.73, sq = 1	R1-Shared	R1-A	R1-B										
6221				Mismatch W = 5.73, L = 11.46, sq = 2				R2-Shared	R2-A	R2-B	İ						3
				Mismatch W = 5.73, L = 22.92, sq = 4							R3-Shared	R3-A	R3-B				
				Mismatch W = 5.73, L = 2.865, sq = 0.5										R4-Shared	R4-A	R4-B	
		i		2K ohm/sq P- POLY RESISTOR - 2 micron trench contacts oriented to current flow									1				
				Mismatch W = 0.69, L = 0.345, sq = 0.5 (may not work for routes using URPM mask)	Common	R1	R2		-		 	-		***************************************	•		
6222				Mismatch W = 1.41, L = 0.705, sq = 0.5		···	····	Common	R1	R2	·	-		***************************************	•		3
0222				Mismatch W = 2.85, L = 1.425, sq = 0.5		···	·····			1	Common	R1	R2				
				Mismatch W = 5.73, L = 114.6, sq = 20							Common	101	102	Common	R1	R2	
				2K ohm/sq P- POLY RESISTOR - 2 micron trench contacts oriented II to current flow								-		Common	RI	RZ	-
					Common	R1	R2					-					
2000				Mismatch W = 2.85, L = 11.4, 5.48 spacing	Common	KI	KZ		ļ								
6223				Mismatch W = 2.85, L = 11.4, 10.48 spacing				Common	R1	R2							3
				Mismatch W = 2.85, L = 11.4, 25.48 spacing							Common	R1	R2				
				Mismatch W = 2.85, L = 11.4, min space, no dummies										Common	R1	R2	
				2K ohm/sq P- POLY RESISTOR - 2 micron trench contacts oriented to current flow													
				Mismatch W = 2.85, L = 57.0, sq = 20	Common	R1	R2										
6224				Mismatch W = 2.85, L = 11.4, sq = 4				Common	R1	R2							3
				Mismatch W = 2.85, L = 5.7, sq = 2							Common	R1	R2				
				Mismatch W = 2.85, L = 2.85, sq = 1										Common	R1	R2	
				HV n-chan field oxide FETs poly1 gate									i				
7003	1			poly1 gate w/l = 1000/0.38 (diff spacing =0.48)	substrate	source	gate 1	drain 1	gate 2	drain 2				-	•		3
				poly1 gate w/l = 1000/0.35 (diff spacing =0.45)			V					source	gate 1	drain 1	gate 2	drain 2	
				HV n-chan gate oxide capacitor (GOX55), no source/drain: large area								333.55	gate :		3-14-		
	5			n+ diff: 10 x W/L=10.82/42.72; poly: 10 x W/L=13.3/44.26	substrate	gate	substrate	gate	substrate	gate	-	-	-				
7012				HV p-chan gate oxide capacitor (GOX55), no source/drain: large area	Jupatrate	gato	3003000	yate	3003040	gate							3
	5			p+ diff: 10 x W/L = 9.77/41.14; poly: 10 x W/L=12.45/42.78							nwell	gate	nwell	gate	nwell	gate	
				Deep Nwell Resistor W/L = 25/25: 1 sq.	Psub	DNW R1	DNW R2				riweii	gate	riweii	gate	riweii	gate	+
				Deep Nwell to Deep Nwell Isolation	PSUD	DINVIRI	DINW KZ										
							<u></u>										
7015	1			DNW to DNW Space = 11.5um	Psub			DNW Hi	DNW Lo								3
				DNW to DNW Space = 9.5um	Psub					DNW Hi	DNW Lo						
				DNW to DNW Space = 7.5um	Psub							DNW Hi	DNW Lo				
		1	1	DNW to DNW Space = 5.5um	Psub				1				1	DNW Hi	DNW Lo		
				Isolated Pwell Resistor under Field													
		1		Pwell Resistor W/L =25/25: 1 sq.	DNW	PW R1	PW R2									Psub	
		1		Pwell to Pwell Isolation in DNW													
7016	1	I		Pwell to Pwell Space = 1.40um	DNW			PW Hi	PW Lo			I			I	Psub	3
		1		Pwell to Pwell Space = 1.20um	DNW			1	1	PW Hi	PW Lo	1	1	1		Psub	
		1		Pwell to Pwell Space = 1.00um	DNW					<u> </u>		PW Hi	PW Lo	<u> </u>		Psub	
		I		Pwell to Pwell Space = 0.84um	DNW						1			PW Hi	PW Lo	Psub	
		i	İ	Isolated Pwell Resistor under N+ Active	1			1	1	1	i e	1	İ	i –	1	1	1
		I		Pwell Resistor W/L =25/25: 1 sq.	DNW	PW R1	PW R2				†	·	·	·		Psub	
		I		Nwell to Deep Nwell Isolation				-	-	+	1	+	+	+			
7017	1	I		Nwell to DNW Space = 7.0um	DNW		-	NW Hi	DNW Lo	 	†	+	+	+	 	Psub	3
1011	'	I		Nwell to DNW Space = 6.0um	DNW	-		INVYIII	DINN LU	NW Hi	DNW Lo	+	+	+	ł	Psub	
		I		Nwell to DNW Space = 5.0um Nwell to DNW Space = 5.0um	DNW					INVV FII	DINVV LO	NW Hi	DNW Lo	-		Psub	
		I					<u></u>		ļ	ļ	ļ	NW HI	DNW LO	- NAZIE	DANAGE		
		 	1	Nwell to DNW Space = 4.5um	DNW				1				+	NW Hi	DNW Lo	Psub	+
		I		High Voltage Nwell to Nwell Isolation							1	ļ	1				
		I		Nwell to Nwell Space = 2.00um		NW Hi	NW Lo				<u> </u>	1	1	1		Psub	
7018	1	I		Nwell to Nwell Space = 2.50um				NW Hi	NW Lo							Psub	3
7010	'	I		Nwell to Nwell Space = 1.50um						NW Hi	NW Lo					Psub	
		I		Nwell to Nwell Space = 1.27um								NW Hi	NW Lo			Psub	
		I		Nwell to Nwell Space = 1.00um	T			T	1	T	T	T	T	NW Hi	NW Lo	Psub	
		•	•	·	•		_	-	-	•	-	•	•	•		•	

Mod #	Group	New Style Name	Old Style Name	Description	Pin 01	Pin 02	Pin 03	Pin 04	Pin 05	Pin 06	Pin 07	Pin 08	Pin 09	Pin 10	Pin 11	Pin 12	Die Row
				HV N+diff Isolation, Poly Gated													
				Gate W/L = 500/0.15 (diff space 0.30)	Psub	Source	Gate	Drain									
7019	1			Gate W/L = 500/0.15 (diff space 0.30)	Psub			Source	Gate	Drain							3
				Gate W/L = 500/0.15 (diff space 0.27)	Psub							Source	Gate	Drain			
				Gate W/L = 500/0.15 (diff space 0.27)	Psub									Source	Gate	Drain	
				HV p+/p-well field FET w/ poly 1 gate													
				p+ / p-well w/l = (6.56*375) / 0.33 (P+ diff to pwell 0.33, poly to diff 0.05) with NWM corner rounding	substrate	n-well	gate	p+									
				HV P+diff Isolation under Poly Gate							T						1
7024	1			Gate W/L = 920/0.15 (diff space 0.30)		•				Substrate			- 3				
				Gate W/L = 760/0.17 (diff space 0.30)							Nwell				Gate	D: n+	-
						•	······································										
				HV n+/n-well field FET w/ poly 1 gate					1								+
				n+/n-well w/l = 26 x 40 / 0.43 (diff to nwell 0.43, poly to diff 0.10)	substrate	n-well	gate	n+ diff									
				n+ / n-well w/l = (6.56*180) / 0.43 (N+ diff to nwell 0.43, poly to diff 0.05) with NWM corner rounding	substrate	n-well	gate	II. uiii				-			-		- 1
7030	1				substrate	n-weii			gate	n+ am							- 3
				HV p-chan field FET w/ poly1 gate													
				p+ / p+ w/l = 23 x 40 / 0.48 (diff to diff 0.48, poly to diff 0.05)									gate	p+ diff			
				p+ / p+ w/l = 19 x 40 / 0.45 (diff to diff 0.45, poly to diff 0.05)							n-well	p+ diff			gate	p+ diff	
				HV p+/p-well field FET w/ poly 1 gate													
				p+ / p-well w/l = 22 x 40 / 0.33 (diff to pwell 0.33, poly to diff 0.05)	n-well	substrate	gate	p+									
7004	١.,			p+ / p-well w/l = 22 x 40 / 0.33 (diff to pwell 0.33, poly to diff 0.05)	n-well	substrate			gate	p+	T	1	1			te Drain te Drain te D; p+ te D; p+ te p+ diff Psub Psub Psub Psub Psub Psub ub ub	١ . ا
7031	1			p+/p-well field FET w/ poly 1 gate	1				1	1	1	1	1	<u> </u>	***************************************		- 3
				p+/p-well w/l = (6.56*200) / 0.18 (P+ diff to pwell 0.18, poly to diff 0.05) with NWM corner rouding				1	1	1	Substrate	n-well	gate	D+		†	1
pr / p-well will = (6.65°(30) / 1.18 (Pr diff to pwell 0.18, poly to diff 0.05) with NVM corner rouding pr / p-well will = (6.65°(45) / 0.15 (Pr diff to pwell 0.15, poly to diff 0.05) with NVM corner rouding	•	···						3		nate	n+	-					
				Pwell in Deep Nwell to Psub Isolation						1	Cubuluio		1	1	guio	P.	+
				Pwell to Psub Space = 0.65um, W = 8 x 43.70um	DNW	Pwell										David.	
				Pwell to Psub Space = 0.84um, W = 8 x 43.70um	DNW	rweii		Pwell		ļ							
7036	1		Pwell to Psub Space Pwell to Psub Space Pwell to Psub Space Pwell to Psub Space Pwell to Psub Space	Pwell to Psub Space = 0.04um, W = 8 x 43.70um Pwell to Psub Space = 1.03um, W = 8 x 43.70um	DNW		<u> </u>	PWeii		DII	ļ			-			3
				Pwell to Psub Space = 1.00um, W = 8 x 43.70um Pwell to Psub Space = 1.20um, W = 8 x 43.70um	DNW	•				-							
				Pwell to Psub Space = 1.20um, W = 6 x 43.70um Pwell to Psub Space = 1.40um, W = 8 x 43.70um	DNW					ļ		PWell		DII			
				HV n-chan gate oxide capacitor: field-edge intensive	substrate	note.	substrate				-			Pwell		PSUD	+
	5			FOM w/s = 0.42/0.48, Active Area = 1740.13 um2, FOX Perimeter = 6776 um	Substrate	gate	Substrate	gate	Substrate	gate							
7137				Hv p-chan gate oxide capacitor: field-edge intensive													3
	5			FOM w/s = 0.42/0.48, Active Area = 2135 um2, FOX Perimeter = 10270.8 um							n-well	gate	n-well	gate	n-well	gate	
				VHV DE NMOS: 50/0.925 ("L=0.7") inside DNW	Pwell	G	S	D	-			-	-		<u> </u>		+
					Pwell	G	3	L D		ļ							
7200	4			VHV DE NMOS: 20/0.925 ("L=0.7") inside DNW VHV DE NMOS: 20/2.425 ("L=2.2") inside DNW	Pwell	G			S	D	S	- D					. 3
7200	4				Pwell						\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	U					3
				VHV DE NMOS: 5/0.925 ("L=0.7") inside DNW	PWell	G							S	U			
				Leave this device Blank	D	_	_								Psub		
				VHV DE NMOS: 60/0.925 ("L=0.7") inside DNW	Pwell Pwell	G	8	D	-l	ļ						-	
	١.			VHV DE NMOS: 20/0.925 ("L=0.7") inside DNW		G			S	D							
7201	4			VHV DE NMOS: 20/2.425 ("L=2.2") inside DNW	Pwell	G				ļ	S	D					3
				VHV DE NMOS: 5/2.425 ("L=2.2") inside DNW	Pwell	G							S	D			
				Leave this device Blank											Psub		
				VHV DE NMOS: 5/0.925 ("L=0.7"), sa=0.68	В	G	S	D		<u> </u>							
				VHV DE NMOS: 20/0.925 ("L=0.7"), sa=0.48	В	G			S	D							
7202	4			VHV DE NMOS: 20/0.925 ("L=0.7"), sa=0.68	В	G				<u> </u>	S	D					3
				VHV DE NMOS: 20/0.925 ("L=0.7"), sa=1.11	В	G				<u> </u>			S	D			
				VHV DE NMOS: 20/0.925 ("L=0.7"), sa=2.5	В	G									S	D	
				VHV DE PMOS: 20/0.920 ("L=0.66"), sa=0.68	В	G	S	D									
				VHV DE PMOS: 5/0.920 ("L=0.66"), sa=0.48	В	G			S	D							
7203	4			VHV DE PMOS: 5/0.920 ("L=0.66"), sa=0.68	В	G					S	D					3
				VHV DE PMOS: 5/0.920 ("L=0.66"), sa=1.11	В	G							S	D			
				VHV DE PMOS: 5/0.920 ("L=0.66"), sa=2.5	В	G									S	D	
				VHV DE NMOS: 5/0.925 ("L=0.7"), sa=2.5	В	G	S	D									
				VHV DE NMOS: 20/2.425 ("L=2.2"), sa=0.48	В	G			S	D							
7204	4			VHV DE NMOS: 20/2.425 ("L=2.2"), sa=0.68	В	G					S	D					3
				VHV DE NMOS: 20/2.425 ("L=2.2"), sa=1.11	В	G				T	1	T	S	D			1
				VHV DE NMOS: 20/2.425 ("L=2.2"), sa=2.5	В	G		1		1	1	1	1	<u> </u>	S	D	1
				VHV DE PMOS: 20/0.920 ("L=0.66"), sa=2.5	В	G	S	D									1 1
				VHV DE PMOS: 20/2.420 ("L=2.16"), sa=0.48	В	G		†	S	D	†	†	†	†	1	†	1
7205	4			VHV DE PMOS: 20/2.420 ("L=2.16"), sa=0.68		G		·	1	† <u>-</u>	S	D	†	†	+	†	4
				VHV DE PMOS: 20/2.420 ("L=2.16"), sa=1.11	B	G		+		†	1	†	S	D			1 1
		1	1								4	4	- 	4			
				VHV DE PMOS: 20/2.420 ("L=2.16"), sa=2.5	l B	G		1		1		1			S	D	

Mad #	C	New Style Name	Old Style Name	Description	Pin 01	Pin 02	Pin 03	Pin 04	Pin 05	Pin 06	Pin 07	Pin 08	Pin 09	Pin 10	Pin 11	Pin 12	Die Row
WOG#	Group	New Style Name	Old Style Name		PIN UT	PIN UZ	S	Pin 04	Pin U3	PIN VO	PIN U/	PIN U6	PIN U9	PIN IU	PIN 11	PIN 1Z	Die Row
				VHV DE NMOS: 60/0.925 ("L=0.7")		G	5	D D									!
				VHV DE NMOS: 20/0.925 ("L=0.7")	В	G			S	D							
7206	4			VHV DE NMOS: 12/0.925 ("L=0.7")	В	G					S	D					4
				VHV DE NMOS: 5/0.925 ("L=0.7")	В	G							S	D			
				VHV DE NMOS: 5/2.425 ("L=2.2")	В	G									S	D	-
				VHV DE PMOS: 60/0.920 ("L=0.66")	В	G	S	D									1
				VHV DE PMOS: 20/0.920 ("L=0.66")	В	G			S	D							-
7207	4			VHV DE PMOS: 12/0.920 ("L=0.66")	B	G			<u>-</u>	<u>-</u>	S	D				+	··· 4
1201	7			VHV DE PMOS: 5/0.920 ("L=0.66")		G							S	n			- 7
				VHV DE PMOS: 5/2.420 ("L=2.16")	B B	G							3	D		D	
							_								5	U	
				VHV DE NMOS: 50/0.925 ("L=0.7") inside DNW	В	G	S	D									
				VHV DE NMOS: 20/0.925 ("L=0.7") inside DNW	В	G			S	D							
7208	4			VHV DE NMOS: 20/2.425 ("L=2.2") inside DNW	В	G					S	D					4
				VHV DE NMOS: 5/0.925 ("L=0.7") inside DNW	В	G							S	D			-
				VHV DE NMOS: 5/2.425 ("L=2.2") inside DNW	В	G									S	D	-
		1		VHV DE NMOS: 60/0.925 ("L=0.7") inside DNW	В	G	S	D	<u> </u>	<u> </u>							1
				VHV DE NMOS: 20/0.925 ("L=0.7") inside DNW	В	G			S	D	-						
7209	4			VHV DE NMOS: 12/0.925 ("L=0.7") inside DNW	В	G				ļ	S	D	-	-			
1209	4				B B	G					- 3	U	+	D			4
				VHV DE NMOS: 5/0.925 ("L=0.7") inside DNW									S	U			
				VHV DE NMOS: 5/2.425 ("L=2.2") inside DNW	В	G									S	D	
				VHV DE NMOS: 50/0.925 ("L=0.7")	В	G	S	D									
l	1	I		VHV DE NMOS: 20/0.925 ("L=0.7")	В	G			S	D							
7210	4			VHV DE NMOS: 20/2.425 ("L=2.2")	В	G					S	D					4
				VHV DE NMOS: 5/0.925 ("L=0.7")	В	G							S	D			
				VHV DE NMOS: 5/2.425 ("L=2.2")	В	G					-			+	S	D	
				VHV DE PMOS: 50/0.920 ("L=0.66")	В	G	S	D	_			+	+				+
				VHV DE PMOS: 20/0.920 ("L=0.66")	B B	G	3		- S	D							
7211	4					G			s		s						4
/211	4			VHV DE PMOS: 20/2.420 ("L=2.16")	В						3	D					4
				VHV DE PMOS: 5/0.920 ("L=0.66")	В	G							S	D			
				VHV DE PMOS: 5/2.420 ("L=2.16")	В	G									S	D	
7212	5			VHV DE NMOS: Gate/Drain Overlap Cap													4
/212	5			VHV DE NMOS: 3188/0.936 ("L=0.7")	В	G	S	D									4
	_			VHV DE PMOS: Gate/Drain Overlap Cap													1
7213	5			VHV DE PMOS: 2645.6/0.92 ("L=0.66")	В	G	S	D									4
				Dense Pad CBCM - POLY 1x 1x (0.15 0.21)	 		-		1						1		+
	10			load length - stub length = 22.14	Istub	lload	Vp	Vn	Vpwr	Vgnd							
7700c				Dense Pad CBCM - LI1 1x 1x (0.17 0.18)							-		+			+	4
	10			load length - stub length = 22.14							Istub	lload	Vp	Vn	Vpwr	Vgnd	
		 		Dense Pad CBCM - M1 1x 1x (0.14 0.14)											1		+
	10			load length - stub length = 22.14	Istub	lload	Vp	Vn	Vpwr	Vgnd							
7704c				Dense Pad CBCM - M2 1x 1x (0.14 0.14)							-		-				4
	10			load length - stub length = 22.14							Istub	lload	Vp	Vn	Vpwr	Vgnd	
		-		Dense Pad CBCM - M3 1x 1x (0.3 0.3) - S8Q	+												+
	10			load length - stub length = 16.03	Istub	lload	Vp	Vn	Vpwr	Vgnd							
7712a				load length - Stub length - 16.03							-						4
	10			Dense Pad CBCM - PY (2.0 4.0) - S8Q load length - stub length = 22.105							Istub	lload	Vp	Vn	Vpwr	Vgnd	
	_																+
7719				top:met5 width:2.000 space:4.000 bot:met4 width:0.000 space:0.000 load-stub length:22.085 (S8PIR/PF)	istub_2	iload_2	vp_2	vn_2	vpwr_2								4
				top:met5 width:1.600 space:1.600 bot:sub width:0.000 space:0.000 load-stub length:22.085 (S8PIR/PF)							istub_1	iload_1	vp_1	vn_1	vpwr_1		
	10			Dense Pad CBCM - LI (2.0 4.0) over PY	Istub	lload	Vp	Vn	Vpwr	Vgnd							
7721c	10			load length - stub length = 22.07	13100	iloau	VP	***	vpm	vgiiu							4
77210	10			Dense Pad CBCM - M1 (2.0 4.0) over LI							Istub	lload	Vp	Vn	Vpwr	Vgnd	1 7
	10			load length - stub length = 22.07							ISUUD	lloau	VΡ	VII	vpwi	vgiiu	
77226				MM4: w=0.3, s= 0.3, load length 23.42 - stub length 5.335 = 18.085, 11 signal lines	istub_1	iload_1	vp_1	vn_1	vpwr_1								4
7722b				MM4: w=2.0, s=4.0, load length 22.52 - stub length 4.435 = 18.085, 1 signal line			······································	- I			istub 2	iload 2	vp 2	vn 2	vpwr_2	1	4
		i	T T	Dense Pad CBCM - M2 (2.0 4.0) over M1 - S8T					1		1	1	1 -	1 -		İ	1
l		I		load length - stub length = 22.07	Istub	lload	Vp	Vn	Vpwr	Vgnd							1 .
7727	l			Dense Pad CBCM - M3 (2.0 4.0) over M2 - S8T				·		·	+		†	-		†	4
	10	I		load length - stub length = 22.07					1	1	Istub	lload	Vp	Vn	Vpwr	Vgnd	1
		 	+	NV Latch Tri-Gates	+				+	 	+	+	 	+	1	<u> </u>	+
7786	6	I		SONOS W/L=1.0/0.5, NHV W/L=1.0/0.5 (prg) and 0.42//0.5um (prg_l)	Psub					·			!			Daniell	4
		-	-		PSUD		source	Vspw	VB	test_n	test_p	VA	prg_l	Vneg	prg	Dnwell	+
		I		S8P - WM3/RSM3 WM4/RSM4 Routed around pads										1		1	
l		I		WM3 - 0.3u Wide; 398.2u Long	ı			V		V	1		1	1			
7821		I		RSM3 - 1.5u Wide; 486.3u Long	I	l l	V		V	1							4
l		I		WM4 - 0.3u Wide; 398.2u Long							l I	I		V		V	
l		I		RSM4 - 1.5u Wide; 486.3u Long	1			1		1	T I	I	V		V		
				1	-			-	-	-		 			· · · · · ·		

Mod # Group New Style Name Old Style Name Description Pin 01 Pin 02 Pin 03 Pin 04 Pin 05 Pin 06 Pin 07 Pin 08 Pin 09	Pin 10 Pin 11 d s d s d s s	Pin 12 Die Ro
Rehort	s d	4
Rehort R	s d	4
Section	s d	4
Institut	s d	4
nshort nshort w=0.420;1=0.150; m=1;in DNW b g s s s s s s s s s	s d	d
Inshort Insh	s d	d
nshort nshort nshort, w=0.420; =0.150; m=1; in DNW		d
nhv nhv; w=500; H=500; m=1; b g s d nhv nhv; w=0.40; H=0.450; m=1; b g s d nhv nhv; w=0.750; H=0.50; m=1; b g s d	S	d
nhv nhv, w=0.420; !=0.450; m=1; b g s d nhv nhv, w=0.750; !=0.450; m=1; b g s d		
nhv		
8043 nhv nhv, w=1.500; i=0.450; m=1; b g s d		4
nhv		
nhv	d	
nhv	s d	
htv htv; w=20.000; i=0.450; m=1; b g	S	d
phy phy w=5000; i=0.500; m=1; b g s d		
phv phy, w=0.420; 1=0.450; m=1; b g s d d phy w=0.420; 1=0.450; m=1; b g s d d phy phy, w=0.750; 1=0.450; m=1; b g s d d phy phy, w=0.750; 1=0.450; m=1; b g s d d phy phy w=0.750; 1=0.450; m=1; b g s d phy phy w=0.750; m=1; b g s d phy phy w=0.750; m=1; b g s d phy phy w=0.750; m=1; b g s d phy phy w=0.750; m=1; b g s d phy phy phy w=0.750; m=1; b g s d phy phy phy w=0.750; m=1; b g s d phy phy phy w=0.750; m=1; b g s d phy phy phy phy phy phy phy phy phy phy		
		4
		4
phv phy, w=5,000;1-04.50; m=1; b g h s s b g b s b g b b g b s s b b g b b g b b g b b g b b g b b g b b g b b g b b g b b g b b g b b g b b g b b g b b g b b g b b g b b g b b g	d	
	s d	d
phv phy, w=20,000;=0.480; m=1;	S	a d
hhv hhv, w=25.000; =0.500; ==1;		
8050 nhv nhv = 420; 1=500; n=1;		4
nhv		
nhv	d	
nhy	s d	
nhv	S	d
nhv		
nhv		
nhv nhv,w=1,000;=0,400;m=1; b q s d		
8053 nhv nhv, w=1,500; =0,400; m=1;		4
nhv		
nhv	d	
nhv	s d	
nhv	S	d
phv phv, w=5.000; i=0.450; m=1; b g s d		
phv phv, w=0.420; i=0.400; m=1; b g s d		
phv phv, w=0.750; l=0.400; m=1; b g s d		
phv phy, w=1.000; l=0.400; m=1; b g s d		
8054 phv phv, w=1.500; i=0.400; m=1; b g s d		4
phv phy, w=3.000; l=0.400; m=1; b g s d		
phv phr, w=5000; I=0.400; m=1; b g s	d	
phv phv, w=7.000; i=0.400; m=1; b g	s d	
phv phv, w=20,000; l=0,400; m=1; b g	S	d
nhv		
nhv		
ntv		
nhv		
8063 nhv nhv, w=1.500; i=0.350; m=1; b g s d		4
nhv		
nhv	d	
ntv	s d	
nhv nhv, w=20,000; i=0,350; m=1; b g	S	d

Mod #	Group	New Style Name	Old Style Name	Description	Pin 01	Pin 02	Pin 03	Pin 04	Pin 05	Pin 06	Pin 07	Pin 08	Pin 09	Pin 10	Pin 11	Pin 12	Die Row
			phv	phv; w=5.000; l=0.300; m=1;	b	9	 S										
			phv	phv; w=0.420; l=0.350; m=1;	b	g	 	S									
			phv	phv; w=0.750; l=0.350; m=1;	b	g	 		S								
0004			phv	phv; w=1.000; l=0.350; m=1; phv; w=1.500; l=0.350; m=1;	b	9	 			S							- 4
8064			phv phv	pnv; w=1.500; i=0.350; m=1; phv; w=3.000; i=0.350; m=1;	b b	9	 				S						. 4
			phv	phy, w=5.000; i=0.350; m=1; phy; w=5.000; l=0.350; m=1;	b	9	 		ļ			8					-
			phy	phy; w=7.000; i=0.350; m=1;	b	g	 								d		-
			phy	phy; w=20.000; i=0.350; m=1;	b	a a	 					-		3		d	-
	 		nhv	nhv; w=0.42; l=20.0; m=1;	b	q	s	А	1					 	, , , , , , , , , , , , , , , , , , ,	, i	
			nhv	nhv; w=20.0; l=0.5; m=1;	b	g	 ŭ		s	d			+		***************************************		
8363			nhv	nhv; w=1.0; l=1.0; m=1;	b	9	 				s	d	-				4
			nhv	nhv; w=1.0; l=2.0; m=1;	b	a							s	d	†		1
			nhv	nhv; w=1.0; l=4.0; m=1;	b	g									S	d	1
	İ		phv	phv; w=0.42; l=20.0; m=1;	b	g	d	s		ĺ							
			phv	phv; w=20.0; I=0.5; m=1;	b	9			d	s							1
8364			phv	phv; w=1.0; l=1.0; m=1;	b	g					d	S					4
			phv	phv; w=1.0; l=2.0; m=1;	b	g							d	S			
			phv	phv; w=1.0; l=4.0; m=1;	b	g									d	S	
			nhv	nhv; w=3.0; l=0.5; m=1;	b	9	S	d									
l			nhv	nhv; w=7.0; l=8.0; m=1;	b	9			S	d							
8389			nhv	nhv; w=7.0; l=0.5; m=1;	b	g	 				s	d					. 4
			nhv	nhv; w=0.42; i=8.0; m=1;	b	g	 						S	d			
			nhv	nhv; w=0.42; I=0.5; m=1;	b	9									S	d	4
			nhvnative	nhvnative; w=10.0; I=0.9; m=1;	b	9	 S	d									
	90		nhvnative	nhvnative; w=1.0; l=25.0; m=1;	b	9	 	S d									
8390			nhvnative	nhvnative; w=0.42; l=0.9; m=1;	b	9	 		ļ		S	d					4
			nhvnative nhvnative	nhvnative; w=10.0; l=4.0; m=1; nhvnative; w=1.0; l=4.0; m=1;	b b	9	 						S	d		d	
	-	-				9		-	1				1	1	3	u u	+
					b b	9	 S										-
nlowet		b	9	 		8	u							- 4			
0391		nlowvt	nlowvt, w=0.42; l=1.0, m=1; nlowvt; w=0.42; l=0.15; m=1;	b	g a					S	u						
			nlowvt	nlowvt; w=0.84; =0.15; m=1;	h	9	 					-	3	u u	s	d	-
	 		nshort	nshort; w=1.68; l=0.15; m=1;	b	0	s	А	1			1	1	1	1	_	
			nshort	nshort; w=7.0; I=8.0; m=1;	b	g q	 <u>.</u>		s	d			-		***************************************		1
8392			nshort	nshort; w=7.0; I=0.15; m=1;	b		 				S	d					- 4
			nshort	nshort: w=0.42: I=8.0: m=1:	b	ā	 						s	d			1
			nshort	nshort; w=0.42; l=0.15; m=1;	b	9	 						1		s	d	1
			ntvnative	ntvnative; w=10.0; I=0.5; m=1;	b	q	s	d									1
			ntvnative	ntvnative; w=0.42; l=0.5; m=1;	b	g			S	d							1
8393			ntvnative	ntvnative; w=0.42; l=0.5; m=1;	b	g					S	d					4
			ntvnative	ntvnative; w=0.42; l=0.5; m=1;	b	g							S	d			
			ntvnative	ntvnative; w=0.42; l=0.5; m=1;	b	g									S	d	
			phighvt	phighvt; w=1.68; I=0.15; m=1;	b	9	 d	S	ļ	ļ		ļ	1	1			
			phighvt	phighvt; w=7.0; l=8.0; m=1;	b	9			d d	S							
8394			phighvt	phighvt; w=7.0; l=0.15; m=1;	b	9	 				d	s					. 4
			phighvt	phighvt; w=0.42; I=8.0; m=1;	<u>b</u>	9	 		ļ				d	S			
	1	-	phighvt	phighvt; w=0.42; i=0.15; m=1;	b	g			-			-		+	0	S	+
			phv	phv; w=3.0; l=0.5; m=1;	b	9	 d	S	ļ	ļ			+		ļ		-
0205			phv	phv; w=7.0; l=8.0; m=1;	b	9			d	S			-	+	-		4
8395			phv	phy; w=7.0; l=0.5; m=1; phy; w=0.42; l=8.0; m=1;	b	9	 		ļ	<u> </u>	d d	S		-	-		- 4
			phy	pnv; w=0.42; i=0.0; m=1; phv; w=0.42; i=0.5; m=1;	b b	9	 							S	d	s	-
	+		Pilv	plowvt; w=3.0; l=1.0; m=1;	-	9	d		1			 		+	1	3	+
				plowvt; w=3.0; l=1.0; m=1; plowvt; w=7.0; l=8.0; m=1;	b b	9	 u	8	 			+	+		+		-
8396				plowvt, w=7.0; 1=0.0; m1=1; plowvt; w=7.0; l=0.35; m=1;	b	9	 		ļ	s	d	+	+		+		- 4
0030				plowvt, w=7.0, 1=0.35, m=1, plowvt: w=0.42: =8.0: m=1:	b	9				l	u		1 4		1		1 7
				plowyt; w=0.42; i=0.0; m=1; plowyt: w=0.42; i=0.35; m=1;	b	<u>9</u>			 			†	u	1 3	Н д	s	1
	† 			pshort; w=1.68; l=0.15; m=1;	b	g 0	d	9						+	<u> </u>		+
				pshort; w=1.00, i=0.13, iii=1; pshort; w=7.0; i=8.0; m=1;	b	, , , , , , , , , , , , , , , , , , ,	 u	3	Н			 	+		 		1
8397				pshort; w=7.0; =0.15; m=1;	b	0	 		† <u>*</u>	l	d	s	T		†		- 4
				pshort; w=0.42; l=8.0; m=1;	b	0	 		†	·		†	d	S	<u> </u>		1
				pshort; w=0.42; l=0.15; m=1;	b	9				 		†	1	Ť	d	s	1
		1	1	Parameter and access on the contract of the co		9						1	1	1			

Mod#	Group	New Style Name	Old Style Name	Description	Pin	01	Pin 02	Pin 03	Pin 04	Pin 05	Pin 06	Pin 07	Pin 08	Pin 09	Pin 10	Pin 11	Pin 12	Die Row
	3791956	New Otyle Name	Old Otyle Hallie	pshort; w=7.0; i=0.18; m=1;sa=2.5;sb=2.5;prox_count=0	b	_	711102	d d	S S	111103	1 111 00	111107	111100	111103	111110		1 111 12	Die Now
1	3731330			pshort; w=7.0; =0.18; m=1;sa=1.11;sb=1.11:prox_count=0	- b		9		d	s								
1				pshort; w=7.0; l=0.18; m=1;sa=0.68;sb=0.68;prox_count=0	b h		9			d	s							
1				pshort; w=7.0; i=0.18; m=1:sa=0.48:sb=0.48:prox_count=0	b		9			u	d d	s						
8404				pshort; w=7.0; i=0.18; m=1:sa=0.40;su=0.40;prox_count=0	b		9				<u>-</u>	d d	s				·	4
0404				pshort; w=7.0; I=0.18; m=1;sa=0.265;sb=0.265;prox_count=0	b h		9					- u	d d	s			+	
1				pshort; w=7.0; =0.15; m=1;sa=0.260;sb=0.260;piox_count=0	b b		9							d	s			
1				pshort; w=7.0; i=0.15; m=1;sa=1.11;sb=1.11;prox_count=0	- b		9							<u> </u>	d	S		
1				pshort; w=7.0; =0.15; m=1;sa=0.68;sb=0.68;orox_count=0	h h		n								, , , , , , , , , , , , , , , , , , ,	d	s	
		1		pshort; w=7.0; l=0.15; m=1;sa=0.48;sb=0.48;prox_count=0	b		0	d	s		1	 	1				<u> </u>	+
1 1				pshort; w=7.0; l=0.15; m=1;sa=0.35;sb=0.35;prox_count=0	b		a		d	S	-			-				
				pshort; w=7.0; =0.15; m=1;sa=0.265;sb=0.265;prox_count=0	b		g g			d	S		-				 	
				pshort; w=1.0; l=0.5; m=1;sa=2.5;sb=2.5;prox_count=0	b		a				d	S						
8405				pshort: w=1.0: I=0.5: m=1:sa=1.11:sb=1.11:prox_count=0	b		a					d	s					4
				pshort; w=1.0; I=0.5; m=1;sa=0.68;sb=0.68;prox_count=0	b		g				··		d	S				
1 1				pshort; w=1.0; l=0.5; m=1;sa=0.48;sb=0.48;prox_count=0	b		9				1			d	S		1	
1 1				pshort; w=1.0; l=0.5; m=1;sa=0.35;sb=0.35;prox_count=0	b		9				T				d	S	1	
1 1				pshort; w=1.0; I=0.5; m=1;sa=0.265;sb=0.265;prox_count=0	b		g				1					d	s	
				pshort; w=0.42; l=0.5; m=1;sa=0.48;sb=0.48;prox_count=0	b		g	d	s									
				pshort; w=0.42; l=0.5; m=1;sa=0.35;sb=0.35;prox_count=0	b		g		d	S	1	1	1				1	
				pshort; w=0.42; l=0.5; m=1;sa=0.265;sb=0.265;prox_count=0	b		g			d	S	I	T				T	
1 1				pshort; w=0.42; l=0.15; m=1;sa=2.5;sb=2.5;prox_count=0	b		g				d	S	T	T			T	
8407				pshort; w=0.42; l=0.15; m=1;sa=1.11;sb=1.11;prox_count=0	b		9					d	S					4
				pshort; w=0.42; l=0.15; m=1;sa=0.68;sb=0.68;prox_count=0	b		9				T		d	S				
				pshort; w=0.42; l=0.15; m=1;sa=0.48;sb=0.48;prox_count=0	b		9							d	S			
				pshort; w=0.42; l=0.15; m=1;sa=0.35;sb=0.35;prox_count=0	b		g								d	S		
				pshort; w=0.42; l=0.15; m=1;sa=0.265;sb=0.265;prox_count=0	b		g									d	S	
				pshort; w=7.0; I=0.15; m=1;sa=1.11;sb=1.11;prox_count=1;prox_spc=0.42	b		g	d	S									
1 [pshort; w=7.0; I=0.15; m=1;sa=1.11;sb=1.11;prox_count=1;prox_spc=0.62	b		g		d	S								
1 [pshort; w=7.0; l=0.15; m=1;sa=2.5;sb=2.5;prox_count=1;prox_spc=0.28	b		g			d	S							
				pshort; w=7.0; l=0.15; m=1;sa=2.5;sb=2.5;prox_count=1;prox_spc=0.32	b		g				d	S						
8413				pshort; w=7.0; l=0.15; m=1;sa=2.5;sb=2.5;prox_count=1;prox_spc=0.42	b		g					d	S					4
				pshort; w=7.0; l=0.15; m=1;sa=2.5;sb=2.5;prox_count=1;prox_spc=0.62	b		9						d	S				
				pshort; w=7.0; l=0.15; m=1;sa=2.5;sb=2.5;prox_count=1;prox_spc=1.0	b		g							d	S			
1 1				pshort; w=7.0; i=0.15; m=1;sa=2.5;sb=2.5;prox_count=1;prox_spc=1.5	b		g								d	S		
				pshort; w=7.0; l=0.15; m=1;sa=2.5;sb=2.5;prox_count=1;prox_spc=2.0	b		g									d	S	
				phighvt; w=7.0; I=0.18; m=1;sa=2.5;sb=2.5;prox_count=0	b		9	d	S									
				phighvt; w=7.0; i=0.18; m=1;sa=1.11;sb=1.11;prox_count=0	b		9		d	S								
				phighvt; w=7.0; l=0.18; m=1;sa=0.68;sb=0.68;prox_count=0	b		9			d	S							
8418				phighvt; w=7.0; l=0.18; m=1;sa=0.48;sb=0.48;prox_count=0	b		9				d	S d						4
8418				phighvt; w=7.0; l=0.18; m=1;sa=0.35;sb=0.35;prox_count=0 phighvt; w=7.0; l=0.18; m=1;sa=0.265;sb=0.265;prox_count=0	b		g					d	S					4
				phighvt; w=7.0; l=0.16; m=1;sa=0.265;sb=0.265;prox_count=0 phighvt; w=7.0; l=0.15; m=1;sa=2.5;sb=2.5;prox_count=0	b h		9						d	s d				
				phighvt; w=7.0; i=0.15; m=1;sa=2.5;s0=2.5;prox_count=0 phighvt; w=7.0; i=0.15; m=1;sa=1.11;sb=1.11;prox_count=0	D h		9							a a	s d			
1				phighvt, w=7.0; 1=0.15; m=1;sa=1.11;su=1.11;piox_count=0	b b		g								u	s d		
\vdash		-	+	phighyt; w=7.0; l=0.15; m=1;sa=0.66;su=0.60;piox_count=0	b		g	d	s	_	-	-	-			u u	S	+
				phighvt; w=7.0; i=0.15; m=1;sa=0.46;s0=0.46;prox_count=0 phighvt; w=7.0; i=0.15; m=1;sa=0.35;sb=0.35;prox_count=0	b h		9	u u	s	s								
}				phighvt; w=7.0; i=0.15; m=1;sa=0.35;s0=0.35;prox_count=0 phighvt; w=7.0; i=0.15; m=1;sa=0.265;sb=0.265;prox_count=0	D h		g			s	s	-						
}				phighvt; w=1.0; l=0.5; m=1;sa=2.5;sb=2.5;prox_count=0	b h		9			u	d d	s	+				 	
8419				phighvt, w=1.0; i=0.5; m=1;sa=2.5;s0=2.5;prox_count=0 phighvt; w=1.0; i=0.5; m=1;sa=1.11;sb=1.11;prox_count=0	b h		9				u	d	s	+			·····	4
0413		 		phighvt; w=1.0; i=0.5; m=1;sa=1.11;sb=1.11;phio_count=0	b		9				+	+	d d	s			 	
				phighvt; w=1.0; i=0.5; m=1;sa=0.06;so=0.06;prox_count=0 phighvt; w=1.0; i=0.5; m=1;sa=0.48;sb=0.48;prox_count=0	b		9				+	 	- u	d d	s			
				phighyt; w=1.0; l=0.5; m=1;sa=0.46;so=0.46;prox_count=0	b h		g					<u> </u>	 	u u	d d	S		
				phightt; w=1.0; i=0.5; m=1;sa=0.365;sb=0.365;prox_count=0	- b		g g					·	 		3	d	s	
		<u> </u>		phight; w=0.42; l=0.5; m=1;sa=0.265;sb=0.265;prox_count=0	b		0	d	s		1	1	<u> </u>			<u> </u>	_ <u> </u>	
				phighyt; w=0.42; l=0.5; m=1;sa=0.35;sb=0.35;prox_count=0	b		g		ď	S	1	1	†	T			İ	
				phighvt; w=0.42; I=0.5; m=1;sa=0.265;sb=0.265;prox_count=0	b		g			d	S	1	†				†	
				phighyt: w=0.42; =0.15; m=1:sa=2.5:sb=2.5;prox count=0	b		a				d	S	†				†	
8421				phighyt; w=0.42; I=0.15; m=1;sa=1.11;sb=1.11;prox_count=0	b		g				1	d	S					4
				phighyt; w=0.42; I=0.15; m=1;sa=0.68;sb=0.68;prox_count=0	b		q					1	d	S			1	
				phighvt; w=0.42; I=0.15; m=1;sa=0.48;sb=0.48;prox_count=0	b		g					<u> </u>	1	d	S			
				phighvt; w=0.42; I=0.15; m=1;sa=0.35;sb=0.35;prox_count=0	b		g				1		1		d	S	1	
				phighvt; w=0.42; l=0.15; m=1;sa=0.265;sb=0.265;prox_count=0	b		g				1					d	S	
				•														_

Mod#	Group	New Style Name	Old Style Name	Description	Pin 01	Pi	in 02	Pin 03	Pin 04	Pin 05	Pin 06	Pin 07	Pin 08	Pin 09	Pin 10	Pin 11	Pin 12	Die Row
				plowvt; w=7.0; I=0.35; m=1;sa=2.5;sb=2.5;prox_count=0	b		g	d	S									
				plowvt; w=7.0; l=0.35; m=1;sa=1.11;sb=1.11;prox_count=0	b		g		d	S								
				plowvt; w=7.0; l=0.35; m=1;sa=0.68;sb=0.68;prox_count=0	b		g			d	S							
				plowvt; w=7.0; I=0.35; m=1;sa=0.48;sb=0.48;prox_count=0	b		g				d	S						
8426				plowvt; w=7.0; l=0.35; m=1;sa=0.35;sb=0.35;prox_count=0	b		g					d	S					4
				plowvt; w=7.0; l=0.35; m=1;sa=0.265;sb=0.265;prox_count=0	b		g						d	S				
				plowvt; w=0.42; l=0.5; m=1;sa=2.5;sb=2.5;prox_count=0	b		g							d	S			
				plowvt; w=0.42; i=0.5; m=1;sa=1.11;sb=1.11;prox_count=0	b		g								d	S		
				plowvt; w=0.42; i=0.5; m=1;sa=0.68;sb=0.68;prox_count=0	b		g									d	S	
				plowvt; w=0.42; i=1.0; m=1;sa=0.48;sb=0.48;prox_count=0	b		g	d	S									
				plowvt; w=0.42; l=1.0; m=1;sa=0.35;sb=0.35;prox_count=0	b		g		d	S								
				plowvt; w=0.42; l=1.0; m=1;sa=0.265;sb=0.265;prox_count=0	b		g			d	S							
				plowvt; w=0.42; l=0.35; m=1;sa=2.5;sb=2.5;prox_count=0	b		g				d	S						
8429				plowvt; w=0.42; i=0.35; m=1;sa=1.11;sb=1.11;prox_count=0	b		g					d	S					4
				plowvt; w=0.42; l=0.35; m=1;sa=0.68;sb=0.68;prox_count=0	b		g						d	S				
				plowvt; w=0.42; l=0.35; m=1;sa=0.48;sb=0.48;prox_count=0	b		g							d	S			
				plowvt; w=0.42; l=0.35; m=1;sa=0.35;sb=0.35;prox_count=0	b		g								d	S		
				plowvt; w=0.42; l=0.35; m=1;sa=0.265;sb=0.265;prox_count=0	b		g									d	s	
				nshort; w=7.0; l=0.18; m=1;sa=2.5;sb=2.5;prox_count=0	b		g	S	d									
				nshort; w=7.0; l=0.18; m=1;sa=1.11;sb=1.11;prox_count=0	b		g		S	d								
				nshort; w=7.0; l=0.18; m=1;sa=0.68;sb=0.68;prox_count=0	b		g			S	d							
				nshort; w=7.0; l=0.18; m=1;sa=0.48;sb=0.48;prox_count=0	b		g				S	d						
8434				nshort; w=7.0; l=0.18; m=1;sa=0.35;sb=0.35;prox_count=0	b		g					S	d					4
				nshort; w=7.0; l=0.18; m=1;sa=0.265;sb=0.265;prox_count=0	b		g						S	d				
				nshort; w=7.0; l=0.15; m=1;sa=2.5;sb=2.5;prox_count=0	b		g							S	d			
				nshort; w=7.0; l=0.15; m=1;sa=1.11;sb=1.11;prox_count=0	b		g								S	d		
				nshort; w=7.0; l=0.15; m=1;sa=0.68;sb=0.68;prox_count=0	b		g									S	d	
				nshort; w=1.0; l=0.15; m=1;sa=2.5;sb=2.5;prox_count=0	b		g	S	d									T
				nshort; w=1.0; l=0.15; m=1;sa=1.11;sb=1.11;prox_count=0	b		g		S	d								"
				nshort; w=1.0; l=0.15; m=1;sa=0.68;sb=0.68;prox_count=0	b		g			S	d							"
				nshort; w=1.0; l=0.15; m=1;sa=0.48;sb=0.48;prox_count=0	b		g				S	d						
8436				nshort; w=1.0; l=0.15; m=1;sa=0.35;sb=0.35;prox_count=0	b		g					S	d					4
				nshort; w=1.0; l=0.15; m=1;sa=0.265;sb=0.265;prox_count=0	b		g						S	d				
				nshort; w=0.42; l=0.5; m=1;sa=2.5;sb=2.5;prox_count=0	b		g							S	d			1
				nshort; w=0.42; l=0.5; m=1;sa=1.11;sb=1.11;prox_count=0	b		g								S	d		"
				nshort; w=0.42; l=0.5; m=1;sa=0.68;sb=0.68;prox_count=0	b		g									S	d	
				nlowvt; w=7.0; l=0.18; m=1;sa=2.5;sb=2.5;prox_count=0	b		g	S	d									T 1
				nlowvt; w=7.0; l=0.18; m=1;sa=1.11;sb=1.11;prox_count=0	b		g		S	d								
				nlowvt; w=7.0; I=0.18; m=1;sa=0.68;sb=0.68;prox_count=0	b		g			s	d							
				nlowvt; w=7.0; l=0.18; m=1;sa=0.48;sb=0.48;prox_count=0	b		g				S	d						-
8442				nlowvt; w=7.0; l=0.18; m=1;sa=0.35;sb=0.35;prox_count=0	b		g					S	d					4
				nlowvt; w=7.0; l=0.18; m=1;sa=0.265;sb=0.265;prox_count=0	b		g						s	d				
				nlowvt; w=7.0; l=0.15; m=1;sa=2.5;sb=2.5;prox_count=0	b		g							S	d			
				nlowvt; w=7.0; l=0.15; m=1;sa=1.11;sb=1.11;prox_count=0	ь		g								S	d		
				nlowvt; w=7.0; l=0.15; m=1;sa=0.68;sb=0.68;prox_count=0	b		9							1		s	d	
				nlowvt; w=1.0; l=0.15; m=1;sa=2.5;sb=2.5;prox_count=0	b		g	s	d									1
				nlowvt; w=1.0; l=0.15; m=1;sa=1.11;sb=1.11;prox_count=0	b		g		s	d								1
				nlowvt; w=1.0; l=0.15; m=1;sa=0.68;sb=0.68;prox_count=0	b		g			s	d		I	I				1
				nlowvt; w=1.0; l=0.15; m=1;sa=0.48;sb=0.48;prox_count=0	b		g			1	S	d	I	I				
8444				nlowvt; w=1.0; l=0.15; m=1;sa=0.35;sb=0.35;prox_count=0	b		g			1	1	S	d	1				4
				nlowvt; w=1.0; l=0.15; m=1;sa=0.265;sb=0.265;prox_count=0	b		g			1	1		s	d				1
				nlowvt; w=0.42; l=1.0; m=1;sa=2.5;sb=2.5;prox_count=0	b		g			1	1		1	S	d	1	1	1
			1	nlowvt; w=0.42; l=1.0; m=1;sa=1.11;sb=1.11;prox_count=0	b		g			1	1		1	1	S	d	1	1
				nlowvt; w=0.42; l=1.0; m=1;sa=0.68;sb=0.68;prox_count=0	b		g			1	1		1	1		s	d	
				nlowvt; w=7.0; l=0.15; m=1;sa=1.11;sb=1.11;prox_count=1;prox_spc=0.42	b		g	s	d									1
			<u> </u>	nlowvt; w=7.0; I=0.15; m=1;sa=1.11;sb=1.11;prox_count=1;prox_spc=0.62	b		g		S	d			1	1				**
			<u> </u>	nlowvt; w=7.0; l=0.15; m=1;sa=2.5;sb=2.5;prox_count=1;prox_spc=0.28	b		g			s	d		1	1				-
			†	nlowvt; w=7.0; l=0.15; m=1;sa=2.5;sb=2.5;prox_count=1;prox_spc=0.32	b		a		İ	T	s	d	†	<u> </u>	<u> </u>		İ	1
8451		<u> </u>	1	nlowvt; w=7.0; i=0.15; m=1;sa=2.5;sb=2.5;prox_count=1;prox_spc=0.42	b		a		İ	1	† <u>-</u>	s	d	1	İ		İ	4
		-		nlowvt; w=7.0; i=0.15; m=1;sa=2.5;sb=2.5;prox_count=1;prox_spc=0.62	b		a a		-	+	t	t	s	d				-1 -
				nlowvt; w=7.0; l=0.15; m=1;sa=2.5;sb=2.5;prox_count=1;prox_spc=1.0	h		g g			·	†		†	s s	d			-
				nlowvt; w=7.0; l=0.15; m=1;sa=2.5;sb=2.5;prox_count=1;prox_spc=1.5	h		g g				İ		 	†	s	d		
			 	nlowvt; w=7.0; l=0.15; m=1;sa=2.5;sb=2.5;prox_count=1;prox_spc=2.0	h		g g				İ		 	 		s	d	-
		1	1		U		9								1			

Mod #	Group	New Style Name	Old Style Name	Description	Pin 01	Pin 02	Pin 03	Pin 04	Pin 05	Pin 06	Pin 07	Pin 08	Pin 09	Pin 10	Pin 11	Pin 12	Die Row
				phv; w=5.0; l=0.5; m=1;sa=2.5;sb=2.5;prox_count=0	b	g	d	s									1
				phv; w=5.0; l=0.5; m=1;sa=1.11;sb=1.11;prox_count=0	b	9		d	S								-
				phv; w=5.0; l=0.5; m=1;sa=0.68;sb=0.68;prox_count=0	b	9			d	S							
				phv; w=5.0; l=0.5; m=1;sa=0.48;sb=0.48;prox_count=0	b	9				d	S						
8456				phv; w=5.0; l=0.5; m=1;sa=0.35;sb=0.35;prox_count=0	b	g					d	S					4
				phv; w=5.0; l=0.5; m=1;sa=0.265;sb=0.265;prox_count=0	b	9						d	S				-
				phv; w=1.0; l=0.5; m=1;sa=0.265;sb=2.5;prox_count=0	b	g							d	S			
				phv; w=1.0; l=0.5; m=1;sa=0.265;sb=0.35;prox_count=0	b	9								d	S		
				phv; w=1.0; l=0.5; m=1;sa=0.265;sb=0.48;prox_count=0	b	g									d	S	"
				phv; w=0.42; l=0.8; m=1;sa=0.48;sb=0.48;prox_count=0	b	g	d	S									T
				phv; w=0.42; l=0.8; m=1;sa=0.35;sb=0.35;prox_count=0	b	g		d	s								-
				phv; w=0.42; l=0.8; m=1;sa=0.265;sb=0.265;prox_count=0	b	g			d	S							
				phy; w=0.42; I=0.5; m=1;sa=2.5;sb=2.5;prox_count=0	b	q				d	S						
8459				phv; w=0.42; I=0.5; m=1;sa=1.11;sb=1.11;prox_count=0	b	9					d	s					4
				phy; w=0.42; I=0.5; m=1;sa=0.68;sb=0.68;prox_count=0	b	q						d	S				-
				phv; w=0.42; I=0.5; m=1;sa=0.48;sb=0.48;prox_count=0	b	q							d	S			
				phv; w=0.42; I=0.5; m=1;sa=0.35;sb=0.35;prox_count=0	b	q					<u> </u>			d	S		
				phy: w=0.42; l=0.5; m=1;sa=0.265;sb=0.265;prox_count=0	ь	a					<u> </u>				d	s	-
				nhy: w=5.0: l=0.5: m=1:sa=2.5:sb=2.5:prox_count=0	b	a	s	d									1
				nhv; w=5.0; l=0.5; m=1;sa=1.11;sb=1.11;prox_count=0	Ь	ā		s	d		<u> </u>	<u> </u>		<u> </u>			-
				nhv: w=5.0: I=0.5: m=1:sa=0.68:sb=0.68:prox_count=0	ь	ā			s	d	<u> </u>						-
		<u> </u>		nhv: w=5.0: I=0.5: m=1:sa=0.48:sb=0.48:prox_count=0	b	ā				S	d			***************************************			-
8466		<u> </u>		nhv: w=5.0: I=0.5: m=1:sa=0.35:sb=0.35:prox_count=0	b	ā	•				S	d		***************************************			- 4
				nhv; w=5.0; l=0.5; m=1;sa=0.265;sb=0.265;prox_count=0	b	ā	•					S	d				-
				nhv; w=1.0; I=0.5; m=1;sa=0.265;sb=2.5;prox_count=0	b	a							S	d			-
				nhy: w=1.0; l=0.5; m=1:sa=0.265;sb=0.35;prox_count=0	b	a a								8	d		-
				nhy: w=1.0; l=0.5; m=1:sa=0.265;sb=0.48;prox_count=0	b	a										d	-
				nhv: w=0.42: I=0.8: m=1:sa=0.48:sb=0.48:prox_count=0	b	0	s	d								1	+
				nhv; w=0.42; I=0.8; m=1;sa=0.35;sb=0.35;prox_count=0	b	a		s	d		·	-		***************************************			-
				nhv; w=0.42; I=0.8; m=1;sa=0.265;sb=0.265;prox_count=0	h	a	•			d	+	-		•			
				nhv: w=0.42: I=0.5: m=1:sa=2.5:sb=2.5:prox_count=0	h	n	•				d		·	•			
8469				nhv: w=0.42: I=0.5: m=1:sa=1.11:sb=1.11:prox_count=0	h	, n					- S	d	+				- 4
0.100				nhv; w=0.42; I=0.5; m=1;sa=0.68;sb=0.68;prox_count=0	h	, a						s	d	-			-
				Inhv: w=0.42: I=0.5: m=1:sa=0.48:sb=0.48:prox_count=0	h	, n							s .	А			-
				nhv: w=0.42: =0.5: m=1:sa=0.35:sb=0.35:prox_count=0	h	n								٩	- Н		
				nhv: w=0.42; =0.5; m=1:sa=0.265;sb=0.265;prox_count=0	h	n								·	s	д	
8649				nlowyt w/l=0.30/0.15 Mismatch (FET B from 8x8 array)	Substr	y		GateB		SourceB	DrainB		+			-	+-
				nlowyt w/l=0.30/0.15 Mismatch (FET A from 8x8 array)	Substr			Guiob	GateA	SourceA	- Diamb	DrainA	+	•			-
				nlowyt w/l=0.30/0.15 singe FET from 8x8 array	Substr	Gate			Odien	Courcer	-	Didilin	Source	Drain			- 4
				nlowyt wii=0.30/0.15 (standard modeling layout)	Substr	Gate							Source	Dialii	Source	Drain	
	 	<u> </u>		nshort; w=0.65; I=0.25; m=1; contact-gate=0.050um	h	0.00	s	- 4			1		1	1	230100	- Drum	+-
		1		nshort; w=0.42; l=0.5; m=1; contact-gate=0.050um	- D	9	3	u	s	d	-	-		+		-	
8701		1		nshort; w=0.42; i=0.5; m=1; contact-gate=0.050um	h	9		+	3	· · · · · · · · · · · · · · · · · · ·		d		+		+	- 4
0,01				nshort, w=0.35; i=0.15; m=1; contact-gate=0.050um	<u>р</u>	9				-	s	u	s	д		+	
				nshort; w=0.39; l=0.15; m=1; contact-gate=0.050um		9					+		- S	- u	9		-
		1	1	manuri, w-0.00, r-0.10, m-1, contact-gate-0.000m	1 0	y				1		1	1	1		L u	