(20%) 1. Figs. 1(a) and 1(b) show a basic current source and Widlar current source, respectively. Assume that V_{BE} is 0.7V at a current of 1mA, the thermal voltage V_T=25mV, V_{CC}=10V, and neglect the effect of finite β. **To generate a current I_O=10μA**,

(a) find **R_1** in Fig. 1(a). (5%)

(b) for Fig. 1(b), if **I_{REF}=1mA**, find **R_2 and R_3**. (10%)

(c) explain the advantage of Widlar current source. (5%)

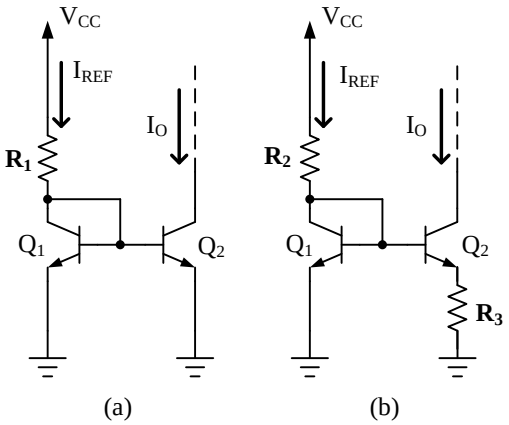

Fig. 1

(15%) 2. Figs. 2(a) and 2(b) show two different types of output stage, respectively. Assume that V_T=25mV, $I_S=3\times10^{-14}$A for Q_{14} and Q_{20}, while $I_S=10^{-14}$A for the other BJTs, R_{10}=40kΩ, and **I_{C13A}=280μA**. Neglect the base currents of all BJTs.

(a) In Fig. 2(a), if **V_{BE18} is found to be 0.6V** iteratively, find **I_{C18}, I_{C19}, and I_{C20}**. (10%)

(b) In Fig. 2(b), if Q_{25} and Q_{26} are used to establish the voltage drop between the bases of Q_{14} and Q_{20}, find **I_{C14}**. (5%)

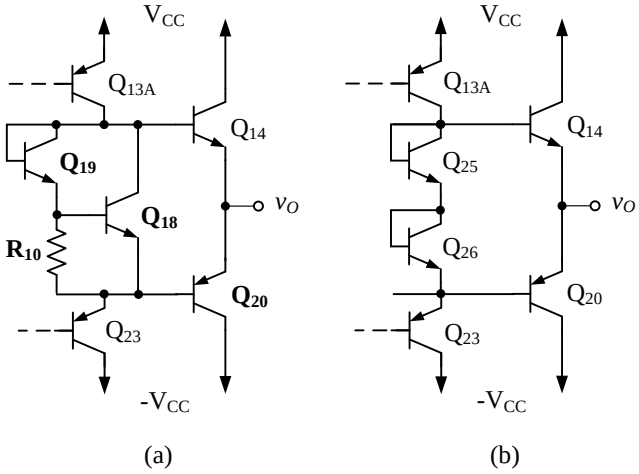

Fig. 2

(15%) 3. Please give definitions of the following terms.

(a) slew rate (5%)

(b) inter-modulation distortion (5%)

(c) total harmonic distortion (5%)

(20%) 4. For a class-B output stage in Fig. 4, let dual-supply voltage V_{CC}=10V and R_L=8Ω. If the output v_O is an **8-V-peak** sinusoid.

(a) Neglecting the crossover distortion, please find the **average power delivered to the load R_L**, the **average power drawn from the supplies**, and the **power-conversion efficiency η**. (15%)

(b) Please explain the crossover distortion for the output stage in Fig. 4 (5%)

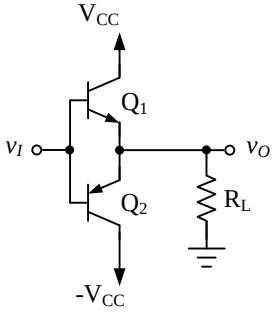

Fig. 4

(15%) 5. Figs. 5(a) and 5(b) show two different types of CMOS class AB output stage, respectively. Assume $|V_{OV}|$=0.2V for all transistors, $|V_{tp}|$=0.8V, V_{tn}=0.7V, and dual-supply voltage V_{CC}=2.5V.

(a) Fig. 5(a) shows a class AB utilizing source followers Q_1 and Q_2, please find the **output swing range of v_O** (5%)

(b) Fig. 5(b) shows a class AB utilizing common-source transistors Q_5 and Q_6, please find the **output swing range of v_O** (5%)

(c) Please **draw** a modified output stage to reduce the output resistance of Fig. 5(b) **by using feedback**. Briefly explain your reason. (5%)

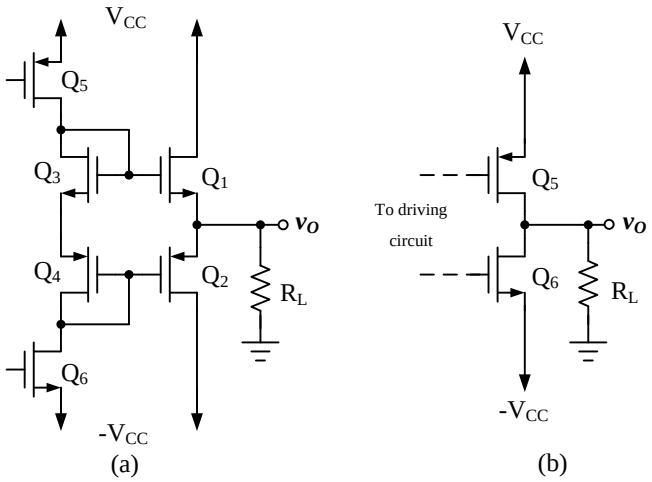

Fig. 5

(15%) 6. When a power transistor is operated at junction temperature T_J of 150°C with a heat sink, the case temperature T_C is found to be 120°C. The case is attached to the heat sink with a bond having a thermal resistance θ_{CS}=0.7°C/W and the thermal resistance of the heat sink θ_{SA}=0.2°C/W, as shown in Fig. 6. If the ambient temperature T_A is 30°C, please calculate

(a) heat sink temperature $\mathbf{T_S}$. (5%)

(b) power dissipated in the device $\mathbf{P_D}$. (5%)

(c) thermal resistance from junction to case, $\boldsymbol{\theta_{JC}}$. (5%)

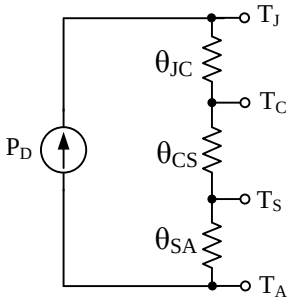

Fig. 6