Mid-term Exam I Microelectronics (III) NCKUEE 10/26/2010

(10%) 1. Feedback circuits can be classified into four basic topologies (e.g. Trans…amplifier). As shown in Fig. P1(a) and (b), please respectively specify which types the two configurations are. Explain your reasons.

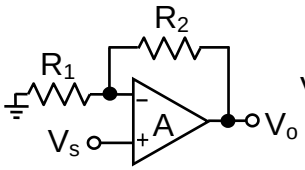

Fig. P1(a)

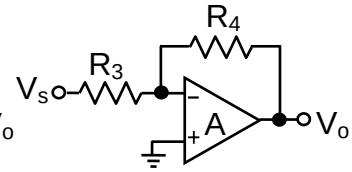

Fig. P1(b)

(20%) 2. The open-loop gain Bode plot of an op amp is shown in Fig. P2. It's a three-pole system with pole locations on 10^6 10^8 and 10^9 Hz. If the op amp is connected in the non-inverting configuration, as shown in Fig. P1(a).

(a) What is the acceptable range of (R_2/R_1) to prevent the system from unstable operation? (10%)

(b) If the phase margin of 63° is required, please find the unity-gain bandwidth of loop gain (Aβ), and the closed-loop gain.(10%)

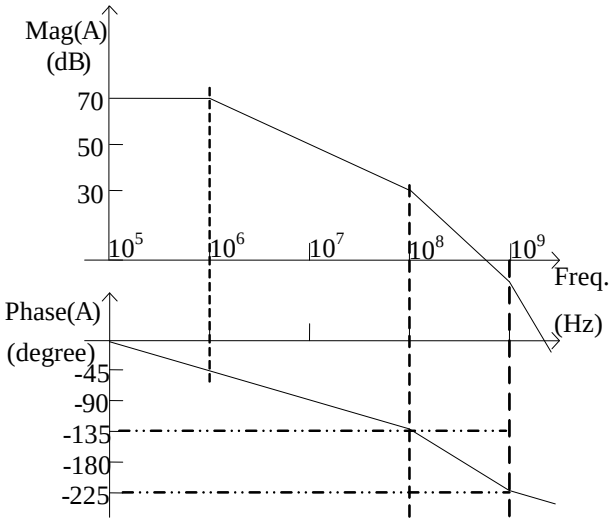

Fig. P2

(15%) 3. Consider a closed-loop circuit shown in Fig. P3. Assume input resistance of the basic amplifier is infinite, open-loop gain $\mu = 10^3$ V/V, $r_o = R_L = 100$k Ω, $R_1 = R_2 = 50$k Ω, $C_L = 1$p F, please calculate the DC-gain of the loop gain, and the dominant pole location of the loop gain.

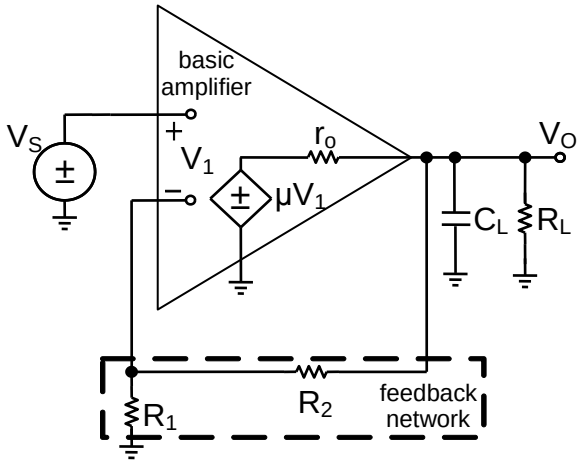

Fig. P3

(20%) 4. Fig. P4(a) shows the simplified small-signal circuit of a two-stage OP before frequency compensation. Let $G_{m1} = 1$m A/V, $G_{m2} = 2$m A/V, $R_1 = R_2 = 100$k Ω, $C_1 = 0.5$p F, $C_2 = 1$p F.

(a) Calculate the pole locations of the system.

(b) C_A is added as shown in Fig. P4(b). To obtain a dominant pole located on 10k Hz, please find C_A.

(c) C_C is inserted as shown in Fig. P4(c). To obtain a dominant pole located on 10k Hz, please find C_C.

(d) Please explain the benefit of inserting C_C.

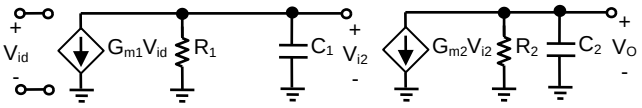

Fig. P4(a)

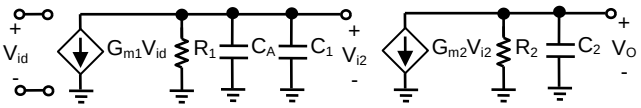

Fig. P4(b)

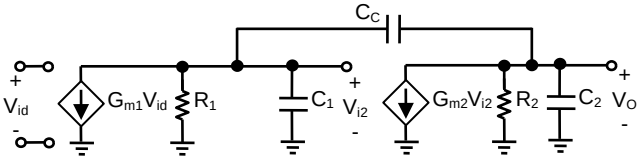

Fig. P4(c)

(15%) 5. A folded-cascode OPAMP is shown in Fig. P5, where I_{M11} = 100μ A, I_{M9} = I_{M10} = 300μ A, and $|V_{OV}|$ for all transistors is 0.2 V. Assume V_{DD} = 3.3 V, Vtn = 0.7 V, |Vtp| = 0.8 V, and C_L=1p F, please find

(a) input common-mode range. (5%)

(b) slew rate. Explain your answer. (10%)

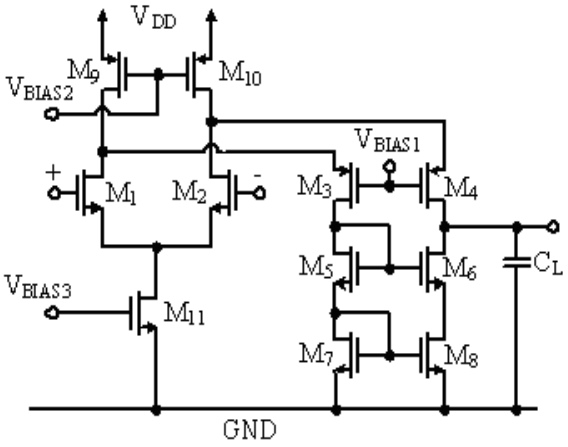

Fig. P5

(20%) 6. A cascode current mirror is shown in Fig. P6(a), and a wide-swing current mirror is shown in Fig. P6(b). The $|V_{OV}|$ for all transistors is 0.2 V and the $|V_t|$ is 0.7 V. All transistors are identical.

(a) Please calculate V_{bias1}, V_{bias2} and the minimum value of V_O in Fig. P6(a). (10%)

(b) Please calculate V_{bias3}, V_{bias4} and the minimum value of V_O in Fig. P6(b). (10%)

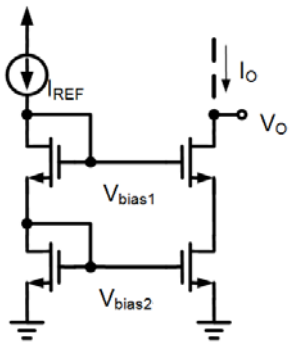

Fig. P6(a)

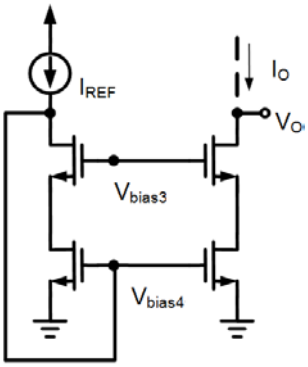

Fig. P6(b)