# Mid-Term Exam II Microelectronics (III) NCKUEE 12/07/2010

**(20%) 1.** Figs. P1(a) and P1(b) are two different types of output stage in the 741 op-amp circuit without the protection circuitry. Assume $V_T$ = 25mV, $I_S = 3\times10^{-14}$A for $Q_{14}$ and $Q_{20}$, $I_S = 10^{-14}$A for the other BJTs, $R_{10}$ = 40kΩ, and $I_{C13A}$ = 280μA. Neglect the base currents of all BJTs.

(a) In Fig. P1(a), if $V_{BE18}$ is found to be 0.6V iteratively, find $I_{C14}$, $I_{C18}$, and $I_{C19}$. **(10%)**

(b) In Fig. P1(b), if $Q_{25}$ and $Q_{26}$ are used to establish the voltage drop between the bases of $Q_{14}$ and $Q_{20}$, find $I_{C14}$. **(10%)**

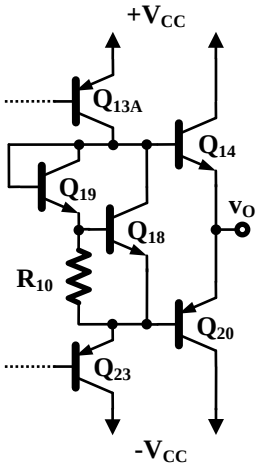


**Fig. P1(a)**

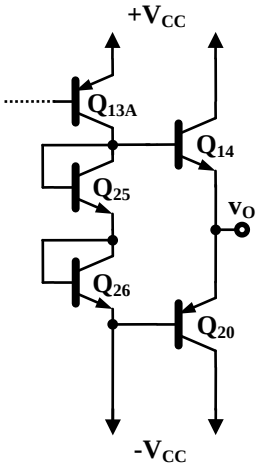


**Fig. P1(b)**

**(20%) 2.** Fig. P2 shows a 3-bit DAC using R-2R resistor ladder network. Given $V_{REF}$ = 1.8V, and R = 10kΩ,

(a) If bits $B_2B_1B_0 = (100)_2$, find $v_X$. **(5%)**

(b) If bits $B_2B_1B_0 = (010)_2$, find $v_X$. **(5%)**

(c) If bits $B_2B_1B_0 = (001)_2$, find $v_X$. **(5%)**

(d) Derive $\frac{V_O}{V_{REF}}$ in terms of $B_0$, $B_1$, $B_2$, $R_1$, and $R_2$. **(5%)**

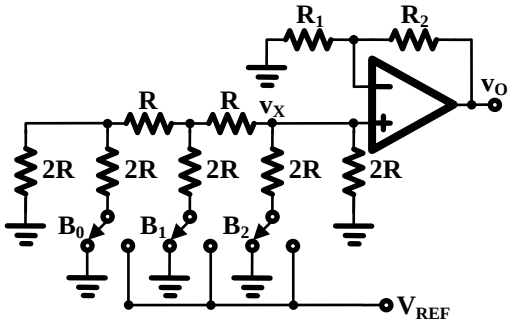


**Fig. P2**

**(10%) 3.** Figs. P3(a) and P3(b) show a 3-bit charge-redistribution ADC, which is operating at hold phase and charge-redistribution phase, respectively.

In Fig. P3(a), switches $B_0$ through $B_2$ are connected to GND. Then, switch $B_2$ is suddenly connected to $V_{REF}$, as shown in Fig. P3(b). Assume $V_{REF}$ = 1.8V and $v_{IN}$ = 1.2V. Find the voltage $v_X$' in Fig. P3(b).

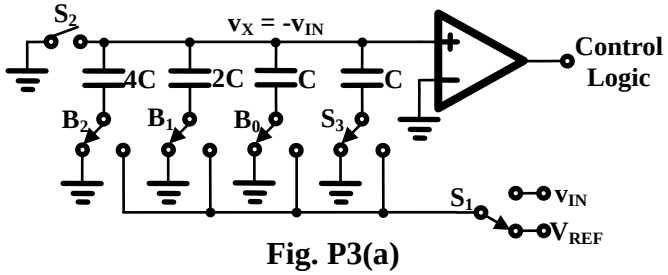


**Fig. P3(a)**

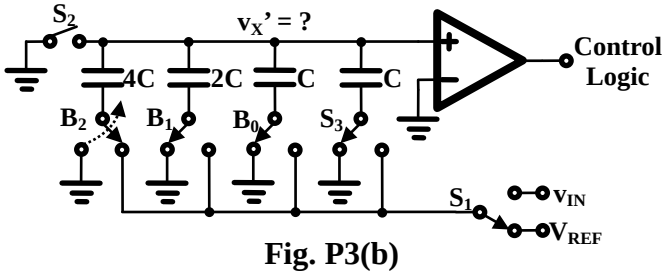


**Fig. P3(b)**

**(10%) 4.** Fig. P4 shows a 14-bit dual-slope ADC. Assume C = 100pF, $V_{REF}$ = -1.8V, and $v_{IN}$ is in the range of 0V and 1.8V. If the maximum conversion time T is 1ms, find the value of R and the required clock frequency $f_{clk}$. ($f_{clk} = 1 / T_{clk}$)

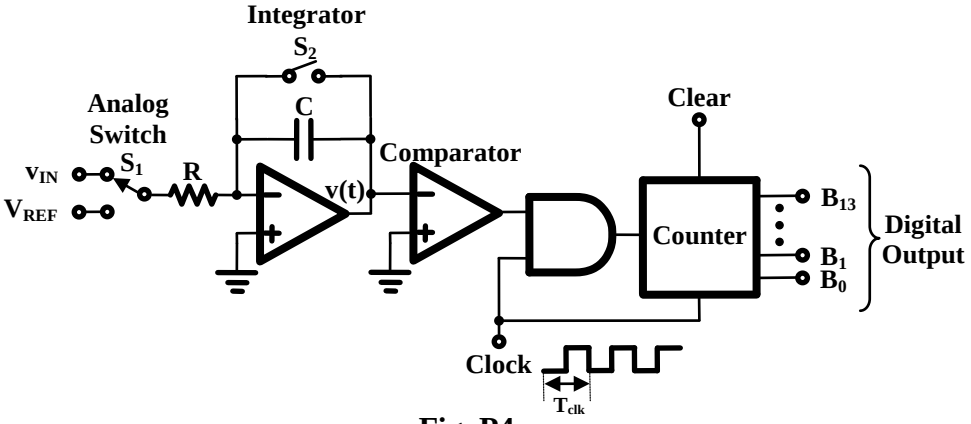


**Fig. P4**

**(20%) 5.** Fig. P5 shows a class AB push-pull amplifier.

(a) Sketch its transfer characteristic $v_O$ vs. $v_{IN}$. **(5%)**

(b) Briefly explain the benefit of adding the two diodes $D_1$ and $D_2$. **(5%)**

(c) Briefly explain "total harmonic distortion." **(5%)**

(d) Show that for matched devices $Q_N$ and $Q_P$, the even-order harmonics at $v_O$ are eliminated. **(5%)**

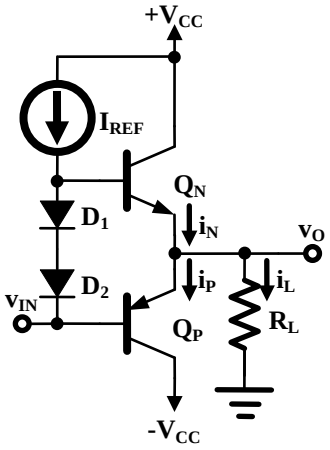


**Fig. P5**

**(20%) 6.** A power BJT is specified to have maximum junction temperature $T_{Jmax}$ of 150°C. Assume the maximum power dissipation is to be derated linearly above 25°C.

(a) Briefly explain "thermal resistance." **(5%)**

(b) Assume this transistor has a maximum power dissipation $P_{D0}$ of 2W at an ambient temperature $T_{A0}$ of 25°C. Find the maximum power $P_{Dmax}$ that can be dissipated safely by this transistor **in free air (with no special arrangements for cooling)** at an ambient temperature $T_A$ = 40°C. **(5%)**

(c) Assume this transistor has a maximum power dissipation $P_{Dmax}(T_{C0})$ of 50W at a case temperature $T_{C0}$ of 25°C, and a heat sink is utilized. The thermal resistance $\theta_{CS}$, between case and heat sink, is 0.5°C/W. $\theta_{SA}$, between heat sink and ambience, is 5°C/W. Find the maximum power $P_{Dmax}$ that can be dissipated safely by this transistor at $T_A$ = 50°C. **(5%)**

(d) Referring to (c), find the maximum power $P_{Dmax}$ that can be dissipated safely by this transistor **with an infinite heat sink** at $T_A$ =50°C. **(5%)**