Solution of Mid-term Exam I

Electronics (III) 2011

Prepared by Shih-Hsiung Chien

Question 1

- With less than 25 words, please list the name of the **four feedback amplifiers** (e.g. Trans... amplifier) and their **corresponding topologies** (e.g. series-shunt). (16%)

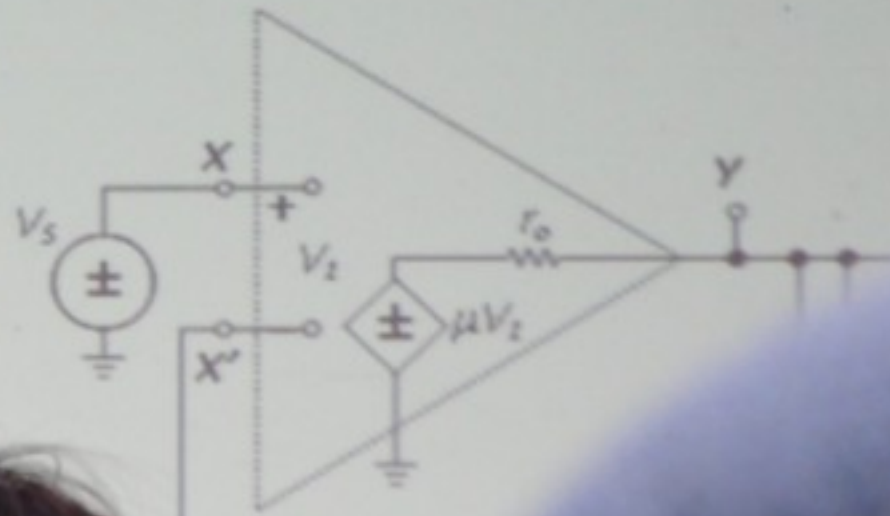
  - Voltage amplifier ↔ series-shunt (4%)
  - Current amplifier ↔ shunt-series (4%)
  - Trans-conductance amplifier ↔ series-series (4%)
  - Trans-impedance amplifier ↔ shunt-shunt (4%) /Trans-resistance amplifier

Question 2

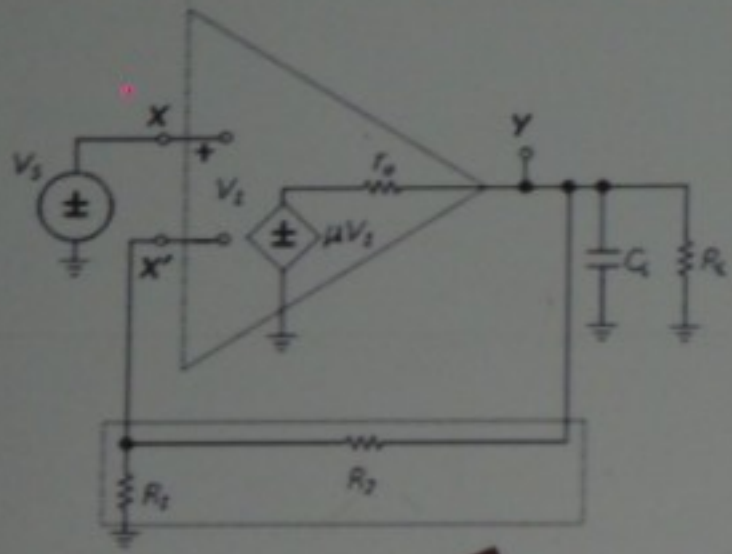
- Consider a closed-loop circuit shown in Fig. P2. Assume that the input impedance of the basic amplifier is **infinite**, open-loop gain μ=6000 V/V, r_o=R_L=100 kΩ, R_1 = R_2 = 50kΩ, C_L=1pF, please **respectively** calculate the **dc gain of the loop gain**, and the **dominant pole location of the loop gain** by

  (a) breaking the loop **at *XX'***. (10%)

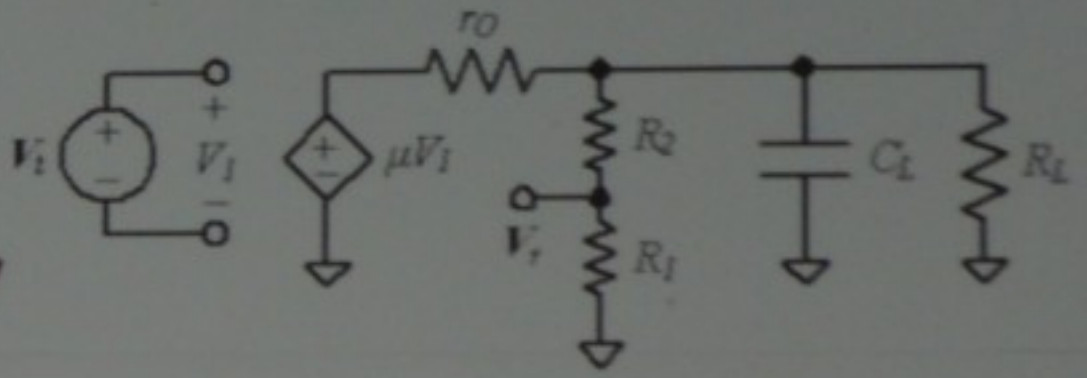
  (b) breaking the loop **at the output of the basic amplifier *Y***. (



Question 2 (cont.)



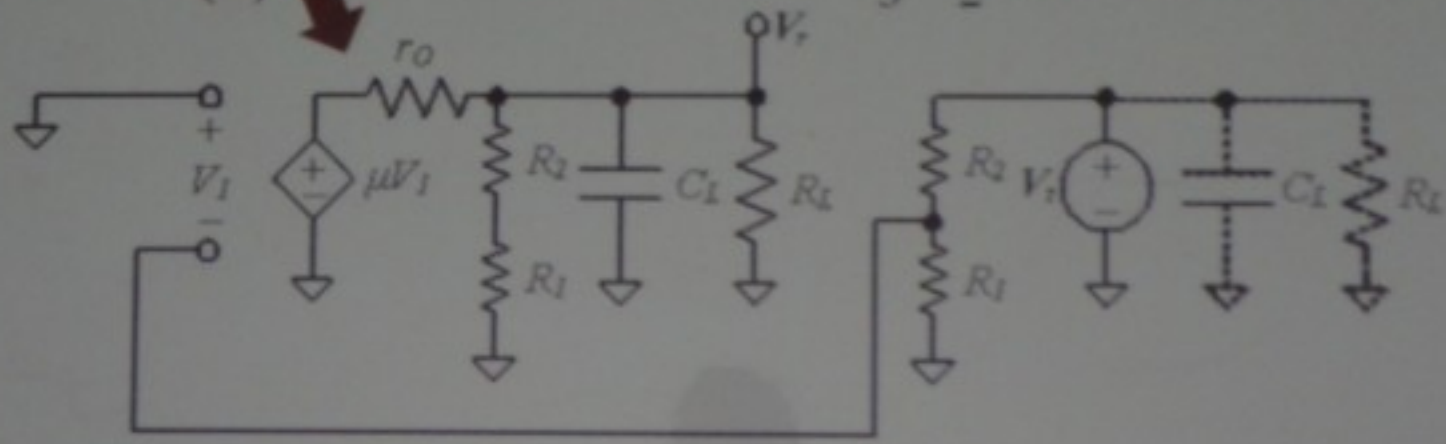
(a)



$$|A\beta| = \mu \cdot \frac{R_L /\!/ (R_1 + R_2)}{r_O + R_L /\!/ (R_1 + R_2)} \cdot \frac{R_1}{R_1 + R_2} \qquad f_{p1} = \frac{1}{2\pi \cdot r_{OUT} C_L}$$

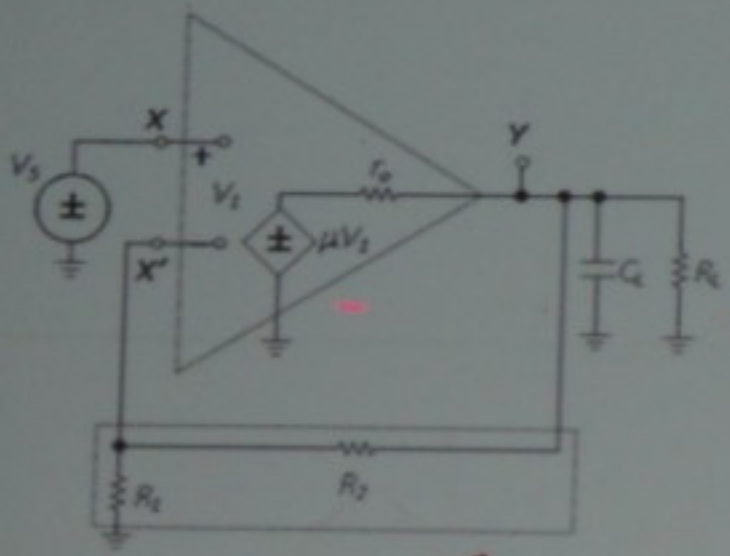
$$= 6000 \times \frac{1}{3} \times \frac{1}{2} = \boxed{1000\ (V/V)} \qquad \boxed{\approx 4.77 MHz}$$

(b)

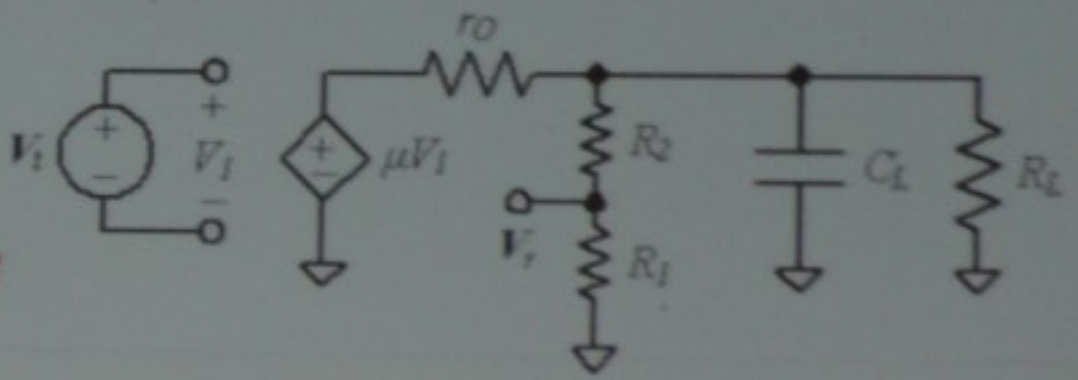


$$|A\beta| = \frac{R_1}{R_1 + R_2} \cdot \mu \cdot \frac{R_L /\!/ (R_1 + R_2)}{r_O + R} = \boxed{1000\ (V/V)} \qquad f_{p1} = \frac{1}{2\pi \cdot r_{OUT} C_L} \qquad \boxed{\approx 4.77\ MHz}$$

Question 2 (cont.)



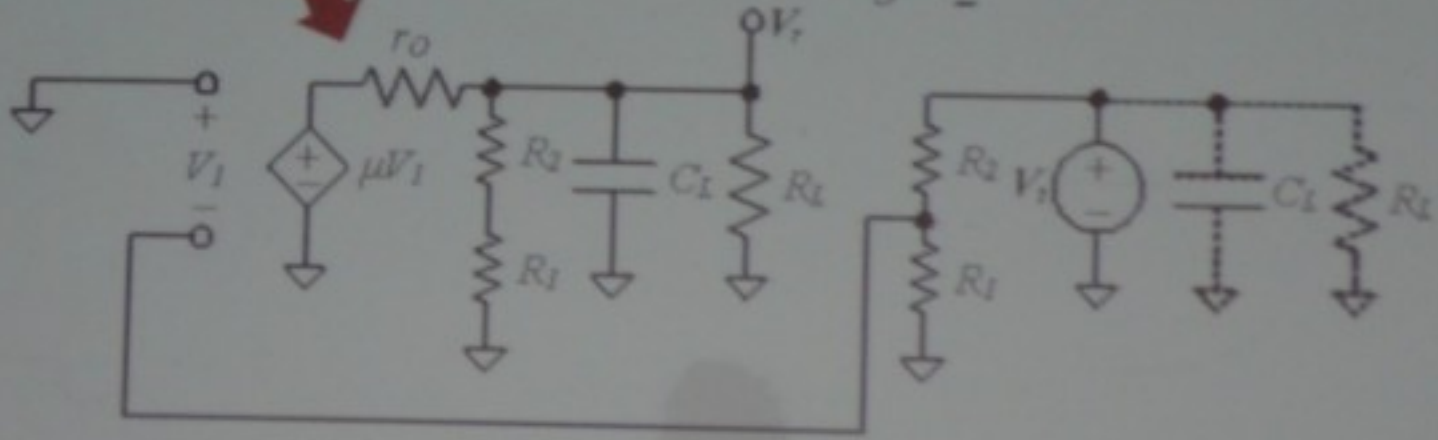
(a)



$$|A\beta| = \mu \cdot \frac{R_L /\!/ (R_1 + R_2)}{r_O + R_L /\!/ (R_1 + R_2)} \cdot \frac{R_1}{R_1 + R_2} \qquad f_{p1} = \frac{1}{2\pi \cdot r_{OUT} C_L}$$

$$= 6000 \times \frac{1}{3} \times \frac{1}{2} = \boxed{1000\ (V/V)} \qquad \boxed{\approx 4.77 MHz}$$

(b)



$$|A\beta| = \frac{R_1}{R_1 + R_2} \cdot \mu \cdot \frac{R_L /\!/ (R_1 + R_2)}{r_O + R_L /\!/ (R_1 + R_2)} = \boxed{1000\ (V/V)} \qquad f_{p1} = \frac{1}{2\pi \cdot r_{OUT} C_L} \qquad \boxed{\approx 4.77\,MHz}$$

Question 3

- Please give definitions of the following terms for an op amp.

(a) -3dB bandwidth (5%)

the frequency at which the gain is attenuated by 3dB, it is also located at the dominant pole frequency.

(b) unity-gain bandwidth (5%)

the frequency at which the gain drops to unity.

(c) CMRR (5%)

ratio of differential gain to common-mode gain

$$\equiv CMRR = \frac{A_{dm}}{A_{cm}}$$

Question 3 (cont.)

(d) PSRR (5%)

$$\begin{cases} PSRR^{+} \equiv \dfrac{A_d}{A^{+}} \\ PSRR^{-} \equiv \dfrac{A_d}{A^{-}} \end{cases} \quad ,where \quad \begin{cases} A^{+} \equiv \dfrac{v_o}{v_{dd}} \\ A^{-} \equiv \dfrac{v_o}{v_{gnd}} \end{cases}$$

$A_d \equiv$ small-signal differential gain

$A^+ \equiv$ small-signal gain from the positive supply rail to the output

$A^- \equiv$ small-signal gain from the negative supply rail to the output

Question 4

- Fig. P4 shows a two-stage op amp with a simple bias circuit. Assume $\mu_n C_{ox}=200\mu A/V^2$, $\mu_p C_{ox}=80\mu A/V^2$, $|V_{tp}|=0.8V$, and $I_{D8}=20\mu A$, $I_{D5}=200\mu A$, $I_{D7}=500\mu A$, and $(W/L)_{M5}=(20\mu m/1\mu m)$, $(W/L)_{M7}=(50\mu m/1\mu m)$, $(W/L)_{M3}=(10\mu m/1\mu m)$. Without considering the channel-length modulation, please

(a) calculate $(W/L)_{M8}$. (5%)

current mirror between M8 and M5

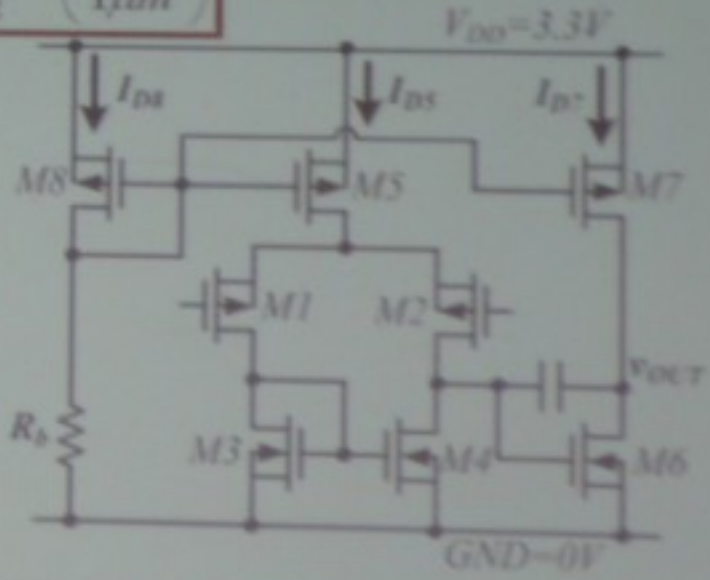
$$\Rightarrow \left(\frac{W}{L}\right)_{M8} : \left(\frac{W}{L}\right)_{M5} = I_{D8} : I_{D5} \Rightarrow \boxed{\left(\frac{W}{L}\right)_{M8} = \left(\frac{2\mu m}{1\mu m}\right)}$$

(b) calculate R_b. (5%)

$$I_{D8} = \frac{1}{2}\mu_p C_{OX}\left(\frac{W}{L}\right)_{M8} V_{OV8}^{\ 2}$$

$$\Rightarrow V_{OV8} = 0.5V$$

$$\Rightarrow R_b = \frac{3.3 - V_{OV8} - |V_{tp}|}{I_{D8}} = \boxed{100k\Omega}$$



Question 4

- Fig. P4 shows a two-stage op amp with a simple bias circuit. Assume $\mu_n C_{ox}=200\mu A/V^2$, $\mu_p C_{ox}=80\mu A/V^2$, $|V_{tp}|=0.8V$, and $I_{D8}=20\mu A$, $I_{D5}=200\mu A$, $I_{D7}=500\mu A$, and $(W/L)_{M5}=(20\mu m/1\mu m)$, $(W/L)_{M7}=(50\mu m/1\mu m)$, $(W/L)_{M3}=(10\mu m/1\mu m)$. Without considering the channel-length modulation, please

(a) calculate $(W/L)_{M8}$. (5%)

current mirror between M8 and M5

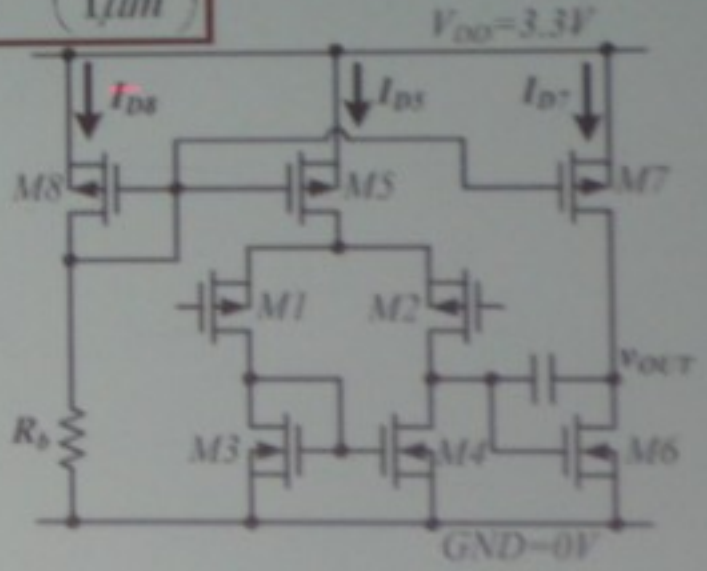
$$\Rightarrow \left(\frac{W}{L}\right)_{M8} : \left(\frac{W}{L}\right)_{M5} = I_{D8} : I_{D5} \Rightarrow \boxed{\left(\frac{W}{L}\right)_{M8} = \left(\frac{2\mu m}{1\mu m}\right)}$$

(b) calculate R_b. (5%)

$$I_{D8} = \frac{1}{2}\mu_p C_{OX}\left(\frac{W}{L}\right)_{M8} V_{OV8}^{\ 2}$$

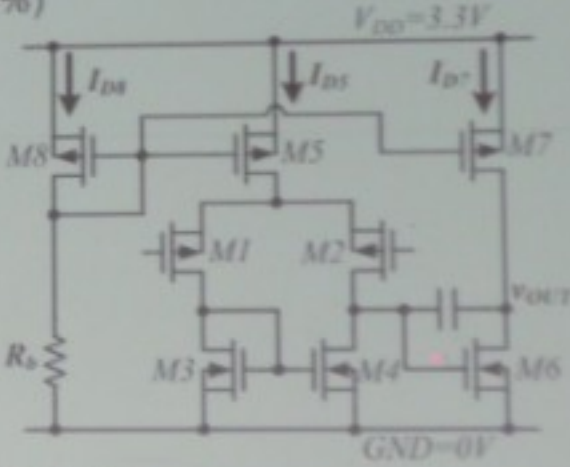
$$\Rightarrow V_{OV8} = 0.5V$$

$$\Rightarrow R_b = \frac{3.3 - V_{OV8} - |V_{tp}|}{I_{D8}} = \boxed{100k\Omega}$$



Question 4 (cont.)

(c) design the $(W/L)_{M6}$ to minimize the input systematic offset if the input stage is perfectly balanced. (5%)



$$I_{D3}:I_{D6}=\left(\frac{W}{L}\right)_{M3}:\left(\frac{W}{L}\right)_{M6}$$

$$I_{D5}:I_{D7}=\left(\frac{W}{L}\right)_{M5}:\left(\frac{W}{L}\right)_{M7}=(2\cdot I_{D3}):I_{D6}$$

$$\left(\frac{W}{L}\right)_{M6}=\frac{2\cdot\left(\frac{W}{L}\right)_{M3}\cdot\left(\frac{W}{L}\right)_{M7}}{\left(\frac{W}{L}\right)_{M5}}=\boxed{\left(\frac{50\mu m}{1\mu m}\right)}$$

(d) find the **output swing** of the op amp. (5%)

$$I_{D6}=\frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_{M6}V_{OV6}^{\ 2}\Rightarrow V_{OV6}\approx 0.316V$$

output swing :

$$\boxed{0.316V}\le\boxed{V_{OV6}\le v_{OUT}\le V_{DD}-V_{OV7}}=VDD-V_{OV5}=\boxed{2.8V}$$

Question 5

- A folded-cascode op amp is shown in Fig. P5 where I_{M11}=200μA, I_{M10}=300μA, and $|V_{OV}|$ for all transistors is 0.2V. Assuming λ_n=0.1V^{-1}, λ_p=0.2V^{-1}, V_{DD}=3.3V, V_{tn}=0.8V, $|V_{tp}|$=0.8V, and C_L=1pF, please

(a) calculate **dc gain**. (5%)

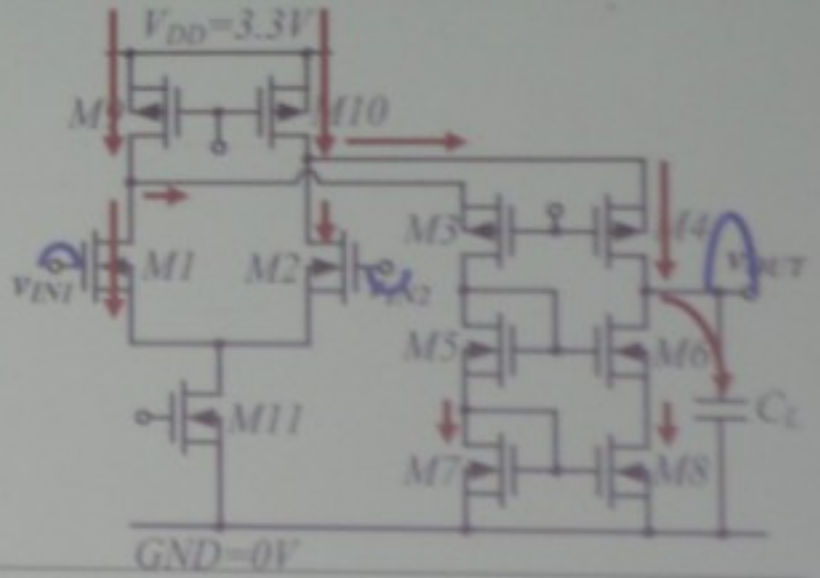
$$r_{ds} = \frac{1}{\lambda I_D},\quad g_m = \frac{2I_D}{V_{OV}}$$

$$A_d = g_{m1} \cdot R_{OUT} = g_{m1} \cdot \{(g_{m4} r_{ds4}) \cdot (r_{ds2} // r_{ds10})\} // [g_{m6} r_{ds6} r_{ds8}] \approx 1m \cdot 625k = \boxed{625\,V/V}$$

(b) calculate **slew rate**. (5%)

$$Slew\ Rate = \frac{I_{D11}}{C_L} = \boxed{200\ (V/\mu s)}$$

(c) specify which node is the **positive** input terminal ($\boxed{v_{IN1}}$ or v_{IN2}). Explain your answer. (5%)



Question 5

- A folded-cascode op amp is shown in Fig. P5 where I_{M11}=200μA, I_{M10}=300μA, and $|V_{OV}|$ for all transistors is 0.2V. Assuming λ_n=0.1V^{-1}, λ_p=0.2V^{-1}, V_{DD}=3.3V, V_{tn}=0.8V, $|V_{tp}|$=0.8V, and C_L=1pF, please

(a) calculate **dc gain**. (5%)

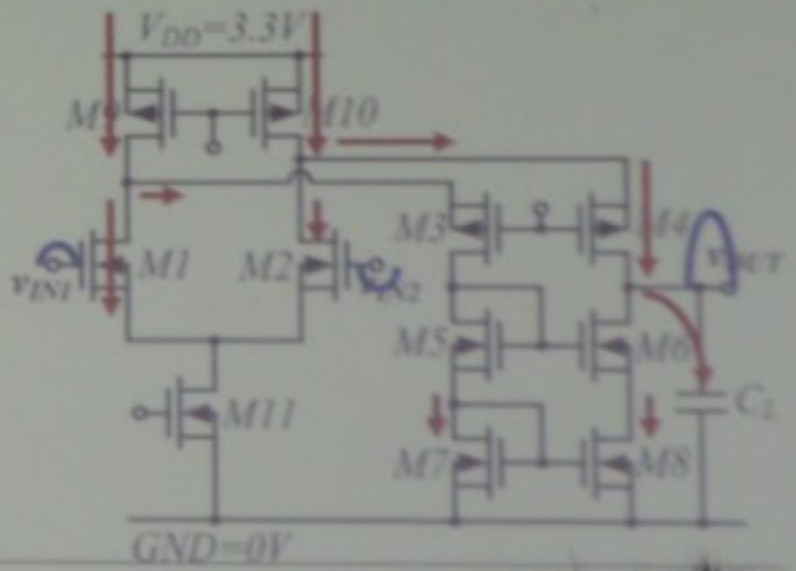
$$r_{ds} = \frac{1}{\lambda I_D}, \quad g_m = \frac{2I_D}{V_{OV}}$$

$$A_d = g_{m1} \cdot R_{OUT} = g_{m1} \cdot \{[(g_{m4} r_{ds4}) \cdot (r_{ds2} // r_{ds10})] // [g_{m6} r_{ds6} r_{ds8}\} \approx 1m \cdot 625k = \boxed{625 (V/V)}$$

(b) calculate **slew rate**. (5%)

$$Slew\ Rate = \frac{I_{D11}}{C_L} = \boxed{200\ (V/\mu s)}$$

(c) specify which node is the **positive** input terminal ($\boxed{v_{IN1}}$ or v_{IN2}). Explain your answer. (5%)



Question 6

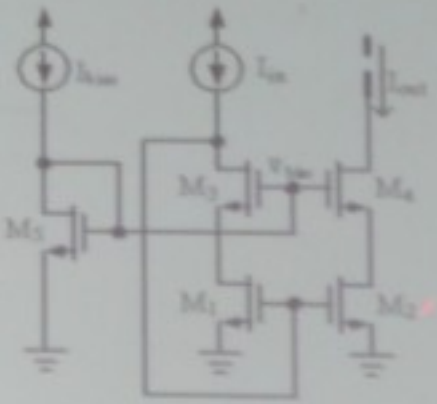
- A wide-swing current mirror is shown in Fig. P6. Assume V_{tn}=0.7V for all transistors, and $I_{bias}=I_{in}=I_{out}$. The V_{OV} of M_1, M_2, M_3, M_4 are 0.3V. In order to minimize the allowable output voltage.

(a) find $\mathbf{V_{OV}}$ **of** $\mathbf{M_5}$. (3%)

$$let\ V_{DS1} = V_{DS4} = V_{OV}$$
$$\Rightarrow V_{bias} = 2 \cdot V_{OV} + V_t = 1.3V$$
$$\Rightarrow V_{OV5} = V_{bias} - V_t = 2V_{OV} = \boxed{0.6V}$$

(b) if $(W/L)_{M1}=(W/L)_{M2}=n_1\cdot(W/L)_{M3}=n_1\cdot(W/L)_{M4}=n_2\cdot(W/L)_{M5}$, what are the values of $\mathbf{n_1}$ and $\mathbf{n_2}$ should be designed? (6%)

$$I \propto \left(\frac{W}{L}\right) \cdot V_{OV}^{\ 2}$$
$$\because I_{bias} = I_{in} = I_{out} \wedge V_{OV5} = 2 \cdot V_{OV1-4}$$
$$\Rightarrow \boxed{\begin{matrix} n_1 = 1 \\ n_2 = 4 \end{matrix}}$$



Question 6

- A wide-swing current mirror is shown in Fig. P6. Assume V_{th}=0.7V for all transistors, and $I_{bias}=I_{in}=I_{out}$. The V_{OV} of M_1, M_2, M_3, M_4 are 0.3V. In order to minimize the allowable output voltage,

(a) find V_{OV} of M_5. (3%)

$$let\ V_{DS2} = V_{DS4} = V_{OV}$$
$$\Rightarrow V_{bias} = 2 \cdot V_{OV} + V_t = 1.3V$$
$$\Rightarrow V_{OV5} = V_{bias} - V_t = 2V_{OV} = 0.6V$$

(b) if $(W/L)_{M1}=(W/L)_{M2}=n_1\cdot(W/L)_{M3}=n_1\cdot(W/L)_{M4}=n_2\cdot(W/L)_{M5}$, what are the values of n_1 and n_2 should be designed? (6%)

$$I \propto \left(\frac{W}{L}\right) \cdot V_{OV}^{\ 2}$$
$$\because I_{bias} = I_{in} = I_{out} \wedge V_{OV5} = 2 \cdot V_{OV1\sim4}$$
$$\Rightarrow \begin{cases} n_1 = 1 \\ n_2 = 4 \end{cases}$$