(16%) 1. With less than 25 words, please list the name of the **four feedback amplifiers** (e.g. Trans… amplifier) and their **corresponding topologies** (e.g. series-shunt). (16%)

(20%) 2. Consider a closed-loop circuit shown in Fig. P2. Assume that the input impedance of the basic amplifier is **infinite**, open-loop gain μ=6000 V/V, r_o=R_L=100 kΩ, R_1 = R_2 = 50kΩ, C_L=1pF, please **respectively** calculate the **dc gain of the loop gain**, and the **dominant pole location of the loop gain** by

(a) breaking the loop **at *XX'***. (10%)

(b) breaking the loop **at the output of the basic amplifier *Y***. (10%)

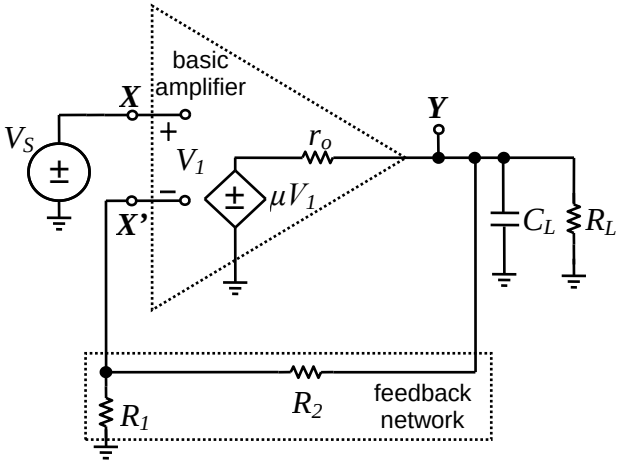

Fig. P2

(20%) 3. Please give definitions of the following terms for an op amp.

(a) -3dB bandwidth (5%) (b) unity-gain bandwidth (5%) (c) CMRR (5%) (d) PSRR (5%)

(20%) 4. Fig. P4 shows a two-stage op amp with a simple bias circuit. Assume $\mu_n C_{ox}$=200μA/V^2, $\mu_p C_{ox}$=80μA/V^2, $|V_{tp}|$=0.8V, and I_{D8}=20μA, I_{D5}=200μA, I_{D7}=500μA, and $(W/L)_{M5}$=(20μm/1μm), $(W/L)_{M7}$=(50μm/1μm), $(W/L)_{M3}$=(10μm/1μm). Without considering the channel-length modulation, please

(a) calculate **$(W/L)_{M8}$**. (5%)

(b) calculate R_b. (5%)

(c) design the **$(W/L)_{M6}$** to minimize the input systematic offset if the input stage is perfectly balanced. (5%)

(d) find the **output swing** of the op amp. (5%)

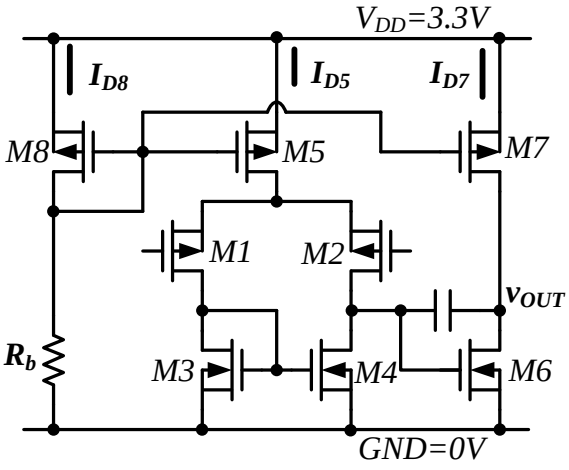

Fig. P4

(15%) 5. A folded-cascode op amp is shown in Fig. P5 where I_{M11}=200μA, I_{M10}=300μA, and $|V_{OV}|$ for all transistors is 0.2V. Assuming λ_n=0.1V^{-1}, λ_p=0.2V^{-1}, V_{DD}=3.3V, V_{tn}=0.8V, $|V_{tp}|$=0.8V, and C_L=1pF, please

(a) calculate **dc gain**. (5%)

(b) calculate **slew rate**. (5%)

(c) specify which node is the **positive** input terminal (***v*$_{IN1}$ or *v*$_{IN2}$**). Explain your answer. (5%)

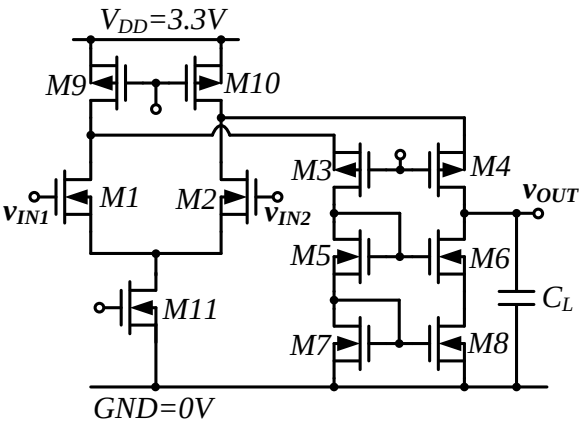

Fig. P5

(9%) 6. A wide-swing current mirror is shown in Fig. P6. Assume V_{tn}=0.7V for all transistors, and $I_{bias}=I_{in}=I_{out}$. The V_{OV} of M_1, M_2, M_3, M_4 are 0.3V. In order to minimize the allowable output voltage,

(a) find $\mathbf{V_{OV}}$ **of** $\mathbf{M_5}$. (3%)

(b) if $(W/L)_{M1}=(W/L)_{M2}=n_1\cdot(W/L)_{M3}=n_1\cdot(W/L)_{M4}=n_2\cdot(W/L)_{M5}$, what are the values of $\mathbf{n_1}$ and $\mathbf{n_2}$ should be designed? (6%)

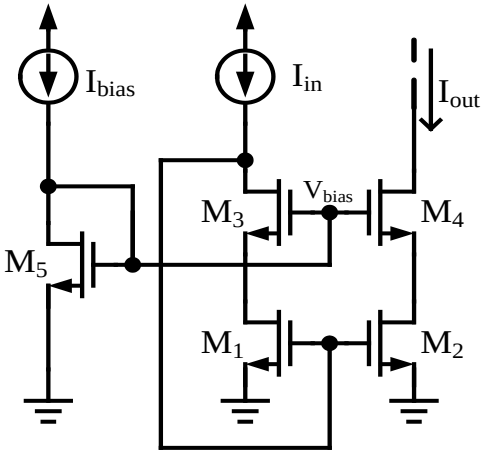

Fig. P6