# SPICE Model for MOSFETs in sedra_lib.lib (1/2)

**Table B.2** Parameters of the SPICE Level-1 MOSFET Model (Partial Listing)

| SPICE Parameter | Book Symbol | Description | Units |
|---|---|---|---|
| | | **Basic Model Parameters** | |
| LEVEL | | MOSFET model selector | |
| TOX | $t_{ox}$ | Gate-oxide thickness | m |
| COX | $C_{ox}$ | Gate-oxide capacitance, per unit area | $F/m^2$ |
| UO | $\mu$ | Carrier mobility | $cm^2/V{\cdot}s$ |
| KP | $k'$ | Process transconductance parameter | $A/V^2$ |
| LAMBDA | $\lambda$ | Channel-length modulation coefficient | $V^{-1}$ |
| | | **Threshold Voltage Parameters** | |
| VTO | $V_{t0}$ | Zero-bias threshold voltage | V |
| GAMMA | $\gamma$ | Body-effect parameter | $V^{1/2}$ |
| NSUB | $N_A$, $N_D$ | Substrate doping | $cm^{-3}$ |
| PHI | $2\phi_f$ | Surface inversion potential | V |
| | | **MOSFET Diode Parameters** | |
| JS | | Body-junction saturation-current density | $A/m^2$ |
| CJ | | Zero-bias body-junction capacitance, per unit area over the drain/source region | $F/m^2$ |
| MJ | | Grading coefficient, for area component | |
| CJSW | | Zero-bias body-junction capacitance, per unit length along F/m the sidewall (periphery) of the drain/source region | |
| MJSW | | Grading coefficient, for sidewall component | |
| PB | $V_0$ | Body-junction built-in potential | V |
| | | **MOSFET Dimension Parameters** | |
| LD | $L_{ov}$ | Lateral diffusion into the channel from the source/drain diffusion regions | m |
| WD | | Sideways diffusion into the channel from the body along the width | m |
| | | **MOS Gate-Capacitance Parameters** | |
| CGBO | | Gate-body overlap capacitance, per unit channel length | F/m |
| CGDO | $C_{ov}/W$ | Gate-drain overlap capacitance, per unit channel width | F/m |
| CGSO | $C_{ov}/W$ | Gate-source overlap capacitance, per unit channel width | F/m |

Reference: Adel S. Sedra and Kenneth C. Smith, Microelectronic Circuit 7th ed. New York, Oxford Univ. Press, 2016 app. B.1.4, ppB-7

# SPICE Model for MOSFETs in sedra_lib.lib (2/2)

| Technology | $L_{min}$ | $W_{min}$ | $(V_{DD}+\lvert V_{SS}\rvert)_{max}$ |
|---|---|---|---|
| 5-μm CMOS | 5 μm | 12.5 μm | 10 V |
| 0.5-μm CMOS | 0.5 μm | 1.25 μm | 3.3 V |
| 0.18-μm CMOS | 0.18 μm | 0.22 μm | 1.8 V |

$L_{min}$: minimum channel length
$W_{min}$: minimum channel width
$(VDD+|VSS|)_{max}$: maximum supply voltage

**Table B.3** Values of the Level-1 MOSFET Model Parameters for Two CMOS Technologies[1]

| | 5-μm CMOS Process | | 0.5-μm CMOS Process | | 0.18-μm CMOS Process | |
|---|---|---|---|---|---|---|
| | NMOS | PMOS | NMOS | PMOS | NMOS | PMOS |
| LEVEL | 1 | 1 | 1 | 1 | 1 | 1 |
| TOX | 8.50e-08 | 8.50e-08 | 9.50e-09 | 9.50e-09 | 4.08e-09 | 4.08e-09 |
| UO | 750 | 250 | ~~460~~ 680 | ~~115~~ 200 | 291 | 102 |
| LAMBDA | 0.01 | 0.03 | 0.1 | 0.2 | 0.08 | 0.11 |
| GAMMA | 1.4 | 0.65 | 0.5 | 0.45 | 0.3 | 0.3 |
| VTO | 1 | −1 | 0.7 | −0.8 | 0.5 | −0.45 |
| PHI | 0.7 | 0.65 | 0.8 | 0.75 | 0.84 | 0.8 |
| LD | 7.00e-07 | 6.00e-07 | 8.00e-08 | 9.00e-08 | 10e-9 | 10e.9 |
| JS | 1.00e-06 | 1.00e-06 | 1.00e-08 | 5.00e-09 | 8.38e-6 | 4.00e-07 |
| CJ | 4.00e-04 | 1.80e-04 | 5.70e-04 | 9.30e-04 | 1.60e-03 | 1.00e-03 |
| MJ | 0.5 | 0.5 | 0.5 | 0.5 | 0.5 | 0.45 |
| CJSW | 8.00e-10 | 6.00e-10 | 1.20e-10 | 1.70e-10 | 2.04e-10 | 2.04e-10 |
| MJSW | 0.5 | 0.5 | 0.4 | 0.35 | 0.2 | 0.29 |
| PB | 0.7 | 0.7 | 0.9 | 0.9 | 0.9 | 0.9 |
| CGBO | 2.00e-10 | 2.00e-10 | 3.80e-10 | 3.80e-10 | 3.80e-10 | 3.50e-10 |
| CGDO | 4.00e-10 | 4.00e-10 | 4.00e-10 | 3.50e-10 | 3.67e-10 | 3.43e-10 |
| CGSO | 4.00e-10 | 4.00e-10 | 4.00e-10 | 3.50e-10 | 3.67e-10 | 3.43e-10 |

[1] In PSpice, we have created MOSFET parts corresponding to the above models. Readers can find these parts in the SEDRA.olb library, which is available online at www.oup.com/us/sedrasmith. The NMOS and PMOS parts for the 0.5-μm CMOS technology are labeled NMOS0P5_BODY and PMOS0P5_BODY, respectively. The NMOS and PMOS parts for the 5-μm CMOS technology are labeled NMOS5P0_BODY and PMOS5P0_BODY, respectively. Furthermore, parts NMOS5P0 and PMOS5P0 are created to correspond to, respectively, part NMOS0P5_BODY with its body connected to net 0 and part PMOS0P5_BODY with its body connected to net $V_{DD}$.

Vacuum permittivity:

$$\varepsilon_0 = 8.854\times10^{-12}(\mathrm{F\cdot m^{-1}})$$

Oxide permittivity:

$$\varepsilon_{ox} = 3.9\varepsilon_0$$