Electronics(3) Homework1

For an OPAMP with V_{DD} = 3.3V and input common-mode voltage(V_{CM})= $\frac{V_{DD}}{2}$, the MOSFET model parameters are listed in **page B-9** of Appendix B on Smith's CD.

(1) As shown in Fig. 1, please calculate $\frac{v_o}{v_{id}}(s)$ with its DC gain and pole locations, where $v_{id}=v_{in}^{+}-v_{in}^{-}$. (refer to Sections 8.5.3 and 9.7.2 in textbook). Then verify your results by PSpice with **0.5μm CMOS model** (in sedra_lib.lib).

The sizes of all MOSFETs are listed below.

$(W/L)_{M1,M2}$ = 12μm/0.5μm
$(W/L)_{M3,M4}$ = 5μm/0.5μm
$(W/L)_{M5}$ = 2.5μm/0.5μm
$(W/L)_{M6}$ = 0.75μm/0.5μm

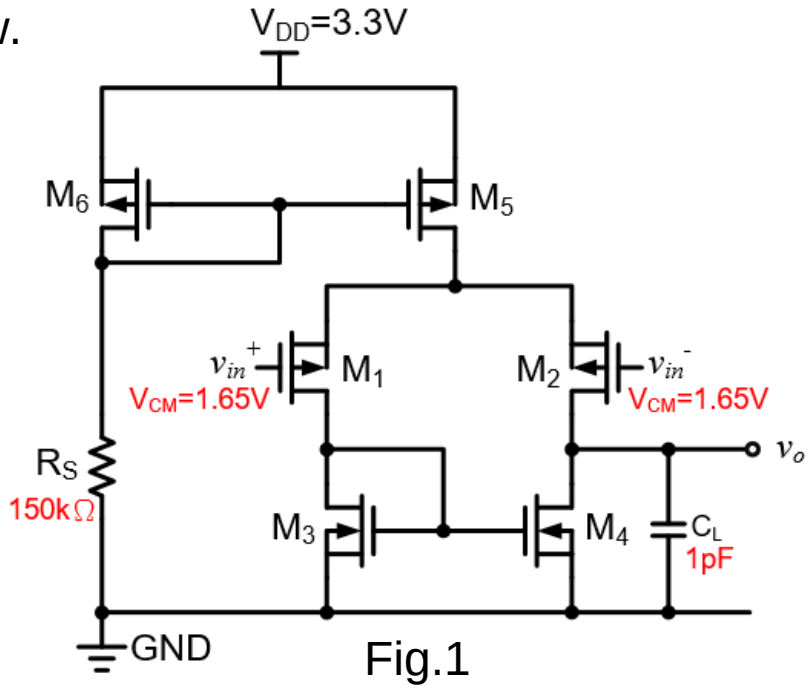


Fig.1

Electronics(3) Homework1

(2) As shown in Fig. 2, for a given resistive load R_L of 200kΩ, please calculate $\frac{v_o}{v_{id}}(s)$ with its DC gain and pole locations. Then verify your results by PSpice.

(3) In Fig. 3, assume that $R_1+R_2=R_L(200k\Omega)$ and $(R_2/R_1)=(X+1)/40$, where X is the last number of your student ID. Find the loop gain **βA(s)** with its DC gain and pole locations. Then verify your results by PSpice.

(Example: E24032114 → X = 4 → R_2/R_1 = 5/40 → R_1=175kΩ, R_2=25kΩ)

<Hint> You have to **break the feedback loop** to find βA(s) (refer to section 10.4.2)

(4) Please show the common-mode voltages of v_o in Figs. 1, 2, and 3, and explain the reasons for their difference.

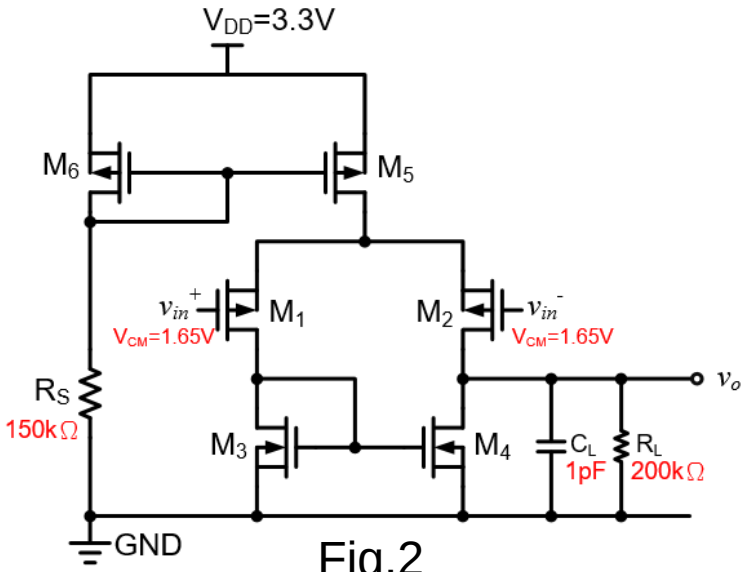


Fig.2

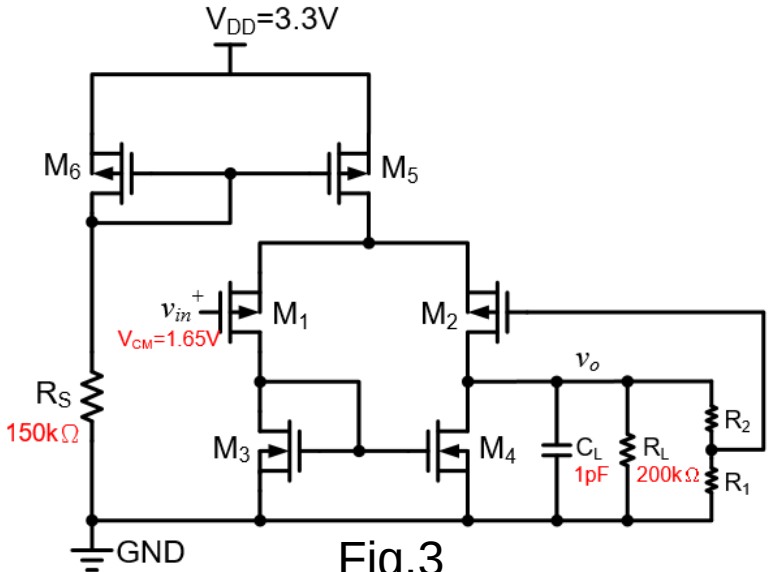


Fig.3

Notes

- When verifying your hand calculation by PSpice
  - Correct the value of LAMBDA for NMOS0P5 to 0.1 (the same as in page B-9 of Appendix B on Sedra's CD)
  - Use 4-terminal MOSFET models (NMOS0P5_BODY and PMOS0P5_BODY)
  - Clearly mark the verification results(DC gain, pole locations…) on Bode plots

- **Upload** your report **to MOODLE** in **Word** format
  - Your report should include
    - Hand calculation progress
    - PSpice schematic graphs
    - PSpice verification results (i.e Bode plots)
  - Deadline: 23:59:59 on 09/18/2023(Mon.)

    (09/22/2023(Fri.)前遲交一天原則上扣 5 分)
  - Filename example: HW1_鄭聿程_E2408XXXX_v1.doc (如有更新請用 v2,v3…)
  - 檔案應小於2MB, 若有特殊需求可向助教提出

Notes (Cont.)

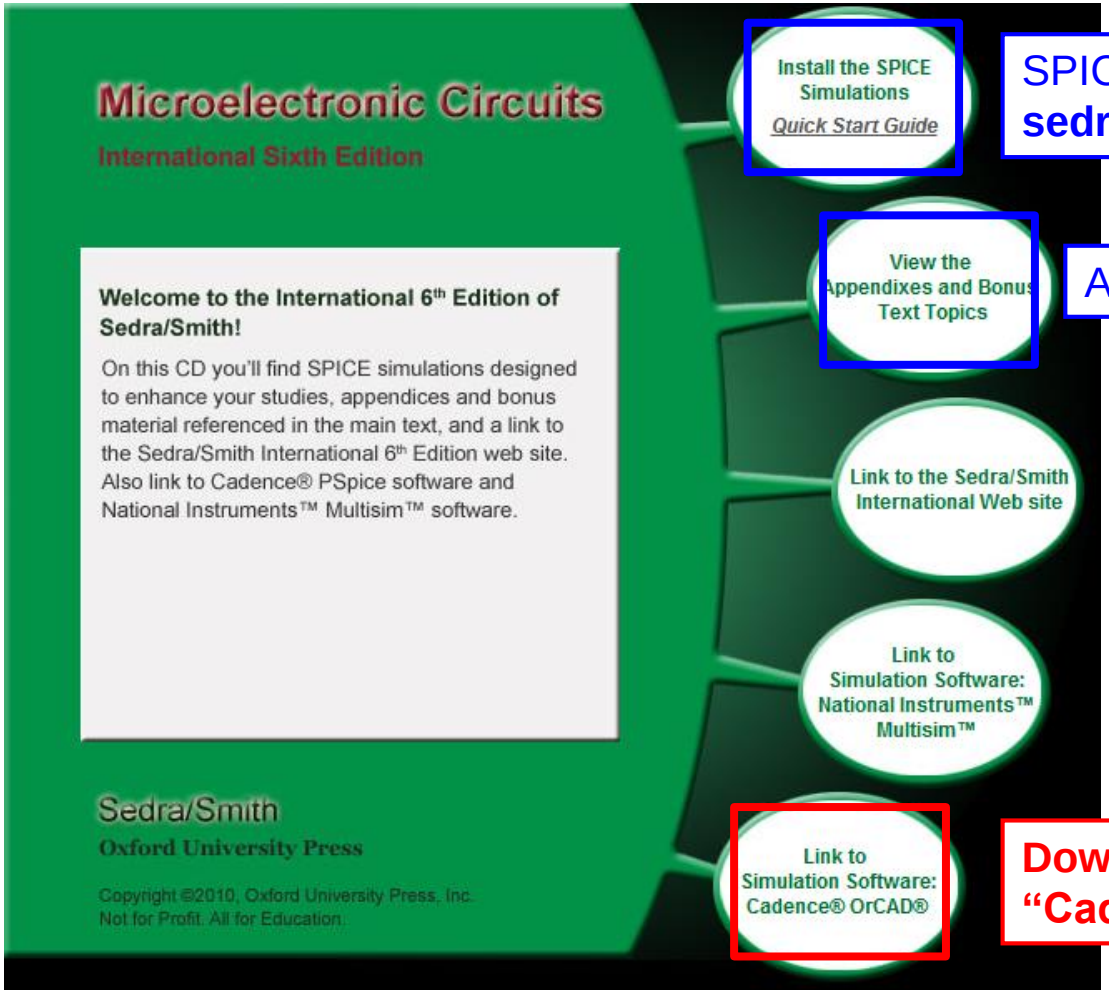
- Others
  - 作業題目下載: http://msic.ee.ncku.edu.tw/ch.html
    (IC設計課程→大學部課程→電子學(三))
  - 作業繳交: http://moodle.ncku.edu.tw/
  - 請勿抄襲，抄襲等同考試作弊，將依校規處理。
  - 此次作業將佔學期成績之5%。
  - 作業上若有遇到問題可於下列時段至奇美樓 95302室。
    - 原定office hours: 每週一17:00~18:00 and 每週五16:00~17:00
    - 新增時段: 09/07/2023(Thu.) and 09/14/2023(Thu.) 10:00~11:00
  - 手算過程若為掃描圖檔務必**清晰並轉正**以利助教判讀
  - Word format
    - 字體12pt、單行間距、中英文字體分別為標楷體與Times New Roman
    - 頁碼置中於頁尾、各邊界2.54公分 (上下邊界可依內容量縮減，但不得小於1.28公分)
    - 分別在每個繪圖下方與表格上方依序編號，並輔以caption描述
    - 圖表中的字體不小於10pt，尤其注意驗證波形圖的座標值
    - 驗證波形圖以**白色**為底，且重要驗證結果應清楚標記

PSpice Tutorial for Homeworks

- Setup Guide
- New a Project
- Create a Schematic Graph
- Circuit Analysis
  - AC Sweep Analysis
  - Transient Analysis

Setup Guide

- Launch the CD-ROM comes with “Microelectronics Circuits 7th ed.”



SPICE examples **and sedra_lib library files**

Appendixes pdf files

Start !!

Download the PSpice Software “Cadence OrCAD”

Download PSpice Software: OrCAD

Free OrCAD Lite Download

Download link on website for lite version is not available anymore

OrCAD® Lite software download is no longer available and has been replaced with new and improved dedicated OrCAD Viewer, OrCAD Trial, and OrCAD Academic versions that provide more advanced PCB design functionality for everyone.

OrCAD Academic Program

OrCAD is committed to offering everything you need to be successful in today's competitive job environment. The OrCAD Academic Program provides students, educators, and research clubs with a complete suite of design and analysis tools to learn, teach, and create electronic hardware.

Learn More

We provide a download link for 16.6 Lite

Please click here→ OrCAD PSpice Download Link

僅供學術使用，
請勿任意散播，
違者自行負責。

OrCAD Viewer

Using the Free OrCAD Viewer allows you to open a project, schematic, or library and access design data very easily. Read-only and secure access to design data makes it effortless for a design project team to review and track the progress of design files created in OrCAD Capture and PCB Editor.

Learn More

OrCAD Free Trial

Download a full featured version of OrCAD for evaluation without limits.

Learn More **Do not click this**

This only provides free trail of full version for only 7 days

Download sedra_lib Library Files without the CD

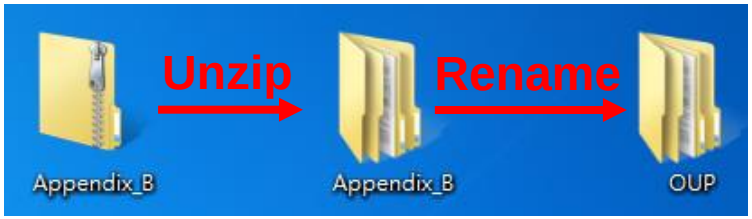
- If you don't have the CD comes with "Microelectronics Circuits 6thed."

  → Link to the website:

  http://global.oup.com/us/companion.websites/9780199339136/student/spice/

1. Click here to download SPICE examples and sedra_lib library files

2. Unzip the Appendix_B.zip file and rename the file as "OUP"

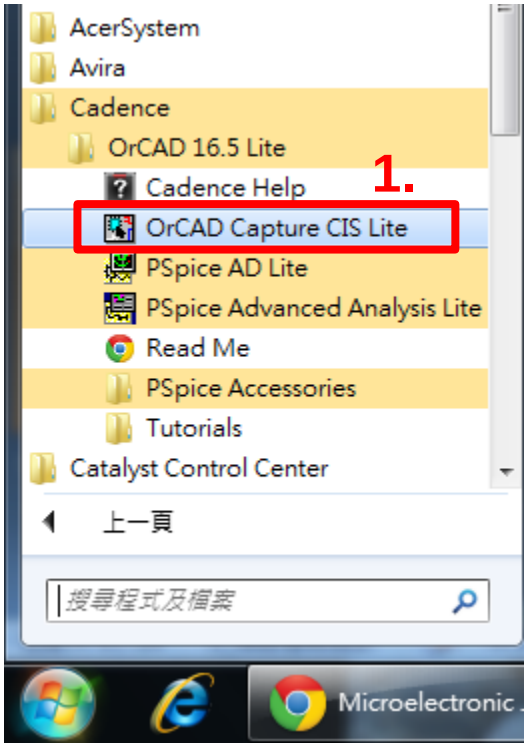


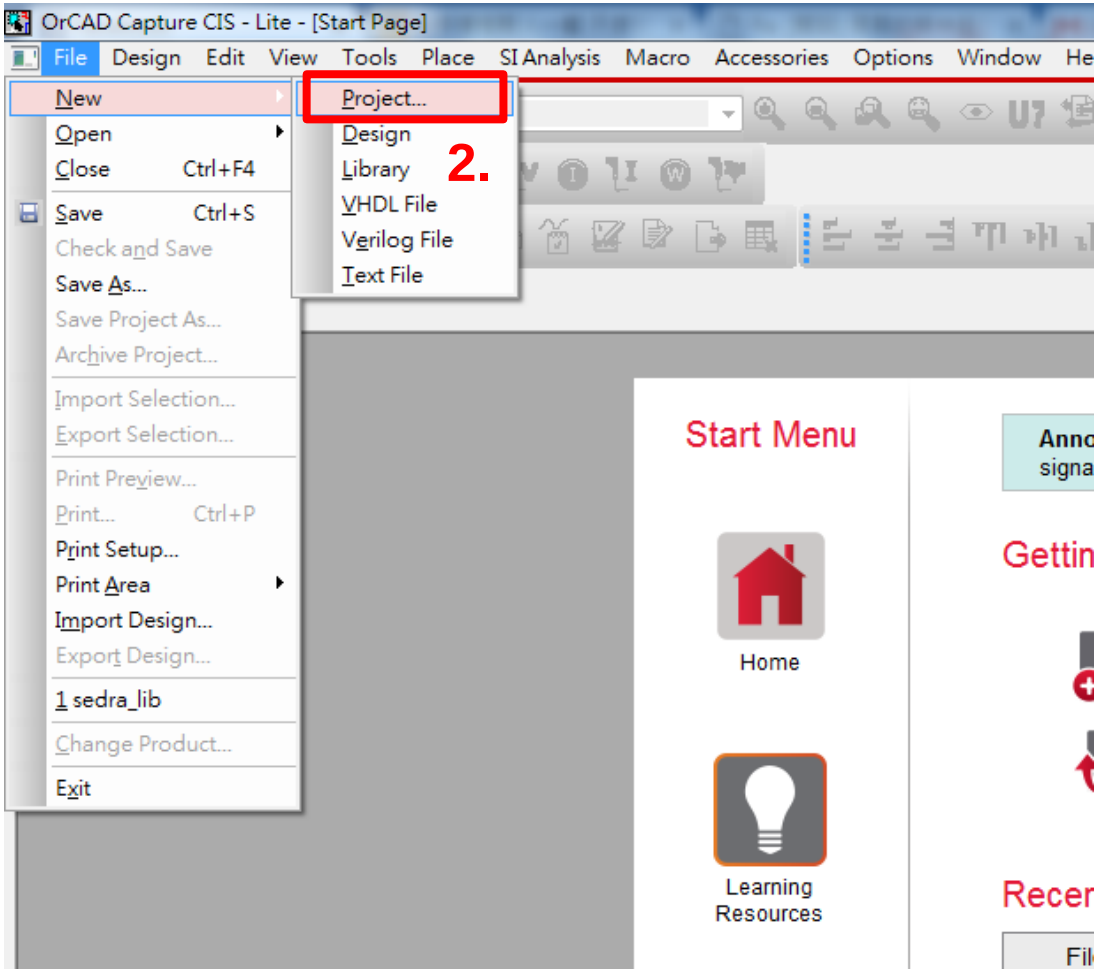
3. Place the "OUP" file @ C:\Program Files (x86)

4. Finish !!! Let's do homework1 !!

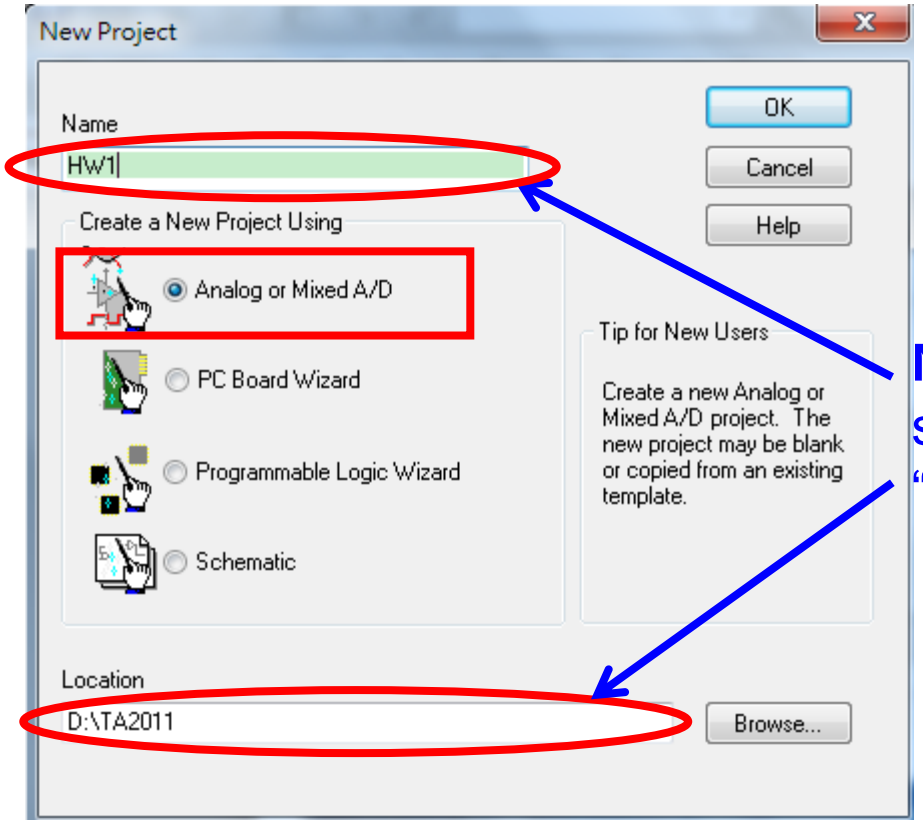
New a Project

- Start the program and New a project

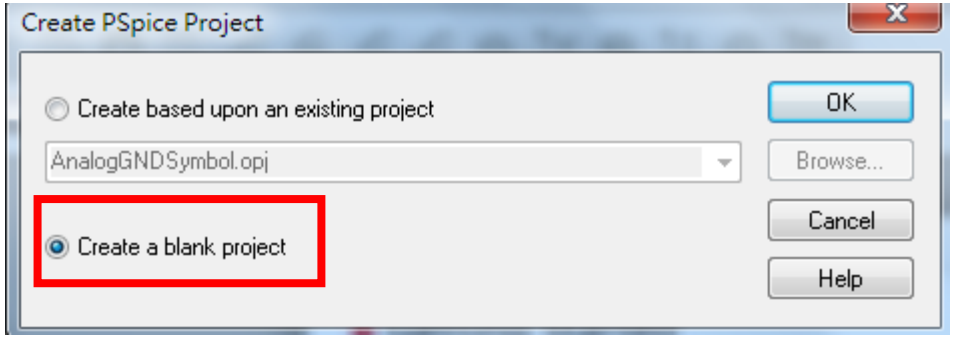




New a Project (Cont.)

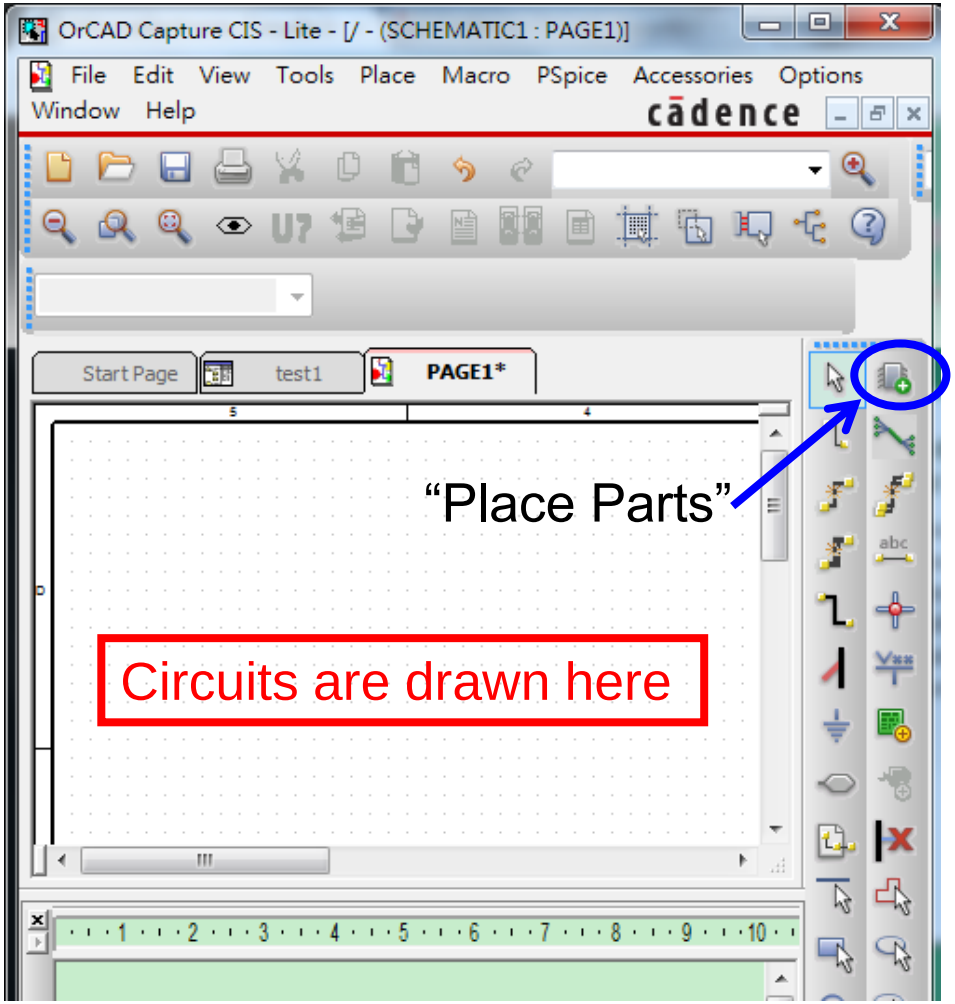


No Chinese while setting “Name” and “Location”



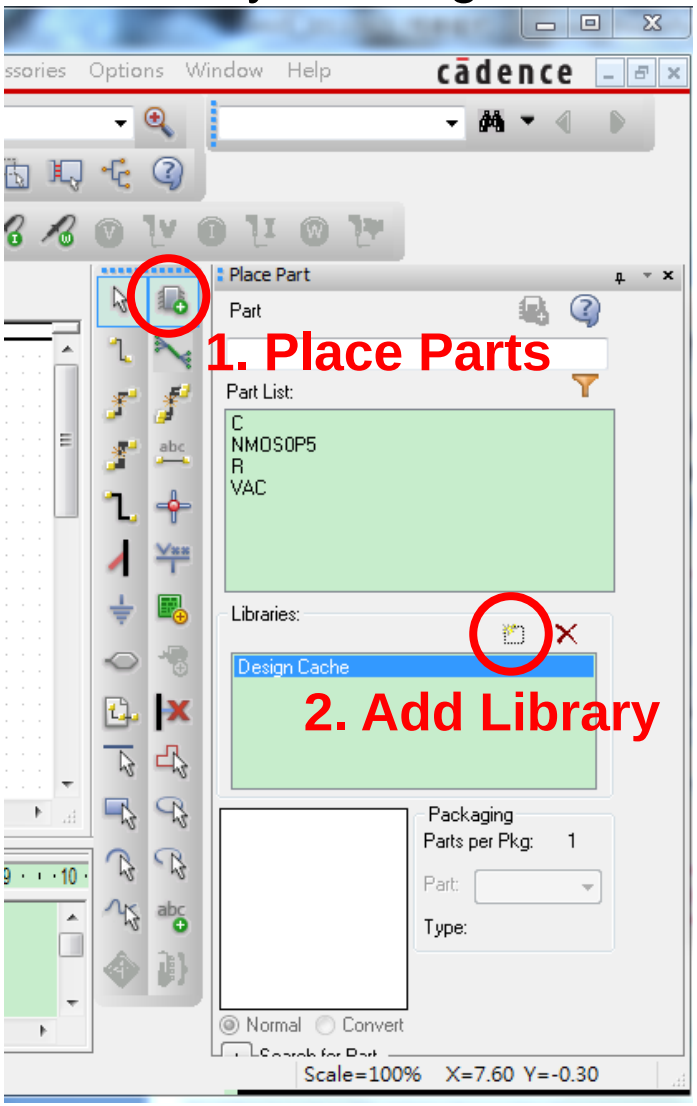
Create a Schematic Graph

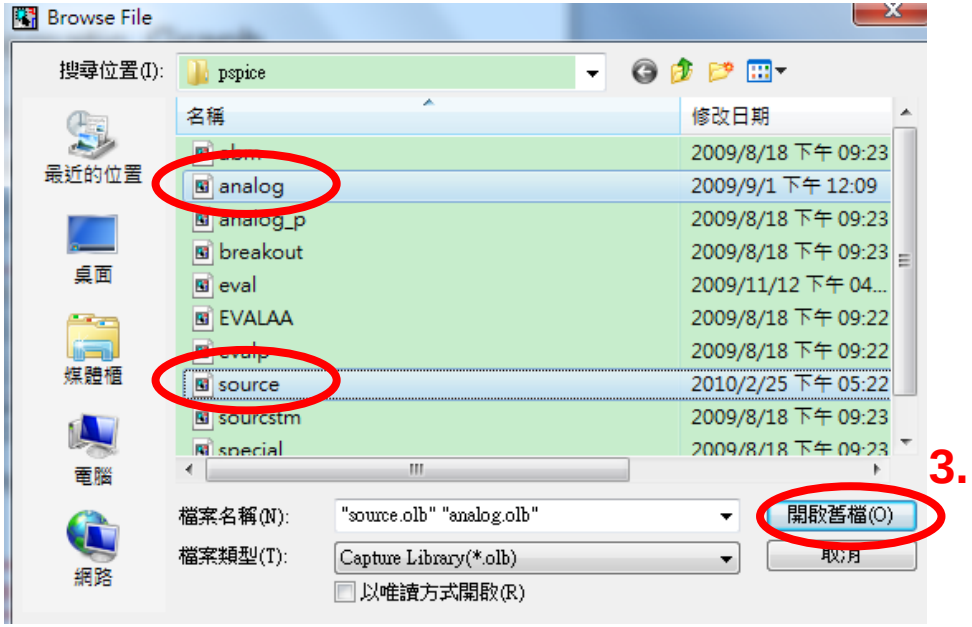
- Project and blank schematic are NEWed
  - Going to place parts on the blank schematic



Place Parts

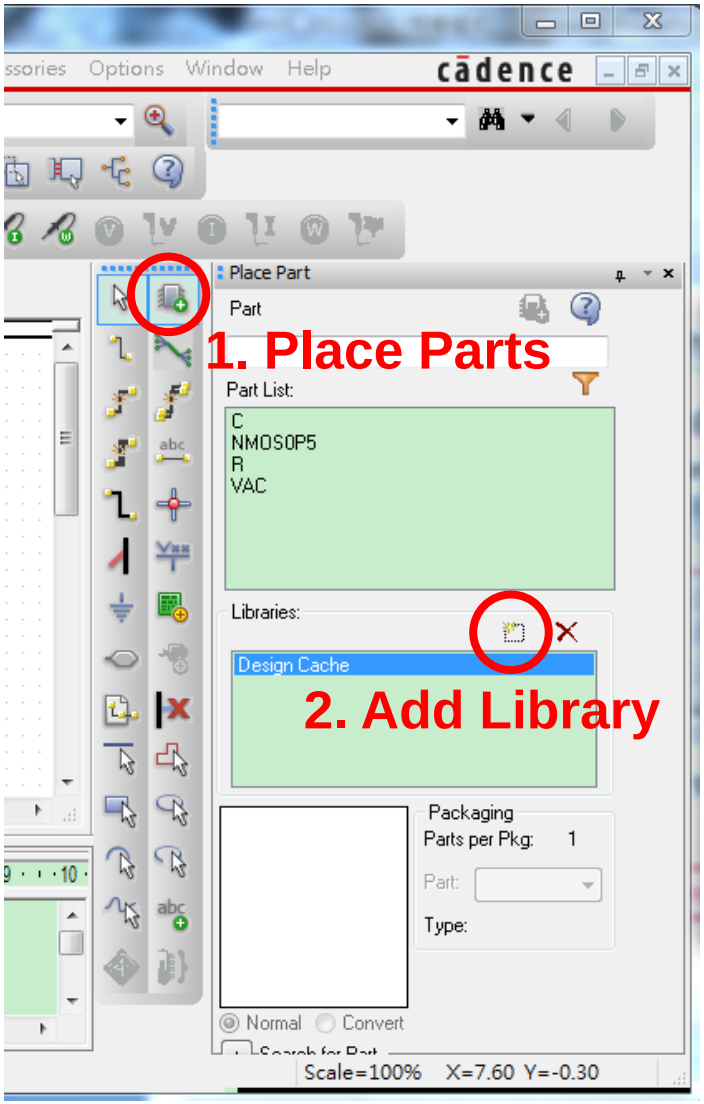
- Add library: “analog.olb” and “source.olb”@ C:\OrCAD\OrCAD_17.2_Lite\tools\capture\library\pspice



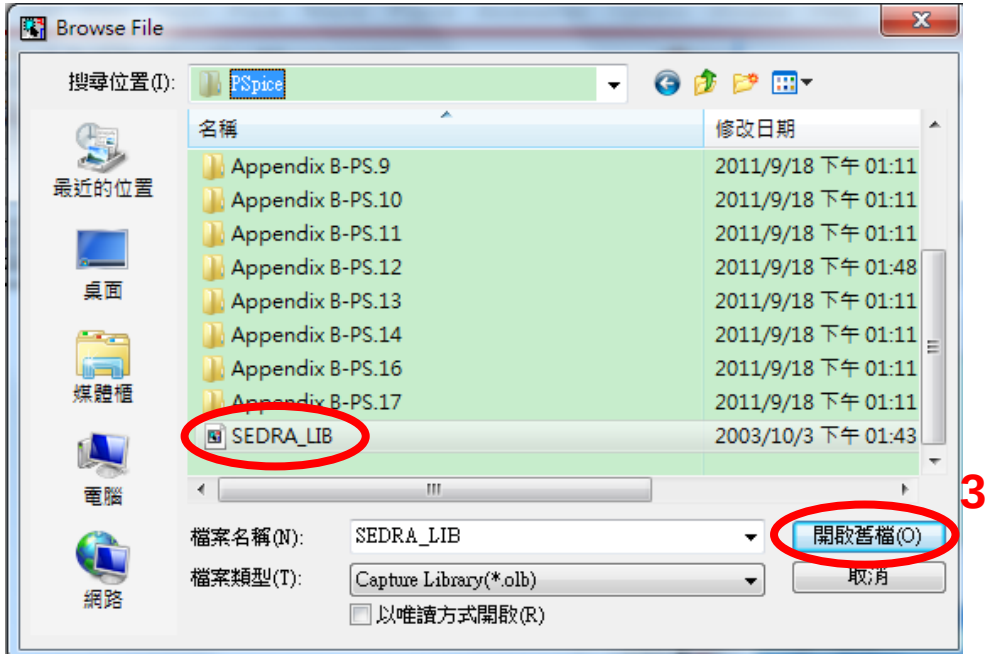


Place Parts (Cont.)

- Add library SEDRA_LIB.olb **in the "SPICE examples" file**

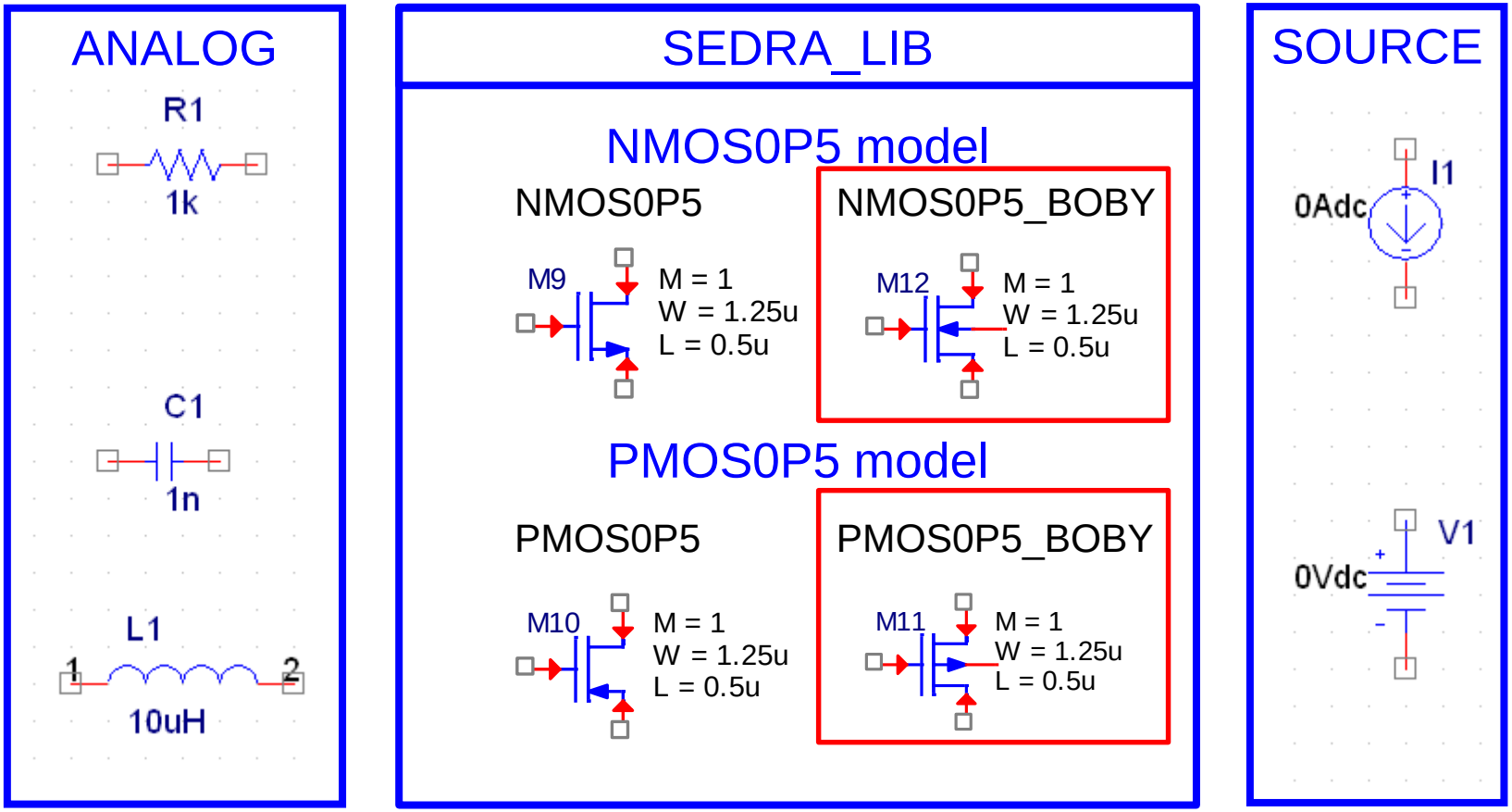


@ C:\Program Files (x86)\OUP\Sedra International 6e SPICE Simulations for Students\PSpice



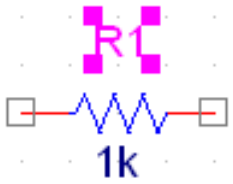
Place Parts (Cont.)

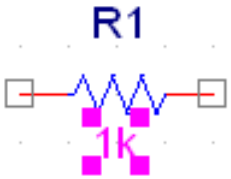
- Different parts are in different .olb files
  - Frequently used components

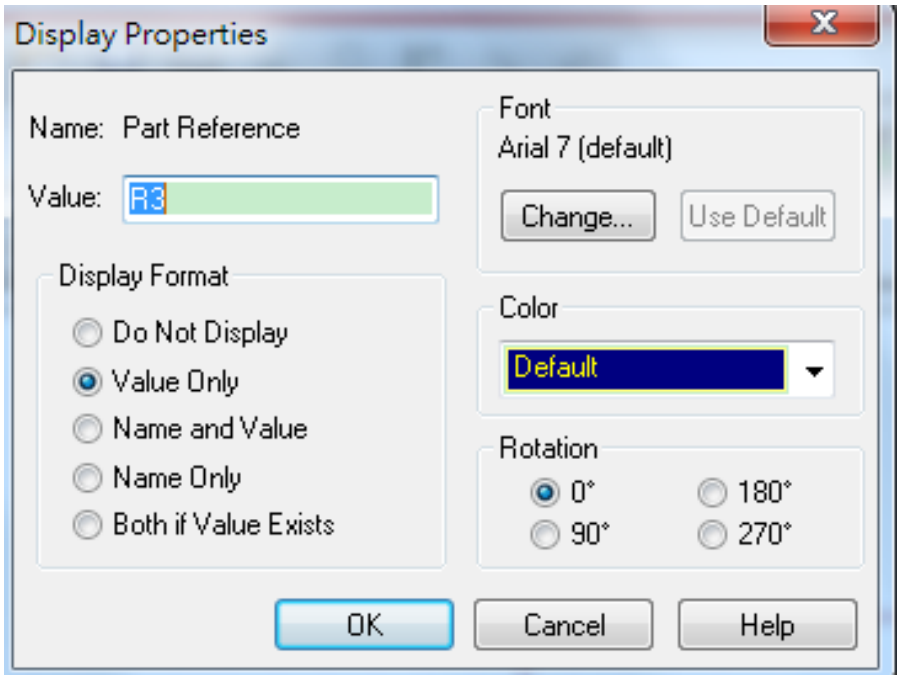


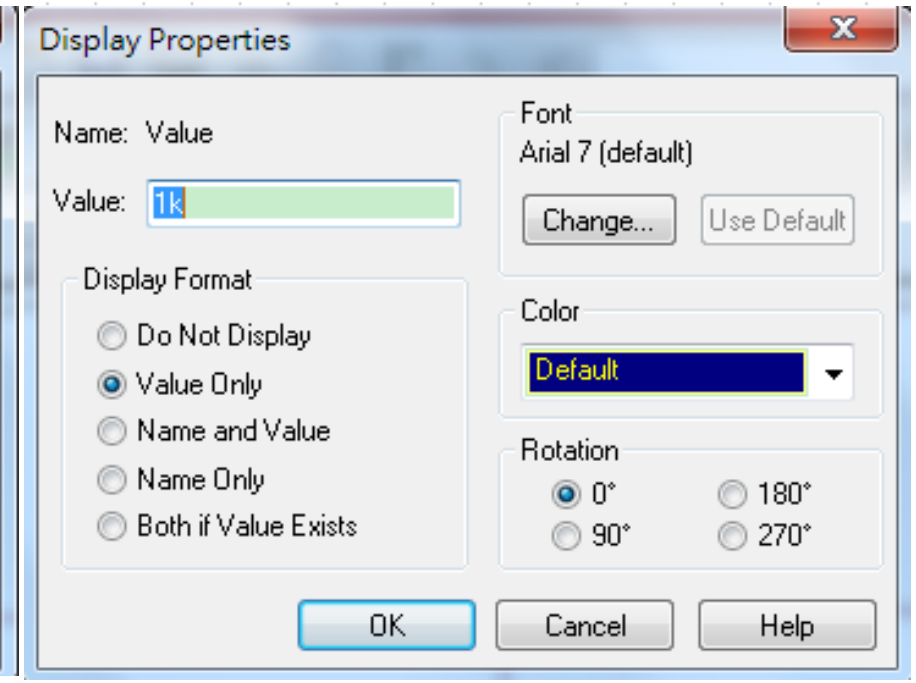
Part Properties

- Double click “R1” to edit its name
  - Same name will not be accepted while compiling (netlist generating)
- Double click “1k” to edit its resistance (capacitance for capacitor)



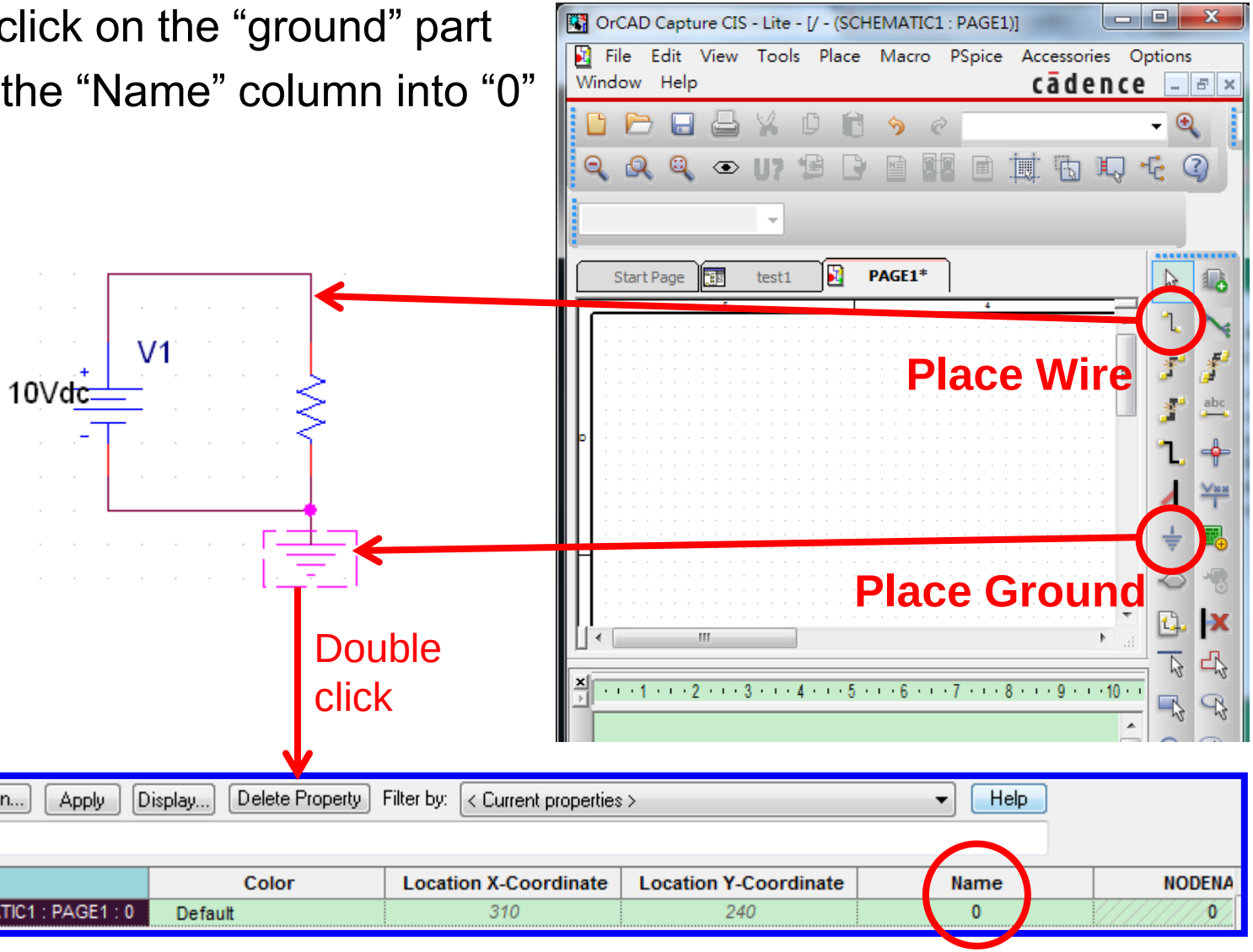






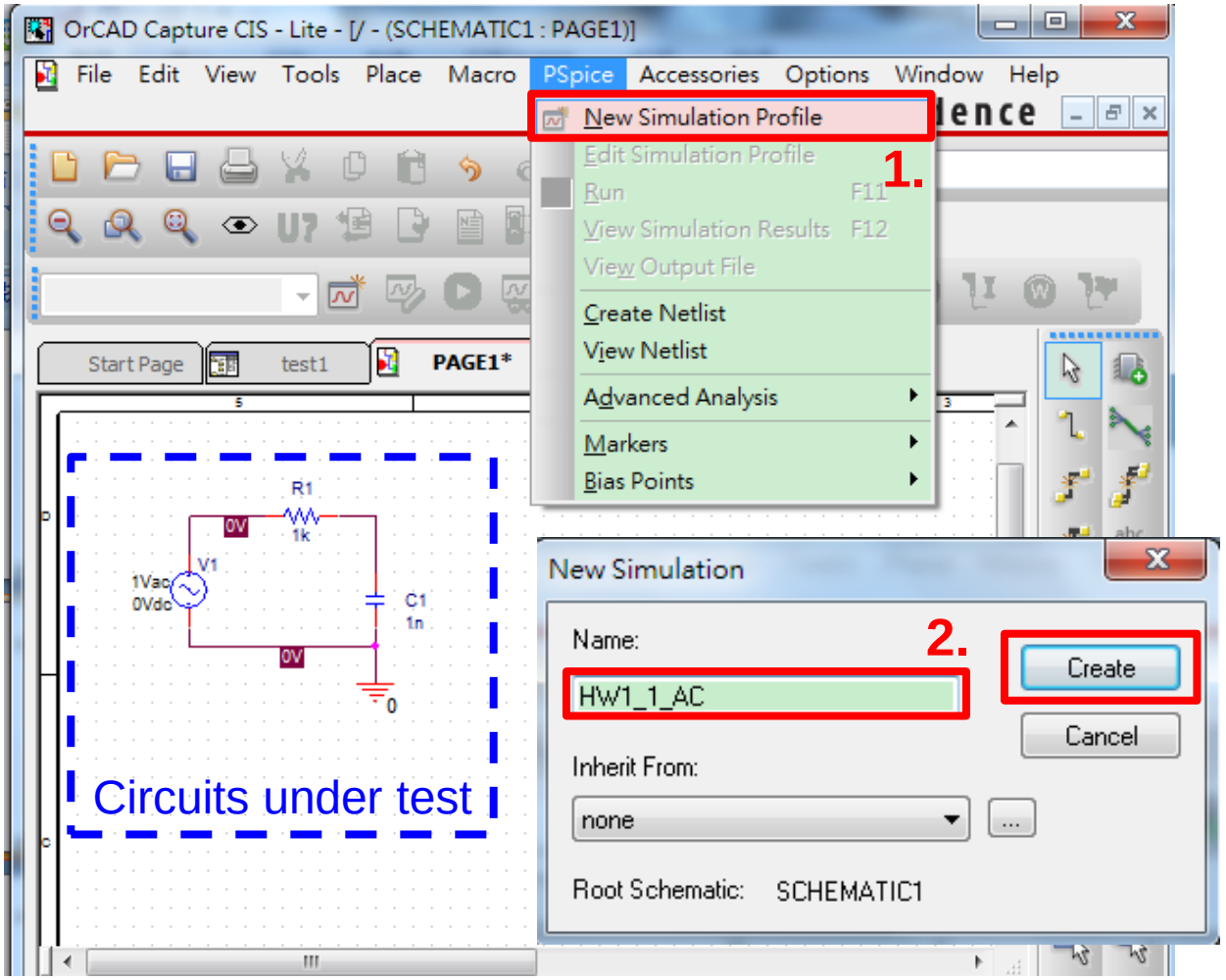
Wiring and Ground Setting

- Double click on the “ground” part
  - Edit the “Name” column into “0”

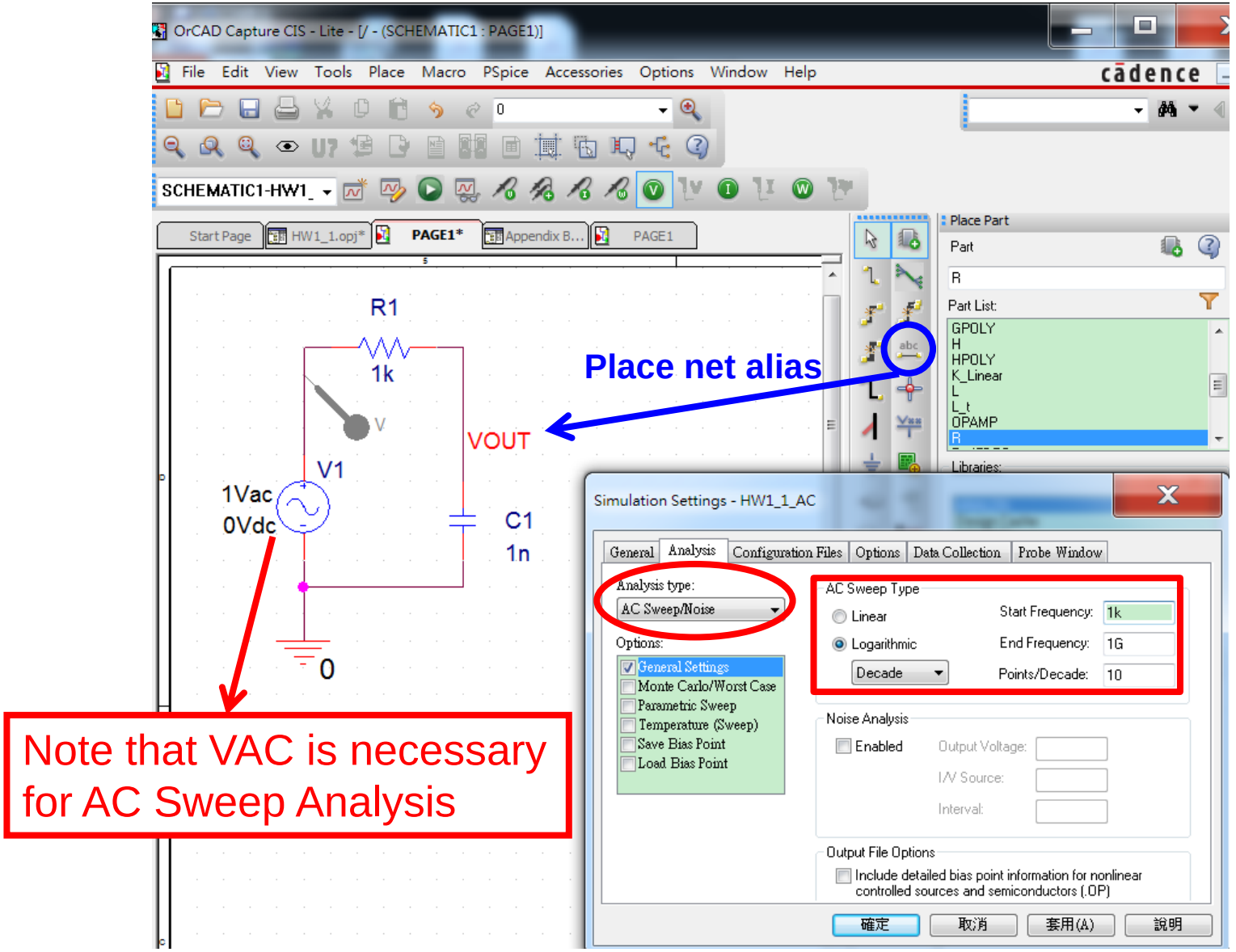


New Simulation Profile

- Settings before simulation



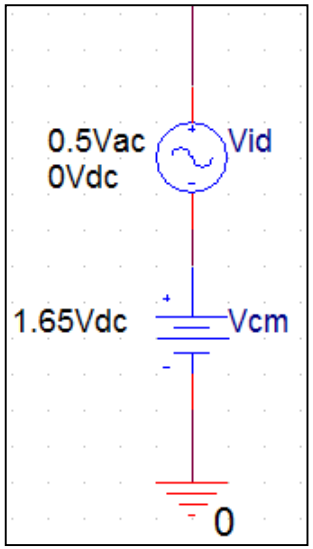
AC Sweep Analysis



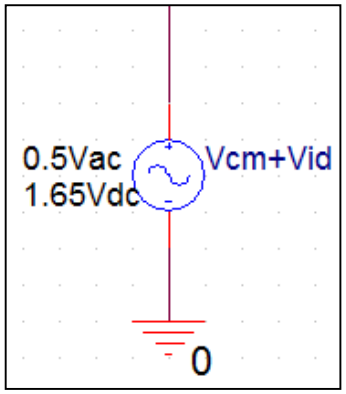
AC Sweep Analysis (Cont.)

- Three methods to place AC source V_{id} with common-mode voltage V_{cm}

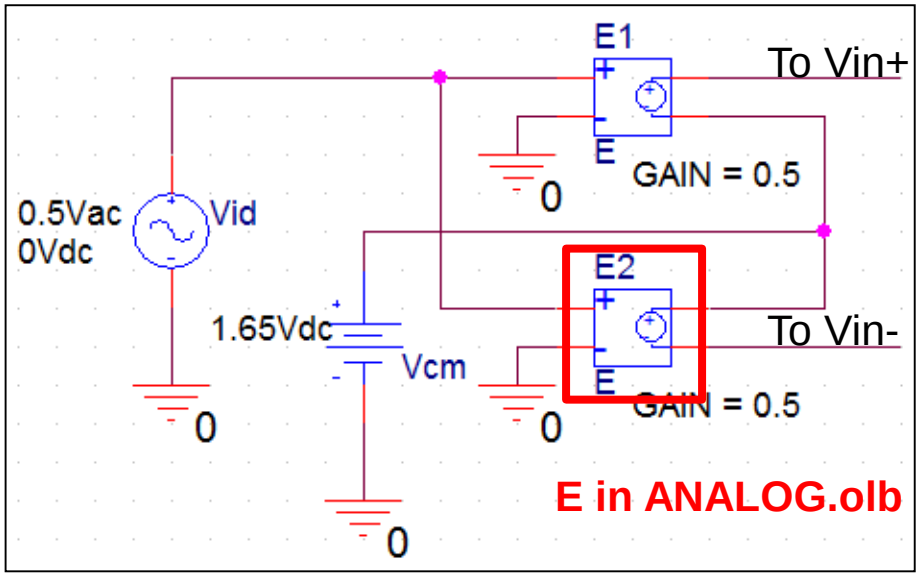
(1)



(2)



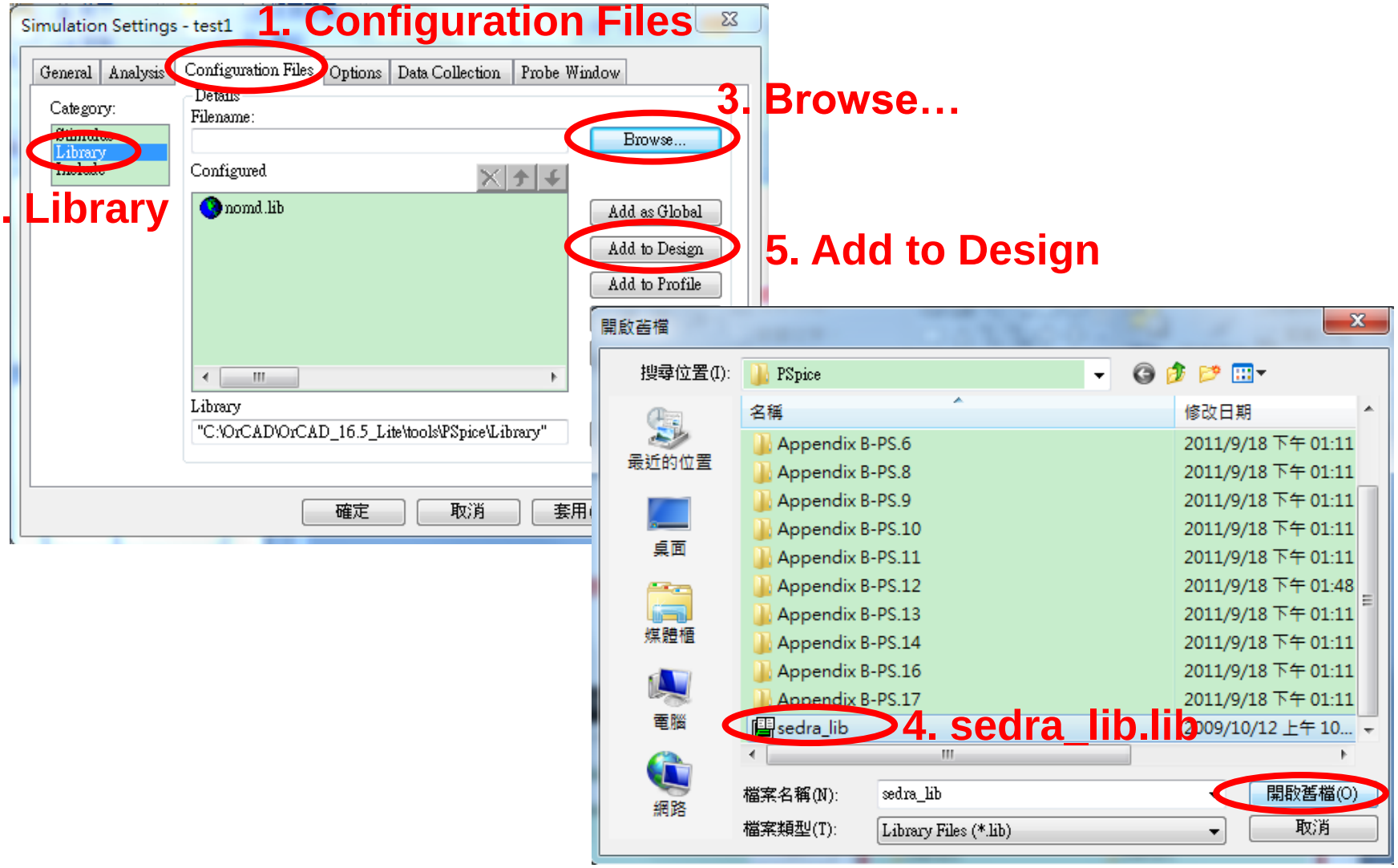
(3)



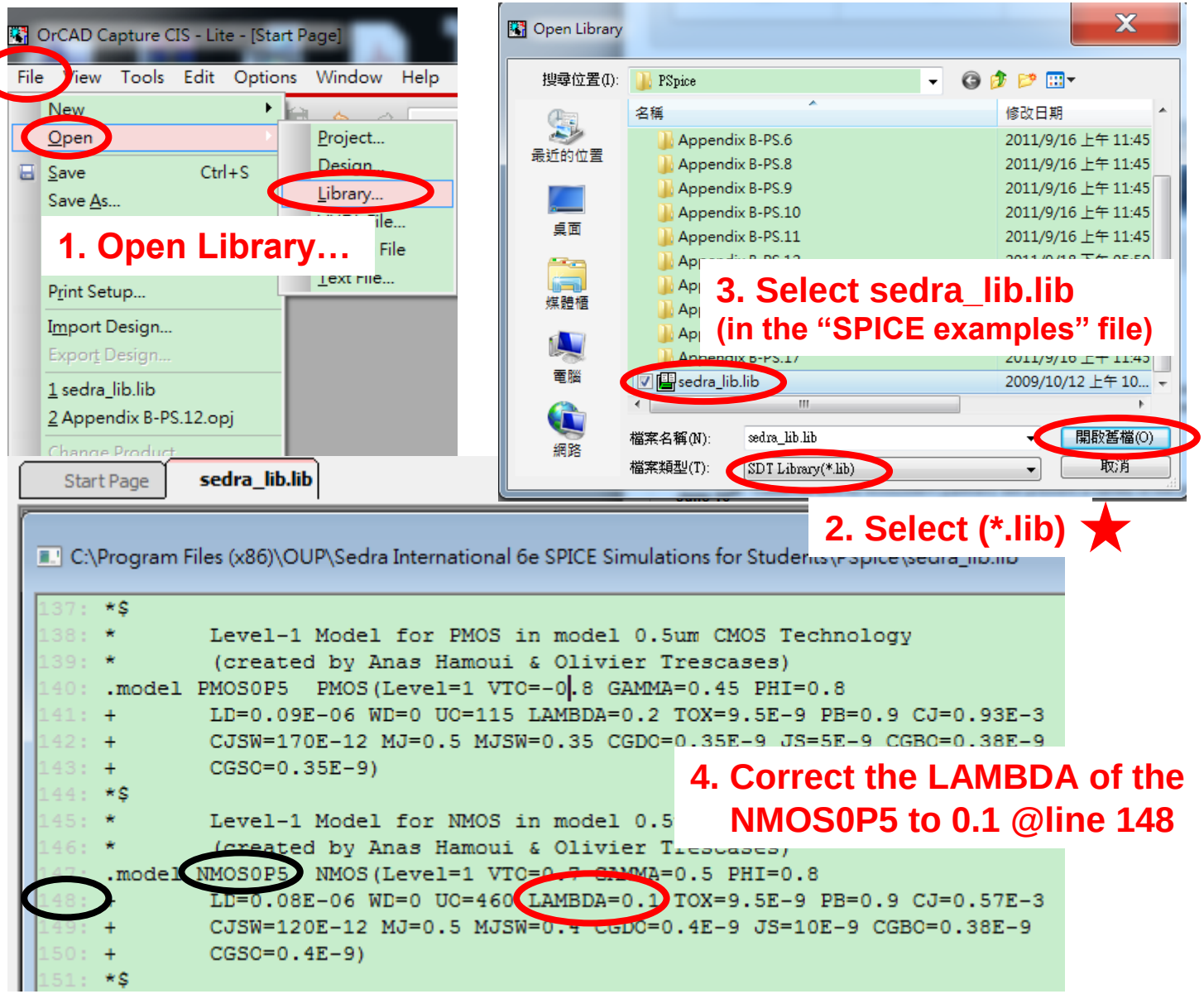
Reference: Adel S. Sedra and Kenneth C. Smith, *Microelectronic Circuits, 6*th ed. New York, Oxford Univ. Press, 2011, app. B-16

Include Sedra_lib Library

- **Add the sedra_lib.lib to design (in the "SPICE examples" file)**

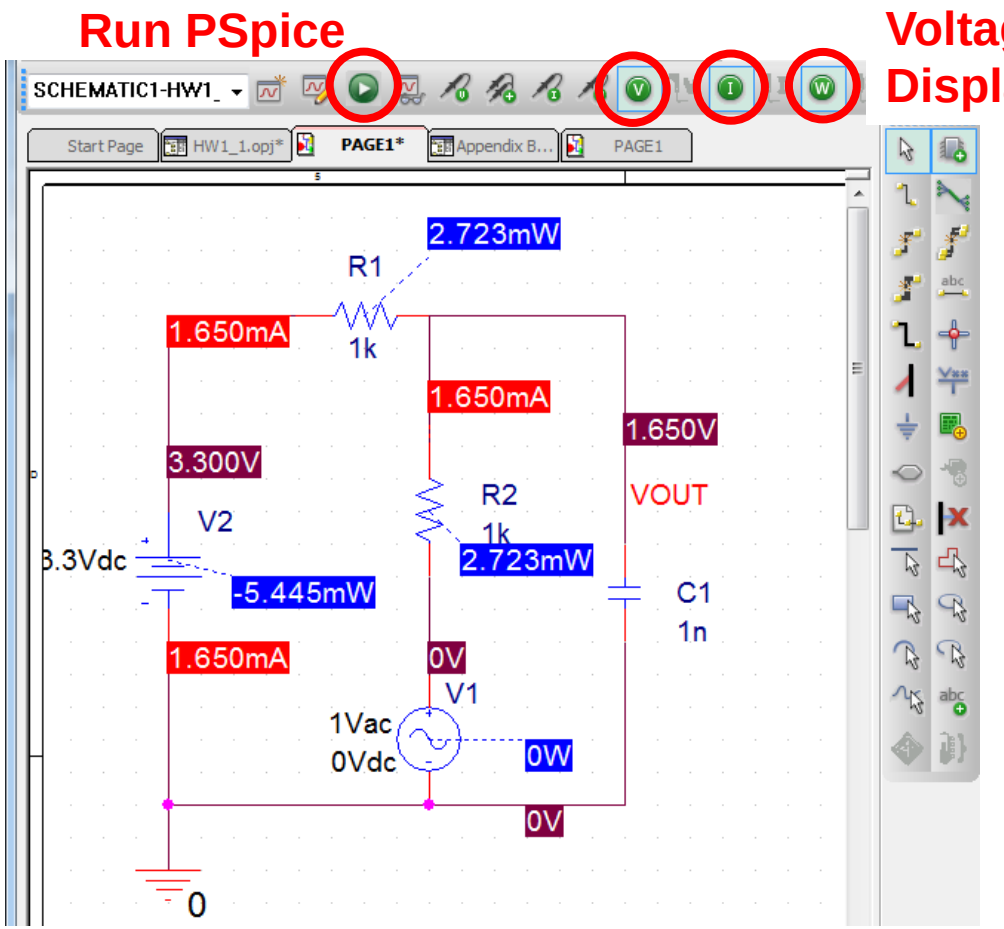


Correct the LAMBDA of the NMOS0P5 to 0.1



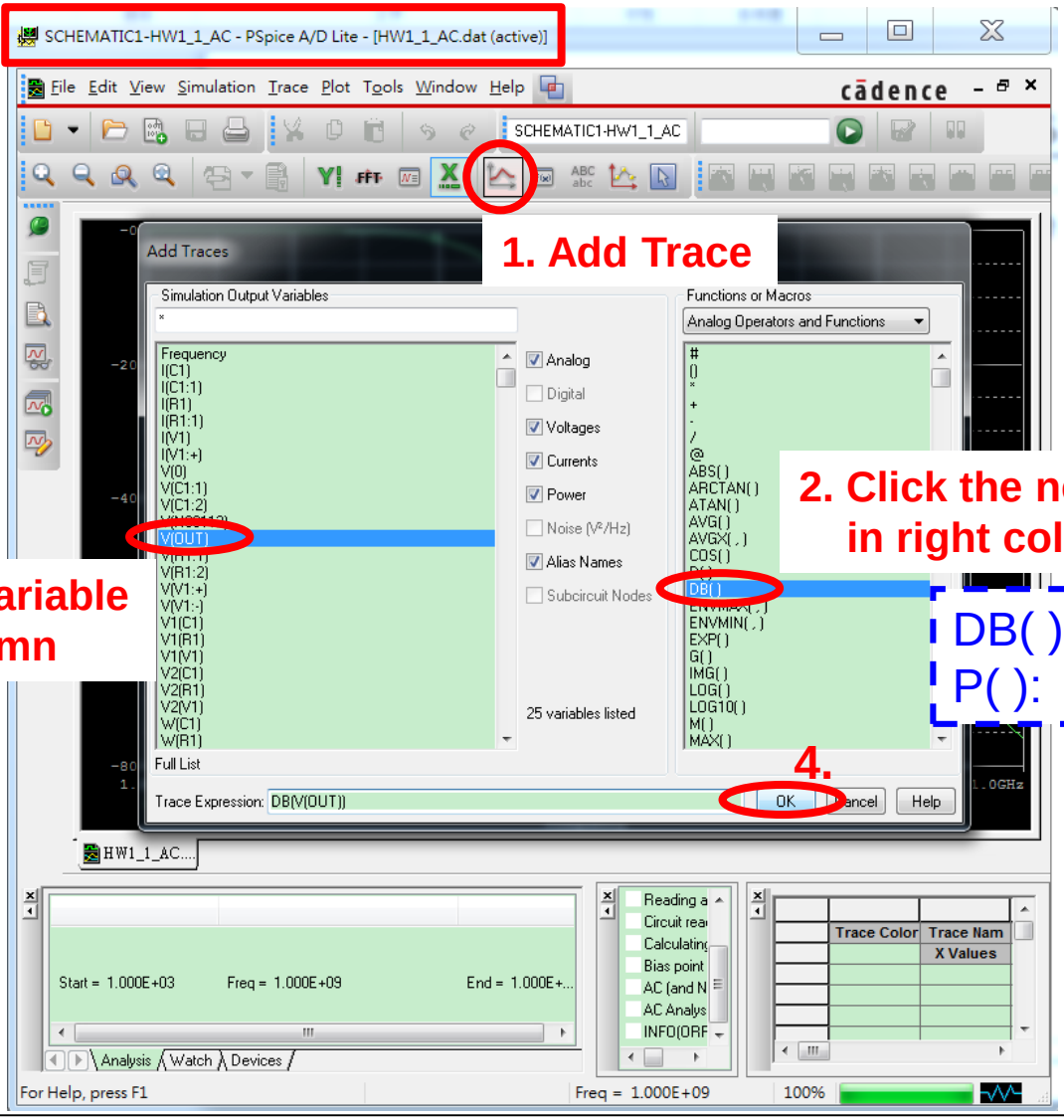
Run PSpice

- After editing the Simulation Profile
  - Run PSpice
  - Enable Bias Voltage/Current/Power Display



AC Sweep Analysis (Cont.)

- After “Run PSpice” → Add traces in “PSpice A/D Lite”

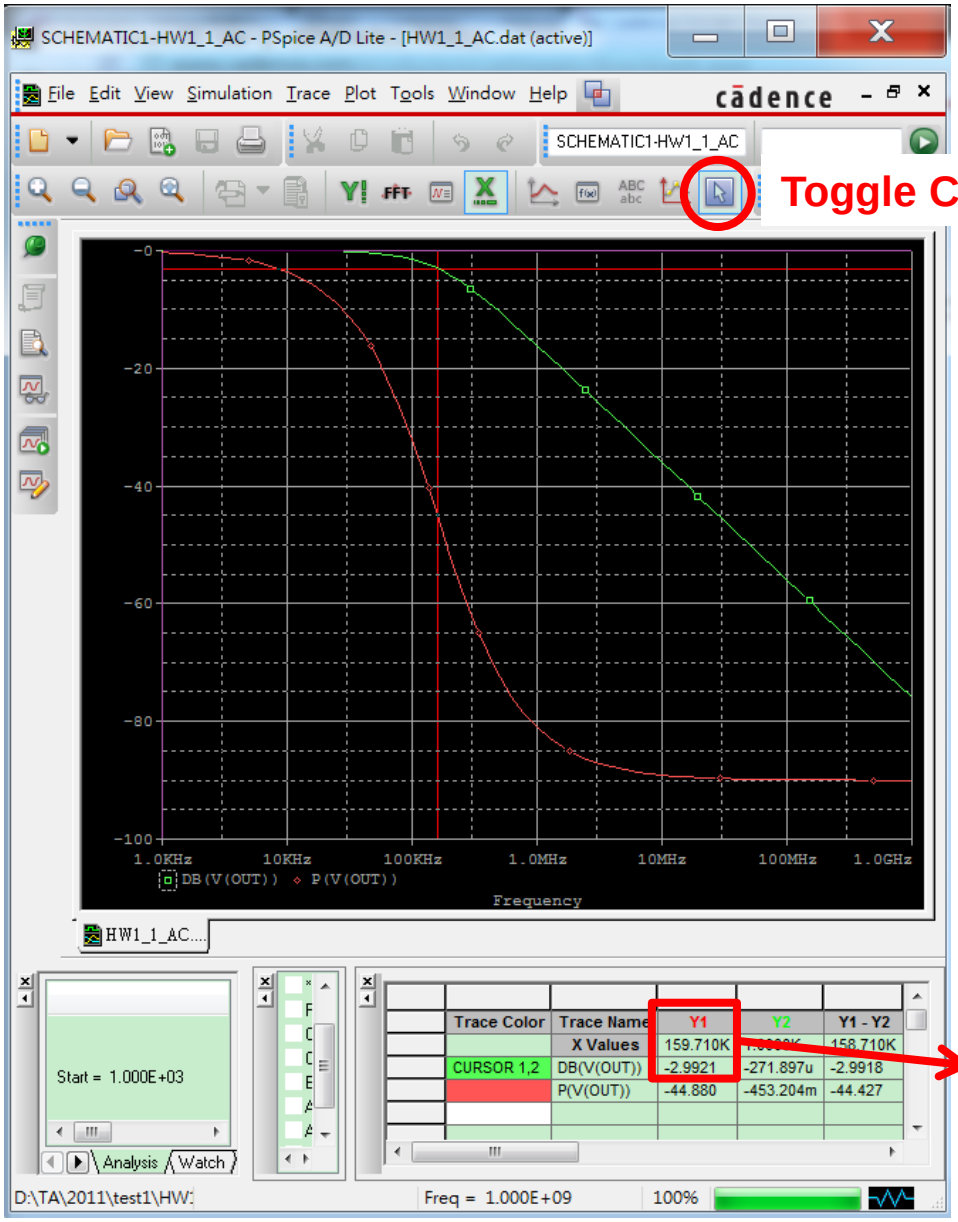


2. Click the needed function in right column

3. Click the variable in left column

DB( ): Magnitude [dB]
P( ): Phase [degree]

AC Sweep Analysis (Cont.)



Verification result:
-3dB freq. ≈ 159kHz

Transient Analysis