JOINT INSTITUTE
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ECE2700J SU24 RC5

FSM Optimization

Wenyue Li
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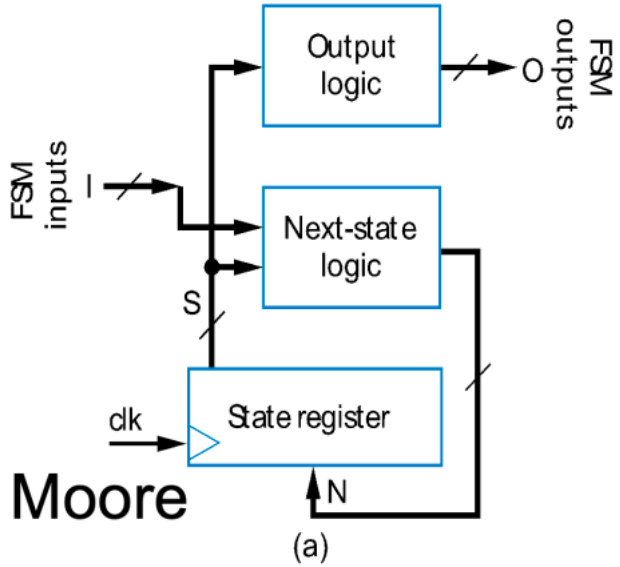
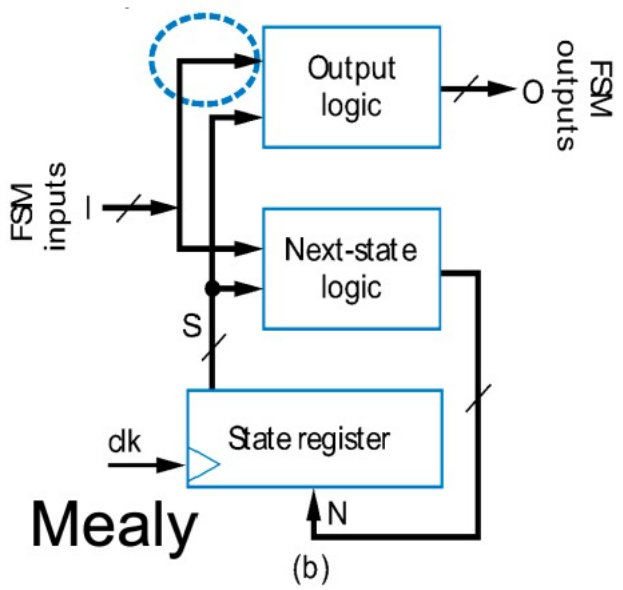
Moore vs. Mealy FSMs

– Output logic

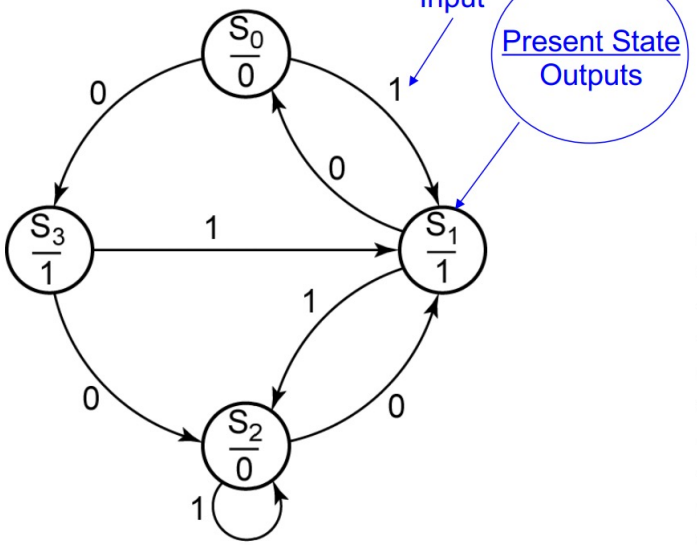
- Depends on present state only – Moore FSM
- Depends on present state and FSM inputs – Mealy FSM



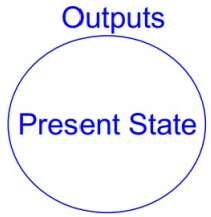


Moore vs Mealy FSMs

State Diagram



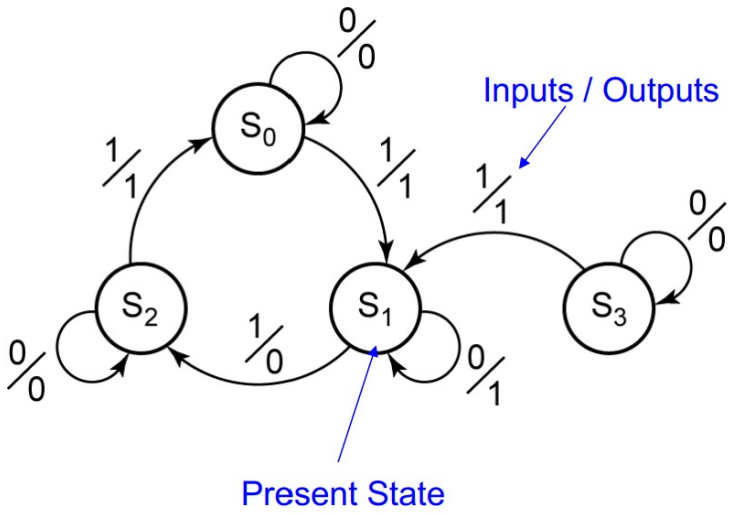
Or



State Table

In	P.S.	N.S.	Out
0	S0	S3	0
1	S0	S1	
0	S1	S0	1
1	S1	S2	
0	S2	S1	0
1	S2	S2	
0	S3	S2	1
1	S3	S1	

State Diagram



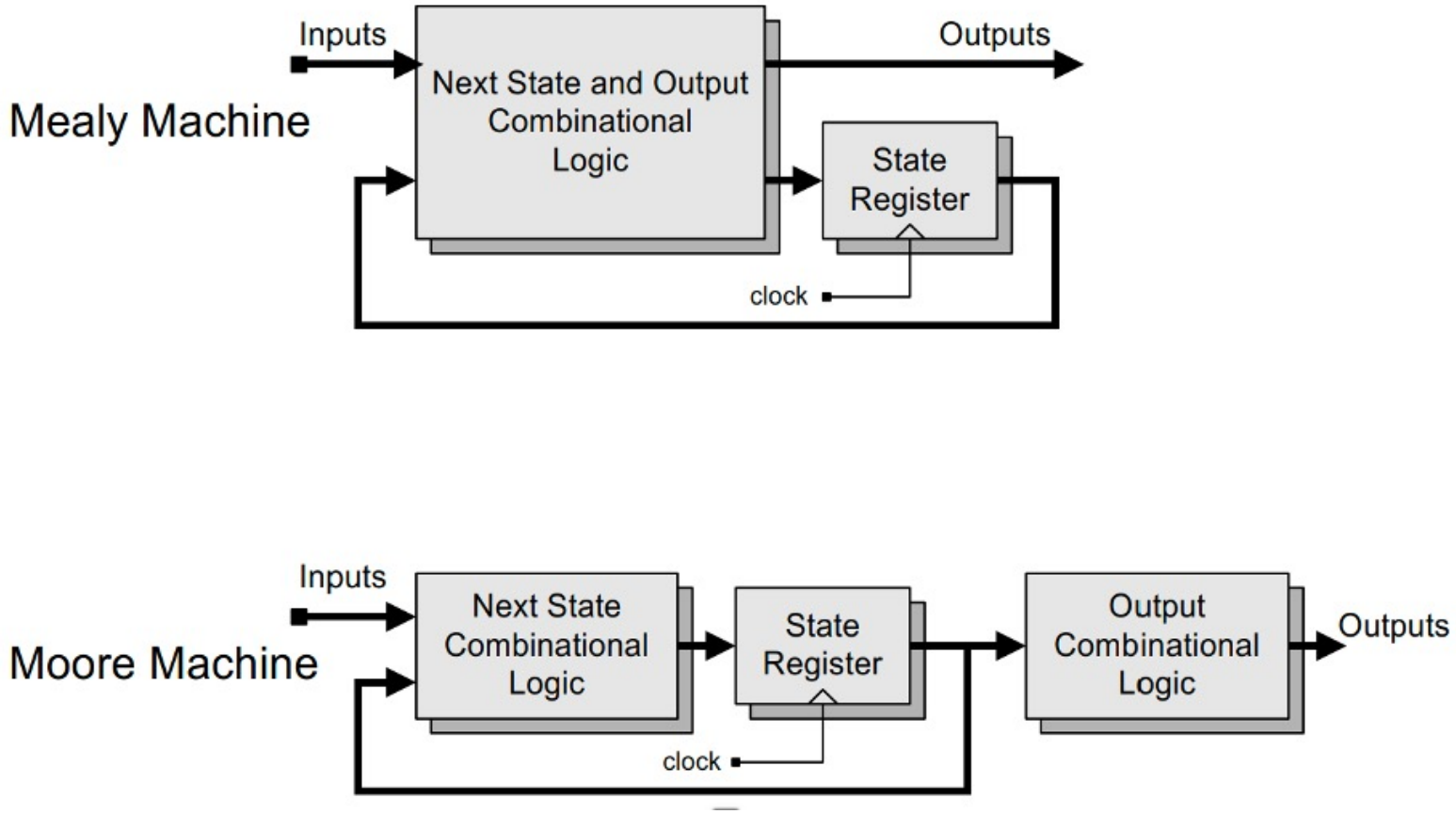
State Table

In	P.S.	N.S.	Out
0	S0	S0	0
1	S0	S1	1
0	S1	S1	1
1	S1	S2	0
0	S2	S2	0
1	S2	S0	1
0	S3	S3	0
1	S3	S1	1

Moore vs Mealy FSMs

- Output
  - Mealy: depends on both inputs and presents
  - Moore: doesn't depend on inputs
- State Diagram
  - Mealy: less states -> potentially less number of flip-flops
  - Moore: more states than Mealy -> possibly bigger circuit
- Speed of output response to the inputs
  - Mealy: quick, as soon as input changes
  - Moore: as long as one clock cycle delay
- TIMING ISSUE
  - Mealy: asynchronous, may cause serious problem
  - Moore: synchronous, more stable

Standard architecture of FSMs

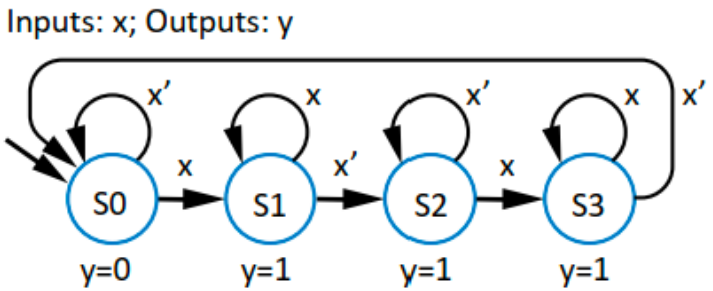


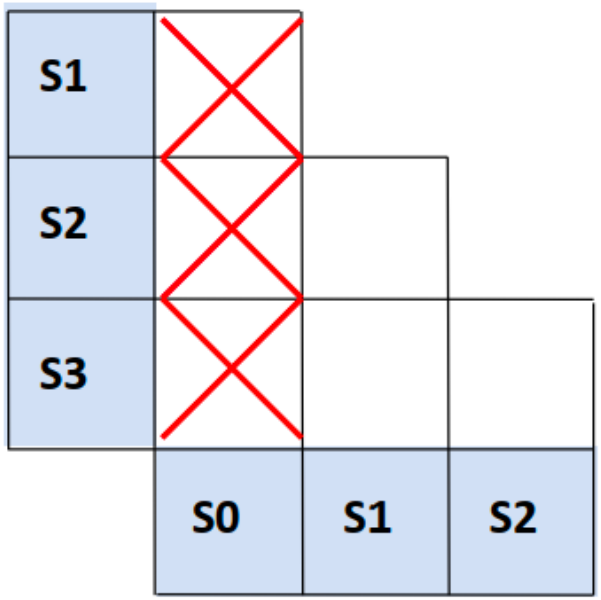
FSM Optimization

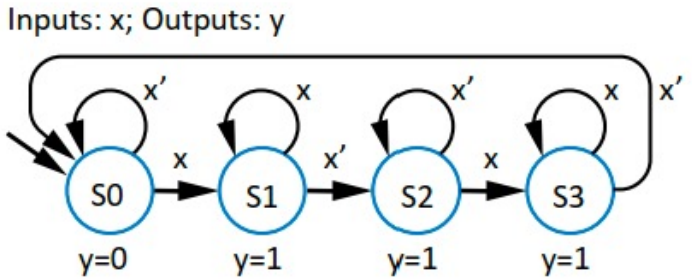
State reduction with Implication tables

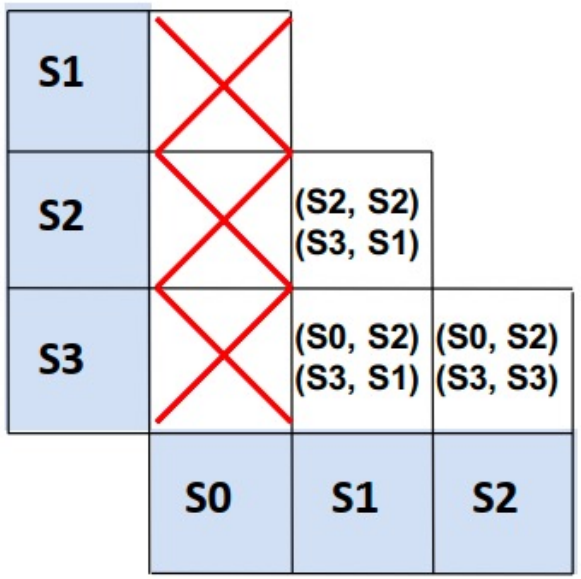
	Step	Description
1	*Mark state pairs having different outputs as nonequivalent*	States having different outputs obviously cannot be equivalent.
2	*For each unmarked state pair, write the next state pairs for the same input values*	
3	*For each unmarked state pair, mark state pairs having nonequivalent next-state pairs as nonequivalent. Repeat this step until no change occurs, or until all states are marked.*	States with nonequivalent next states for the same input values can't be equivalent. Each time through this step is called a ***pass***.
4	*Merge remaining state pairs*	Remaining state pairs must be equivalent.

FSM Optimization

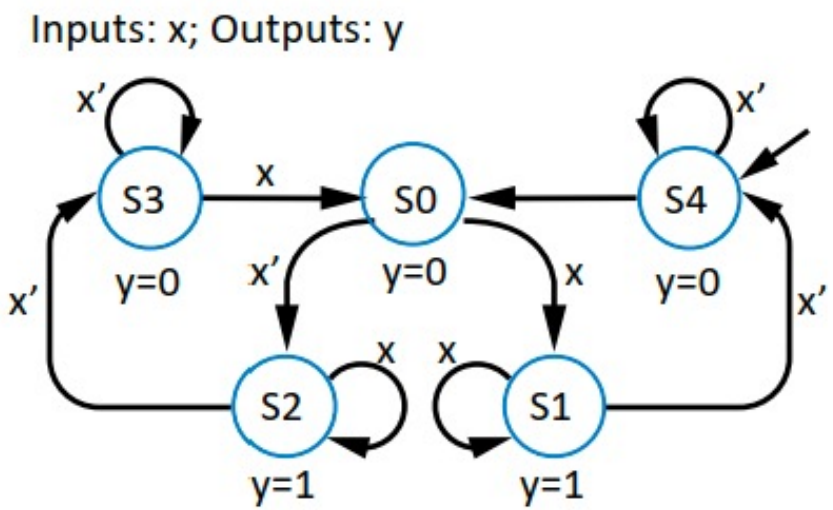








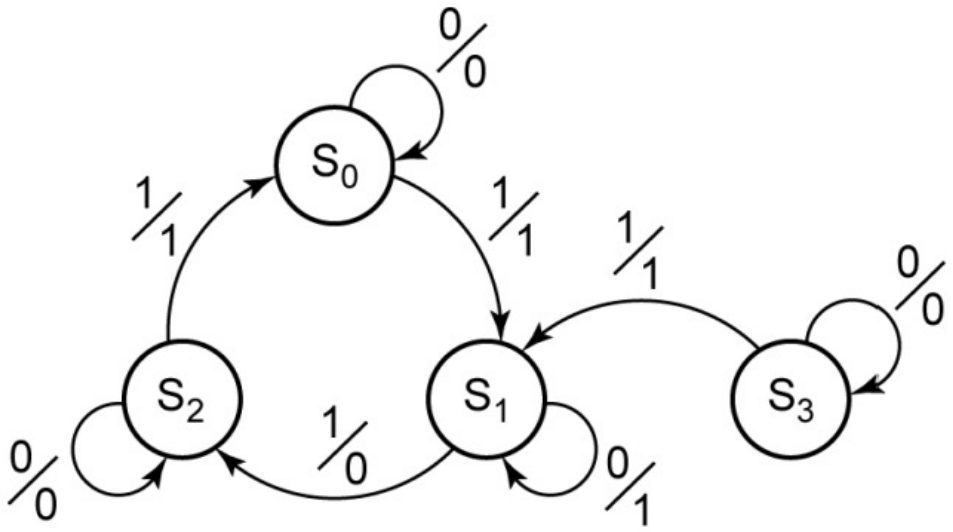
FSM Optimization



Exercise: Use the implication tables to optimize the example in the slide by yourself step by step.

FSM Optimization of Mealy FSM

- Example:



- Should have both next state pairs and output pairs in a cell for comparison