

# PRITAM PEGU

Chemical Engineering, [NIT Arunachal Pradesh](#)  
Interest: Digital System Design and Verification

Near Cenral Bank of India  
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## Education

National Institute of Technology Sikkim, Ravangla, India.  
**Bachelor of Technology**, Electronics and Communication Engineering. *2015 - 2019*  
CGPA: 7.54/10

Govt. Sr. Sec. School Rhenock, Sikkim, India.  
**High School**, CBSE *2014 - 2015*  
Percentage: 78.4 %

## Current Position

ASIC Verification Trainee Engineer, [PerfectVIPs Techno Solutions Pvt. Ltd.](#)  
*Bhubaneshwar, India. Jul '19 - Present*

## Experience

Summer Intern, [Indian Institute of Technology Bombay](#)  
*Mentor : Prof. Virendra Singh* *May '18 - Jul '18*

- Worked on hardware implementation of [AES](#) algorithm.
- Technologies/Tools: Verilog HDL and Xilinx Vivado Software.

Summer Trainee, [Motilal Nehru National Institute of Technology Allahabad](#)  
*Topics Covered: VLSI Design and Embedded System* *Jun '17 - Jul '17*

- Covered basics concepts of VLSI Design and Embedded System.
- Technologies/Tools: Verilog HDL, AT89C51, Xilinx ISE Design Suite and mikroC Pro.

## Technical Skills

**Programming Languages** C, Verilog HDL, System Verilog HVL, Assembly (x86), Core Java, Python,  $\text{\LaTeX}$ .  
**Software Tools:** Synopsys VCS, Xilinx ISE, Vivado, HFSS 13.0, MATLAB, PyCharm, IntelliJ IDEA.  
**EDA | FPGA Tools:** Cadence Virtuoso | Basys-3.  
**Platforms:** Comfortable with Windows and Linux System.

## Projects

Some Studies on Multi-Band Frequency Selective Surfaces:  
*BTech Major Project | Supervisor: Dr. Ayan Chatterjee* *Aug '18 - May '19*

- Designed different types of filter using HFSS 13.0 Software and analysing their performance and other parameters.

Single Pipelined 128 bit AES Algorithm:  
*Topic : Cryptography | Mentor : Prof. Virendra Singh* *May '18 - Jul '18*

- Implemented a efficient [Single Pipelined 128 bit AES](#) Encryption algorithm using Verilog HDL.

Digital Clock:  
*Topic: Embedded System* *Jun '17 - Jul '17*

- Designed a Digital Clock using Embedded C, AT89C51 micro Controller board and displayed the DATE, TIME and NAMES of days on 16X2 LCD Screen of the development board.

## Position of Responsibility

Student Coordinator Training and Placement Cell, NIT Sikkim.  
Technical Coordinator, UDGAM | Cultural fest of NIT Sikkim.  
Technical Coordinator, ABHIYANTRAN | Technical fest of NIT Sikkim.

## Hobbies

Singing, Travelling, Playing Chess, Cricket and Football.