PerfectVIPs

ANIL SHARMA

PROFESSIONAL SUMMARY

- **9 Months** of working experience as an "**ASIC Verification Engineer"** at **PerfectVIPs**.
- Good grip in **OOPs, Randomization** and **Functional Coverage** of **System Verilog.**
- Proficient in **debugging**.
- Hands-on expertise of working on **Test bench development** in **UVM** environment.
- Worked on **AHB back to back multi master multi slave VIP** verification.
- Currently Working on UFS 2.0 VIP Development.
- Good knowledge in **Verilog, System Verilog,UVM and Python.**

PROFESSIONAL EXPERIENCE

- **Presently** working as **ASIC Verification Engineer** in **PerfectVIPs Techno Solutions Pvt. Ltd**.

Company: PerfectVIPs **ASIC Verification Engineer** **July 2019-till date**

PROJECT DETAILS

Project: UFS VIP Development (UVM) **February 2020 – Till Date**

Description: This project involves studying of **UFS 2.0 protocol specification**, understanding the **UFS architecture** and **Development of UFS VIP** from Scratch.

Roles & Responsibilities:

- Developed **Test Bench Architecture.**
- Written the Skeleton code for Test Bench Architecture.
- Developing the **Test Plan.**

Languages: System Verilog
Methodology: UVM
Tools: QuestaSim

Project: AHB back to back VIP verification (UVM) **January 2020 - February 2020**

Description: This project involves studying of **AHB protocol specification**, understanding the **AHB VIP** and **Verification of AHB back to back Multi Master Multi Slave VIP** from Scratch.

Roles & Responsibilities:

- Developed the **Test Plan**.
- Developed **Test Bench architecture.**
- Written **configuration class for SLAVE part to generate multiple slave agent** and status of each agent as **ACTIVE** or **PASSIVE**.
- Written **SLAVE Driver logic** which involves **writing and reading** of **HDATA** and giving response(**HRESP**) back to respective **bus MASTER**.
- Written the arbitration logic for the interconnect to select the particular master agent through **HBUSREQ** and **HGRANTx** signals of AHB.
- Debugged the complete VIP to synchronized the Master and Slave.
- Run Various test cases and achieved 80% coverage.

Languages: System Verilog
Methodology: UVM
Tools: VCS

Project: Single Clock Synchronous RAM verification (UVM) **November 2019**

Description: This project involves **design & verification** of **single clock synchronous RAM**.

Roles & Responsibilities:

- Developed the **test plan**.
- Developed **test bench architecture.**
- Developed **UVM environment** for the same and **run different test cases**.

Languages: System Verilog
Methodology: UVM
Tools: VCS

Project: Full Adder Design and Verification (System Verilog) **October 2019**

Description: This project involves **design & verification** of 4-bit **Full Adder using System Verilog**.

Roles & Responsibilities:

- Design the **DUT** of **4-bit Full Adder**.
- Developed the **test plan.**
- Developed **test bench architecture.**
- Implemented **Callback in test bench architecture to drop and pass the generated transactions**.
- Developed **System Verilog based environment** for the same and verified the DUT.

Languages: System Verilog
Tools: VCS

Project: Traffic light controller **August 2019**

Description: This project involves implementation of a **traffic light controller** with one traffic running in one direction and under assumption that green or yellow light in one direction implies red in other directions.

Roles & Responsibilities:

- Developed the design **for traffic light controller** with the given specifications.

Languages: Verilog

B.Tech Project: Some Studies on Multi Band Frequency Selective Surfaces. **2018 - 2019**

Description: This project involves **design of multi band FSS filters** and studying their performance and other parameters for **wireless applications**.

Tools: HFSS 13.0 (ANSYS)

Summer Intern Project: Design of Single Pipelined 128 bit AES Algorithm **May – July 2018**

Description: This project involves design of **single pipelined 128-bit Advanced Encryption Algorithm (AES). It is a highly secured and modern cryptographic algorithm.**

Roles & Responsibilities:

- Developed the **design for AES** by considering the standard specifications provided by the **National Institute of Standards and Technology (NIST).**
- Verified the design results using the **sample key and plain text given by the NIST**.

Languages: Verilog
Tools: Xilinx ISE Design Suite

TECHNICAL SKILLS

Protocol Knowledge:	**AES, AMBA AHB, UFS 2.0**
Programming Languages:	**C, Java, Python.**
HDL & HVL:	**Verilog, System Verilog.**
Tools:	**Synopsys VCS, Questa Simulator, Xilinx ISE Design Suite, Vivado.**
Methodology:	**UVM.**
Operating system:	**Linux, Windows.**

EDUCATION 2015-2019

- **B-Tech** in **Electronics and Communication Engineering** from **National Institute of Technology, Sikkim** with a **CGPA** of **7.54 out of 10**.