

# ANIL SHARMA

Senior Undergraduate, Electronics and Communication, **NIT Sikkim**  
Interest: Digital System Design, Embedded System, Software Development.

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## Education

National Institute of Technology Sikkim, Ravangla, India.  
**Bachelor of Technology**, Electronics and Communication Engineering. *2015 - 2019*  
CGPA: **7.52/10** (Dec 2018)

Govt. Sr. Sec. School Rhenock, Sikkim, India.  
**High School**, CBSE *2014 - 2015*  
Percentage: **78.4 %**

## Experience

Summer Intern, **Indian Institute of Technology Bombay**  
*Mentor : Prof. Virendra Singh* *May '18 - Jul '18*

- Worked on hardware implementation of **AES** algorithm.
- Technologies/Tools: Verilog HDL, Xilinx Vivado Software.

Summer Trainee, **Motilal Nehru National Institute of Technology Allahabad**  
*Topics Covered: VLSI Design and Embedded System* *Jun '17 - Jul '17*

- Covered basics concepts of VLSI Design and Embedded System.
- Technologies/Tools: Verilog HDL, ATCAT89C51, Xilinx ISE Design Suite and mikroC Pro.

## Technical Skills

Languages: C, Core Java, Python, Verilog, SQL, L<sup>A</sup>T<sub>E</sub>X, Assembly (x86).  
Software Tools: Xilinx ISE, Vivado, HFSS 13.0, MATLAB, PyCharm, IntelliJ IDEA.  
EDA | **FPGA Tools**: Cadence Virtuoso, Mentor Graphics | Basys-3, Spartan-3E.  
Platforms: Comfortable with Windows and Linux System.

## Projects

Studies on polarization Independent Frequency Selective Surfaces:  
*Final Year Project | Supervisor: Dr. Ayan Chatterjee* *Aug '18 - present*

- Filter Design using HFSS 13.0 Software(Ongoing).

Single Pipelined 128 bit AES Algorithm:  
*Topic : Cryptography | Mentor : Prof. Virendra Singh* *May '18 - Jul '18*

- Implemented a **Single Pipelined 128 bit AES** Encryption algorithm using Verilog HDL.

Class C Power Amplifier:  
*Mini Project | Supervisor: Dr. Sanjay Kumar Jana* *Feb '18 - May '18*

- Designed a Class C Power Amplifier for RF application Using Cadence Virtuoso Software.

Digital Clock:  
*Topic: Embedded System* *Jun '17 - Jul '17*

- Designed a Digital Clock using Embedded C, AT89C51 micro Controller board and displayed the DATE, TIME and NAMES of days on 16X2 LCD Screen of the development board.

## Position of Responsibility

Student Coordinator Training and Placement Cell, NIT Sikkim.  
Technical Coordinator, UDGM | Cultural fest of NIT Sikkim.  
Technical Coordinator, ABHIYANTRAN | Technical fest of NIT Sikkim.

## Hobbies

Singing, Travelling, Playing Chess, Cricket and Football.