TN0018
Technical note

Linear accelerometers in LGA package surface mounting guidelines

Introduction

This document is a general guidelines about soldering accelerometer products packaged in LGA surface mount.

Note: Data provided in this document are to be intended as reference for PCB design and soldering process. For device specification refer to corresponding datasheet.

Contents

1 General guidelines about soldering surface mount accelerometer

As common PCB design and industrial practice when considering accelerometer soldering there are always 3 elements to take into consideration:

1. PCB with its own conductive layers (i.e. copper) and other organic materials used for board protection and dielectric isolation.
2. Accelerometer to be mounted on the board. Accelerometer senses acceleration, but it senses also the mechanical stress coming from the board. This stress is minimized with simple PCB design rules.
3. Soldering paste like Sn/Ag/Cu. This soldering paste can be dispensed on the board with a screen printing method through a stencil. The pattern of the soldering paste on the PCB is given by the stencil mask itself.

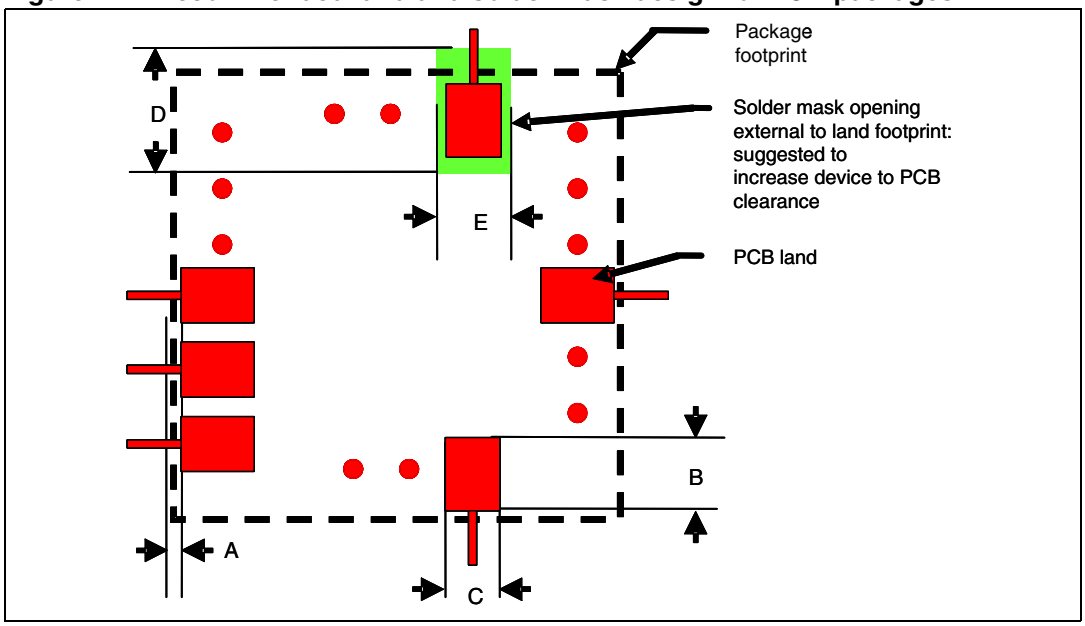
2 PCB design guidelines

PCB land and solder masking general recommendations are shown in *Figure 1*. Refer to device datasheet or *Appendix A: LGA packages outlines* for pad count, size and pitch.

- It is recommended to open solder mask external to PCB land;
- The area below the sensor (on the same side of the board) must be defined as keep-out area. It is strongly recommended to not place any structure in top metal layer underneath the sensor;
- Traces connected to pads should be as much symmetric as possible. Symmetry and balance for pad connection will help component self alignment and will lead to a better control of solder paste reduction after reflow;
- For better performances over temperature it is strongly recommended not to place large insertion components like buttons or shielding boxes at distance less than 2 mm from the sensor;
- Pin #1 indicator must be left unconnected to ensure proper device functionality.

2.1 PCB design rules

Figure 1. Recommended land and solder mask design for LGA packages



A = Clearance from PCB land edge to solder mask opening ≥ 0.25 mm to ensure that solder mask is opened externally to device area

B = PCB land length = LGA solder pad length + 0.1 mm

C = PCB land width = LGA solder pad width + 0.1 mm

D = Solder mask opening length = PCB land length + 0.3 mm: design 0.05mm inside and 0.25 mm outside

E = Solder mask opening width = PCB land width + 0.1 mm

3 Stencil design and solder paste application

The thickness and the pattern of the soldering paste are important for the proper accelerometer mounting process

- Stainless steel stencils are recommended for solder paste application;
- A stencil thickness of 90 - 150 µm (3.5 - 6 mils) is recommended for screen printing;
- The final thickness of soldering paste should allow proper cleaning of flux residuals and clearance between sensor package and PCB;
- Stencil aperture should have rectangular shape with dimension up to 25 µm (1 mil) smaller than PCB land;
- The openings of the stencil for the signal pads should be between 70% and 90% of the PCB pad area;
- Optionally, for better solder paste release, the aperture walls should be trapezoidal and the corners rounded;
- The fine pitch of the IC leads requires accurate alignment of the stencil to the printed circuit board. The stencil and printed circuit assembly should be aligned to within 25 µm (1 mil) prior to application of the solder paste.

4 Process consideration

- In case of use of no self-cleaning solder paste it is mandatory proper washing of the board after soldering to eliminate any possible source of leakage between adjacent pads due to flux residues;
- The PCB soldering profile depends on the number, size and placement of components in the application board. It is not functional to define a specific soldering profile for the accelerometer only. Customer should use a time and temperature reflow profile that is derived from the PCB design and manufacturing experience.
- No solder material reflow on the side of the package is allowed since LGA packages show metal trace out of package side.

5 Solder heat resistance and environmental specification

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

LGA packages for accelerometer are qualified for soldering heat resistance according to JEDEC J-STD-020C, in MSL3 condition.

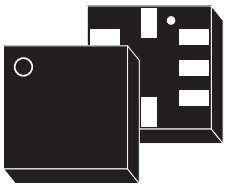
Appendix A LGA packages outlines

A.1 LGA 5x5x1.6 mm, 8 lead

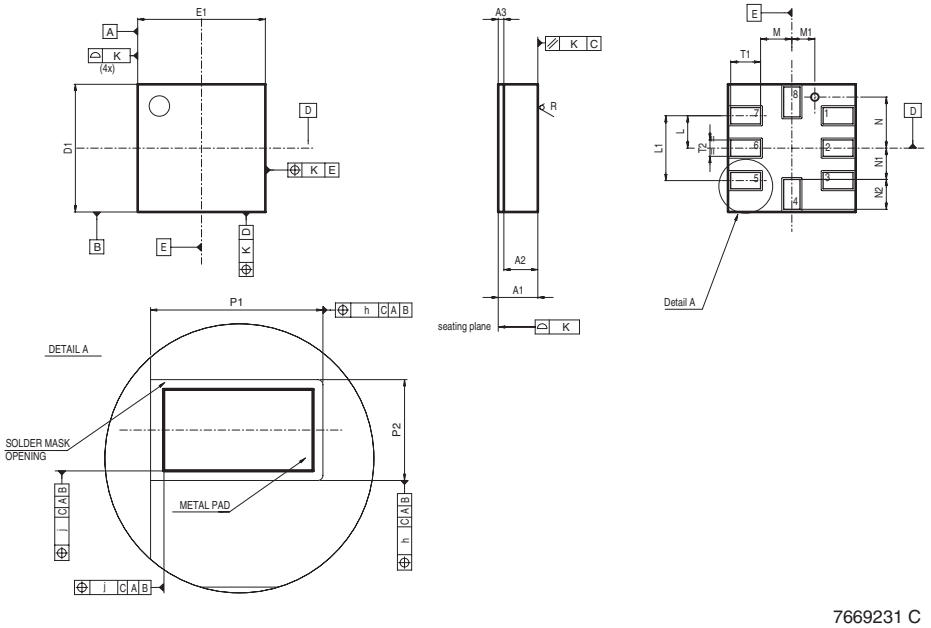
Figure 2. LGA 5x5x1.6 mm, 8 lead

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A1	1.460	1.520	1.600	0.0574	0.0598	0.0629
A2			1.330			0.0523
A3	0.180	0.220	0.260	0.007	0.0086	0.0102
D1	4.850	5.000	5.150	0.190	0.1968	0.2027
E1	4.850	5.000	5.150	0.190	0.1968	0.2027
L		1.270			0.05	
L1		2.540			0.1	
M		1.225			0.0482	
M1	0.875	0.900	0.925	0.0344	0.0354	0.0364
N		2.000			0.0787	
N1		1.225			0.0482	
N2		1.170			0.046	
P1	1.300	1.350	1.400	0.0511	0.0531	0.0551
P2	0.740	0.790	0.840	0.0291	0.0311	0.033
T1		1.170			0.046	
T2	0.615	0.640	0.665	0.0242	0.0251	0.0261
R	1.200		1.600	0.0472		0.0629
h		0.150			0.0059	
k		0.050			0.0019	
j		0.100			0.0039	

OUTLINE AND MECHANICAL DATA



LGA8 (5x5x1.6mm)
Land Grid Array Package

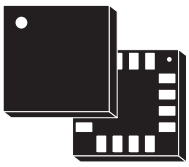


A.2 LGA 5x5x1.6 mm, 16 lead

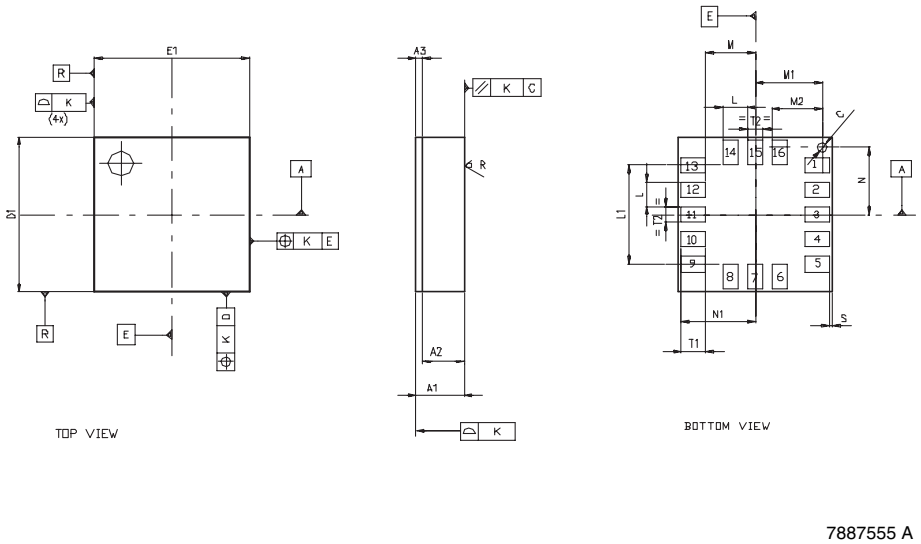
Figure 3. LGA 5x5x1.6 mm, 16 lead

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A1	1.460	1.500	1.600	0.575	0.0591	0.0630
A2	1.		330			0.0524
A3	0.160	0.200	0.240	0.0063	0.0079	0.0094
C	0	.300			0.0118	
D1	4.850	5.000	5.150	0.1909	0.1969	0.2028
E1	4.850	5.000	5.150	0.1909	0.1969	0.2028
L	0	.800			0.0315	
L1	3	.200			0.1260	
M	1	.600			0.0630	
M1	2.150	2.180	2.200	0.0846	0.0858	0.0866
M2	1	.630			0.0642	
N	2	.180			0.0858	
N1	2	.400			0.0945	
T1	0	.800			0.0315	
T2	0.480	0.500	0.530	0.0189	0.0197	0.0209
R	1.200		1.600	0.0472		0.0630
S	0	.100			0.0039	
h	0	.150			0.0059	
k	0	.050			0.0020	
j	0	.100			0.0039	

OUTLINE AND MECHANICAL DATA



LGA16 (5x5x1.6mm)
Land **G**rid **A**rray **P**ackage

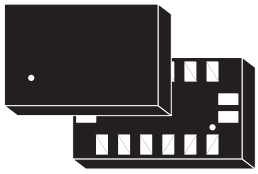


A.3 LGA 4.4x7.5x1 mm, 16 lead

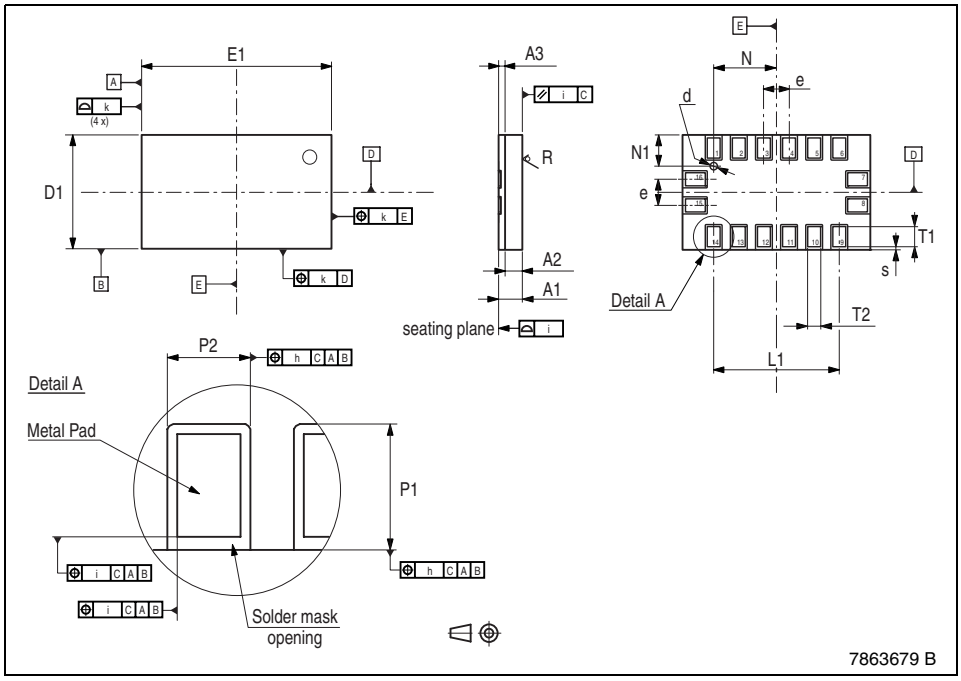
Figure 4. LGA 4.4x7.5x1 mm, 16 lead

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A1		0.92	1			0.0394
A2			0.7			0.0276
A3	0.180	0.220	0.260	0.0071	0.0087	0.0102
D1	4.250	4.400	4.550	0.1673	0.1732	0.1791
E1	7.350	7.500	7.650	0.2894	0.2953	0.3012
e		1.0			0.0394	
d		0.3			0.0118	
L1		5.000			0.1969	
N		2.5			0.0984	
N1		1.2			0.0472	
P1	0.965	0.975	0.985	0.0380	0.0384	0.0388
P2	0.64	0.65	0.66	0.0252	0.0256	0.0260
T1	0.75	0.8	0.85	0.0295	0.0315	0.0335
T2	0.45	0.5	0.55	0.0177	0.0197	0.0217
R	1.200		1.600	0.0472		0.0630
h		0.150			0.0059	
k		0.050			0.0020	
i		0.100			0.0039	
s		0.100			0.0039	

OUTLINE AND MECHANICAL DATA



LGA16 (4.4x7.5x1mm)
Land **G**rid **A**rray **P**ackage

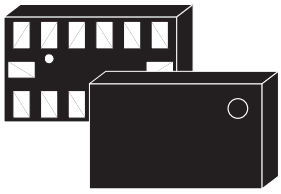


A.4 LGA 3x5x0.9 mm, 14 lead

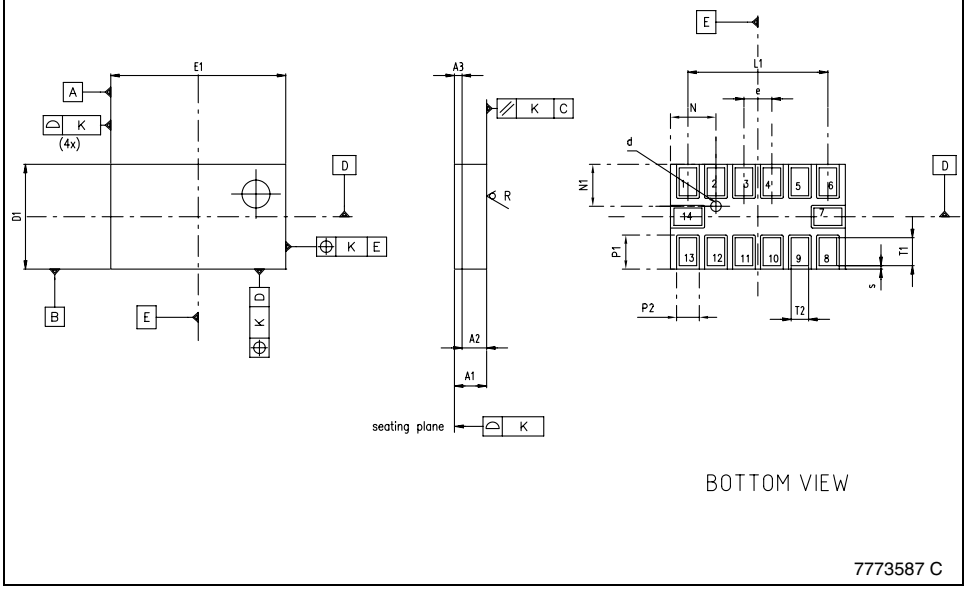
Figure 5. LGA 3x5x0.9 mm, 14 lead

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A1		0.920	1.000		0.0362	0.0394
A2			0.700			0.0275
A3	0.180	0.220	0.260	0.0071	0.0087	0.0102
D1	2.850	3.000	3.150	0.1122	0.1181	0.1240
E1	4.850	5.000	5.150	0.1909	0.1968	0.2027
e		0.800			0.0315	
d		0.300			0.0118	
L1		4.000			0.1575	
N		1.360			0.0535	
N1		1.200			0.0472	
P1	0.965	0.975	0.985	0.0380	0.0384	0.0386
P2	0.640	0.650	0.660	0.0252	0.0256	0.0260
T1	0.750	0.800	0.850	0.0295	0.0315	0.0335
T2	0.450	0.500	0.550	0.0177	0.0197	0.0217
R	1.200		1.600	0.0472		0.0630
h		0.150			0.0059	
k		0.050			0.0020	
i		0.100			0.0039	
s		0.100			0.0039	

OUTLINE AND MECHANICAL DATA



LGA14 (3x5x0.92mm) Pitch 0.8mm
Land **G**rid **A**rray **P**ackage

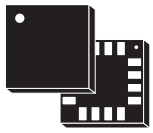


A.5 LGA 4x4x1.5 mm, 16 lead

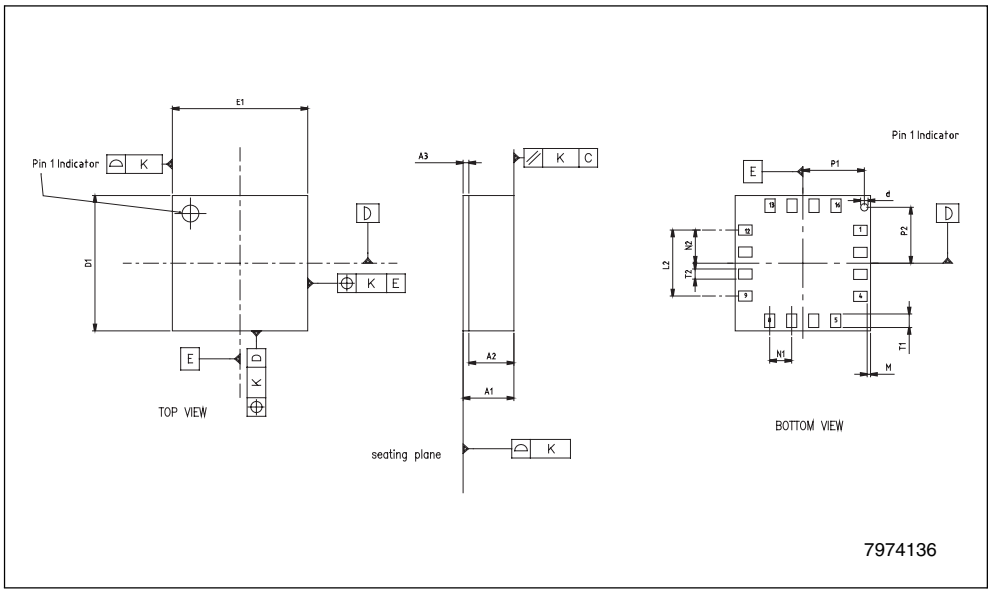
Figure 6. LGA 4x4x1.5mm, 16 lead

Dimensions						
Ref.	mm			inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A1		1.500	1.600		0.0591	0.0630
A2			1.330			0.0524
A3	0.160	0.200	0.240	0.0063	0.0079	0.0094
d		0.300			0.0118	
D1	3.850	4.000	4.150	0.1516	0.1575	0.1634
E1	3.850	4.000	4.150	0.1516	0.1575	0.1634
L2		1.950			0.0768	
M		0.100			0.0039	
N1		0.650			0.0256	
N2		0.975			0.0384	
P1		1.750			0.0689	
P2		1.525			0.0600	
T1		0.400			0.0157	
T2		0.300			0.0118	
k		0.050			0.0020	

Outline and mechanical data



LGA 16L (4x4x1.5mm)
Land Grid Array Package

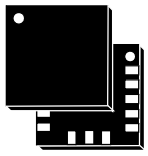


A.6 LGA 3x3x1.0mm, 16 lead

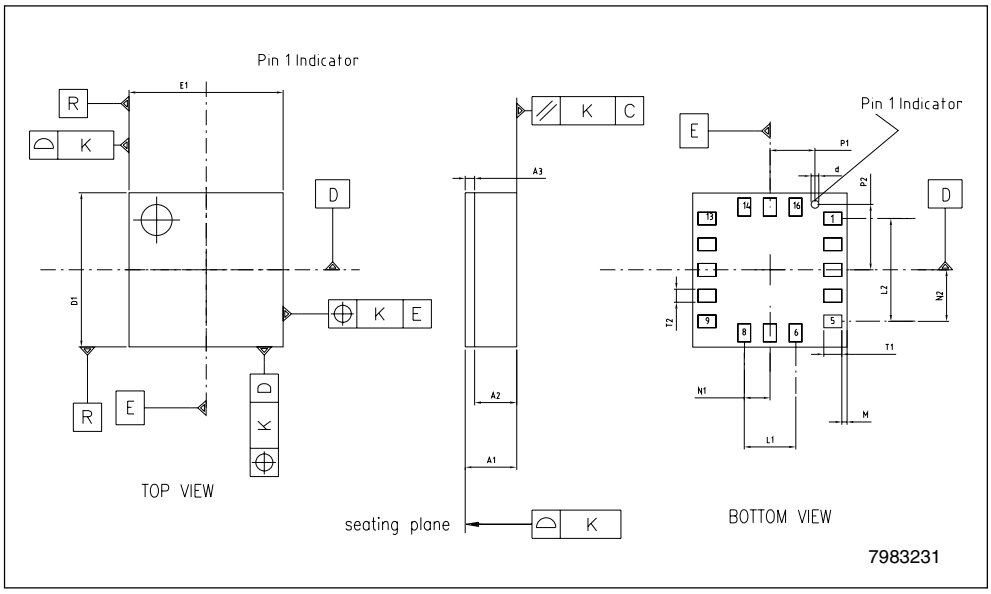
Figure 7. LGA 3x3x1.0mm, 16 lead

Dimensions						
Ref.	mm			inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A1			1.000			0.0394
A2		0.785			0.0309	
A3		0.200			0.0079	
D1	2.850	3.000	3.150	0.1122	0.1181	0.1240
E1	2.850	3.000	3.150	0.1122	0.1181	0.1240
L1		1.000	1.060		0.0394	0.0417
L2		2.000	2.060		0.0787	0.0811
N1		0.500			0.0197	
N2		1.000			0.0394	
M	0.040	0.100	0.160	0.0016	0.0039	0.0063
P1		0.875			0.0344	
P2		1.275			0.0502	
T1	0.290	0.350	0.410	0.0114	0.0138	0.0161
T2	0.190	0.250	0.310	0.0075	0.0098	0.0122
d		0.150			0.0059	
k		0.050			0.0020	

Outline and mechanical data



LGA16 (3x3x1.0mm)
Land Grid Array Package



6 Revision history

Table 1. Document revision history

Date	Revision	Changes
12-Oct-06	1	Initial release.
30-Apr-08	2	Added appendix paragraphs *A.5: LGA 4x4x1.5 mm, 16 lead* and *A.6: LGA 3x3x1.0mm, 16 lead*