Angad Singh

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SUMMARY

Systems Engineer specializing in High-Performance Networking and Kernel Bypass. Combining deep academic research in DPDK/RISC-V with 4+ years of industry experience building scalable enterprise infrastructure.

SKILLS

Systems & Architecture: C, C++ (Modern), RISC-V Assembly, SystemVerilog, POSIX, Pipelining, Cache Coherency, Memory Barriers
Networking & Tools: DPDK (PMD), F-Stack, Zero-copy DMA, TCP/IP, Linux Kernel, Verilator, GDB/Valgrind, Docker, Git, Bash/Python
Backend & Cloud: Java 17, Spring Boot, Redis, Kafka, AWS (Lambda, VPC), gRPC

PROJECTS

User-Space Networking on RISC-V | *C, RISC-V, DPDK, F-Stack, Linux, Networking*

- Engineered a custom DPDK Poll Mode Driver (PMD) for a proprietary FPGA NIC, implementing Memory-Mapped I/O (MMIO) to control hardware registers directly from user space.
- Resolved critical race conditions on the RISC-V weak memory model by injecting assembly FENCE instructions, ensuring DMA descriptor consistency before triggering the hardware doorbell.
- Implemented a Zero-Copy data path by allocating Hugepages and mapping DMA rings via the VFIO-platform driver, bypassing the Linux kernel to eliminate context switch overhead.

5-Stage RISC-V CPU with Cache & Branch Prediction | *SystemVerilog, Verilator*

- Designed a 5-stage pipelined RV64IM processor with a Data Forwarding Unit to resolve Read-After-Write (RAW) data hazards without stalling, maximizing instruction throughput (IPC).
- Implemented a 2-way Set-Associative Cache (Write-Back/Write-Allocate) and a Dynamic Branch Predictor (2-bit saturating counter) to minimize memory access latency and control penalties.

Geo-Distributed Database Engine | *C++, Multi-Paxos, Hybrid Logical Clocks*

- Timestamp-ordered execution with a 2-WRTT commit bound; 30–60× higher throughput than OCC in multi-shard geo setups.
- Built on Mako (OSDI'25); TPC-C benchmarks on cloud infrastructure with simulated network latency.

Raft Consensus Implementation | *C++, RPC, Fault Tolerance*

- Architected a fault-tolerant Key-Value store using Raft (Leader Election, Log Replication, Persistence), validating linearizability under partition scenarios.

EDUCATION

Stony Brook University Stony Brook, NY | Aug 2024 - May 2026
Master of Science in Computer Science ***GPA***: 3.56/4.0
Systems-Relevant Coursework: Operating Systems, Computer Architecture, Distributed Systems, Database Systems
Research: RISC-V based User-Space Networking with DPDK & F-Stack (Prof. Michael Ferdman)

SRM Institute of Science and Technology Chennai, India| July 2016 - June 2020
Bachelor of Technology in Computer Science and Engineering ***GPA***: 3.99/4.0 (Top 5%)
Systems-Relevant Coursework: Compiler Design, Computer Networks, Data Structures & Algorithms

EXPERIENCE

Veolia North America **Paramus, NJ**
Java & Web Platform Intern – MW Regulated Utility Team *June 2025 – Present*

- Developed a real-time observability dashboard using AWS (Lambda, DynamoDB, CloudWatch) to monitor system health, automating infrastructure alerts to reduce Mean Time to Detection (MTTD) for production issues.

Volante Technologies **Chennai, India**
Senior Software Engineer *June 2020 – July 2024*

- **Architected the core engine migration** to Java 17, resolving 15+ legacy architectural bottlenecks and ensuring zero-downtime stability for mission-critical payment flows.
- **Optimized system observability** by redesigning the logging and exception handling framework, reducing I/O overhead by 50% and accelerating production incident resolution.
- Mentored 6 engineers and led technical reviews; awarded "Dream Team" Recipient (2x) for engineering excellence.