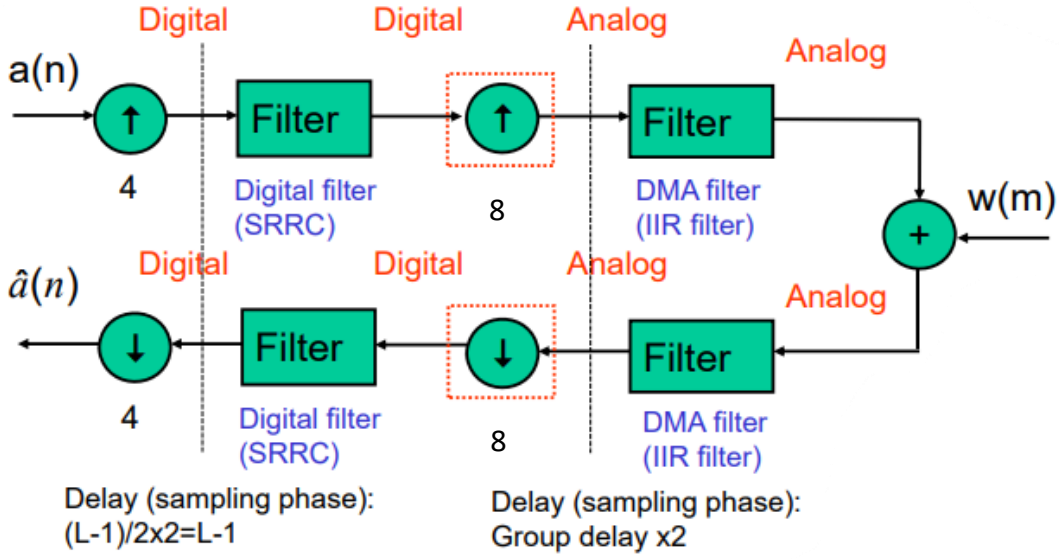
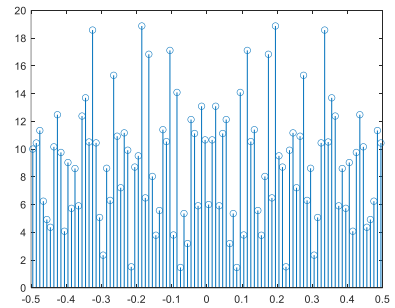
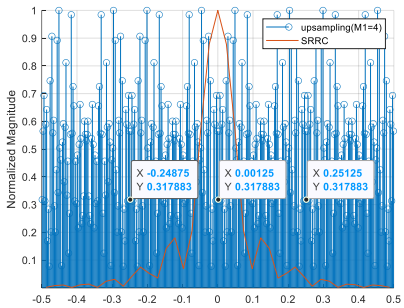
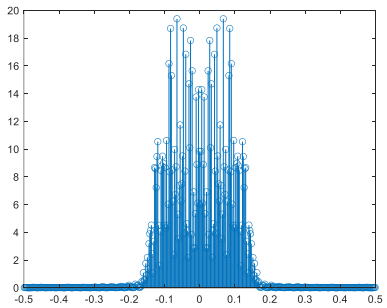
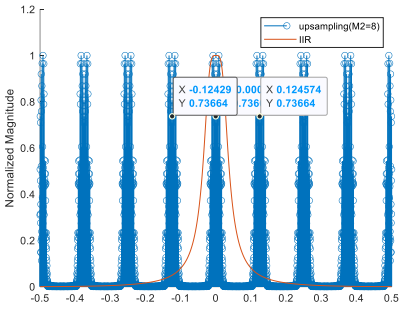
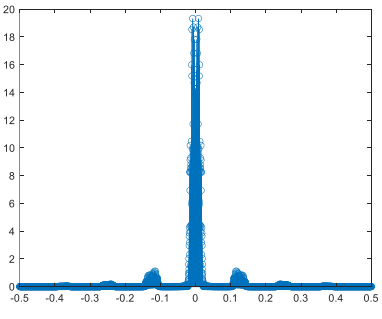
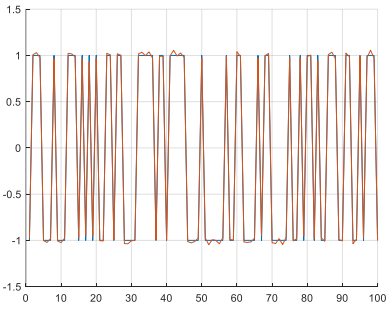
PROBLEM:

- Let the symbol rate for a system be 1MHz, the sampling rate of the DAC be 4MHz, and sampling rate for DMA filter be 32MHz.
- Let the modulation be BPSK, and the digital pulse shaping is SRRC.
- Design an IIR DMA filter with 5 coefficients (second order and one section) that maximizes stopband attenuation.
- Conduct the transmit and receive operation for a sequence (without carrier).

I. 流程：因為 analog filter 實作較困難，所以前面先加上一層易於實現的 digital filter，將訊號的頻譜間距拉開，後面 analog filter 比較好把訊號濾出來。
1MHz → 4MHz → 32MHz，取 M1 = 4，M2 = 8。



(1) x[n]	(2) up-sampling (M1 = 4)	(3) SRRC digital filter
		
(4) up-sampling (M2 = 8)	**(5) LPF analog filter**	**(6) RX recovered signal**
		

II. IIR DMA filter design：M2 = 8，所以 F_{stop} 預測為 $\frac{1}{8}-\frac{1}{64}=0.109375$ 附近，F_{pass} 預測為 $\frac{1}{64}=0.015625$ 附近，最後取 $F_{stop}=0.1, F_{pass}=0.02$。