Digital IC Design

Project Report

Exercise 3: Sequential Circuit

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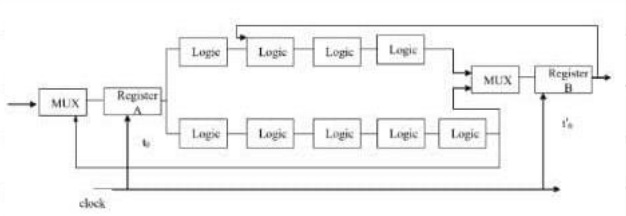
Ex3-1: Static Timing Analysis

- Assume a unit delay through the Register and Logic blocks (t_R= t_L = 1) (Tpcq = Tccq = 1).
- Assume that the registers, which are positive edge-triggered, have a set-up time t_S of 1, hold time of 0.5. The delay through the multiplexer t_M equals 5 t_R.

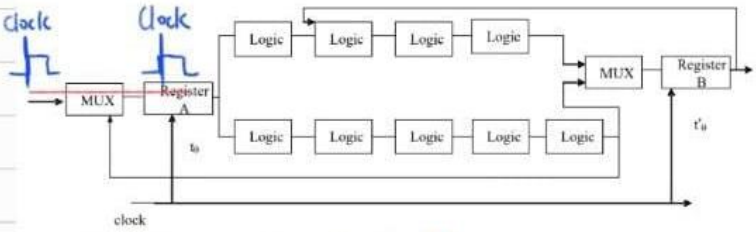


※ Four Types of Critical Path

1. Input → Delay 2. Delay → Delay
3. Delay → Output 4. Input → Output

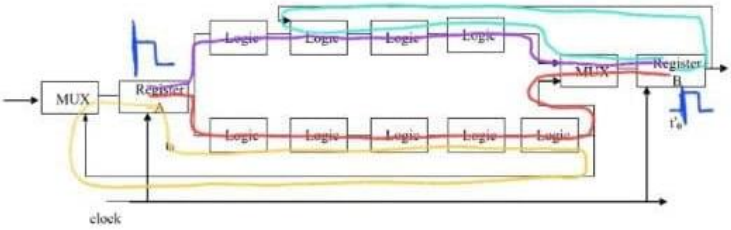
a) Determine the minimum clock period. Disregard clock skew.

Type 1. Critical path : Input → Delay



Total Delay = 5 + 1 + 1 = 7
(MUX) (Reg Delay) (Reg setup)

Type 2. Delay → Delay



$T_c \geq t_{pcq} + t_{pd} + t_{setup}$

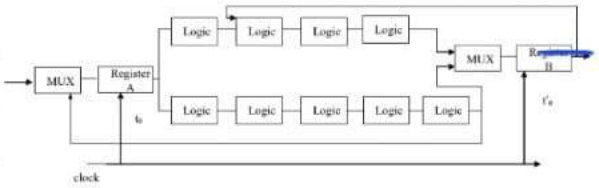
Path 1 Delay = 1 + 5 + 5 + 1 + 1 = 13 #
(RegA Tpcq) (5 Logics) (MUX) (RegB Delay) (RegB Setup)

Path 2. Delay = 1 + 4 + 5 + 1 + 1 = 12
(RegA t_{pcq}) (4 logics) (MUX) (RegB t_{delay}) (RegB t_{setup})

Path 3. Delay = 1 + 3 + 5 + 1 + 1 = 11
(RegB t_{pcq}) (3 logics) (MUX) (RegB t_{setup}) (RegB t_{delay})

Path 4. Delay = 1 + 5 + 5 + 1 + 1 = 13 #
(RegA t_{pcq}) (5 logics) (MUX) (RegA t_{delay}) (RegA t_{setup})

Type 3. Delay → Output



Delay = 0.5
(RegB t_{hold})

Type 4. Input → Output
(None)

Ans: Minimum Clock Period = 13 (Path 1 & 4)

b) Repeat part a, assume a non-zero clock skew $\delta = t'_\theta - t_\theta = -1$.

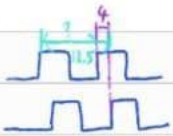
$\delta = t'_\theta - t_\theta = -1 \Rightarrow t'_\theta$ is 1 ahead t_θ

We need 1 extra for clock skew

$Tc' - 1 \geq 13$, $Tc' \geq 14$

Ans: Minimum clock period = 14

c) Repeat part a, assume in a non-zero clock skew $\delta = t'_\theta - t_\theta = 4$.



$Tc' + t_{skew} \geq t_{pcq} + t_{pd} + t_{setup}$

$Tc' + 4 \geq 13$, $Tc' \geq 9$

Ans: Minimum clock period = 9

d) Derive the maximum positive clock skew that can be tolerated before the circuit fails (setup time violation)

$t_{skew} \leq T_{clk} - (t_{pcq} + t_{pd} + t_{setup})$

$t_{skew} \leq T_{clk} - 13$

Ans: Maximum positive clock skew = $T_{clk} - 13$

e) Derive the maximum skew that can be tolerated before the circuit fails (hold time violation).

(t_{pd})

$t_{cd} + t_{ccq} \geq t_{hold} + t_{skew}$

$11 + 1 \geq 0.5 + t_{skew}$

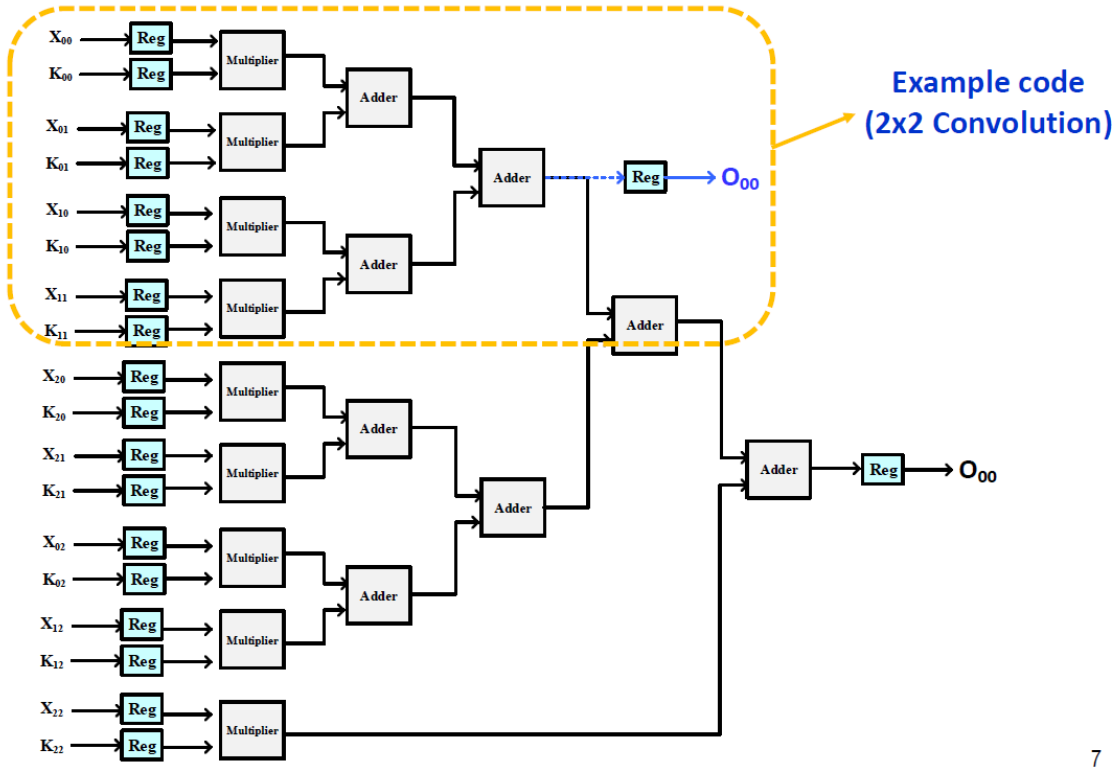
$t_{skew} \leq 11.5$

Ans: Maximum skew = 11.5

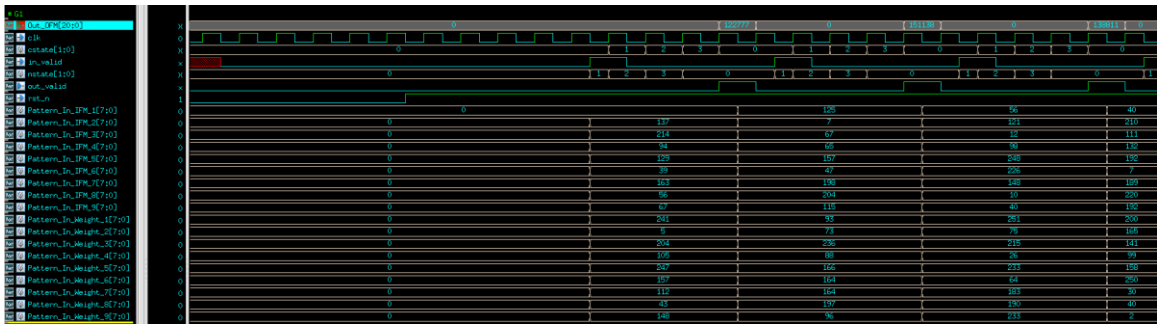
Ex3-2: Timing/Area Analysis of Sequential Circuits

❖ Design 1. 3x3 Convolution Kernel (without pipeline)

- Block Diagram:



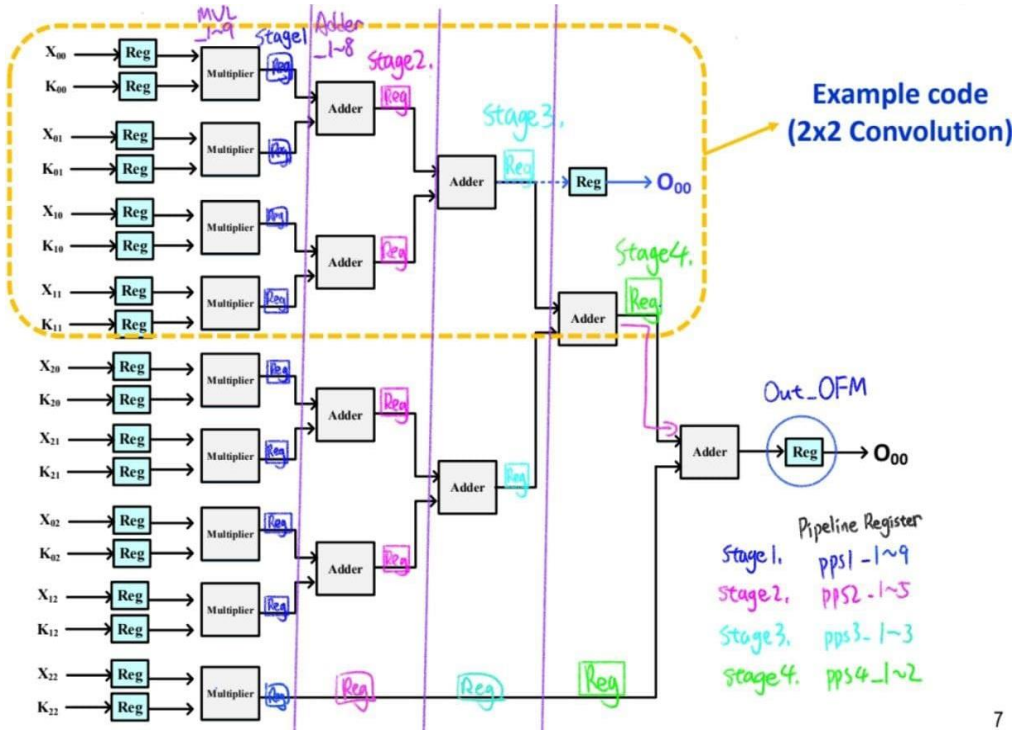
- Waveform:



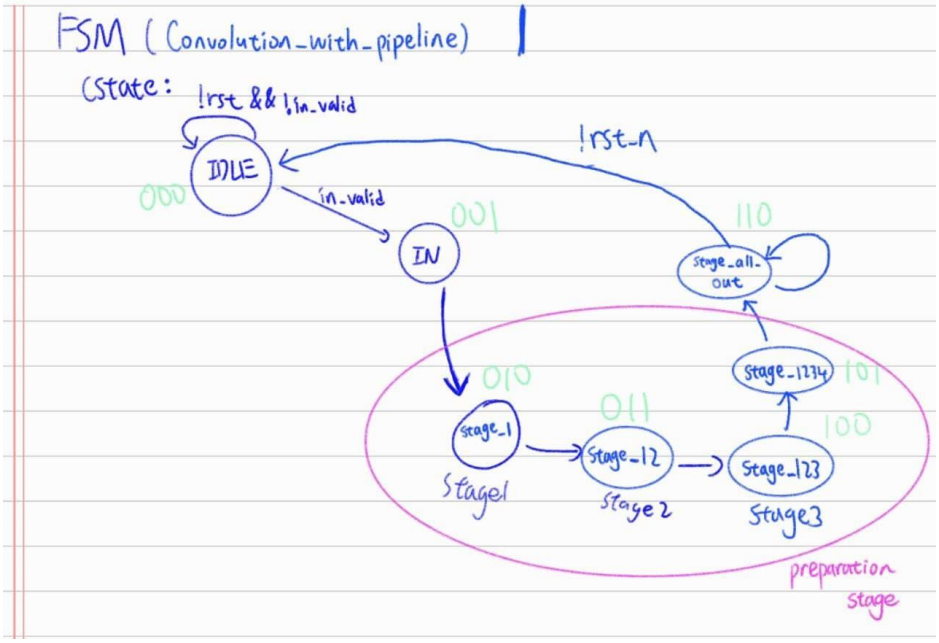
Logic Verification: PASS!

❖ Design 2. 3x3 Convolution Kernel (pipeline)

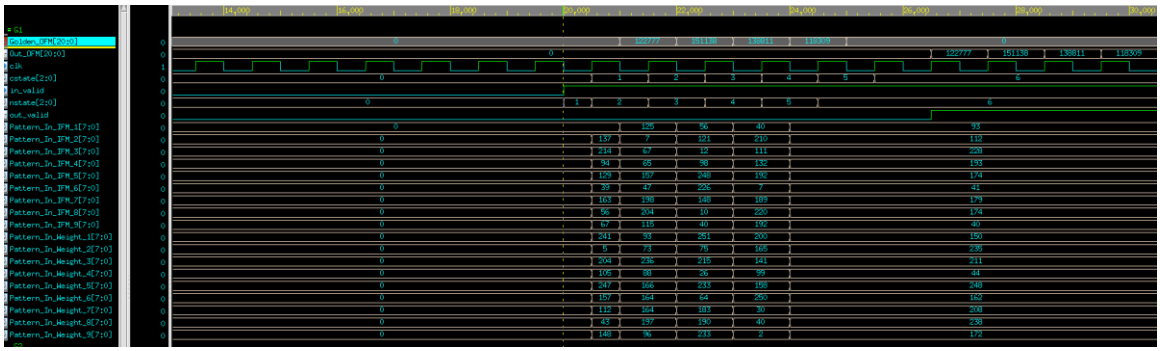
- Block Diagram:



- Finite State Machine:



- Waveform:



Explanation: My pipeline has six stages in total, including input and output stage. It has 6 states in its finite state machine. The first output will be ready after the first sixth stage and continuously output the result in the following clock cycle.

➢ Compare and Analysis two Designs

○ Convolution without pipeline

Synthesis with clock cycle = 1ns

Critical Path:

Point	Incr	Path
clock clk (rise edge)	0.00	0.00
clock network delay (ideal)	0.00	0.00
weigts9_reg[1]/CLK (ASYNC_DFFHx1_ASAP7_75t_R)	0.00	0.00 r
weigts9_reg[1]/QN (ASYNC_DFFHx1_ASAP7_75t_R)	48.16	48.16 f
U715/Y (BUFx8_ASAP7_75t_R)	30.26	78.42 f
U712/Y (INVx4_ASAP7_75t_R)	7.96	86.37 r
U1630/Y (NAND4xp25_ASAP7_75t_R)	38.07	124.45 f
U1000/Y (NAND2xp5_ASAP7_75t_R)	32.20	156.64 r
DP_OP_45J1_122_1156/U819/SN (FAx1_ASAP7_75t_R)	68.61	225.25 f
DP_OP_45J1_122_1156/U811/CON (FAx1_ASAP7_75t_R)	31.13	256.38 r
U1211/Y (BUFx3_ASAP7_75t_R)	24.46	280.85 r
U1201/Y (INVx3_ASAP7_75t_R)	6.18	287.02 f
DP_OP_45J1_122_1156/U781/SN (FAx1_ASAP7_75t_R)	61.05	348.07 f
DP_OP_45J1_122_1156/U776/CON (FAx1_ASAP7_75t_R)	41.55	389.63 r
DP_OP_45J1_122_1156/U731/CON (FAx1_ASAP7_75t_R)	32.42	422.05 f
DP_OP_45J1_122_1156/U671/CON (FAx1_ASAP7_75t_R)	29.73	451.78 r
U1196/Y (BUFx5_ASAP7_75t_R)	28.42	480.20 r
U1195/Y (INVx4_ASAP7_75t_R)	6.17	486.37 f
DP_OP_45J1_122_1156/U600/CON (FAx1_ASAP7_75t_R)	18.48	504.85 r
U1212/Y (BUFx3_ASAP7_75t_R)	24.56	529.41 r
U1203/Y (INVx3_ASAP7_75t_R)	6.18	535.59 f
DP_OP_45J1_122_1156/U521/CON (FAx1_ASAP7_75t_R)	24.68	560.27 r
DP_OP_45J1_122_1156/U439/CON (FAx1_ASAP7_75t_R)	32.79	593.06 f
DP_OP_45J1_122_1156/U439/SN (FAx1_ASAP7_75t_R)	19.56	612.63 r
U768/Y (BUFx4_ASAP7_75t_R)	31.15	643.77 r
U964/Y (INVx2_ASAP7_75t_R)	5.82	649.59 f
U2389/Y (MAJIxp5_ASAP7_75t_R)	24.89	674.48 r
U2393/Y (MAJIxp5_ASAP7_75t_R)	34.08	708.56 f
U1219/Y (MAJx2_ASAP7_75t_R)	32.98	741.54 f
U2400/Y (MAJx2_ASAP7_75t_R)	30.64	772.18 f
U1227/Y (MAJIxp5_ASAP7_75t_R)	17.12	789.30 r
U2406/Y (MAJx2_ASAP7_75t_R)	29.62	818.92 r
U2410/Y (MAJIxp5_ASAP7_75t_R)	22.33	841.25 f
U2414/Y (MAJIxp5_ASAP7_75t_R)	31.78	873.04 r
U2419/Y (MAJIxp5_ASAP7_75t_R)	26.48	899.52 f
U2420/Y (XOR2xp5_ASAP7_75t_R)	26.21	925.72 f
U2421/SN (HAxp5_ASAP7_75t_R)	25.77	951.49 f
U2422/Y (NOR2xp33_ASAP7_75t_R)	14.63	966.12 r
Out_OFM_reg[17]/D (ASYNC_DFFHx1_ASAP7_75t_R)	0.00	966.12 r
data arrival time		966.12

Timing Report:

```
clock clk (rise edge)                                    1000.00    1000.00
clock network delay (ideal)                                 0.00    1000.00
Out_OFM_reg[17]/CLK (ASYNC_DFFHx1_ASAP7_75t_R)              0.00    1000.00 r
library setup time                                        -18.38     981.62
data required time                                                   981.62
---------------------------------------------------------------------------
data required time                                                   981.62
data arrival time                                                   -966.12
---------------------------------------------------------------------------
slack (MET)                                                          15.50
```

Area:

```
Number of ports:                          169
Number of nets:                          3189
Number of cells:                         2504
Number of combinational cells:           2337
Number of sequential cells:               167
Number of macros/black boxes:               0
Number of buf/inv:                        681
Number of references:                      29

Combinational area:               3818.327000
Buf/Inv area:                      939.651831
Noncombinational area:            1012.901753
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:                  4831.228754
Total area:                 undefined
```

Synthesis with clock cycle = 0.75ns

Critical Path:

```
Point                                                   Incr       Path
-----------------------------------------------------------------------------
clock clk (rise edge)                                   0.00       0.00
clock network delay (ideal)                             0.00       0.00
weigts5_reg[4]/CLK (ASYNC_DFFHx1_ASAP7_75t_R)           0.00       0.00 r
weigts5_reg[4]/QN (ASYNC_DFFHx1_ASAP7_75t_R)           46.43      46.43 f
U1085/Y (BUFx5_ASAP7_75t_R)                            26.75      73.18 f
U1753/Y (NOR2xp33_ASAP7_75t_R)                         30.97     104.15 r
DP_OP_45J1_122_8509/U767/CON (FAx1_ASAP7_75t_R)        36.02     140.17 f
DP_OP_45J1_122_8509/U682/CON (FAx1_ASAP7_75t_R)        29.02     169.19 r
U922/Y (BUFx3_ASAP7_75t_R)                             24.11     193.30 r
U890/Y (INVx3_ASAP7_75t_R)                              6.17     199.47 f
DP_OP_45J1_122_8509/U596/CON (FAx1_ASAP7_75t_R)        24.68     224.15 r
DP_OP_45J1_122_8509/U511/SN (FAx1_ASAP7_75t_R)         95.57     319.72 f
U1797/Y (XNOR2xp5_ASAP7_75t_R)                         37.96     357.68 f
U1796/Y (XOR2xp5_ASAP7_75t_R)                          26.66     384.34 f
DP_OP_45J1_122_8509/U488/CON (FAx1_ASAP7_75t_R)        37.42     421.76 r
DP_OP_45J1_122_8509/U488/SN (FAx1_ASAP7_75t_R)         25.53     447.29 f
DP_OP_45J1_122_8509/U484/CON (FAx1_ASAP7_75t_R)        37.65     484.94 r
DP_OP_45J1_122_8509/U484/SN (FAx1_ASAP7_75t_R)         18.25     503.18 f
U965/Y (BUFx4_ASAP7_75t_R)                             32.15     535.34 f
U684/Y (XNOR2xp5_ASAP7_75t_R)                          27.36     562.70 f
U831/Y (XNOR2xp5_ASAP7_75t_R)                          27.69     590.39 f
U672/Y (NAND2x1_ASAP7_75t_R)                           17.88     608.28 r
U787/Y (NAND2x1_ASAP7_75t_R)                           11.85     620.12 f
U803/Y (NAND2x1_ASAP7_75t_R)                           15.27     635.39 r
U999/Y (AND2x2_ASAP7_75t_R)                            23.41     658.80 r
U830/Y (NOR2x1p5_ASAP7_75t_R)                          10.09     668.89 f
U829/Y (NOR3xp33_ASAP7_75t_R)                          15.64     684.53 r
U985/Y (OR2x2_ASAP7_75t_R)                             21.06     705.59 r
U983/Y (XNOR2xp5_ASAP7_75t_R)                          16.86     722.45 r
U807/Y (NOR2xp67_ASAP7_75t_R)                          11.95     734.40 f
Out_OFM_reg[17]/D (ASYNC_DFFHx1_ASAP7_75t_R)            0.00     734.40 f
data arrival time                                                734.40
```

Timing Report:

```
clock clk (rise edge)                                 750.00     750.00
clock network delay (ideal)                             0.00     750.00
Out_OFM_reg[17]/CLK (ASYNC_DFFHx1_ASAP7_75t_R)          0.00     750.00 r
library setup time                                    -15.45     734.55
data required time                                               734.55
-----------------------------------------------------------------------------
data required time                                               734.55
data arrival time                                               -734.40
-----------------------------------------------------------------------------
slack (MET)                                                       0.16
```

Area

```
Number of ports:                          169
Number of nets:                          3539
Number of cells:                         2925
Number of combinational cells:           2758
Number of sequential cells:               167
Number of macros/black boxes:               0
Number of buf/inv:                        773
Number of references:                      38

Combinational area:               4434.886039
Buf/Inv area:                     1128.142068
Noncombinational area:            1012.901753
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:                  5447.787792
Total area:                 undefined
```

Synthesis with clock cycle = 0.4ns

Critical Path

Point	Incr	Path
clock clk (rise edge)	0.00	0.00
clock network delay (ideal)	0.00	0.00
weigts5_reg[5]/CLK (ASYNC_DFFHx1_ASAP7_75t_R)	0.00	0.00 r
weigts5_reg[5]/QN (ASYNC_DFFHx1_ASAP7_75t_R)	66.88	66.88 r
U2626/Y (NOR2xp33_ASAP7_75t_R)	37.93	104.80 f
U1225/Y (XNOR2xp5_ASAP7_75t_R)	27.99	132.80 r
U1204/Y (XOR2xp5_ASAP7_75t_R)	33.40	166.20 r
U1203/Y (MAJIxp5_ASAP7_75t_R)	31.06	197.26 f
U1733/Y (MAJx2_ASAP7_75t_R)	36.29	233.55 f
U1828/Y (XNOR2x1_ASAP7_75t_R)	25.49	259.04 f
U1071/Y (XNOR2xp5_ASAP7_75t_R)	30.80	289.84 f
U1111/Y (XNOR2x1_ASAP7_75t_R)	28.40	318.24 f
U1110/Y (XNOR2x1_ASAP7_75t_R)	26.82	345.06 f
U1499/Y (MAJIxp5_ASAP7_75t_R)	27.47	372.53 r
U2144/Y (XNOR2x1_ASAP7_75t_R)	29.06	401.59 r
U1497/Y (XNOR2x1_ASAP7_75t_R)	27.70	429.30 r
U1496/Y (XNOR2xp5_ASAP7_75t_R)	21.93	451.23 r
U1407/Y (XNOR2xp5_ASAP7_75t_R)	21.91	473.14 r
U1565/Y (NOR2x1_ASAP7_75t_R)	17.55	490.69 f
U1837/Y (NOR2x1_ASAP7_75t_R)	15.75	506.43 r
U1493/Y (NAND2xp5_ASAP7_75t_R)	12.96	519.39 f
U2251/Y (AND2x2_ASAP7_75t_R)	22.46	541.85 f
U4134/Y (OR3x1_ASAP7_75t_R)	25.96	567.81 f
U3515/Y (NAND2xp5_ASAP7_75t_R)	8.69	576.50 r
U3514/Y (NOR3xp33_ASAP7_75t_R)	15.33	591.83 f
Out_OFM_reg[16]/D (ASYNC_DFFHx1_ASAP7_75t_R)	0.00	591.83 f
data arrival time		591.83

Timing Report

```
clock clk (rise edge)                                  400.00     400.00
clock network delay (ideal)                              0.00     400.00
Out_OFM_reg[16]/CLK (ASYNC_DFFHx1_ASAP7_75t_R)           0.00     400.00 r
library setup time                                     -16.34     383.66
data required time                                                383.66
--------------------------------------------------------------------------
data required time                                                383.66
data arrival time                                                -591.83
--------------------------------------------------------------------------
slack (VIOLATED)                                                 -208.17
```

Area

```
Number of ports:                          169
Number of nets:                          4525
Number of cells:                         4348
Number of combinational cells:           4181
Number of sequential cells:               167
Number of macros/black boxes:               0
Number of buf/inv:                        754
Number of references:                      47

Combinational area:               6827.405729
Buf/Inv area:                     1071.455023
Noncombinational area:            1012.901753
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:                  7840.307482
```

- Convolution with pipeline

  Synthesis with clock cycle = 1ns

  Critical Path

Point	Incr	Path	
clock clk (rise edge)	0.00	0.00	
clock network delay (ideal)	0.00	0.00	
weigts3_reg[1]/CLK (ASYNC_DFFHx1_ASAP7_75t_R)	0.00	0.00	r
weigts3_reg[1]/QN (ASYNC_DFFHx1_ASAP7_75t_R)	46.43	46.43	f
U2320/Y (BUFx5_ASAP7_75t_R)	26.99	73.42	f
U2311/Y (INVx4_ASAP7_75t_R)	8.30	81.72	r
U2978/Y (NAND2xp33_ASAP7_75t_R)	12.71	94.44	f
U6080/Y (NOR3xp33_ASAP7_75t_R)	44.84	139.28	r
mult_x_3/U108/SN (FAx1_ASAP7_75t_R)	77.73	217.01	f
mult_x_3/U105/CON (FAx1_ASAP7_75t_R)	39.33	256.34	r
mult_x_3/U105/SN (FAx1_ASAP7_75t_R)	24.88	281.22	f
mult_x_3/U104/CON (FAx1_ASAP7_75t_R)	45.37	326.59	r
mult_x_3/U104/SN (FAx1_ASAP7_75t_R)	26.30	352.89	f
U5246/SN (HAxp5_ASAP7_75t_R)	45.43	398.31	f
U3753/Y (NOR2xp33_ASAP7_75t_R)	14.15	412.46	r
U5412/Y (NOR2xp33_ASAP7_75t_R)	39.63	452.09	f
U3761/Y (MAJIxp5_ASAP7_75t_R)	32.04	484.13	r
U5489/SN (HAxp5_ASAP7_75t_R)	37.30	521.43	r
U3104/Y (NAND2xp33_ASAP7_75t_R)	12.31	533.74	f
U3103/Y (NAND2xp33_ASAP7_75t_R)	33.00	566.74	r
U5707/Y (MAJIxp5_ASAP7_75t_R)	30.02	596.75	f
U5708/Y (MAJIxp5_ASAP7_75t_R)	29.18	625.94	r
U3196/Y (NAND2xp33_ASAP7_75t_R)	12.57	638.51	f
U4453/Y (NAND2xp33_ASAP7_75t_R)	31.99	670.49	r
U5927/SN (HAxp5_ASAP7_75t_R)	34.84	705.33	r
U5928/SN (HAxp5_ASAP7_75t_R)	22.86	728.18	r
U4017/Y (NAND2xp33_ASAP7_75t_R)	10.92	739.11	f
U3466/Y (NAND2xp33_ASAP7_75t_R)	22.62	761.73	r
pps1_3_reg[14]/D (ASYNC_DFFHx1_ASAP7_75t_R)	0.00	761.73	r
data arrival time		761.73	

  Timing Report

clock clk (rise edge)	1000.00	1000.00	
clock network delay (ideal)	0.00	1000.00	
pps1_3_reg[14]/CLK (ASYNC_DFFHx1_ASAP7_75t_R)	0.00	1000.00	r
library setup time	-19.51	980.49	
data required time		980.49	
data required time		980.49	
data arrival time		-761.73	
slack (MET)		218.76	

Area

```
Number of ports:                          170
Number of nets:                          5726
Number of cells:                         5264
Number of combinational cells:           4781
Number of sequential cells:               483
Number of macros/black boxes:               0
Number of buf/inv:                       1148
Number of references:                      41

Combinational area:               6910.919949
Buf/Inv area:                     1980.547161
Noncombinational area:            2929.530221
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:                  9840.450170
Total area:                 undefined
```

Synthesis with clock cycle = 0.75ns

Critical Path:

Point	Incr	Path
clock clk (rise edge)	0.00	0.00
clock network delay (ideal)	0.00	0.00
pps3_1_reg[0]/CLK (ASYNC_DFFHx1_ASAP7_75t_R)	0.00	0.00 r
pps3_1_reg[0]/QN (ASYNC_DFFHx1_ASAP7_75t_R)	56.37	56.37 r
U4802/Y (NOR2xp33_ASAP7_75t_R)	42.78	99.15 f
U4809/Y (MAJIxp5_ASAP7_75t_R)	35.56	134.70 r
U4524/Y (NAND2xp33_ASAP7_75t_R)	14.29	148.99 f
U3151/Y (NAND2xp33_ASAP7_75t_R)	23.73	172.73 r
U3276/Y (NAND2xp33_ASAP7_75t_R)	14.12	186.84 f
U3274/Y (NAND2xp33_ASAP7_75t_R)	23.66	210.50 r
U3154/Y (NAND2xp33_ASAP7_75t_R)	14.12	224.62 f
U3152/Y (NAND2xp33_ASAP7_75t_R)	23.66	248.28 r
U2947/Y (NAND2xp33_ASAP7_75t_R)	16.41	264.70 f
U5065/Y (NAND2xp5_ASAP7_75t_R)	16.18	280.88 r
U3156/Y (NAND2xp33_ASAP7_75t_R)	11.30	292.18 f
U4543/Y (NAND2xp33_ASAP7_75t_R)	29.99	322.17 r
U5066/Y (MAJx2_ASAP7_75t_R)	31.79	353.96 r
U3159/Y (NAND2xp33_ASAP7_75t_R)	9.17	363.13 f
U3157/Y (NAND2xp33_ASAP7_75t_R)	22.62	385.74 r
U3279/Y (NAND2xp33_ASAP7_75t_R)	14.12	399.86 f
U3277/Y (NAND2xp33_ASAP7_75t_R)	23.66	423.52 r
U3161/Y (NAND2xp33_ASAP7_75t_R)	14.12	437.64 f
U3160/Y (NAND2xp33_ASAP7_75t_R)	23.66	461.30 r
U3164/Y (NAND2xp33_ASAP7_75t_R)	14.12	475.42 f
U3162/Y (NAND2xp33_ASAP7_75t_R)	23.66	499.08 r
U2948/Y (NAND2xp33_ASAP7_75t_R)	16.42	515.50 f
U5608/Y (NAND2xp5_ASAP7_75t_R)	16.18	531.68 r
U3166/Y (NAND2xp33_ASAP7_75t_R)	11.30	542.98 f
U4544/Y (NAND2xp33_ASAP7_75t_R)	29.99	572.97 r
U5747/Y (MAJx2_ASAP7_75t_R)	31.79	604.76 r
U3169/Y (NAND2xp33_ASAP7_75t_R)	9.17	613.93 f
U3167/Y (NAND2xp33_ASAP7_75t_R)	30.00	643.93 r
U5902/Y (MAJIxp5_ASAP7_75t_R)	29.58	673.51 f
U3822/Y (MAJx2_ASAP7_75t_R)	33.39	706.90 f
U4140/Y (NAND2xp33_ASAP7_75t_R)	10.56	717.46 r
U4002/Y (NAND2xp33_ASAP7_75t_R)	14.17	731.64 f
pps4_1_reg[18]/D (ASYNC_DFFHx1_ASAP7_75t_R)	0.00	731.64 f
data arrival time		731.64

Timing Report:

```
clock clk (rise edge)                                  750.00     750.00
clock network delay (ideal)                              0.00     750.00
pps4_1_reg[18]/CLK (ASYNC_DFFHx1_ASAP7_75t_R)            0.00     750.00 r
library setup time                                     -16.70     733.30
data required time                                                733.30
---------------------------------------------------------------------------
data required time                                                733.30
data arrival time                                                -731.64
---------------------------------------------------------------------------
slack (MET)                                                         1.66
```

Area:

```
Number of ports:                          170
Number of nets:                          5740
Number of cells:                         5278
Number of combinational cells:           4795
Number of sequential cells:               483
Number of macros/black boxes:               0
Number of buf/inv:                       1162
Number of references:                      42

Combinational area:               6953.610189
Buf/Inv area:                     2017.638681
Noncombinational area:            2929.530221
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:                  9883.140410
Total area:                 undefined
```

Synthesis with clock cycle = 0.4ns

Critical Path

```
Point                                                   Incr       Path
---------------------------------------------------------------------------
clock clk (rise edge)                                   0.00       0.00
clock network delay (ideal)                             0.00       0.00
In_5_reg[3]/CLK (ASYNC_DFFHx1_ASAP7_75t_R)              0.00       0.00 r
In_5_reg[3]/QN (ASYNC_DFFHx1_ASAP7_75t_R)              46.43      46.43 f
U2638/Y (BUFx5_ASAP7_75t_R)                            30.30      76.73 f
U2521/Y (NOR2xp33_ASAP7_75t_R)                         30.51     107.24 r
U3294/Y (XOR2x2_ASAP7_75t_R)                           35.44     142.68 f
U2681/Y (XOR2xp5_ASAP7_75t_R)                          21.47     164.15 f
U5681/Y (XNOR2xp5_ASAP7_75t_R)                         29.49     193.64 f
U2666/Y (XNOR2x1_ASAP7_75t_R)                          29.64     223.28 f
U2742/Y (XOR2x2_ASAP7_75t_R)                           40.63     263.91 r
U2340/Y (NOR2xp33_ASAP7_75t_R)                         13.91     277.82 f
U5115/Y (NAND2xp5_ASAP7_75t_R)                         11.00     288.81 r
U3399/Y (NAND2xp5_ASAP7_75t_R)                         14.01     302.83 f
U3048/Y (OR2x6_ASAP7_75t_R)                            31.81     334.64 f
U5816/Y (NAND3xp33_ASAP7_75t_R)                        11.56     346.20 r
U5815/Y (NAND4xp25_ASAP7_75t_R)                        16.46     362.66 f
U6809/Y (NAND2xp5_ASAP7_75t_R)                         18.96     381.61 r
pps1_5_reg[12]/D (ASYNC_DFFHx1_ASAP7_75t_R)             0.00     381.61 r
data arrival time                                                381.61
```

Timing Report

```
clock clk (rise edge)                                  400.00     400.00
clock network delay (ideal)                              0.00     400.00
pps1_5_reg[12]/CLK (ASYNC_DFFHx1_ASAP7_75t_R)            0.00     400.00 r
library setup time                                     -18.08     381.92
data required time                                                381.92
-------------------------------------------------------------------------
data required time                                                381.92
data arrival time                                                -381.61
-------------------------------------------------------------------------
slack (MET)                                                         0.31
```

Area

```
Number of ports:                          170
Number of nets:                          7717
Number of cells:                         7516
Number of combinational cells:           7033
Number of sequential cells:               483
Number of macros/black boxes:               0
Number of buf/inv:                       1253
Number of references:                      58

Combinational area:               9134.078420
Buf/Inv area:                     1462.665607
Noncombinational area:            2929.530221
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:                 12063.608641
Total area:                 undefined
```

Clock period / Design	1000ps	750ps	400ps
3x3 without pipeline Convolution	Cell Area=4831.228754 Critical path=966.12ps Slack=15.5ps	Cell Area=5447.787792 Critical path=734.4ps Slack=0.16ps	Cell Area=7840.307482 Critical path=591.83 Slack=-208.17
3x3 pipeline Convolution	Cell Area=9840.45017 Critical path=761.73ps Slack=218.76ps	Cell Area=9883.140410 Critical path=731.64ps Slack=1.66ps	Cell Area=12063.608641 Critical path=381.61 Slack=0.31

Final Discussion:

From the diagram above, the cell area of the pipeline design is two time larger than the non-pipeline design. The reason is that, it contains more registers in order to store the states of the circuit. Those pipeline registers will largely increase its cell area. However, operating under high clock frequency, the merit of pipeline design shows up. It has a shorter critical path so that it can work successfully without getting a negative slack and having a greater throughput.

Comparing to the same design different clock cycle, we can see whenever the clock period grows, the area of the cell will increase. After I took a close observation to the changes of critical path and our cell library, I found out that this issue is strongly related to our synthesis tool and time constraint. When the clock frequency increase, we tighten the time constraint. Simultaneously, the synthesis tool will automatically pick the bigger cell, for example changing NOR2xp33(#14.63ps) to NOR2xp67(#11.95ps), which can take larger current and voltage from our cell library to speedup the circuit fulfilling the time constraint. On the contrary, when we slow down the clock frequency, which means to release the time constraint, synthesis tool will look for the smaller but slower cell to compose our circuit.