Digital IC Design Report

Exercise 5: SRAM Model in Verilog

Professor: Po-Tsang Huang

Student/ID: 尤彥捷/310591036

Ex5-1: 512x32 SRAM Module

In this exercise, we have to design a 512*32 SRAM module in Verilog based on the following I/O description (Figure1.) and timing specification (Figure 2.) .

Input	Description
clk	Clock signal
CEN	CEN = 0 (enable) CEN = 1 (disable)
WEN	WEN = 0 (Write operation) WEN = 1 (Read operation)
Din[31:0]	Data input
Addr[8:0]	Address
Output	**Description**
Dout[31:0]	Data output

Figure 1. I/O description of SRAM module

Maximum Frequency	2GHz
Read latency	450ps
Setup time of Input	20ps
Hold time of input	20ps

Figure 2. Timing Spec. of SRAM module

❖ Simulation & Function Verification

✓ SRAM Function & Read Latency

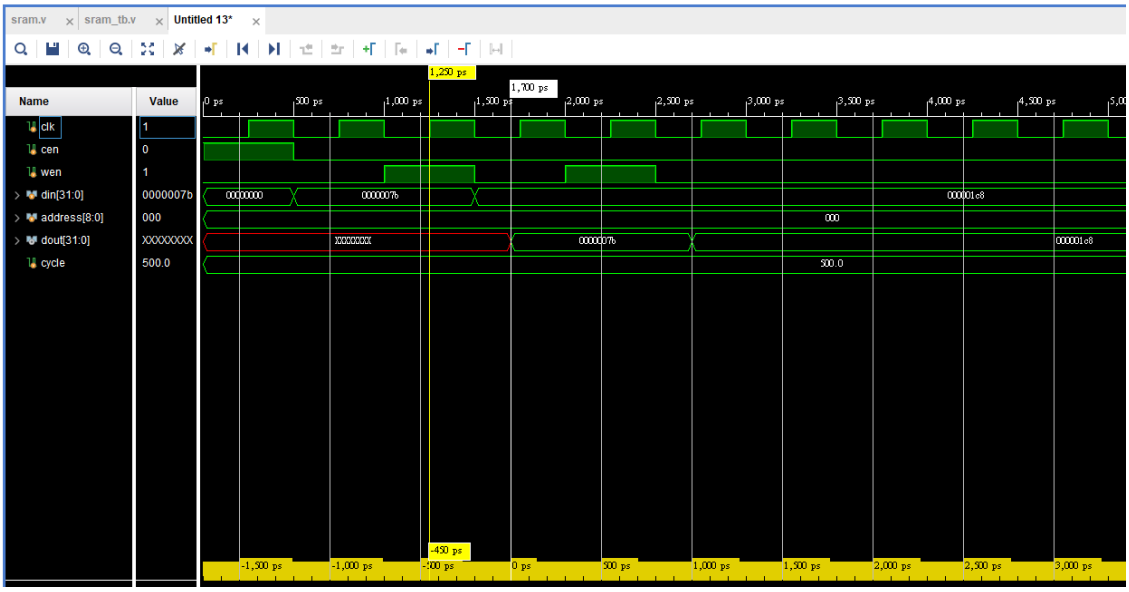

Figure 3. The regular SRAM function test. The read command operate at 1,250ps and the dout register received it after 450ps read latency

✓ Maximum Frequency Test

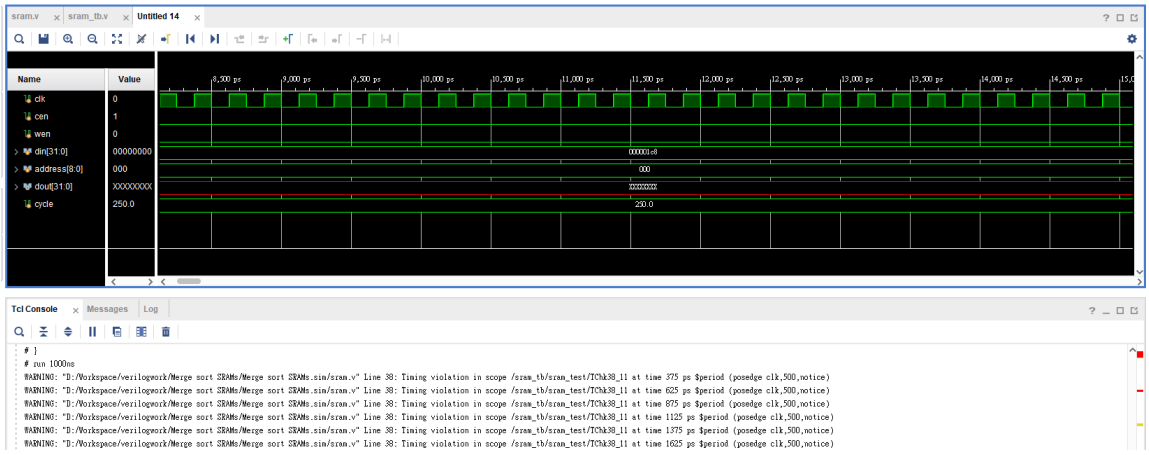

Figure 4. To adjust period to 250ps, system pops up warning and dout register goes to unknown

✓ Setup time & Hold time Test

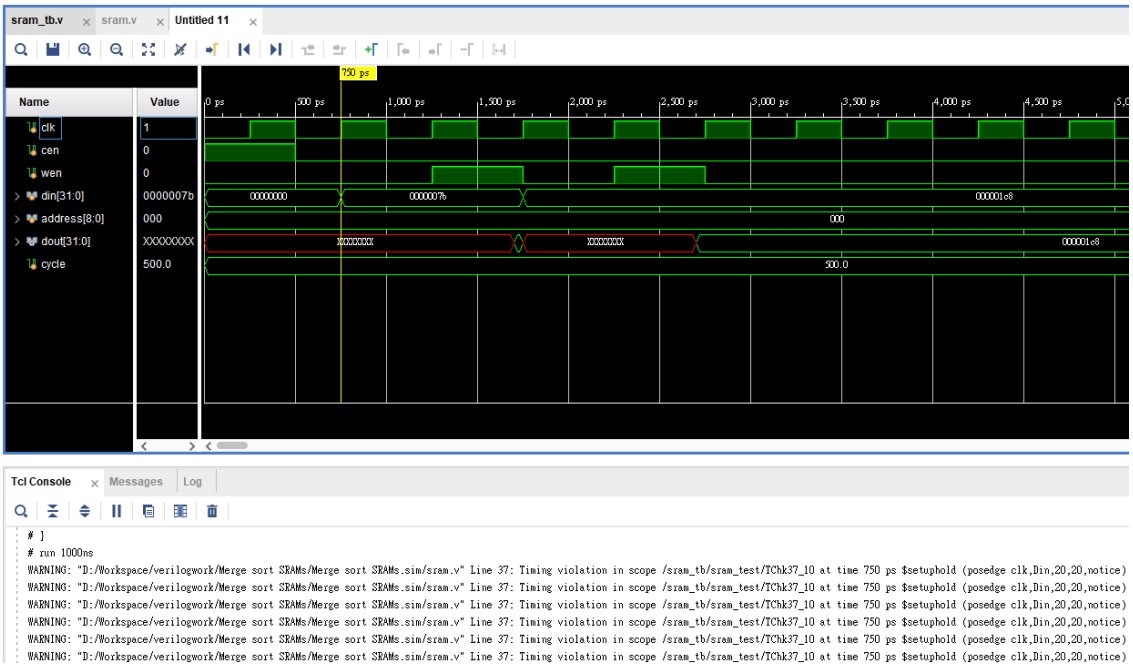

Figure 5. Setup time test, the data come in right on the positive edge of clock. It should come in 20ps earlier. System pops up warning message and set output to unknown.

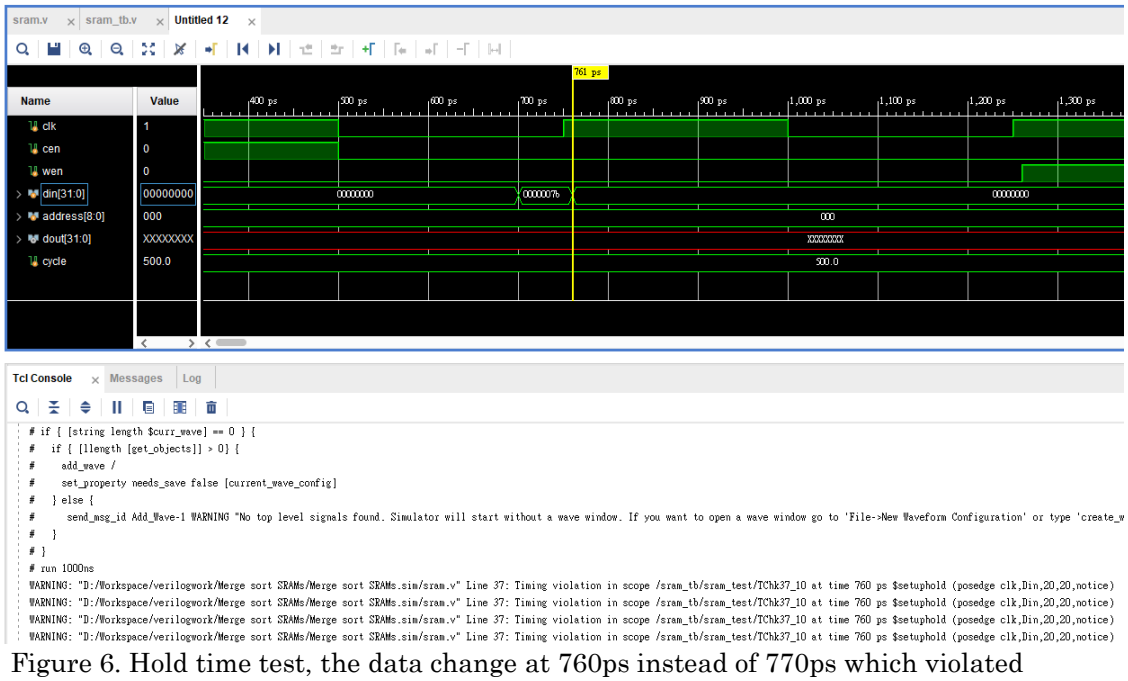

Figure 6. Hold time test, the data change at 760ps instead of 770ps which violated the spec. of hold time. System pops up warning message and set output to unknown.

Ex5-2: Merge Sort with two 512x32 SRAMs

❖ Finite State Machines

I use two FSMs to handle the sram and merge sort algorithm respectively.

FSM(cstate, nstate)

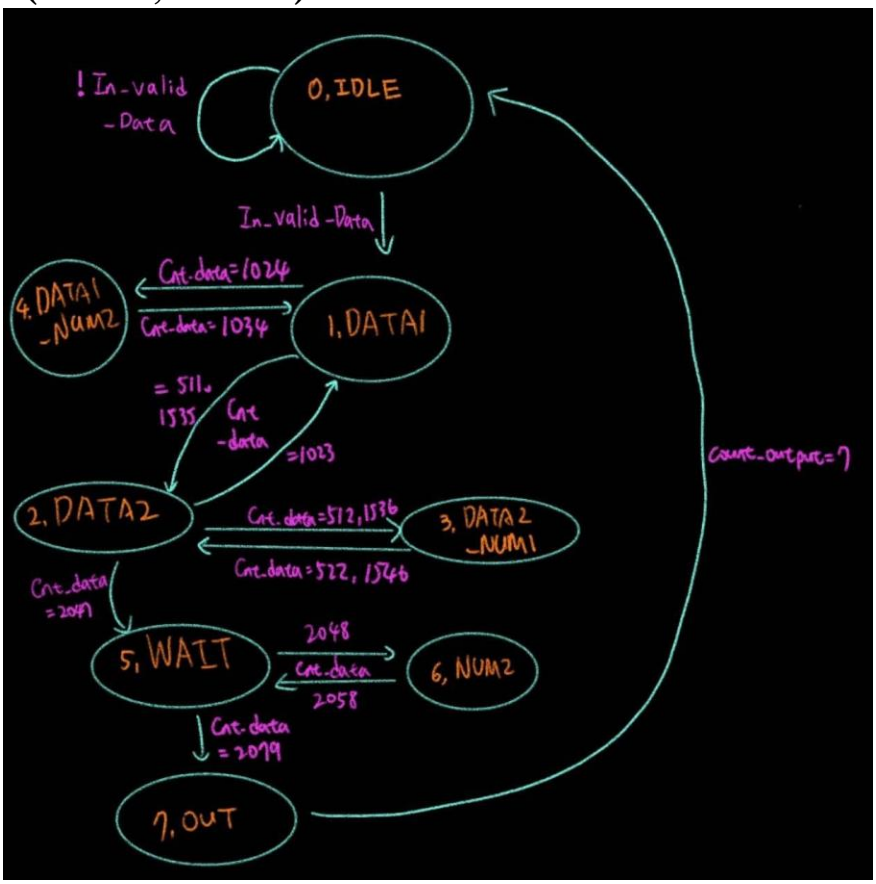

Figure 7. FSM state diagram for handling SRAM

FSM(nstate_sort, cstate_sort)

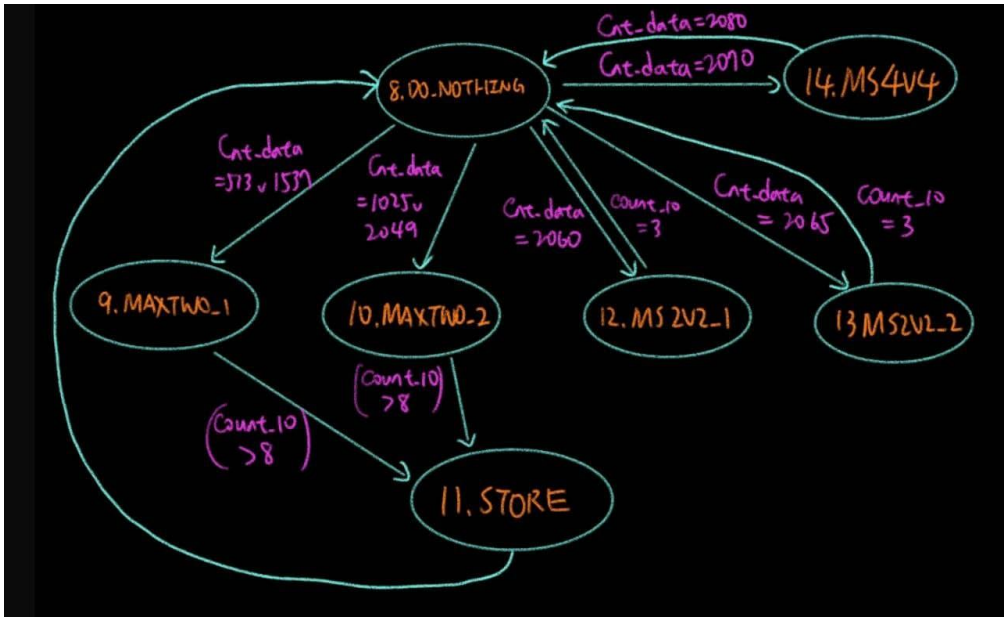

Figure 8. FSM for handling merge sorts

❖ Behavior Simulation

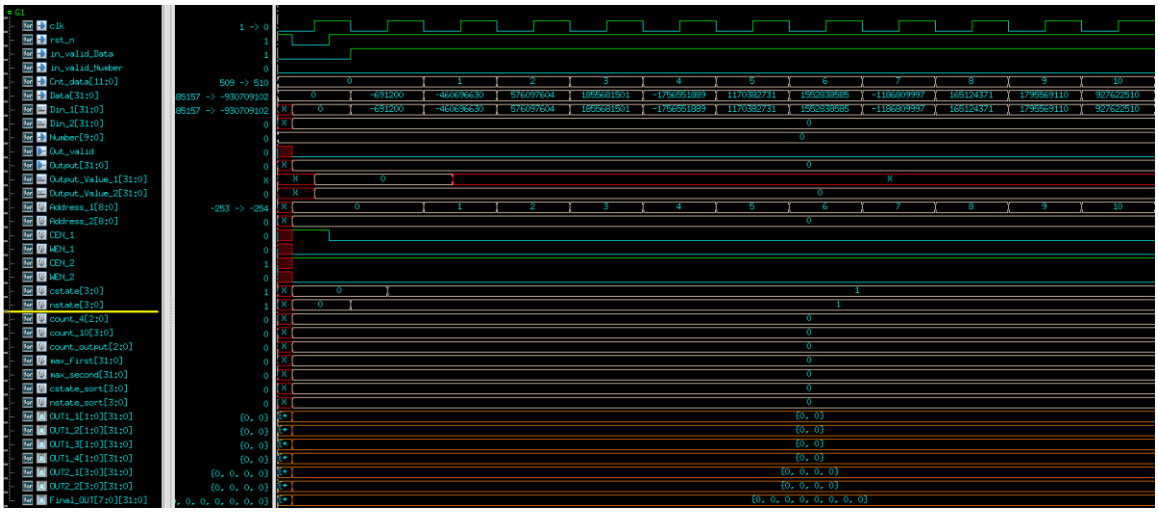

Figure 9. Start of the behavior simulation.

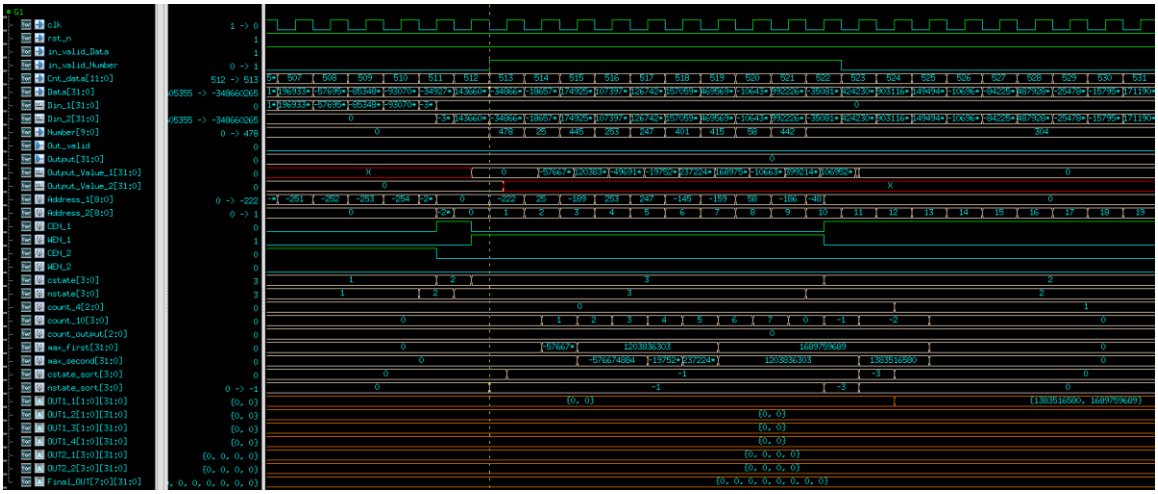

Figure 10. When Cnt_data = 513, Invalid_Number = 1, SRAM1 starts to output ten data based on the random address.

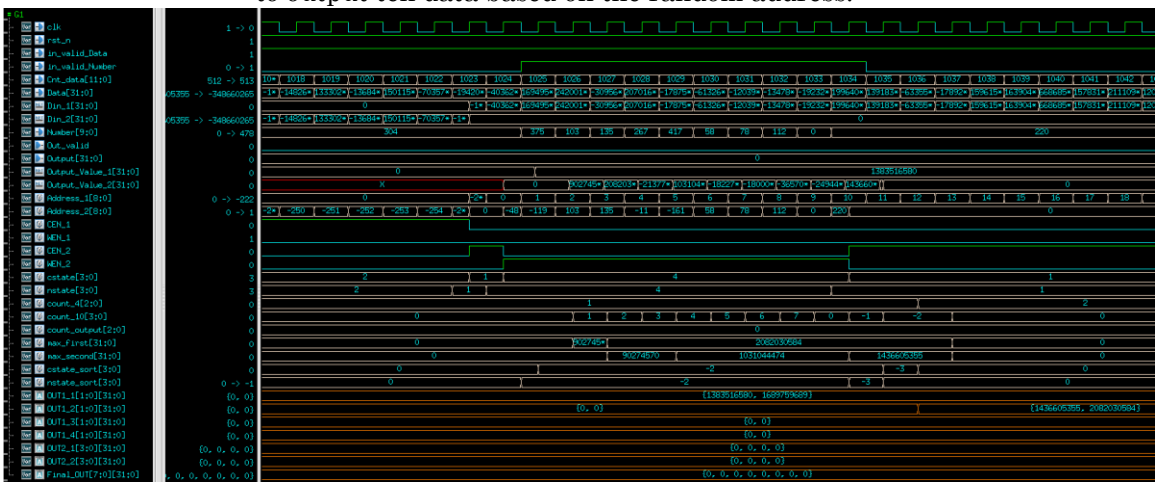

Figure 11. When Cnt_data = 1025, Invalid_Number = 1, SRAM2 starts to output ten data based on the random address.

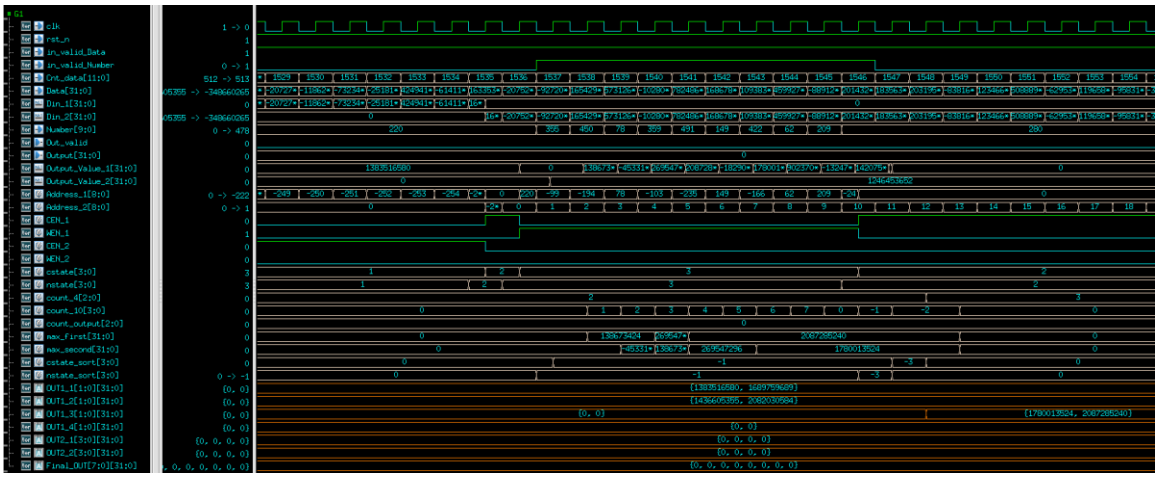

Figure 12. When Cnt_data = 1537, Invalid_Number = 1, SRAM1 starts to output ten data based on the random address.

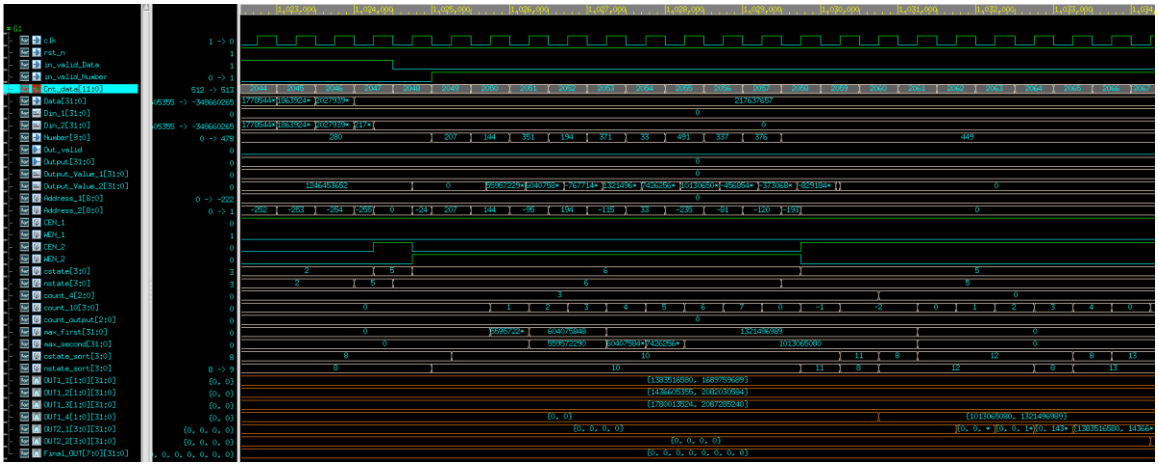

Figure 13. When Cnt_data = 2049, Invalid_Number = 1, SRAM2 starts to output ten data based on the random address.

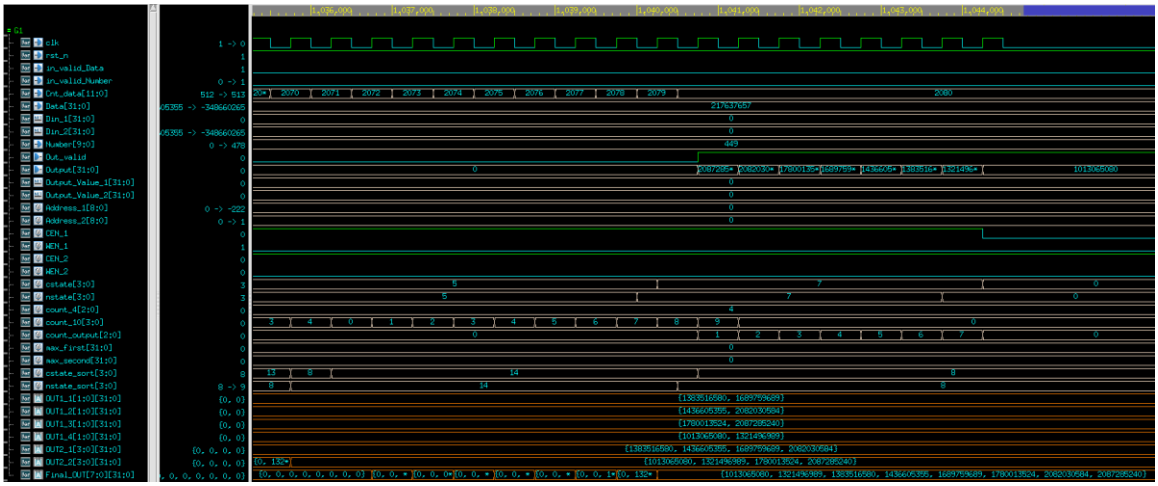

Figure 14. After cstate_sort = 14, it convert to merge sort state. It will use merge sort algorithm to put data into a [7:0] arrays from big to small.

❖ Synthesis

Clock period = 500ps

Timing Report

```
Point                                                   Incr       Path
--------------------------------------------------------------------------
clock clk (rise edge)                                   0.00       0.00
clock network delay (ideal)                             0.00       0.00
i_reg_0_/CLK (ASYNC_DFFHx1_ASAP7_75t_R)                 0.00       0.00 r
i_reg_0_/QN (ASYNC_DFFHx1_ASAP7_75t_R)                 50.25      50.25 r
U5548/Y (BUFx8_ASAP7_75t_R)                            27.54      77.79 r
U5554/Y (INVx11_ASAP7_75t_R)                           13.49      91.28 f
U5551/Y (INVx11_ASAP7_75t_R)                           16.37     107.65 r
U5543/Y (OR2x2_ASAP7_75t_R)                            44.65     152.30 r
U9664/Y (NOR2xp33_ASAP7_75t_R)                         24.18     176.48 f
U9665/Y (OR4x2_ASAP7_75t_R)                            44.69     221.16 f
U6940/Y (NOR2xp33_ASAP7_75t_R)                         18.17     239.33 r
U7455/Y (OR2x2_ASAP7_75t_R)                            20.78     260.11 r
U6816/Y (NAND2xp33_ASAP7_75t_R)                         9.35     269.46 f
U8153/Y (NAND2xp5_ASAP7_75t_R)                         10.65     280.11 r
U7806/Y (AND3x1_ASAP7_75t_R)                           21.09     301.20 r
U5370/Y (NOR2xp33_ASAP7_75t_R)                         11.21     312.41 f
U5368/Y (NOR3xp33_ASAP7_75t_R)                         16.03     328.44 r
U5362/Y (AND2x2_ASAP7_75t_R)                           32.29     360.73 r
U5354/Y (NAND2xp5_ASAP7_75t_R)                         14.89     375.62 f
U6707/Y (NOR2xp33_ASAP7_75t_R)                         24.85     400.48 r
U10570/Y (NAND2xp33_ASAP7_75t_R)                       15.96     416.44 f
U10572/Y (AND2x2_ASAP7_75t_R)                          29.04     445.48 f
U9247/Y (OR2x2_ASAP7_75t_R)                            22.80     468.28 f
U6855/Y (NAND2xp33_ASAP7_75t_R)                        13.26     481.54 r
Final_OUT_reg_6__17_/D (ASYNC_DFFHx1_ASAP7_75t_R)       0.00     481.54 r
data arrival time                                                481.54

clock clk (rise edge)                                 500.00     500.00
clock network delay (ideal)                             0.00     500.00
Final_OUT_reg_6__17_/CLK (ASYNC_DFFHx1_ASAP7_75t_R)     0.00     500.00 r
library setup time                                    -18.32     481.68
data required time                                               481.68
--------------------------------------------------------------------------
data required time                                               481.68
data arrival time                                               -481.54
--------------------------------------------------------------------------
slack (MET)                                                        0.14
```

Area Report

```
****************************************
Report : area
Design : MS_310591036
Version: P-2019.03
Date   : Fri Jan 14 15:40:09 2022
****************************************

Library(s) Used:

    asap7sc7p5t_SIMPLE_RVT_TT_08302018 (File: /disk2/others/dsd_310591036/DIC_hw/NLDM/asap7sc7p5t_SIMPLE_RVT_TT_08302018.db)
    asap7sc7p5t_INVBUF_RVT_TT_08302018 (File: /disk2/others/dsd_310591036/DIC_hw/NLDM/asap7sc7p5t_INVBUF_RVT_TT_08302018.db)
    asap7sc7p5t_SEQ_RVT_TT_08302018 (File: /disk2/others/dsd_310591036/DIC_hw/NLDM/asap7sc7p5t_SEQ_RVT_TT_08302018.db)

Number of ports:                         91
Number of nets:                        8812
Number of cells:                       8694
Number of combinational cells:         7720
Number of sequential cells:             974
Number of macros/black boxes:             0
Number of buf/inv:                     1793
Number of references:                    51

Combinational area:              10283.682208
Buf/Inv area:                     3611.874141
Noncombinational area:            5674.769254
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:                 15958.451463
Total area:                 undefined
```

Total Cell Area = 15958.451463

Latency: measure from (Cnt_data = 2057 -> 2058) to (out_valid = 1 -> 0) = 15,320 ps

Performance

Performance = 15958.451463 * 15.320 ns = **244,483.47641316**