BMI System using an Adder Circuit, Decoder Circuit, Encoder Circuit, Register Circuit, and a Counter Circuit

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**ABSTRACT**

**Applying the topics learned in the course *Logic Circuits and Design Laboratory*, we are to design a system that would display a BMI counter. The system will contain the following circuits: Adder, Decoder, Encoder, Register, and a Counter. All these circuits will be connected to each other to display the user's BMI through the 7-Segment Display. Since the system only accepts binary inputs, it can be complicated to translate the binary output into decimal value. The Counter and the Register are the circuits that are critical in this design since these circuits control the binary value that will be translated and displayed to the 7-Segment Display. The system will only work if the sensor input values are either greater than or equal to the threshold input values, if the threshold values are equal however, then there will be no change in the BMI counter.**

**INDEX TERMS**

**Body Mass Index (BMI), Parallel Input Parallel Output (PIPO) Shift Register, Serial Input Parallel Output (SIPO) Shift Register, Encoder, Decoder**

1. **INTRODUCTION\***

Monitoring body fat helps in identifying the risk factors a person can have. A person can identify the status of the health of their bodies by using Body Mass Index (BMI). It is a metric for defining anthropometric height/weight characteristics in adults and categorizing them into groups. Using Body Mass Index (BMI) to predict the physical health of a person can have positive impact on the person's life as it gives the person an idea of the status of their body and their health [1]. In this project, we aim to design a system that will show the user their Body Mass Index. This project will use

1. **SYSTEM DESIGN\***

The Body Mass Index System was constructed using the circuit simulation *Logisim.* Fig. 1 shows the circuit layout for the 180 Counter (Fig. 1A), Parallel Input Parallel Output Shift Register (Fig. 1B), and Serial Input Parallel Output Shift Register (Fig. 1C) respectively.

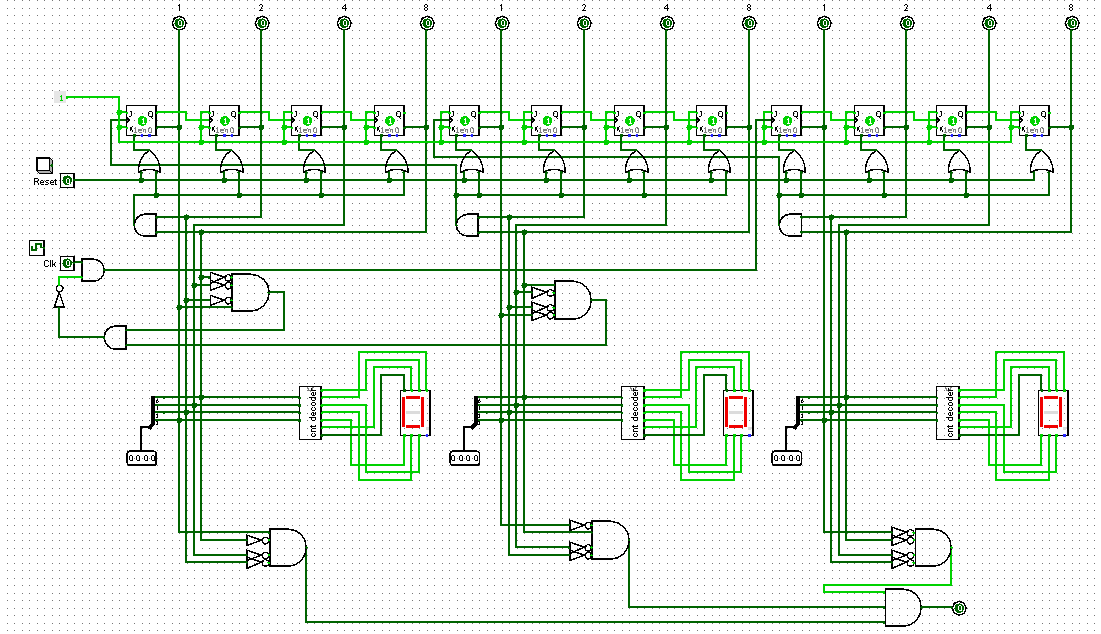


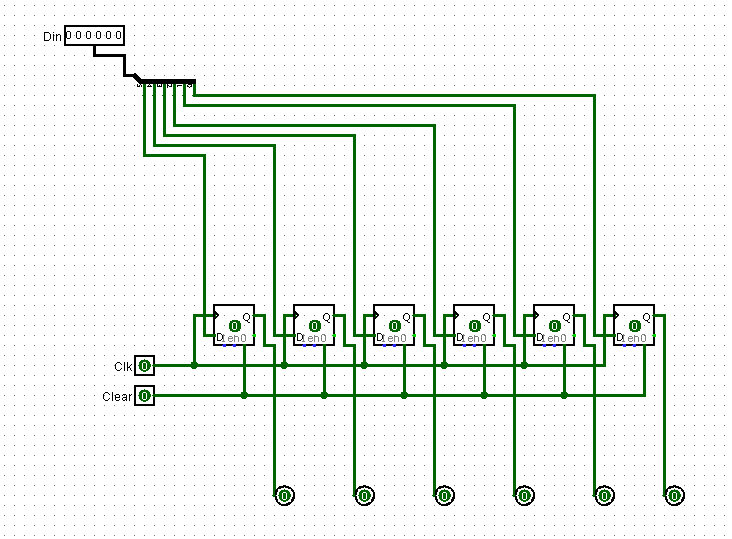
Fig. 1A. 180 Counter Circuit using J-K Flip Flops, OR Gate, AND gate, and NOT Gate with 4-Bits Pin for the output, Reset Input and a Clock Input.   


Fig. 1B. Parallel Input Parallel Output Shift Register using

D - Flip Flops with 5-Bit Data Input Pin, 5-Bit Output connected parallel to the D - Flip Flop, a Clock Input and a Clear Input.

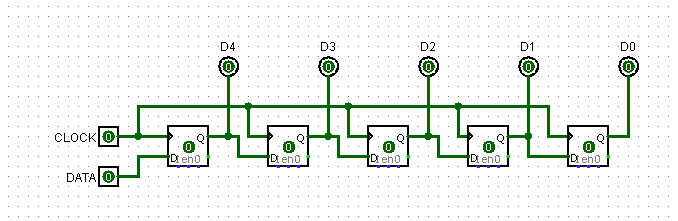


Fig. 1C. Serial Input Parallel Output Shift Register using D -Flip Flops with one Data Input Pin, a Clock Input, and 5-Bit Output connected parallel to the D - Flip Flop.

1. **SYSTEM SETUP\***

Initially, the system was designed separately with one design that requires only the Adder and Decoder Circuit and the other incorporated the Register and Counter Circuit alongside the Adder and Decoder Circuits. The system design with the Adder and Decoder Circuits only were done at an ample of time since we were already introduced and familiar with the concept of how to build the following component circuits. Additionally, we were tasked to include another Register Circuit between the Sensor Input Pin and the Comparator Circuit. We also included a 5x1 Multiplexer Circuit in which the output of the Serial Input Parallel Output Shift Register will multiplex into one main output to inject into the input pin of the Comparator Circuit.

Fig. 2. shows the original Main Circuit with the Adder and Decoder Circuits only and input pins where the value/s to be computed inside the adder circuit is to be initiated by the user (Fig. 2A.) as well the Main Circuit where the Register and Counter Circuit are included in the overall system design (Fig. 2B.).

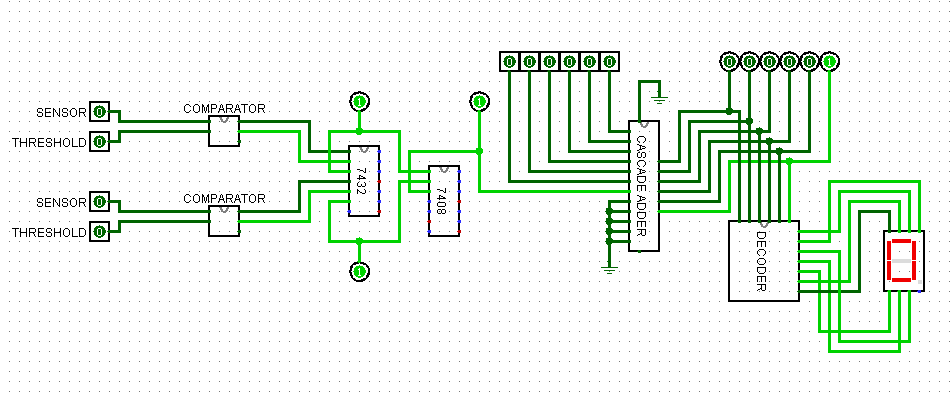


Fig. 2A. Original Main Circuit using a Cascaded Adder with 6-Bit Input Pins & 6-Bit Output and a Decoder Circuit.

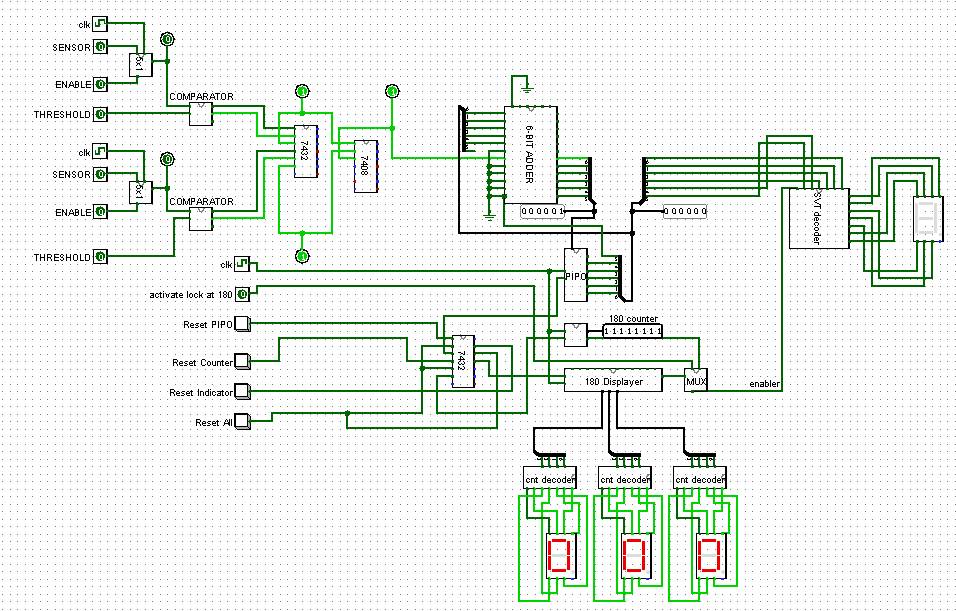


Fig. 2B. Main Circuit included with Serial Input Parallel Output Shift Register, Parallel Input Parallel Output Shift Register Circuit and 180 Counter

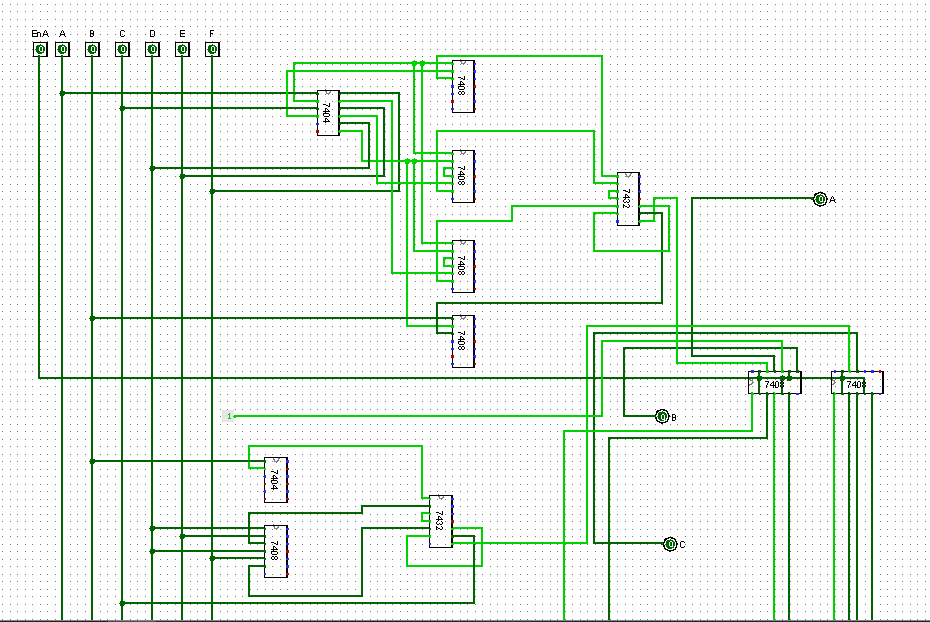
For the system design included the Register and Counter however it took quite a challenge since it solely rely on our own circuit diagram design idea nevertheless, we were able to design such a Component Circuit/s that were able to connect to the other circuits. To translate the binary values and display the severity, we were given a table for reference where in the severity will be determined based on the APNEA-HYPONEA INDEX (AHI) count (TABLE 1) which is the value stored inside the Register Circuit.

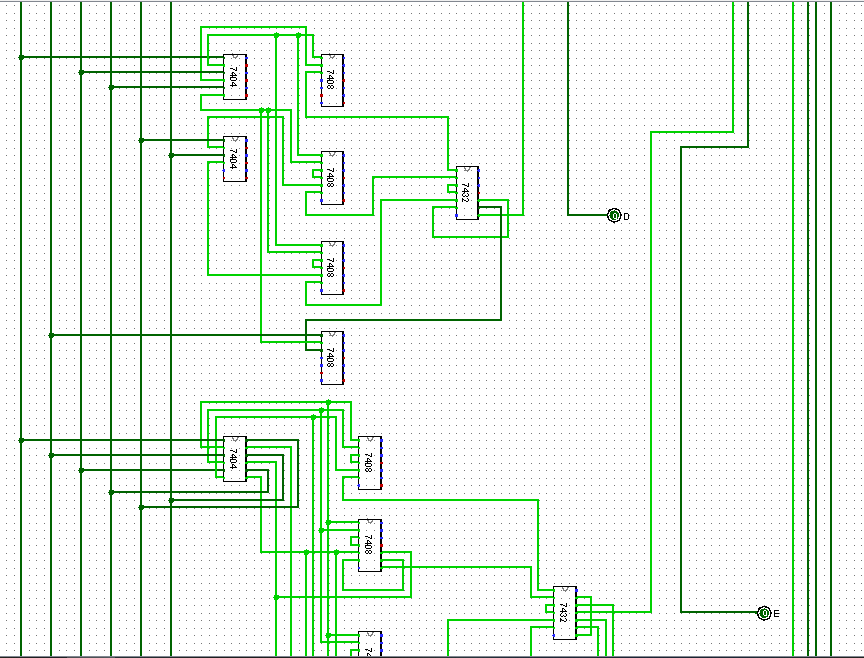
TABLE 1

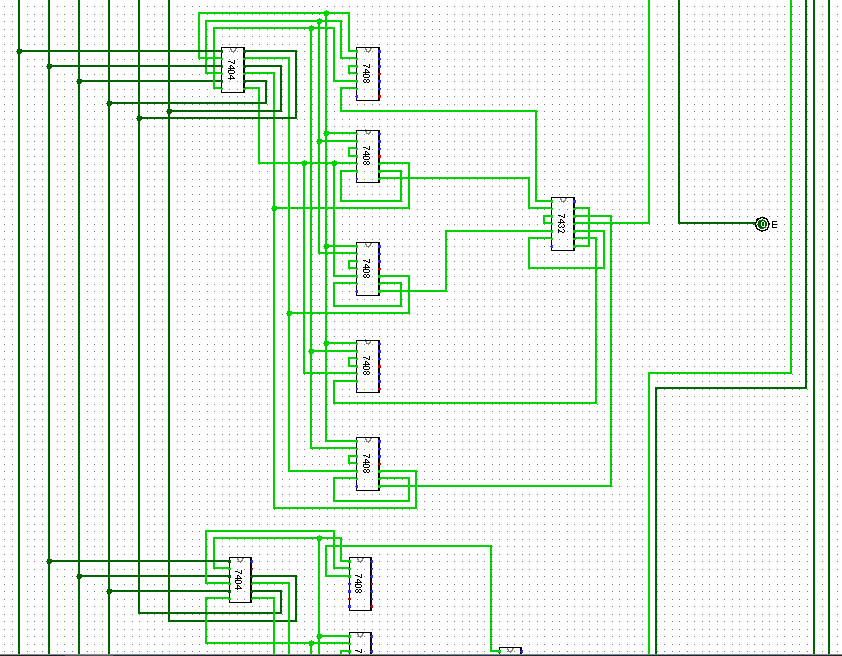
BODY MASS INDEX TABLE

|  |  |  |
| --- | --- | --- |
| **Meaning** | **Value** | **Output** |
| UNDERWEIGHT | 0-9 | 0 |
| FAIRLY NORMAL | 10-18 | A |
| NORMAL | 19-24 | B |
| OVERWEIGHT | 25-30 | C |
| OBESITY | 31 | D |

In Fig. 3. it shows each of the 7-Segment output are determined from the binary values generated by the 180 Counter and Parallel Input Parallel Output Shift Register.







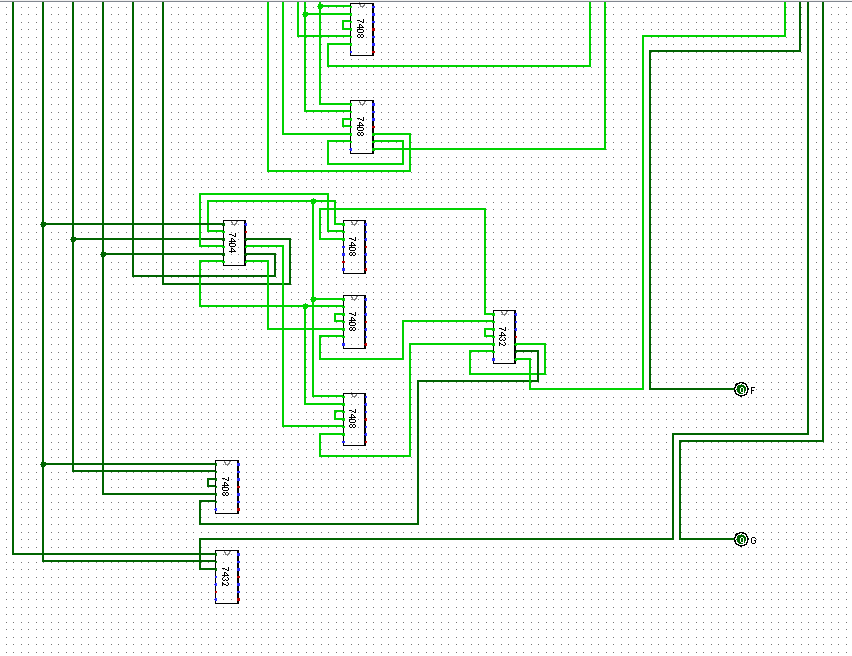


Fig 3. 6-Bit Decoder using IC 7404 (NOT Gate), IC 7408 (AND Gate), and an IC 7432 (OR Gate) with 7-Outputs.

In Fig. 4. it shows the Serial Input Parallel Output Shift Register connected to the built 5x1 Multiplexer Circuit using 2x1 Multiplexer Circuit (Fig. 4A) and the circuit design of the 2x1 Multiplexer used in both to design the 5x1 Multiplexer and to enable the 180 Counter Circuit (Fig. 4B).

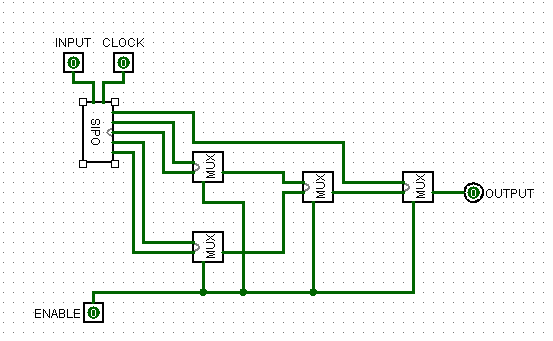


Fig. 4A. The output of the 5-Bit Serial Input Parallel Output Shift Register multiplexed in a 5x1 Multiplexer Circuit using 2x1 Multiplexer Circuits with an Input Pin, a Clock Pin, and an Enable Pin.

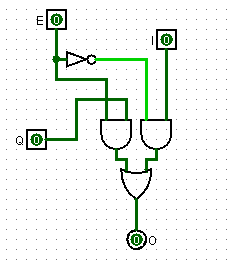


Fig. 4B. 2x1 Multiplexer Circuit with an Enabler Pin, Data Input Pins, and an Output Pin.

1. **SYSTEM RESULTS\***

Setting the sensor values equal to the threshold values, the sensor value would then be stored in the Shift Input Parallel Output Shift Register and to pass the value the Enable Pin must be on in order to transfer from in the Serial Input Parallel Output Shift Register and multiplexed in the 5x1 Multiplexer Circuit. Their values (Sensor and Threshold) would then be compared in the Comparator Circuit which would provide an output value of ‘1’ which would be our input value in the Adder Circuit. The output of the Adder Circuit will be passed on to the Parallel Input Parallel Output Shift Register where it’s clock is connected synchronously with the 180 Counter. The reason as to why the Register and Counter Circuit are synchronously connected is because the Counter Circuit needs to count up to 3 minutes or 180 hence the label “180 Counter”. After reaching the 180 count, then it will be allowed to output the severity in the 7-Segment Display. In TABLE 2 shows the truth table regarding the decoder for the 180 Counter in order for the user to monitor whether it has reached the specified count or not.

TABLE 2

180 COUNTER DECODER TRUTH TABLE

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| A | B | C | D | A2 | B2 | C2 | D2 | E | F | G |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 |
| 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 |

The purpose of the 180 Counter is to allow the 6-Bit Decoder to translate the binary value stored in the Parallel Input Parallel Output Shift Register to decimal value (Severity) according to the APNEA-HYPONEA INDEX (AHI) reference table (TABLE 1).

In Fig. 5. it shows how does the value of sensor and threshold input pins affect the severity output. When sensor values are equal to the threshold values, all of the component circuits are enabled.

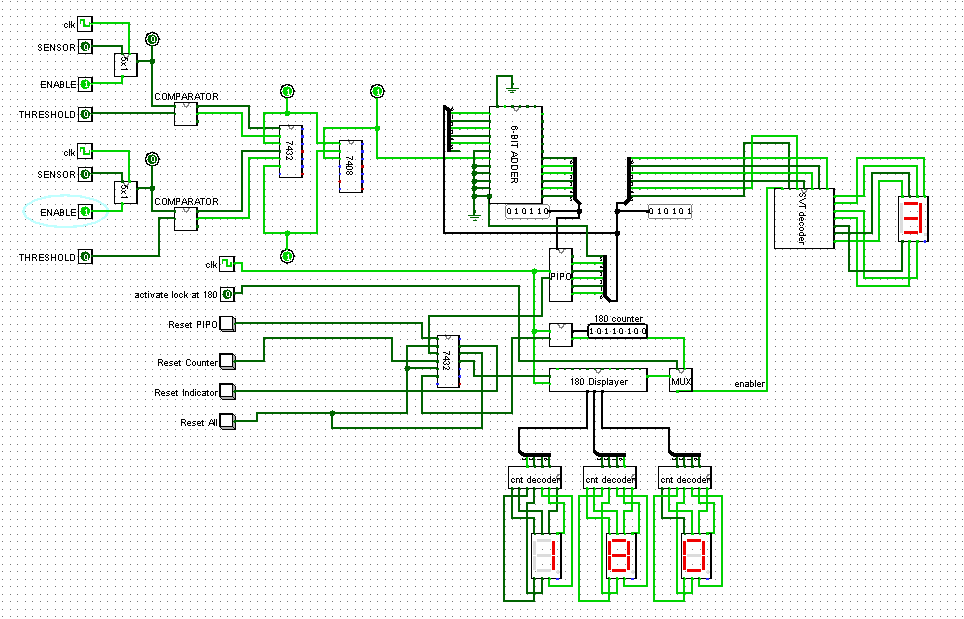


Fig. 5. Main Circuit with equal Sensor and Threshold Values

In Fig. 6. it shows when sensor values are not equal to the threshold values, some of the component circuits are disabled.

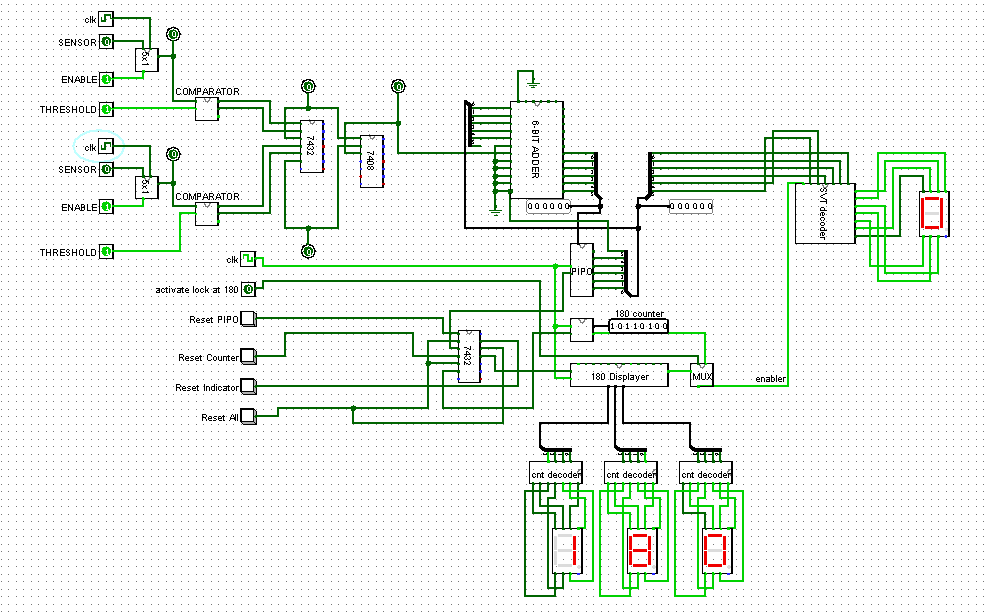


Fig. 6. Main Circuit with equal Threshold Values.

1. **CONCLUSION\***

This project shows that a Sleep Disorder Severity System using logic component circuits can provide an immediate and accurate result. The only flaw in this system is that when the sensor and threshold values do not match, the system wouldn’t work at all since some of the Component Circuits are disabled most especially the Adder Circuit where it’s binary output determines the APNEA-HYPONEA INDEX (AHI) Count.

**REFERENCES**

1. <https://www.ncbi.nlm.nih.gov/pmc/articles/PMC4890841/>