The Schematics have been analyzed from
a die picture by InfosecDJ.
The chip is identified as:

MSM OKi
79H041

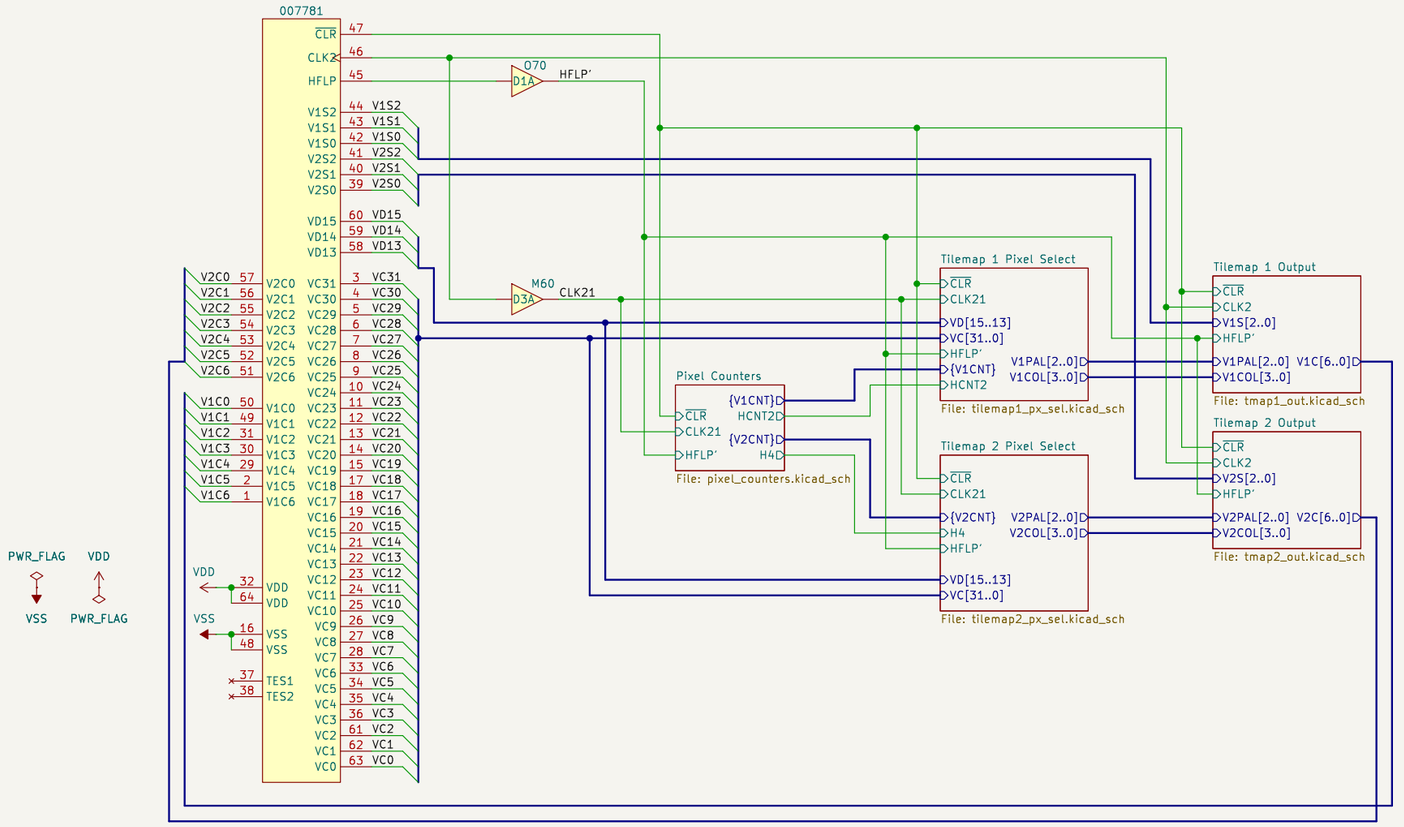
It is a MSM79V000 gate array
from the MSM70V000 series.
– 3289 Basic Cells
– 23 Columns, 143 Rows

The konami 007781 is a tilemap pixel shift register
with scroll. The tiles are 8x8 pixels, but the 007781
don't care about vertical line position. 007781 handles
two tilemaps at a time:
– V1, tilemap 1
– V2, tilemap 2

8 pixels, 4 bits each, of color data at a time are latched
into the registers. The palette code is latched 8 pixel
clocks earlier from VRAM. This is because the
data in the 007780 DRAM controller and DRAM takes 8
pixel clocks to process.

V1 latches pixels when the horizontal counter, going
from 0 to 7, goes to 2 (HCNT2) and V2 latches when
the horizontal counter goes to 4.
Data latched for:
– V1, when HCNT[2:0] == 2
– V2, when HCNT[2:0] == 4

The pixel code and palette color data are shifted
out between 1 to 9 pixel clocks after HCNT[2:0] == 4,
depending on if scroll or horizontal flip are active.

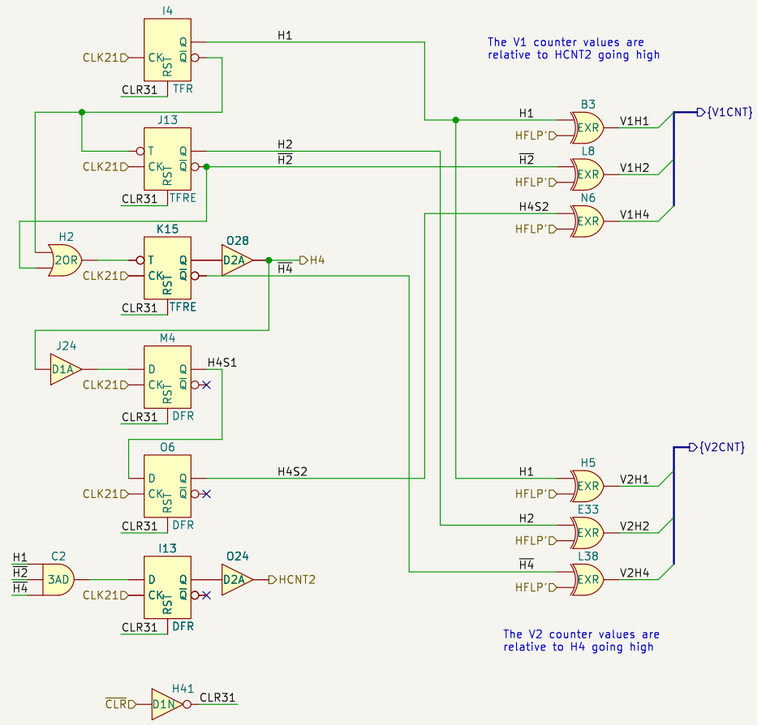


Ulf Skutnabba, twitter: @skutis77

Sheet: /
File: 007781.kicad_sch

Title: Konami 007781

Size: A3	Date: 2024-09-08	**Rev:**
KiCad E.D.A. 8.0.6		Id: 1/6



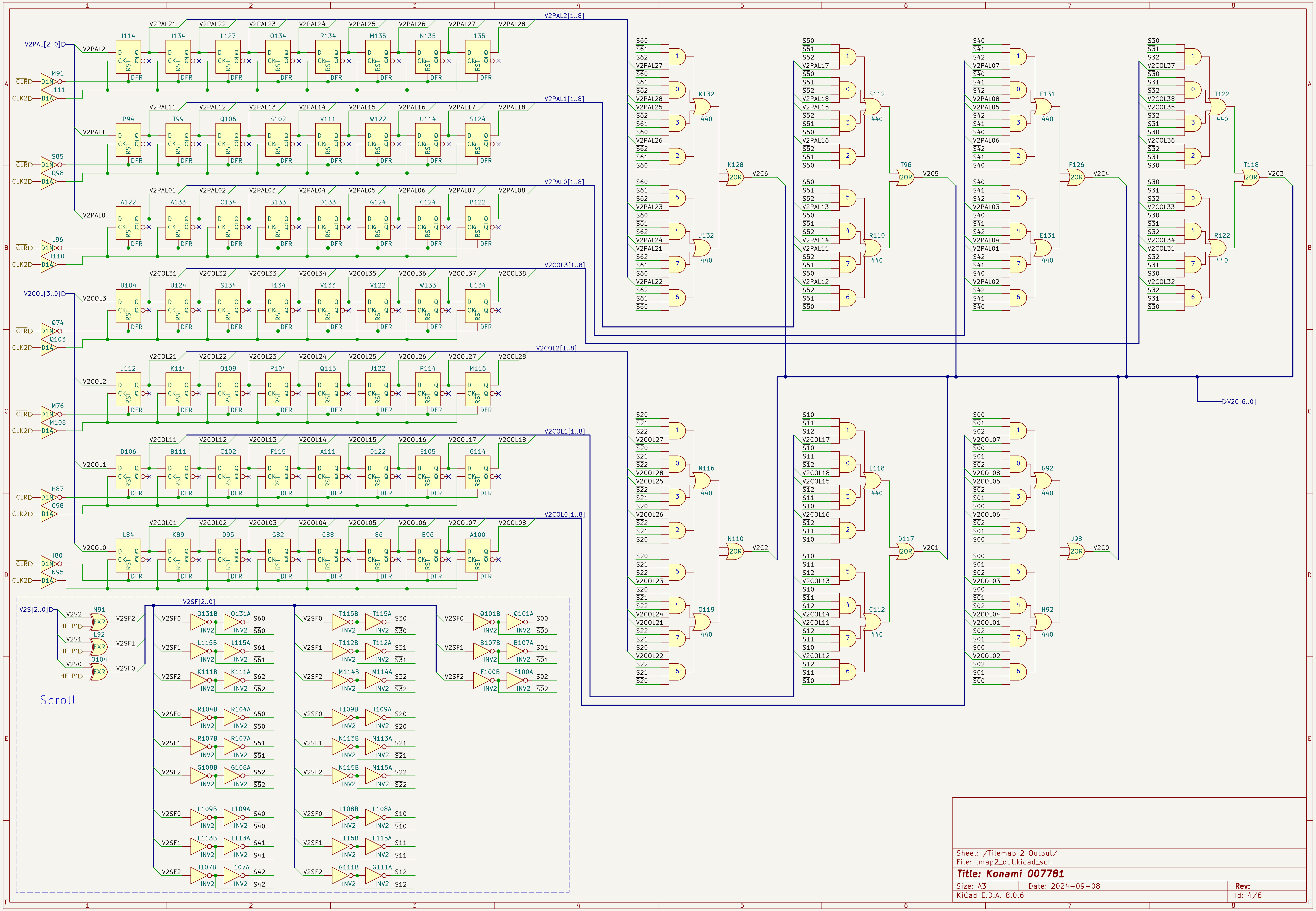
Sheet: /Pixel Counters/		
File: pixel_counters.kicad_sch		
Title: Konami 007781		
Size: A3	Date: 2024-09-08	**Rev:**
KiCad E.D.A. 8.0.6		Id: 2/6

V1PAL[2..0]
V1PAL2
V1PAL1
V1PAL0
V1COL[3..0]
V1COL3
V1COL2
V1COL1
V1COL0
V1PAL2[1..8]
V1PAL1[1..8]
V1PAL0[1..8]
V1COL3[1..8]
V1COL2[1..8]
V1COL1[1..8]
V1COL0[1..8]
V1C[6..0]
V1SF[2..0]
V1S[2..0]
Scroll
P79
M33
M80
E93
G75
F88
T83
T80
S90
M125
K124
L116
K100
G104
I95
T60
W80
S73
K73
L70
I67
V1C6
V1C5
V1C4
V1C3
V1C2
V1C1
V1C0

Sheet: /Tilemap 1 Output/
File: tmap1_out.kicad_sch

Title: Konami 007781

Size: A3	Date: 2024-09-08	**Rev:**
KiCad E.D.A. 8.0.6		Id: 3/6


V2PAL[2..0]
V2PAL2[1..8]
V2PAL1[1..8]
V2PAL0[1..8]
V2COL[3..0]
V2COL3[1..8]
V2COL2[1..8]
V2COL1[1..8]
V2COL0[1..8]
V2S[2..0]
V2SF[2..0]
V2C[6..0]
CLRD
CLK2D
HFLP'D
Scroll
Sheet: /Tilemap 2 Output/
File: tmap2_out.kicad_sch
Title: Konami 007781
Size: A3
Date: 2024-09-08
Rev:
KiCad E.D.A. 8.0.6
Id: 4/6

The pixel data is latched when
HCNT2 goes high.
The pixel data order is

1. VC31,VC30,VC29,VC28
2. VC27,VC26,VC25,VC24
3. VC23,VC22,VC21,VC20
4. VC19,VC18,VC17,VC16
5. VC15,VC14,VC13,VC12
6. VC11,VC10,VC9,VC8
7. VC7,VC6,VC5,VC4
9. VC3,VC2,VC1,VC0

The palette color is delayed 8 pixels. It is because
the 007780 takes 8 pixels to process the pixel data.

Sheet: /Tilemap 1 Pixel Select/	
File: tilemap1_px_sel.kicad_sch	
Title: Konami 007781	
Size: A3	Date: 2024-09-08
KiCad E.D.A. 8.0.6	Rev:
	Id: 5/6

The pixel data is latched when
HC4 goes high.
The pixel data order is

1. VC31,VC30,VC29,VC28
2. VC27,VC26,VC25,VC24
3. VC23,VC22,VC21,VC20
4. VC19,VC18,VC17,VC16
5. VC15,VC14,VC13,VC12
6. VC11,VC10,VC9,VC8
7. VC7,VC6,VC5,VC4
8. VC3,VC2,VC1,VC0

When flip is not active
pixel data is delayed one pixel.

Sheet: /Tilemap 2 Pixel Select/		
File: tilemap2_px_sel.kicad_sch		
Title: Konami 007781		
Size: A3	Date: 2024-09-08	**Rev:**
KiCad E.D.A. 8.0.6		Id: 6/6