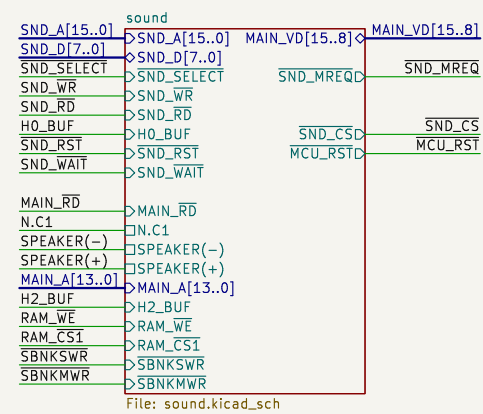
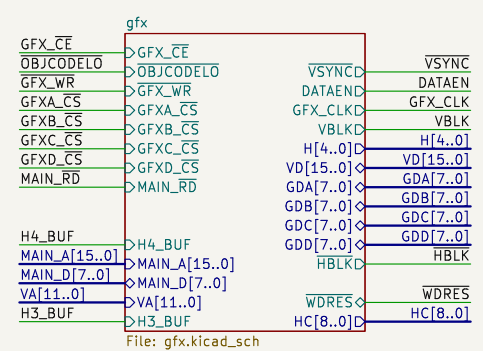
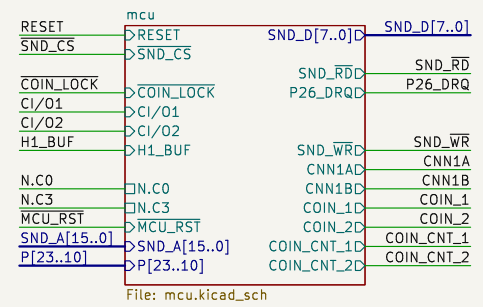
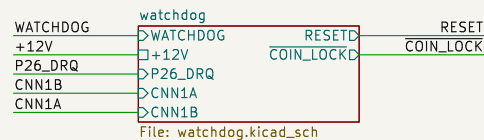
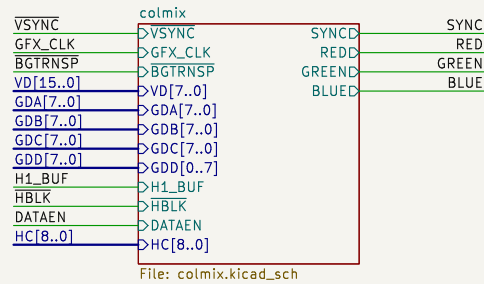
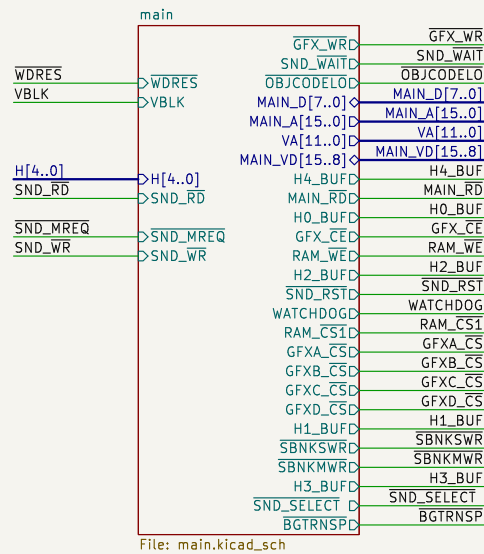
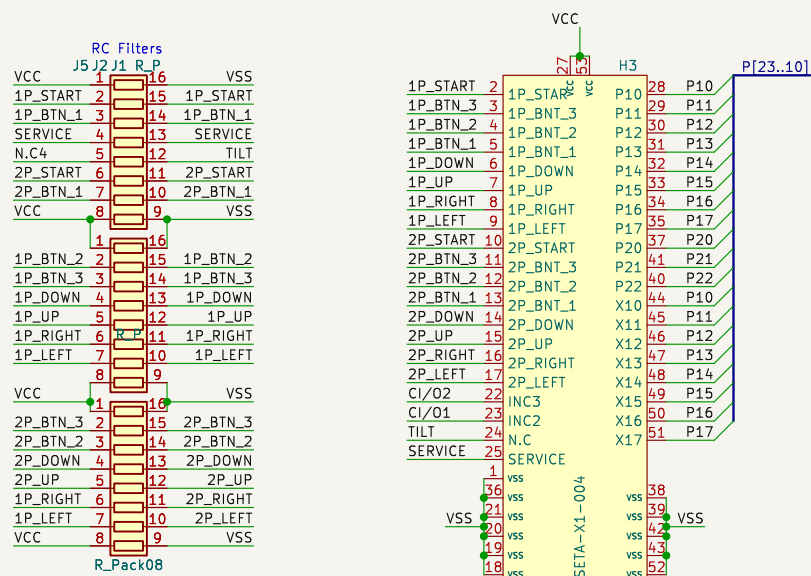
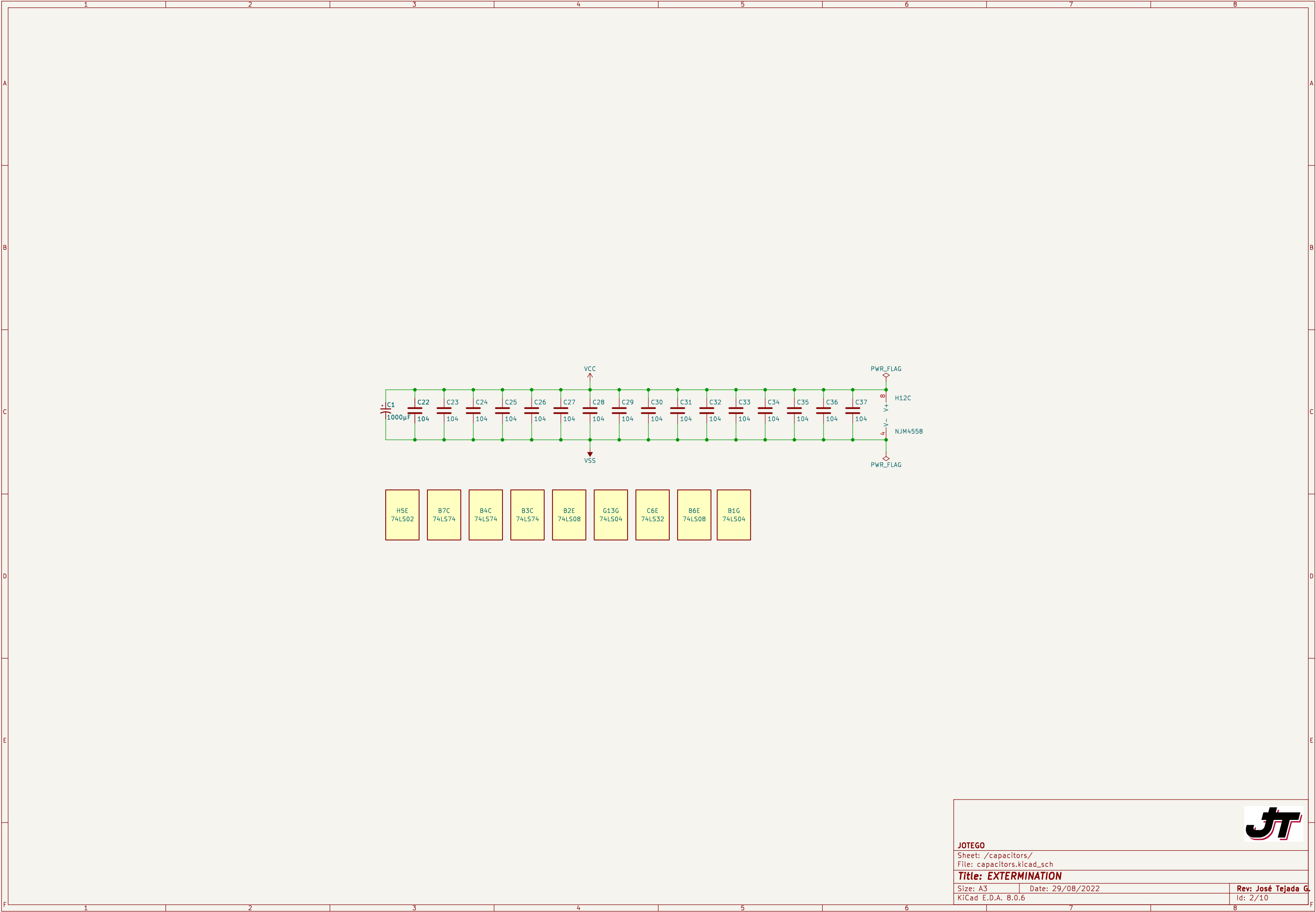
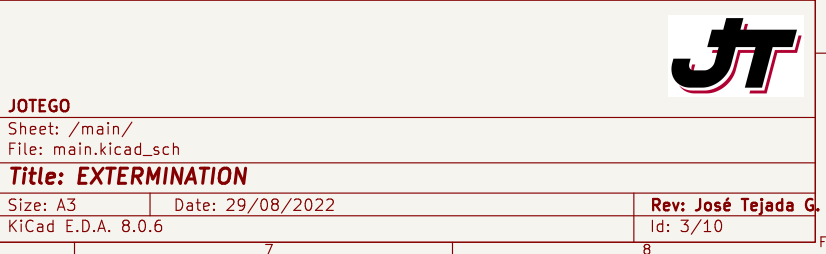
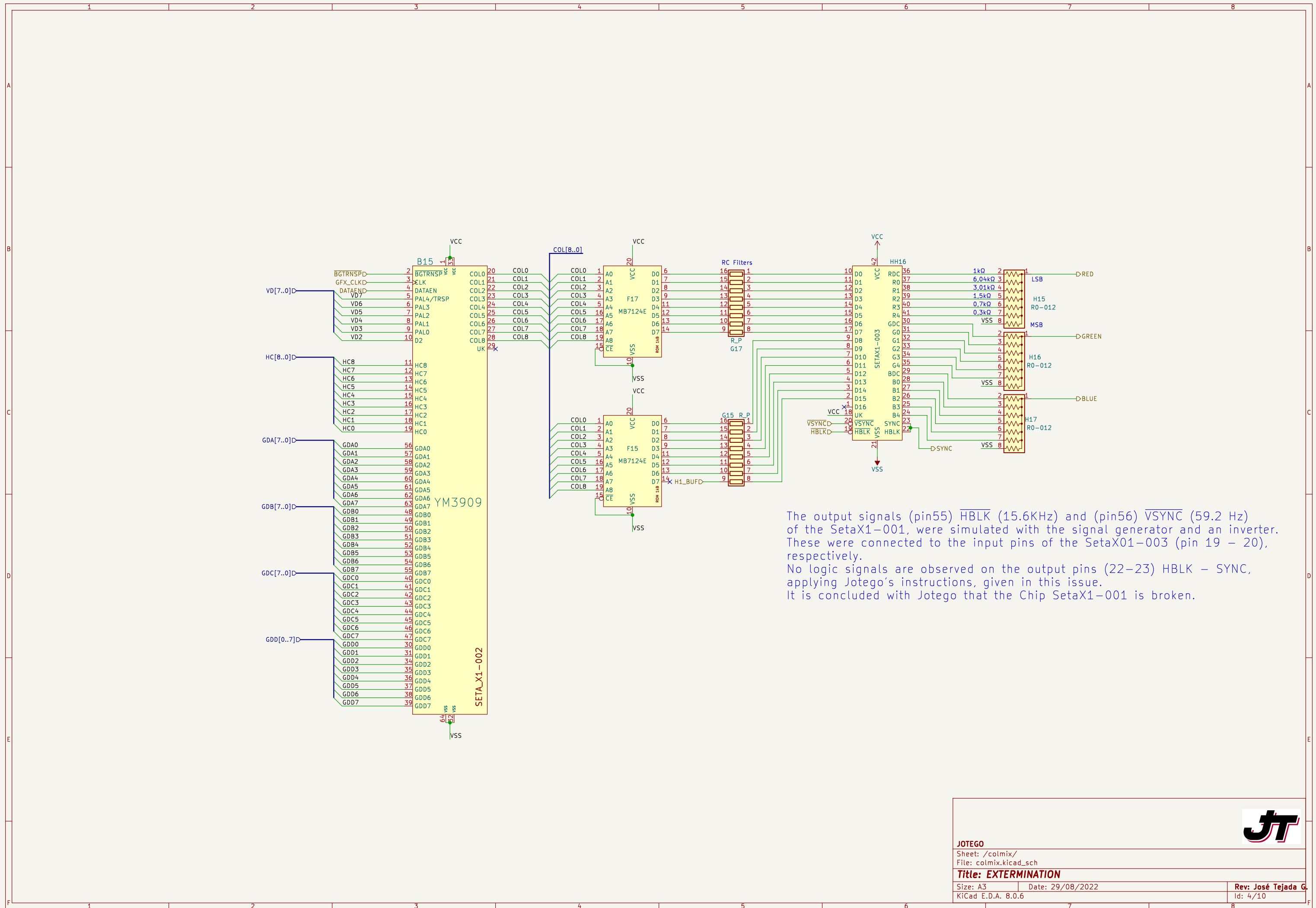


CABINET I/O





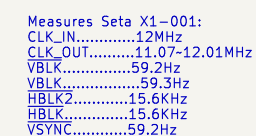




The output signals (pin55) $\overline{\text{HBLK}}$ (15.6KHz) and (pin56) $\overline{\text{VSYNC}}$ (59.2 Hz) of the SetaX1-001, were simulated with the signal generator and an inverter. These were connected to the input pins of the SetaX01-003 (pin 19 – 20), respectively.

No logic signals are observed on the output pins (22-23) $\text{HBLK} - \text{SYNC}$, applying Jotego's instructions, given in this issue.

It is concluded with Jotego that the Chip SetaX1-001 is broken.



counter.

gfx_ram

H3_BUF → H3_BUF

MAIN_A[15..0] → MAIN_A[15..0]

GFXA_CS → GFXA_CS

GFXB_CS → GFXB_CS

GFXC_CS → GFXC_CS

GFXD_CS → GFXD_CS

GFX_WR → GFX_WR

SPBANK1D → SPBANK1

VA[11..0] → VA[11..0]

VD[15..0] → VD[15..0]

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File: gfx_rom.kicad_sch

JOTEGO

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File: watchdog.kicad_sch

Title: EXTERMINATION

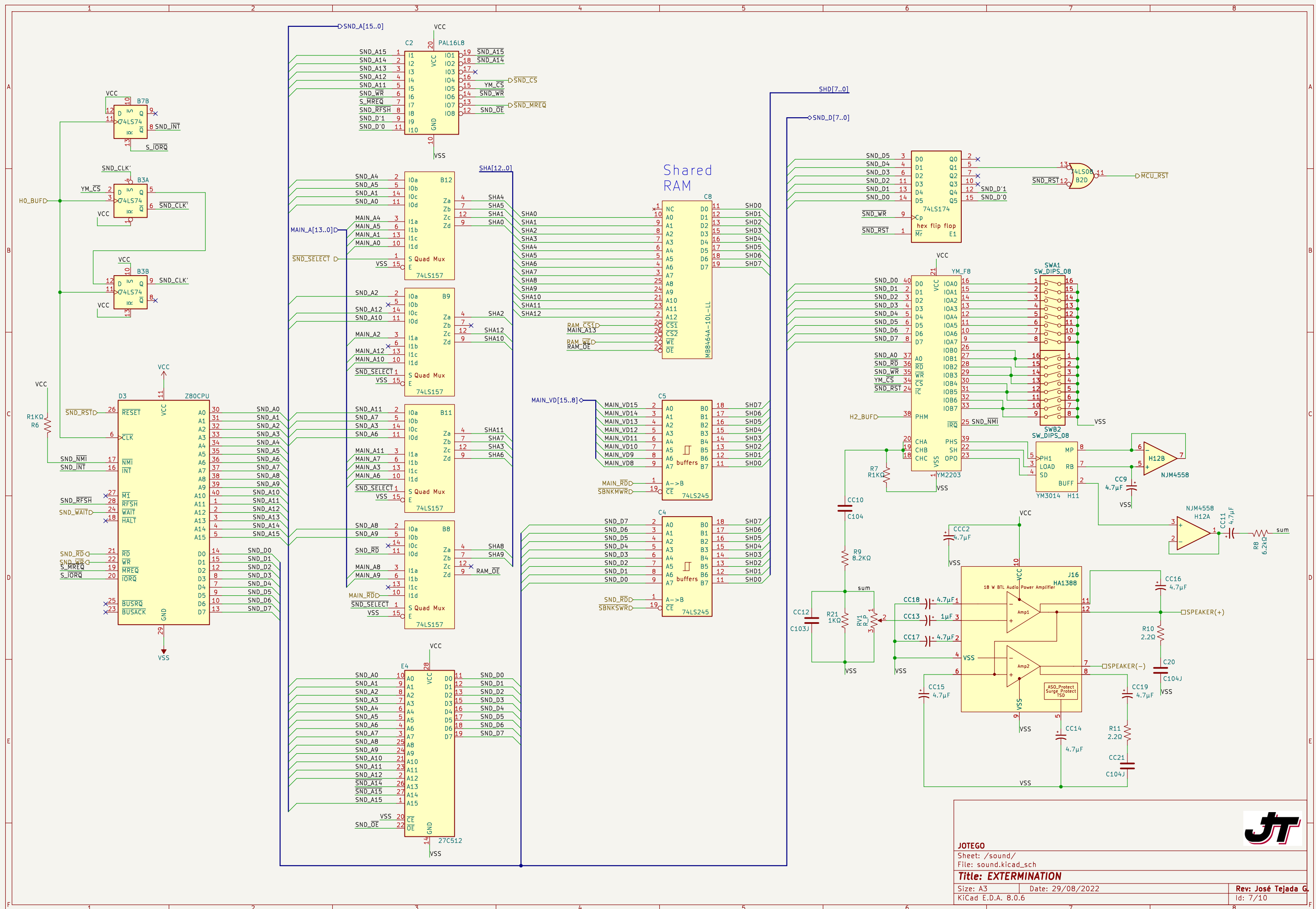
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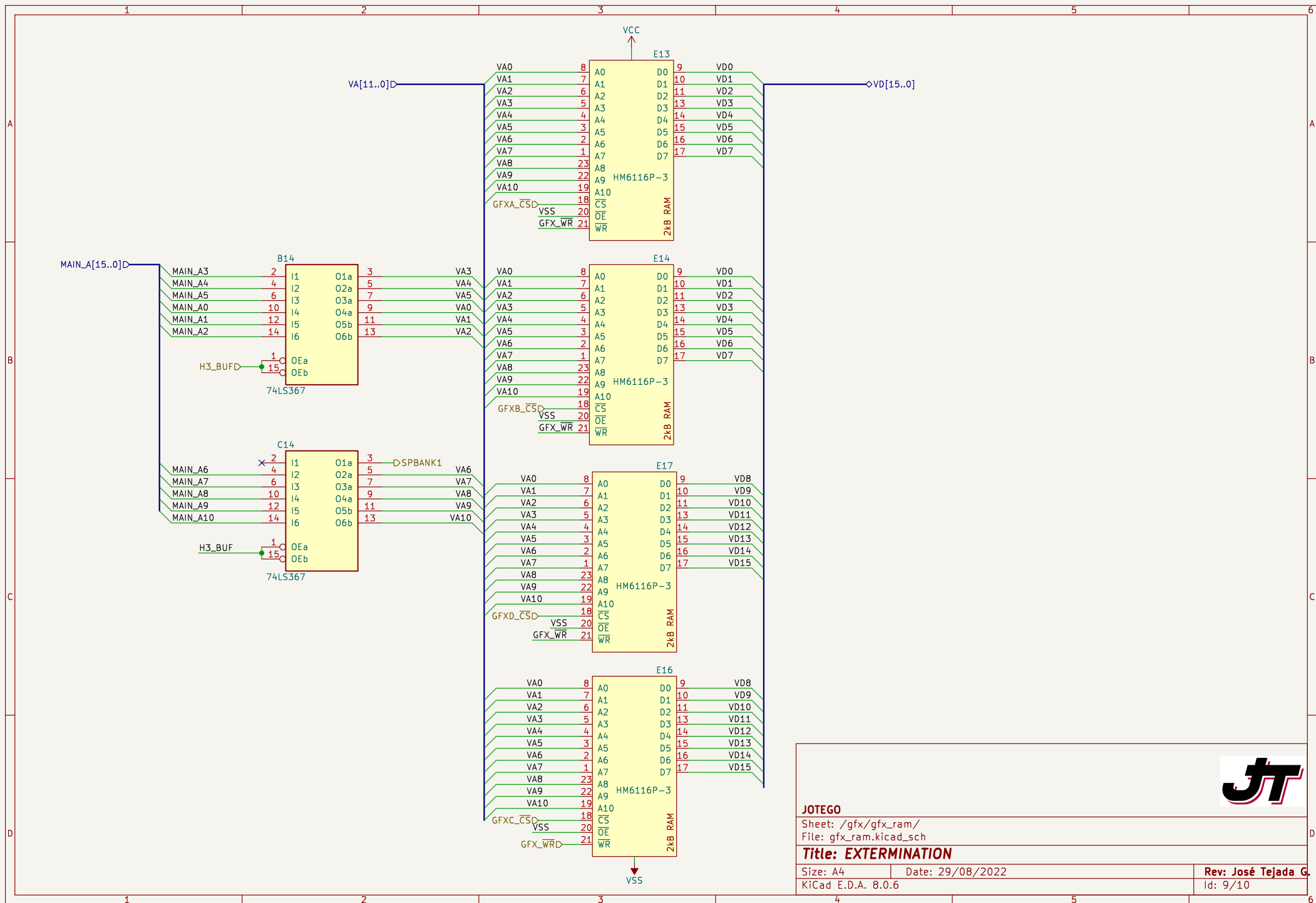
Rev: José Tejada G

Id: 6/10









JOTEGO

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Size: A4

Date: 29/08/2022

KiCad E.D.A. 8.0.6

Rev: José Tejada G.

Id: 9/10



