







Object Character Select Address

Object (Sprite) tiles are called characters on the twin16 platform.

Truth Table:

VSIZE1	VSIZE0	VSIZE	HSIZE1	HSIZE0	HSIZE	OCA52	OCA51	OCA50				
0	0	0	0	0	0	0	0	0	0	16H16V	256	
0	0	0	0	0	16	0	0	1	1	32H16V	512	
0	0	0	0	1	0	0	1	0	0	64H16V	1024	
0	0	0	1	0	0	0	1	0	1	128H16V	2048	
0	0	0	1	1	0	0	0	0	0	16H32V	512	
0	0	1	0	0	0	0	0	1	1	32H32V	1024	
0	0	1	0	1	0	0	1	0	0	64H32V	2048	
0	1	0	0	0	0	0	0	1	1	128H32V	4096	
0	1	0	0	1	0	0	1	0	0	16H64V	1024	
0	1	0	1	0	0	0	0	1	1	32H64V	2048	
0	1	0	1	1	0	0	1	0	0	64H64V	4096	
0	1	1	0	0	0	0	0	1	1	128H64V	8192	
0	1	1	0	1	0	0	1	0	0	16H128V	2048	
0	1	1	1	0	0	0	0	1	1	32H128V	4096	
0	1	1	1	1	0	0	1	0	0	64H128V	8192	
1	0	0	0	0	0	1	1	1	1	128H128V	16384	

Logic Schematic:

The logic schematic is a complex digital circuit. It starts with inputs HSIZE[0..1] and VSIZE[0..1]. These inputs are processed through a series of gates (AND, OR, NOT) to generate intermediate signals like OCA50, OCA51, and OCA52. These signals are then combined in a large OR gate (V3) to produce OCA1. This process is repeated in a series of stages (OCA2, OCA3, OCA4, OCA5, OCA6, OCA7, OCA8, OCA9, OCA10) to eventually produce the output OCA[10..0]. The circuit also includes a truth table for object character selection, which is used to generate the OCA50, OCA51, and OCA52 signals. The output OCA[10..0] is used to address a memory array (OCH) and a counter (OCHC).

Title Block:

Sheet: /Obejct Character Address/ File: object_character_address.kicad_sch		
Title:		
Size: A3	Date: 2023-12-22	Rev:
KiCad E.D.A. 8.0.6		Id: 5/7

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0	0	0	0	0	16	0	1	0	0	64H16V	1024	
0	0	0	0	1	16	0	1	1	1	128H16V	2048	
0	0	0	1	0	32	0	0	0	4	16H32V	512	
0	0	0	1	0	32	0	1	0	1	32H32V	1024	
0	0	0	1	1	32	0	1	1	2	64H32V	2048	
0	1	0	0	0	64	0	0	0	3	128H32V	4096	
0	1	0	0	1	64	0	1	0	2	16H64V	1024	
0	1	0	0	1	64	0	1	1	3	32H64V	2048	
0	1	0	1	0	64	1	0	0	6	64H64V	4096	
0	1	0	1	1	64	1	1	1	7	128H64V	8192	
1	0	0	0	0	128	0	0	0	6	16H128V	2048	
1	0	0	0	1	128	0	1	0	7	32H128V	4096	
1	0	0	1	0	128	1	0	0	6	64H128V	8192	
1	0	0	1	1	128	1	1	1	7	128H128V	16384	

Logic Schematic:

The schematic shows the implementation of the object character select address logic. It includes a truth table, a logic diagram with various gates (AND, OR, NOT, XOR, MUX), and a register (V90) for the HFLPD signal. The output is a 10-bit address (OCA[10..0]).

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0	0	0	0	0	16	0	0	0	1	32H16V	512
0	0	0	0	1	0	0	0	0	2	64H16V	1024
0	0	0	1	0	0	0	0	0	3	128H16V	2048
0	0	0	1	1	0	0	0	0	4	16H32V	512
0	0	1	0	0	0	0	0	0	5	32H32V	1024
0	0	1	0	1	0	0	0	0	6	64H32V	2048
0	0	1	1	0	0	0	0	0	7	128H32V	4096
0	1	0	0	0	0	0	0	0	2	16H64V	1024
0	1	0	0	1	0	0	0	0	3	32H64V	2048
0	1	0	1	0	0	0	0	0	6	64H64V	4096
0	1	0	1	1	0	0	0	0	7	128H64V	8192
1	0	0	0	0	0	0	0	0	6	16H128V	2048
1	0	0	0	1	0	0	0	0	7	32H128V	4096
1	0	0	1	0	0	0	0	0	6	64H128V	8192
1	0	0	1	1	0	0	0	0	7	128H128V	16384

Logic Schematic:

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