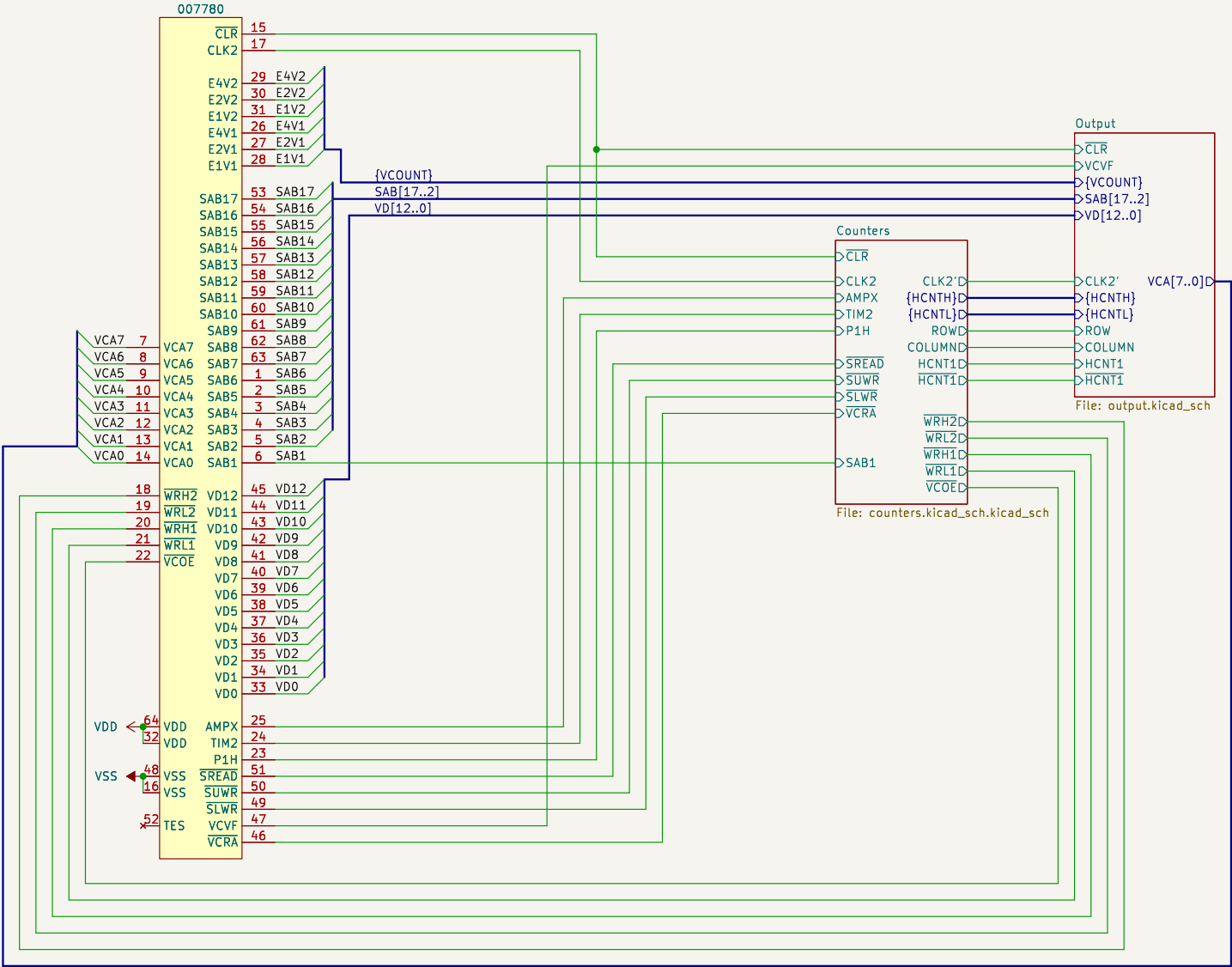The Schematics have been analyzed from
a die picture by InfosecDJ.
The chip is identified as:

Fujitsu
673174U
C 1985

It is a C850AVB, MB673174 device
from the AVB-CMOS series.
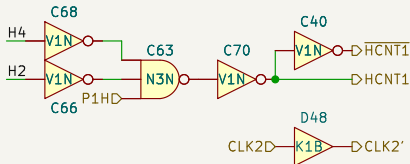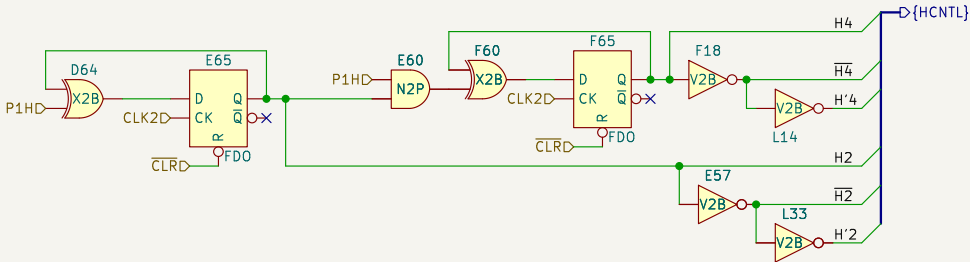- 852 Basic Cells
- 12 Columns, 71 Rows

Note: compared to the other devices from
the AVB series the VDD and VSS rails are flipped.
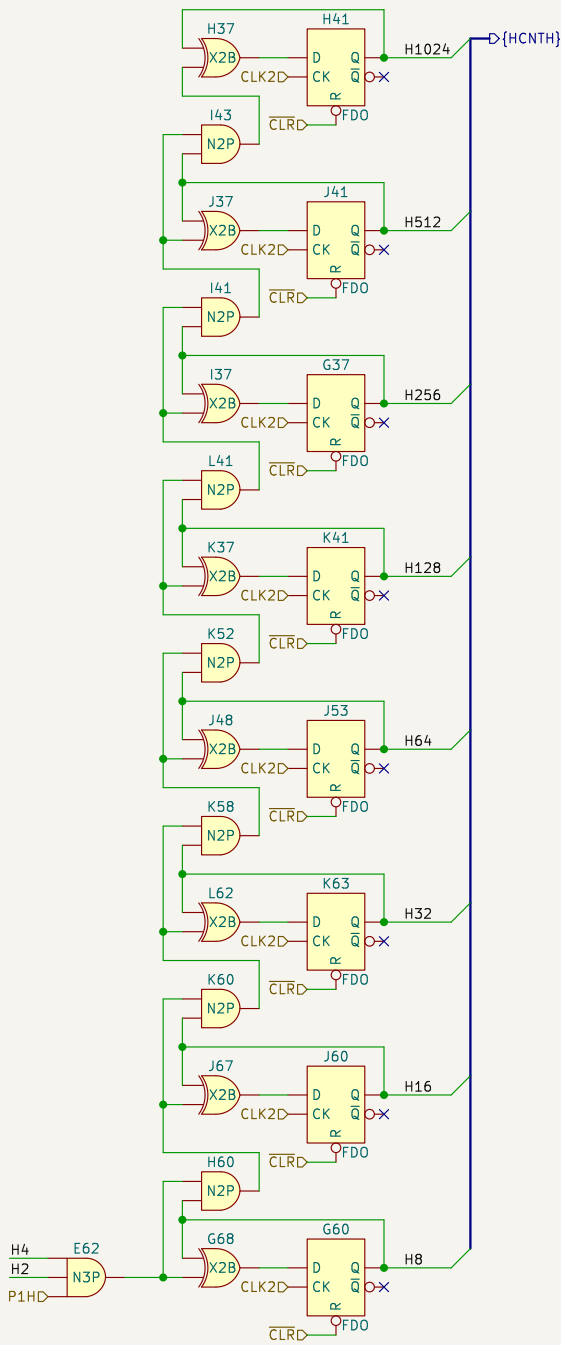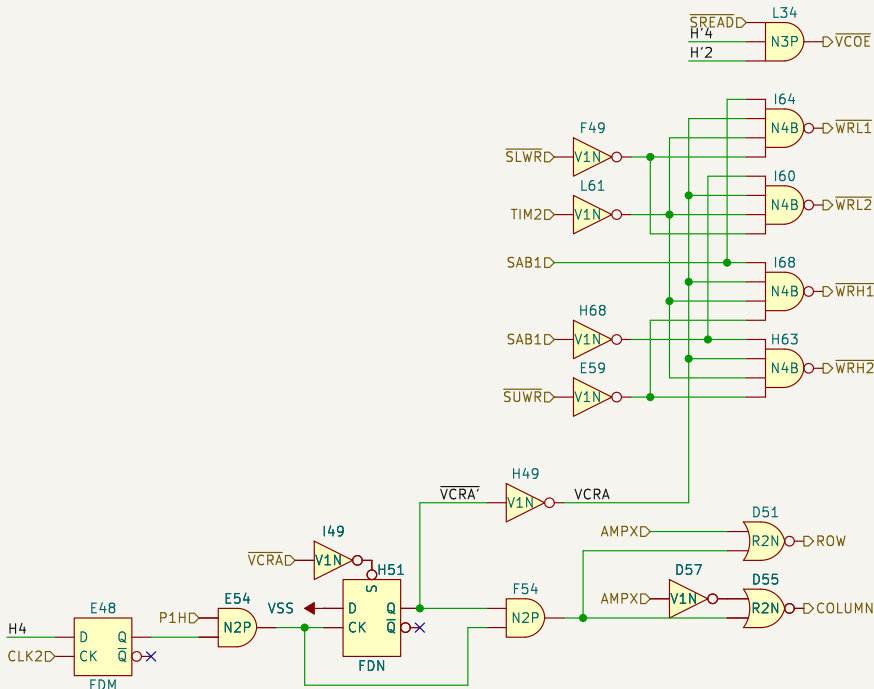When analysed the picture has been flipped and rotated
to help identify cells.

007780

Pin	Signal
15	CLR
17	CLK2
29	E4V2
30	E2V2
31	E1V2
26	E4V1
27	E2V1
28	E1V1
53	SAB17
54	SAB16
55	SAB15
56	SAB14
57	SAB13
58	SAB12
59	SAB11
60	SAB10
61	SAB9
62	SAB8
63	SAB7
1	SAB6
2	SAB5
3	SAB4
4	SAB3
5	SAB2
6	SAB1

Pin	Signal
7	VCA7
8	VCA6
9	VCA5
10	VCA4
11	VCA3
12	VCA2
13	VCA1
14	VCA0

Pin	Signal
18	WRH2
19	WRL2
20	WRH1
21	WRL1
22	VCOE

Pin	Signal
45	VD12
44	VD11
43	VD10
42	VD9
41	VD8
40	VD7
39	VD6
38	VD5
37	VD4
36	VD3
35	VD2
34	VD1
33	VD0

Pin	Signal
64	VDD
32	VDD
25	AMPX
24	TIM2
23	P1H
51	SREAD
50	SUWR
49	SLWR
47	VCVF
46	VCRA
48	VSS
16	VSS
52	TES

VDD

VSS

Counters
CLR
CLK2   CLK2'
AMPX   {HCNTH}
TIM2   {HCNTL}
P1H   ROW
            COLUMN
SREAD   HCNT1
SUWR   HCNT1
SLWR
VCRA

SAB1

WRH2
WRL2
WRH1
WRL1
VCOE

File: counters.kicad_sch.kicad_sch

Output
CLR
VCVF
{VCOUNT}
SAB[17..2]
VD[12..0]
CLK2'   VCA[7..0]
{HCNTH}
{HCNTL}
ROW
COLUMN
HCNT1
HCNT1

File: output.kicad_sch

{VCOUNT}
SAB[17..2]
VD[12..0]

Ulf Skutnabba, twitter: @skutis77

Horizontal clock P1H and $\overline{CLR}$ initiates the timing of the
007780. H2 and H4 are also generated which creates a 3-bit
counter, HCNT, which controls the timing of the device. There are
2^3 = 8 different counter values: 0..7.

HCNT 0,1 Render Tilemap 1
HCNT 2,3 Render Tilemap 2
HCNT 4,5 idle, writing to page 0
HCNT 6,7 CPU read/write cycle

TIM2 is active low during HCNT cycles 6 and 7.
When HCNT is 4 or 5 then row address = 0. The column address
is incremented by one for each HCNT cycle. Is this used to
not wear out the DRAM modules?

{HCNTL}

{HCNTH}

H4
$\overline{H4}$
H'4
H2
$\overline{H2}$
H'2

H1024
H512
H256
H128
H64
H32
H16
H8

HCNT1
$\overline{HCNT1}$
CLK2'

DRAM Control Signals

$\overline{VCOE}$
$\overline{WRL1}$
$\overline{WRL2}$
$\overline{WRH1}$
$\overline{WRH2}$

$\overline{SREAD}$
H'4
H'2

$\overline{SLWR}$
TIM2
SAB1
SAB1
$\overline{SUWR}$

$\overline{VCRA'}$
VCRA
$\overline{VCRA}$

AMPX
AMPX

ROW
COLUMN

VSS
P1H

VD[12:5] = CA[7:0], row address
{VD[4:0],4V,2V,1V} = CA[7:0], column address

SAB[17:10] = CA[7:0], row address
SAB[9:2] = CA[7:0], column address

Tilemap 1 data latched when HCNT goes to 1.

Tilemap 2 data latched when HCNT goes to 4.

Title: Konami 007780