JM1

JAMMA_CONN

VSS	1	GND	GND	A
	2	VSSA	GND	B
VCC	3	VDDA	VCC	C
−5V	4	+5V	+5V	D
+12V	5	−5V	−5V	E
	6	+12V	+12V	F
COIN_CNT_1	8	COIN_CNT_1	COIN_CNT_2	J
N.C0	9	NC	NC	K
	10	SPEAKER_(+)	SPEAKER_(−)	L
N.C1	11	NC	NC	M
RED	12	NC	NC	N
BLUE	13	RED	GREEN	P
VSS	14	BLUE	SYNC	R
	15	VIDEO_GND	SERVICE	S
	16	NC	NC	T
COIN_1	17	COIN_1	COIN_2	U
1P_START	18	1P_START	2P_START	V
1P_UP	19	1P_UP	2P_UP	W
1P_DOWN	20	1P_DOWN	2P_DOWN	X
1P_LEFT	21	1P_LEFT	2P_LEFT	Y
1P_RIGHT	22	1P_RIGHT	2P_RIGHT	Z
1P_BTN_1	23	1P_BTN_1	2P_BTN_1	a
1P_BTN_2	24	1P_BTN_2	2P_BTN_2	b
1P_BTN_3	25	1P_BTN_3	2P_BTN_3	c
	26	1P_BTN_4	2P_BTN_4	d
	27	1P_SELECT	2P_SELECT	e
VSS	28	GND	GND	f

VCC
VSS
ZD1
BZD27
PWR_FLAG
PWR_FLAG

SPEAKER_(+) SPEAKER_(−)
1P_START 2P_START

CABINET I/O

RC Filters
J5 J2 J1 R_P

R_Pack08

H3
SETA-X1-004
P[23..10]

VCC
VSS
1P_START, 1P_BTN_3, 1P_BTN_2, 1P_BTN_1, 1P_DOWN, 1P_UP, 1P_RIGHT, 1P_LEFT, 2P_START, 2P_BTN_3, 2P_BTN_2, 2P_BTN_1, 2P_DOWN, 2P_UP, 2P_RIGHT, 2P_LEFT, CI/O2, CI/O1, TILT, N.C, SERVICE

P10 P11 P12 P13 P14 P15 P16 P17 P20 P21 P22 X10 X11 X12 X13 X14 X15 X16 X17
INC3 INC2

main
File: main.kicad_sch

GFX_WR, SND_WAIT, OBJCODELO, MAIN_D[7..0], MAIN_A[15..0], VA[11..0], MAIN_VD[15..8], H4_BUF, MAIN_RD, H0_BUF, GFX_CE, RAM_WE, H2_BUF, SND_RST, WATCHDOG, RAM_CS1, GFXA_CS, GFXB_CS, GFXC_CS, GFXD_CS, H1_BUF, SBNKSWR, SBNKMWR, H3_BUF, SND_SELECT, BGTRNSP

WDRES, VBLK, H[4..0], SND_RD, SND_MREQ, SND_WR

colmix
File: colmix.kicad_sch

VSYNC, GFX_CLK, BGTRNSP, VD[7..0], GDA[7..0], GDB[7..0], GDC[7..0], GDD[7..0], H1_BUF, HBLK, DATAEN, HC[8..0]

SYNCD, REDD, GREEND, BLUED
SYNC, RED, GREEN, BLUE

watchdog
File: watchdog.kicad_sch

WATCHDOG, +12V, P26_DRQ, CNN1A, CNN1B
RESETD, COIN_LOCKD
RESET, COIN_LOCK

capacitors
File: capacitors.kicad_sch

mcu
File: mcu.kicad_sch

RESET, SND_CS, COIN_LOCK, CI/O1, CI/O2, H1_BUF, N.C0, N.C3, MCU_RST, SND_A[15..0], P[23..10]

SND_D[7..0], SND_RD, P26_DRQ, CNN1A, CNN1B, COIN_1, COIN_2, COIN_CNT_1, COIN_CNT_2

gfx
File: gfx.kicad_sch

GFX_CE, OBJCODELO, GFX_WR, GFXA_CS, GFXB_CS, GFXC_CS, GFXD_CS, MAIN_RD, H4_BUF, MAIN_A[15..0], MAIN_D[7..0], VA[11..0], H3_BUF

VSYNC, DATAEN, GFX_CLK, VBLK, H[4..0], VD[15..0], GDA[7..0], GDB[7..0], GDC[7..0], GDD[7..0], HBLK, WDRES, HC[8..0]

sound
File: sound.kicad_sch

SND_A[15..0], SND_D[7..0], SND_SELECT, SND_WR, SND_RD, H0_BUF, SND_RST, SND_WAIT, MAIN_RD, N.C1, SPEAKER(−), SPEAKER(+), MAIN_A[13..0], H2_BUF, RAM_WE, RAM_CS1, SBNKSWR, SBNKMWR

MAIN_VD[15..8], SND_MREQ, SND_CS, MCU_RST

VCC

PWR_FLAG

C1	C22	C23	C24	C25	C26	C27	C28	C29	C30	C31	C32	C33	C34	C35	C36	C37
1000µF	104	104	104	104	104	104	104	104	104	104	104	104	104	104	104	104

H12C

NJM4558

VSS

PWR_FLAG

H5E	B7C	B4C	B3C	B2E	G13G	C6E	B6E	B1G
74LS02	74LS74	74LS74	74LS74	74LS08	74LS04	74LS32	74LS08	74LS04

VCC

B15

BGTRNSP
GFX_CLK
DATAEN
VD7
VD6
VD5
VD4
VD3
VD2

BGTRNSP
CLK
DATAEN
PAL4/TRSP
PAL3
PAL2
PAL1
PAL0
D2

COL0
COL1
COL2
COL3
COL4
COL5
COL6
COL7
COL8
UK

COL0
COL1
COL2
COL3
COL4
COL5
COL6
COL7
COL8

COL[8..0]

VD[7..0]

HC[8..0]

HC8
HC7
HC6
HC5
HC4
HC3
HC2
HC1
HC0

GDA[7..0]

GDA0
GDA1
GDA2
GDA3
GDA4
GDA5
GDA6
GDA7

GDB[7..0]

GDB0
GDB1
GDB2
GDB3
GDB4
GDB5
GDB6
GDB7

GDC[7..0]

GDC0
GDC1
GDC2
GDC3
GDC4
GDC5
GDC6
GDC7

GDD[0..7]

GDD0
GDD1
GDD2
GDD3
GDD4
GDD5
GDD6
GDD7

YM3909

SETA_X1-002

VSS

RC Filters

COL0
COL1
COL2
COL3
COL4
COL5
COL6
COL7
COL8

A0
A1
A2
A3
A4
A5
A6
A7
A8
CE

VCC
F17
MB7124E
ROM 148
VSS

D0
D1
D2
D3
D4
D5
D6
D7

R_P
G17

VSS

COL0
COL1
COL2
COL3
COL4
COL5
COL6
COL7
COL8

A0
A1
A2
A3
A4
A5
A6
A7
A8
CE

VCC
F15
MB7124E
ROM 148
VSS

D0
D1
D2
D3
D4
D5
D6
D7

G15 R_P

H1_BUF

VSS

HH16

D0
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13
D14
D15
D16
UK
VSYNC
HBLK

RDC
R0
R1
R2
R3
R4
GDC
G0
G1
G2
G3
G4
BDC
B0
B1
B2
B3
B4
SYNC
HBLK

SETAX1-003

VCC

VSYNC
HBLKD

VCC

VSS

1kΩ
6,04kΩ
3,01kΩ
1,5kΩ
0,7kΩ
0,3kΩ

LSB
H15
R0-012
MSB

RED

VSS

GREEN

H16
R0-012

VSS

BLUE

H17
R0-012

VSS

SYNC

The output signals (pin55) HBLK (15.6KHz) and (pin56) VSYNC (59.2 Hz)
of the SetaX1-001, were simulated with the signal generator and an inverter.
These were connected to the input pins of the SetaX01-003 (pin 19 - 20),
respectively.
No logic signals are observed on the output pins (22-23) HBLK - SYNC,
applying Jotego's instructions, given in this issue.
It is concluded with Jotego that the Chip SetaX1-001 is broken.

GA[15..0]

VD[15..0]

MAIN_D[7..0]

E11

MAIN_D1 2	A0	B0	18	VD9		VD10	3	D0	Q0	2	GA7
MAIN_D0 3	A1	B1	17	VD8		VD11	4	D1	Q1	5	GA8
MAIN_D7 4	A2	B2	16	VD15		VD12	7	D2	Q2	6	GA9
MAIN_D6 5	A3	B3	15	VD14		VD13	8	D3	Q3	9	GA10
MAIN_D5 6	A4	B4	14	VD13		VD14	13	D4	Q4	12	GA11
MAIN_D4 7	A5	B5	13	VD12		VD8	14	D5	Q5	15	GA5
MAIN_D3 8	A6	B6	12	VD11		VD9	17	D6	Q6	16	GA6
MAIN_D2 9	A7	B7	11	VD10		VD15	18	D7	Q7	19	GA12

buffers   A16   flip flops

OBJCODELO 74LS04 B6A   C6D 74LS37

MAIN_RD1   A->B   H4_BUF 11 Cp   VCC 1 Mr
GFX_WR   19 CE   74LS245   74LS273

H3_BUF

E12

MAIN_D1 2	A0	B0	18	VD1		VD1	3	D0	Q0	2	GA14
MAIN_D0 3	A1	B1	17	VD0		VD0	4	D1	Q1	5	GA13
MAIN_D7 4	A2	B2	16	VD7		VD5	6	D2	Q2	7	ROM_CE
MAIN_D6 5	A3	B3	15	VD6		VD4	11	D3	Q3	10	ROM_OE
MAIN_D5 6	A4	B4	14	VD5		VD3	13	D4	Q4	12	GA15
MAIN_D4 7	A5	B5	13	VD4		VD2	14	D5	Q5	15	
MAIN_D3 8	A6	B6	12	VD3							
MAIN_D2 9	A7	B7	11	VD2							

buffers   74LS174 hex flip flop

GFX_CE 74LS37 C6A   MAIN_RD A->B 19 CE 74LS245   H4_BUF 9 Cp   VCC 1 Mr   A15

VCC   R4 3.3kΩ   R3 22Ω

A17
Standby VDD Out
12.000MHz   GND VSS

C17
VCC VCC

YM3906
SETA_X1-001

63	CLK	CLKO	62	GFX_CLK
2	RD	VBLK	58	VBLK
3	WR	HBLK2	57	
60	FLIPX	VSYNC	56	VSYNC
59	FLIPY	HBLK	55	HBLK
4	XC0	DATAEN	61	DATAEN

B1F 74LS04

MAIN_RD
GFX_WR
VD7
VD6
VD0

7	D7	HC8	54	HC8
8	D6	HC7	53	HC7
9	D5	HC6	52	HC6
10	D4	HC5	51	HC5
11	D3	HC4	50	HC4
12	D2	HC3	49	HC3
13	D1	HC2	48	HC2
14	D0	HC1	47	HC1
		HC0	46	HC0

HC[8..0]

15	A0	H8	43	H4
16	A1	H4	42	H3
17	A2	H2	41	H2
18	A3	H0	40	H0
19	A4	HPH90	39	H1
20	A5	H		
21	A6			
22	A7	CHA0	35	GA0
23	A8	CHA1	36	GA1
24	A9	CHA2	37	GA2
25	A10	CHA4	38	GA4
28	A11	HBB	34	HRB

H[4..0]

GA[15..0]

VA[11..0]

| 26 | SPBANK1 | ~{WDRES} | 29 | WDRES |
| 27 | SPBANK2 | RW | 30 | |

SPBANK1
MAIN_A11

MAIN_A[15..0]

MAIN_RD B1D 74LS04   74LS37 C6B GFX_WR

UK UK UK UK UK
VSS VSS

VSS

gfx_ram

H3_BUF	H3_BUF	SPBANK1	SPBANK1
MAIN_A[15..0]	MAIN_A[15..0]	VA[11..0]	VA[11..0]
GFXA_CS	GFXA_CS	VD[15..0]	VD[15..0]
GFXB_CS	GFXB_CS		
GFXC_CS	GFXC_CS		
GFXD_CS	GFXD_CS		
GFX_WR	GFX_WR		

File: gfx_ram.kicad_sch

gfx_rom

ROM_CE	ROM_CE	GDA[7..0]	GDA[7..0]
ROM_OE	ROM_OE	GDB[7..0]	GDB[7..0]
GA[15..0]	GA[15..0]	GDC[7..0]	GDC[7..0]
HRB	HRB	GDD[7..0]	GDD[7..0]

File: gfx_rom.kicad_sch

VCC

SND_A[15..0]

SND_A0

P[23..10]

SND_D[7..0]

SND_D0			

G3

VDD VCC

A0 D0 SND_D0
P10 D1 SND_D1
P11 D2 SND_D2
P12 D3 SND_D3
P13 D4 SND_D4
P14 D5 SND_D5
P15 D6 SND_D6
P16 D7 SND_D7
P17 P24_OBF
P20 P26_DRQ P26_DRQ
P21 P27_DACK
P22 RD SND_RD
P23 WR SND_WR
PROG SYNC
P25_IBF
TEST0 TEST0
TEST1 TEST1
XTAL1 H1_BUF
XTAL2 H1_BUF
RESET MCU_RST
SS VCC
CS SND_CS
EA VSS

INTEL8742
8-BIT SLAVE
MICROCONTROLLER

VSS

RESET

VSS

JJ10

COIN_2 COIN_2 COINOUT2 TEST1
COIN_1 COIN_1 COINOUT1 TEST0
CI/O2 UK COIN_CNT_1 COIN_CNT_1
CI/O1 UK COIN_CNT_2 COIN_CNT_2
COIN_LOCK COIN1_LOCK LOCK-OUT1 N.C0
OBF LOCK-OUT2 N.C3
DACK CNN1 CNN1A
IBF CNN2 CNN1B
UK UK.N.C
UK.NC
VSS UK.NC
VSS
VSS VCC
VCC VCC
VSS VCC

VSS

PC050CM

VCC

H5D
74LS02

H5B
74LS02

74LS02
H5C

VCC

R20
R330Ω

H1_BUF

G15E
74LS04

H1_BUF

VCC

E13
HM6116P-3
2kB RAM

E14
HM6116P-3
2kB RAM

E17
HM6116P-3
2kB RAM

E16
HM6116P-3
2kB RAM

B14
74LS367

C14
74LS367

VA[11..0]

VD[15..0]

MAIN_A[15..0]

H3_BUF

H3_BUF

SPBANK1

GFXA_CS
GFXB_CS
GFXC_CS
GFXD_CS
GFX_WR

VSS

GA[15..0]

NOT POPULATED

VCC

A13
27C512
GDA0 GDA1 GDA2 GDA3 GDA4 GDA5 GDA6 GDA7

A12
27C512
GDA[7..0]

A10
27C512
GDB0 GDB1 GDB2 GDB3 GDB4 GDB5 GDB6 GDB7

A8
27C512
GDB[7..0]

A7
27C512
GDC0 GDC1 GDC2 GDC3 GDC4 GDC5 GDC6 GDC7

A5
27C512
GDC[7..0]

A4
27C512
GDD0 GDD1 GDD2 GDD3 GDD4 GDD5 GDD6 GDD7

A2
27C512
GDD[7..0]

ROM_CE
B1E
74LS04
ROM_CE'

ROM_CE
ROM_OE

GA0 GA1 GA2 HR8 GA4 GA5 GA6 GA7 GA8 GA9 GA10 GA11 GA12 GA13 GA14 GA15

A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15

D0 D1 D2 D3 D4 D5 D6 D7

CE OE VCC VSS GND