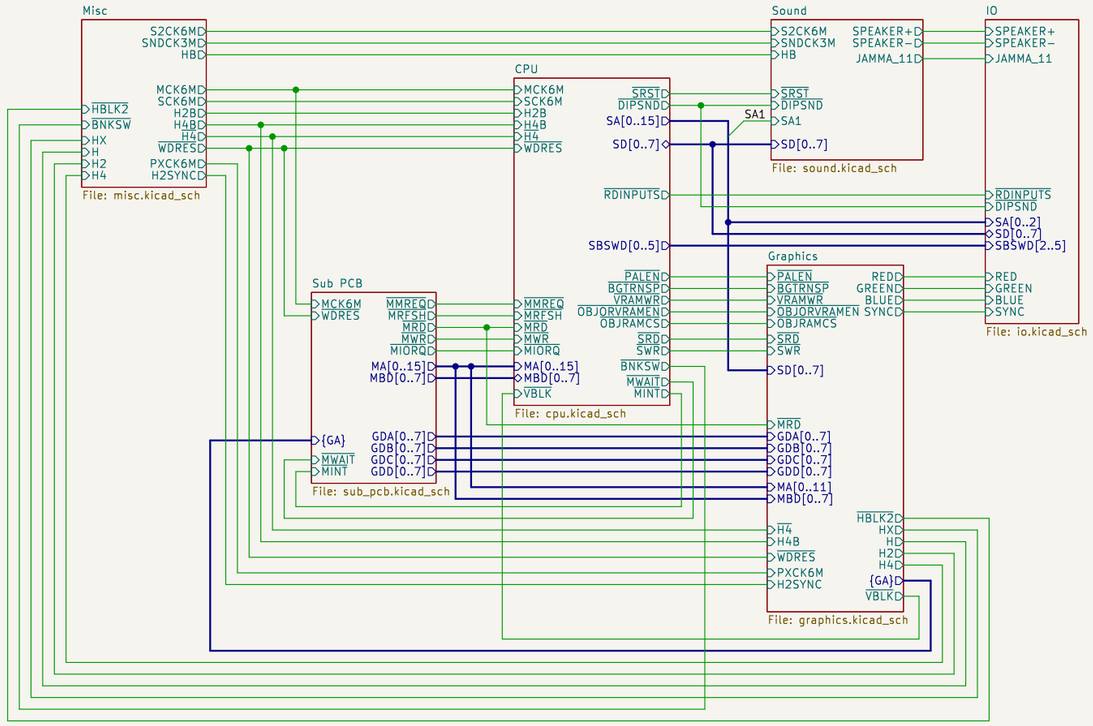

Note: The reference designator refers to the position on the PCB. If the reference designator already exists the letter is doubled. I.e. C1 -> CC1.

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Sheet: /
File: tnzs.kicad_sch

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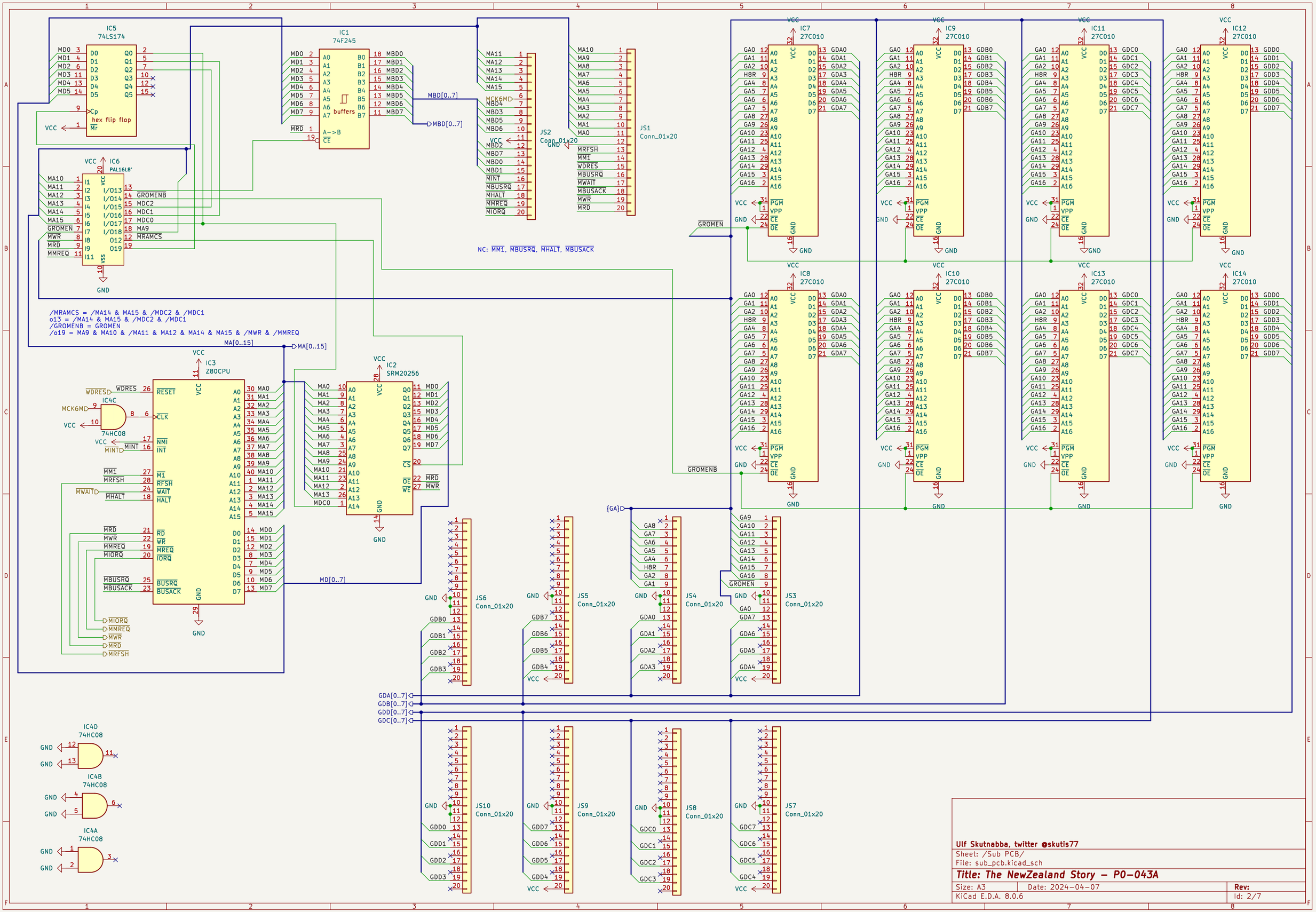
IC5
74LS174
hex flip flop
IC1
74F245
buffers
A->B
IC6
PAL16L8
IC3
Z80CPU
IC2
SRM20256
IC4C
74HC08
IC7
27C010
IC8
IC9
IC10
IC11
IC13
IC12
IC14
JS1
Conn_01x20
JS2
Conn_01x20
JS3
JS4
JS5
JS6
JS7
JS8
JS9
JS10
IC4D
IC4B
IC4A
NC: MM1, MBUSRQ, MHALT, MBUSACK
/MRAMCS = /MA14 & MA15 & /MDC2 & /MDC1
o13 = /MA14 & MA15 & /MDC2 & /MDC1
/GROMENB = GROMEN
/o19 = MA9 & MA10 & /MA11 & MA12 & MA14 & MA15 & /MWR & /MMREQ
MA[0..15]
MD[0..7]
MBD[0..7]
GDA[0..7]
GDB[0..7]
GDD[0..7]
GDC[0..7]
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Sheet: /Sub PCB/
File: sub_pcb.kicad_sch
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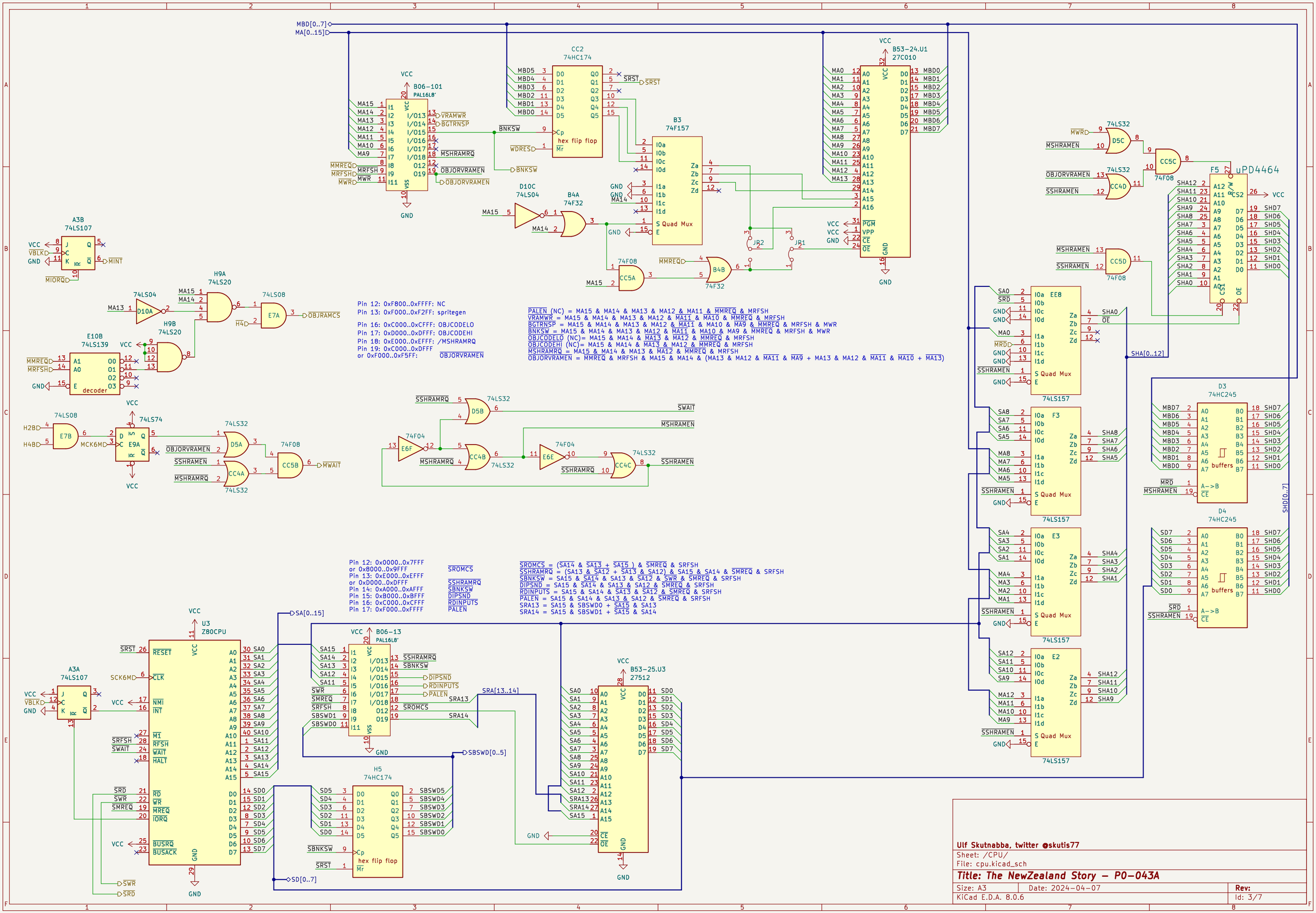
MBD[0..7]
MA[0..15]
CC2
74HC174
hex flip flop
B06-101
PAL16L8'
B3
74F157
S Quad Mux
B53-24.U1
27C010
D10C
74LS04
B4A
74F32
A3B
74LS107
H9A
74LS20
H9B
74LS20
E10B
74LS139
decoder
74LS08
74LS74
74LS32
74F08
74F04
74HC174
U3
Z80CPU
B06-13
PAL16L8'
B53-25.U3
27512
74LS157
F5
uPD4464
D3
74HC245
D4
74HC245
buffers
Pin 12: 0xF800..0xFFFF: NC
Pin 13: 0xF000..0xF2FF: spritegen
Pin 16: 0xC000..0xCFFF: OBJCODELO
Pin 17: 0xD000..0xDFFF: OBJCODEHI
Pin 18: 0xE000..0xEFFF: /MSHRAMRQ
Pin 19: 0xC000..0xDFFF
or 0xF000..0xF5FF: OBJORVRAMEN
PALEN (NC) = MA15 & MA14 & MA13 & MA12 & MA11 & MMREQ & MRFSH
VRAMWR = MA15 & MA14 & MA13 & MA12 & MA11 & MA10 & MMREQ & MRFSH
BGTRNSP = MA15 & MA14 & MA13 & MA12 & MA11 & MA10 & MA9 & MMREQ & MRFSH & MWR
BNKSW = MA15 & MA14 & MA13 & MA12 & MA11 & MA10 & MA9 & MMREQ & MRFSH & MWR
OBJCODELO (NC)= MA15 & MA14 & MA13 & MA12 & MMREQ & MRFSH
OBJCODEHI (NC)= MA15 & MA14 & MA13 & MA12 & MMREQ & MRFSH
MSHRAMRQ = MA15 & MA14 & MA13 & MA12 & MMREQ & MRFSH
OBJORVRAMEN = MMREQ & MRFSH & MA15 & MA14 & (MA13 & MA12 & MA11 & MA9 + MA13 & MA12 & MA11 & MA10 + MA13)
Pin 12: 0x0000..0x7FFF
or 0x8000..0x9FFF
Pin 13: 0xE000..0xEFFF
or 0xD000..0xDFFF
Pin 14: 0xA000..0xAFFF
Pin 15: 0xB000..0xBFFF
Pin 16: 0xC000..0xCFFF
Pin 17: 0xF000..0xFFFF
SROMCS
SSHRAMRQ
SBNKSW
DIPSND
RDINPUTS
PALEN
SROMCS = (SA14 & SA13 + SA15) & SMREQ & SRFSH
SSHRAMRQ = (SA13 & SA12 + SA13 & SA12) & SA15 & SA14 & SMREQ & SRFSH
SBNKSW = SA15 & SA14 & SA13 & SA12 & SWR & SMREQ & SRFSH
DIPSND = SA15 & SA14 & SA13 & SA12 & SMREQ & SRFSH
RDINPUTS = SA15 & SA14 & SA13 & SA12 & SMREQ & SRFSH
PALEN = SA15 & SA14 & SA13 & SA12 & SMREQ & SRFSH
SRA13 = SA15 & SBSWD0 + SA15 & SA13
SRA14 = SA15 & SBSWD1 + SA15 & SA14
SA[0..15]
SRA[13..14]
SBSWD[0..5]
SD[0..7]
SHA[0..12]
SHD[0..7]
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Sheet: /CPU/
File: cpu.kicad_sch
Title: The NewZealand Story – PO-043A
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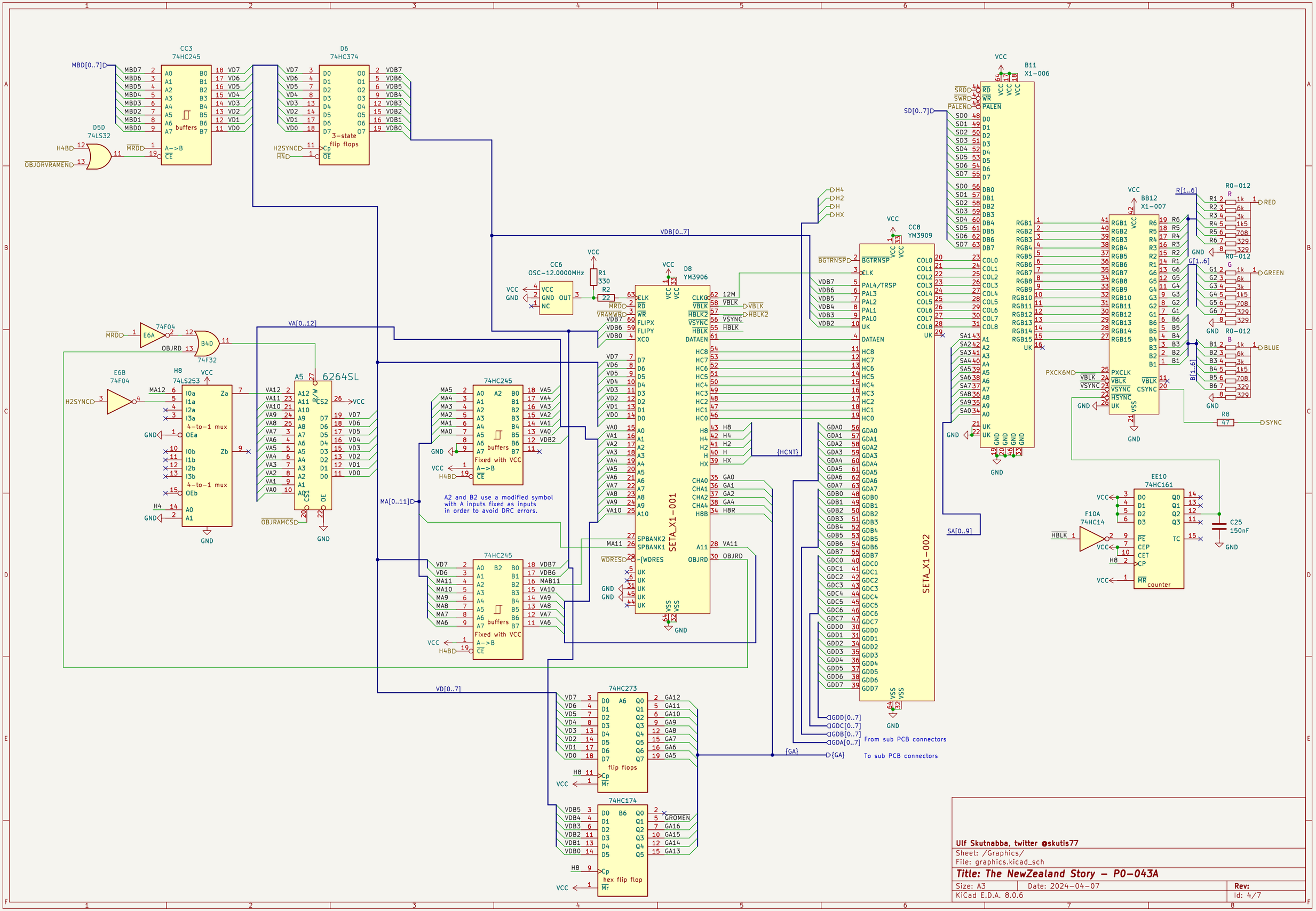
CC3
74HC245
buffers
D6
74HC374
3-state
flip flops
D5D
74LS32
E6A
74F04
B4D
74F32
E6B
74F04
H8
74LS253
4-to-1 mux
A5
6264SL
buffers
Fixed with VCC
74HC245
A2 and B2 use a modified symbol
with A inputs fixed as inputs
in order to avoid DRC errors.
CC6
OSC-12.0000MHz
D8
YM3906
SETA_X1-001
CC8
YM3909
SETA_X1-002
B11
X1-006
BB12
X1-007
EE10
74HC161
counter
F10A
74HC14
C25
150nF
R8
47
74HC273
flip flops
74HC174
hex flip flop
From sub PCB connectors
To sub PCB connectors
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Sheet: /Graphics/
File: graphics.kicad_sch
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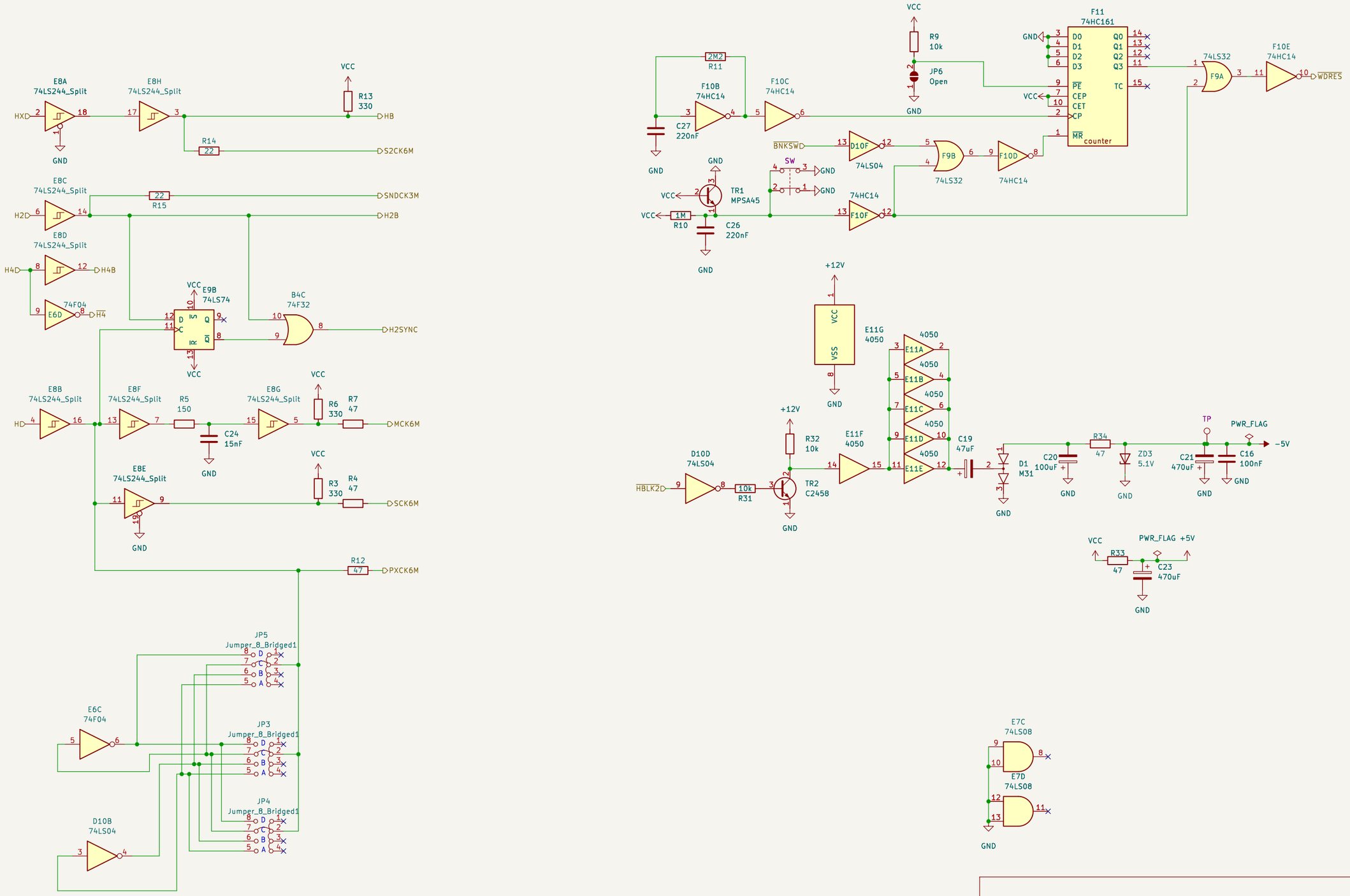

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Sheet: /Misc/

File: misc.kicad_sch

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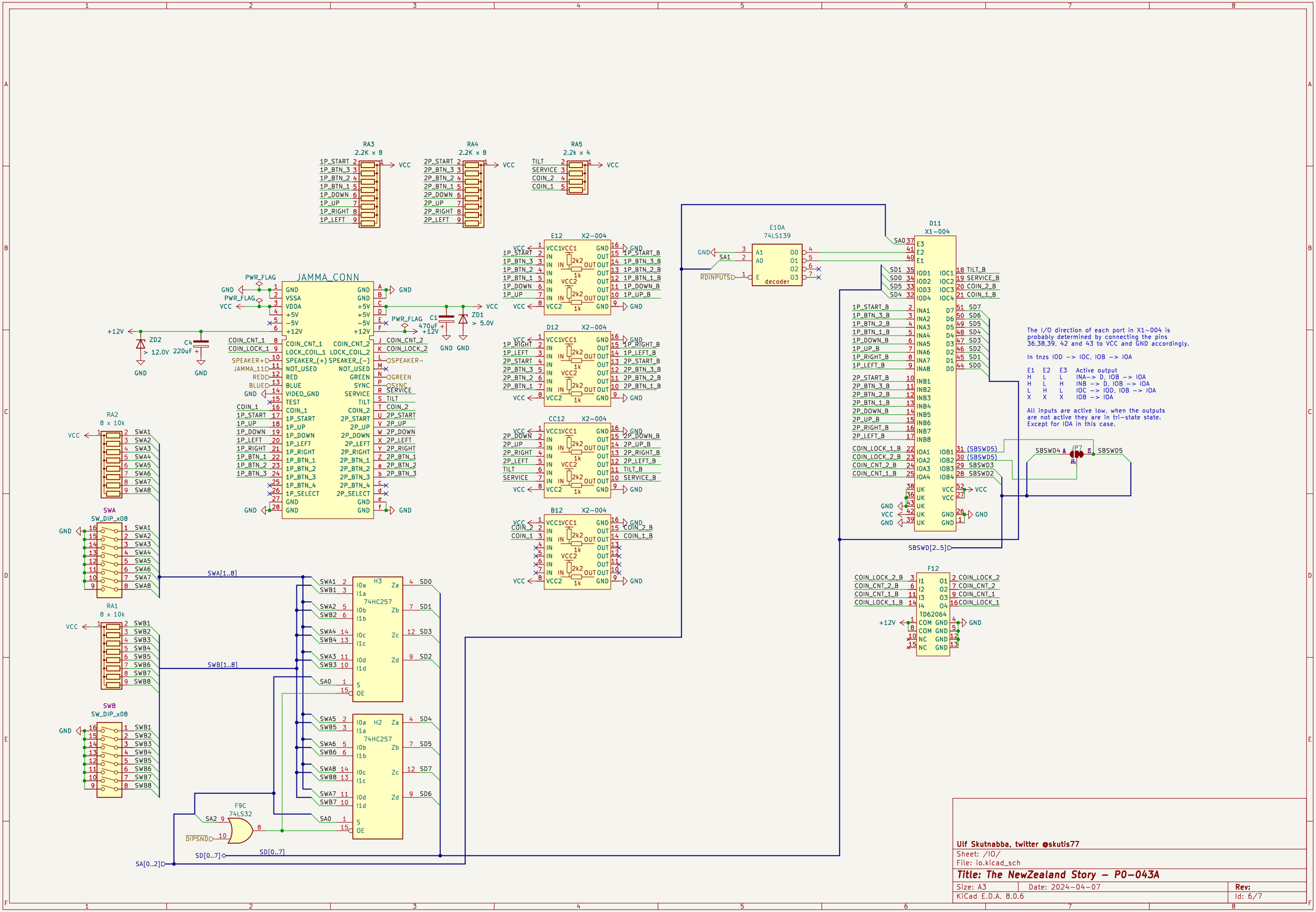
RA3
2.2K x 8
RA4
2.2K x 8
RA5
2.2k x 4
JAMMA_CONN
E12 X2-004
D12 X2-004
CC12 X2-004
B12 X2-004
E10A
74LS139
D11
X1-004
F12
TD62064
RA2
8 x 10k
SWA
SW_DIP_x08
RA1
8 x 10k
SWB
SW_DIP_x08
H3
74HC257
H2
74HC257
F9C
74LS32
ZD2
> 12.0V
C4
220uF
C1
470uF
ZD1
> 5.0V
JP7
SA[0..2]
SD[0..7]
SWA[1..8]
SWB[1..8]
SBSWD[2..5]
The I/O direction of each port in X1-004 is probably determined by connecting the pins 36,38,39, 42 and 43 to VCC and GND accordingly.
In tnzs IOD -> IOC, IOB -> IOA
E1 E2 E3 Active output
H L L INA-> D, IOB -> IOA
H L H INB -> D, IOB -> IOA
L H L IOC -> IOD, IOB -> IOA
X X X IOB -> IOA
All inputs are active low, when the outputs are not active they are in tri-state state. Except for IOA in this case.
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Sheet: /IO/
File: io.kicad_sch
Title: The NewZealand Story - PO-043A
Size: A3
Date: 2024-04-07
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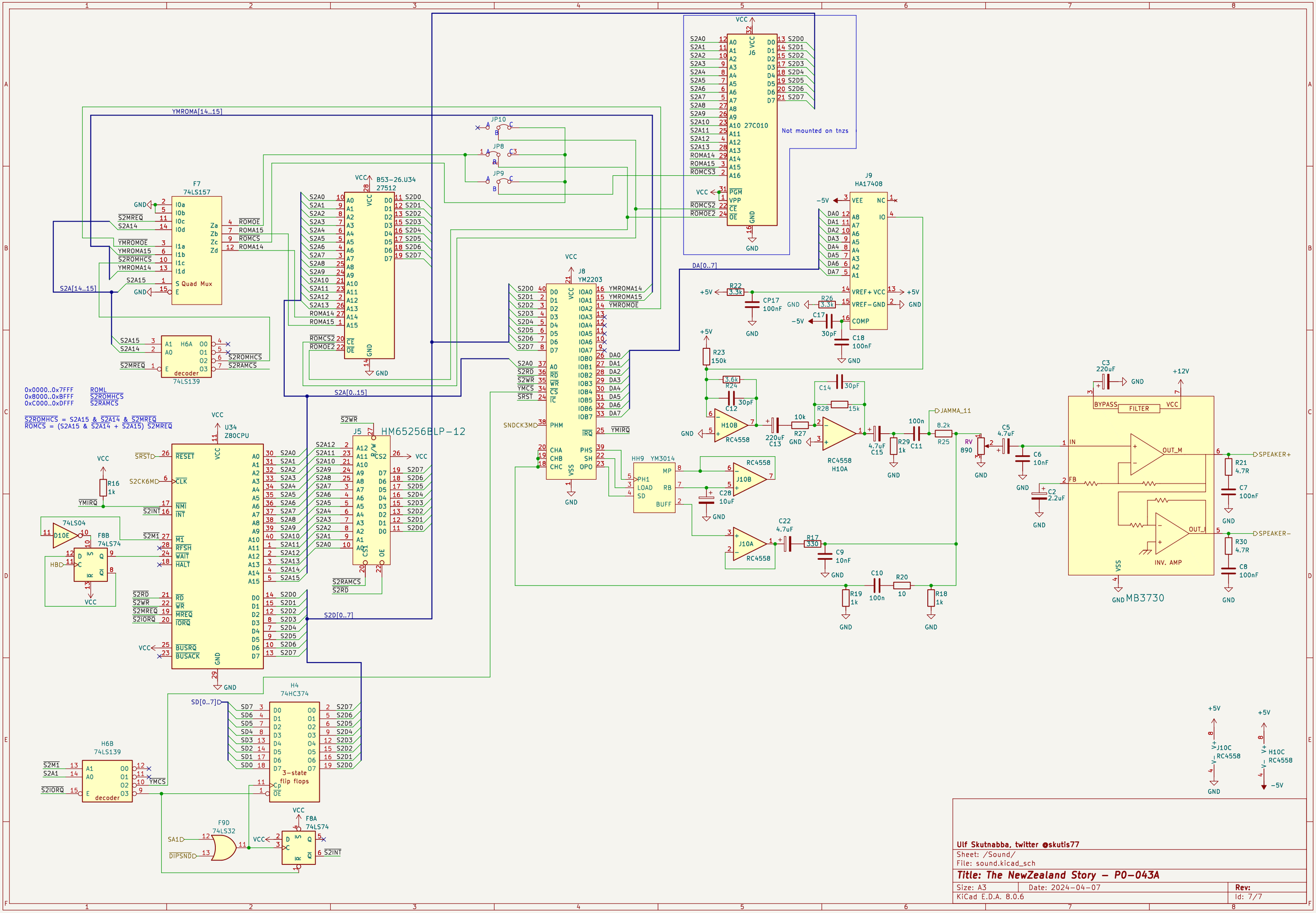

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Sheet: /Sound/

File: sound.kicad_sch

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