The Schematics have been analyzed from
a die picture by InfosecDJ.
The chip is identified as:

MSM OKi
79H041

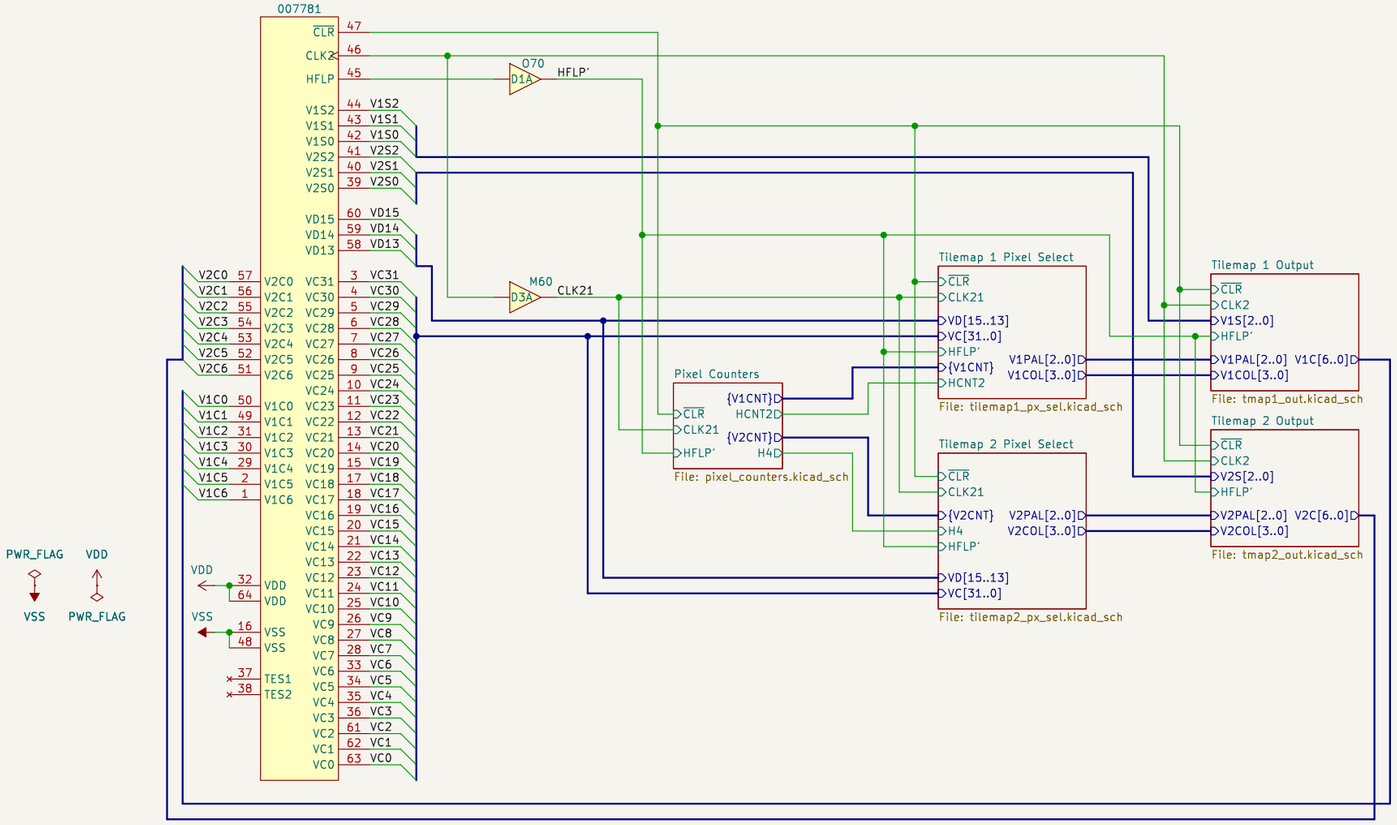
It is a MSM79V000 gate array
from the MSM70V000 series.
- 3289 Basic Cells
- 23 Columns, 143 Rows

The konami 007781 is a tilemap pixel shift register
with scroll. The tiles are 8x8 pixels, but the 007781
don't care about vertical line position. 007781 handles
two tilemaps at a time:
- V1, tilemap 1
- V2, tilemap 2

8 pixels, 4 bits each, of color data at a time are latched
into the registers. The palette code is latched 8 pixel
clocks earlier from VRAM. This is because the
data in the 007780 DRAM controller and DRAM takes 8
pixel clocks to process.

V1 latches pixels when the horizontal counter, going
from 0 to 7, goes to 2 (HCNT2) and V2 latches when
the horizontal counter goes to 4.
Data latched for:
- V1, when HCNT[2:0] == 2
- V2, when HCNT[2:0] == 4

The pixel code and palette color data are shifted
out between 1 to 9 pixel clocks after HCNT[2:0] == 4,
depending on if scroll or horizontal flip are active.

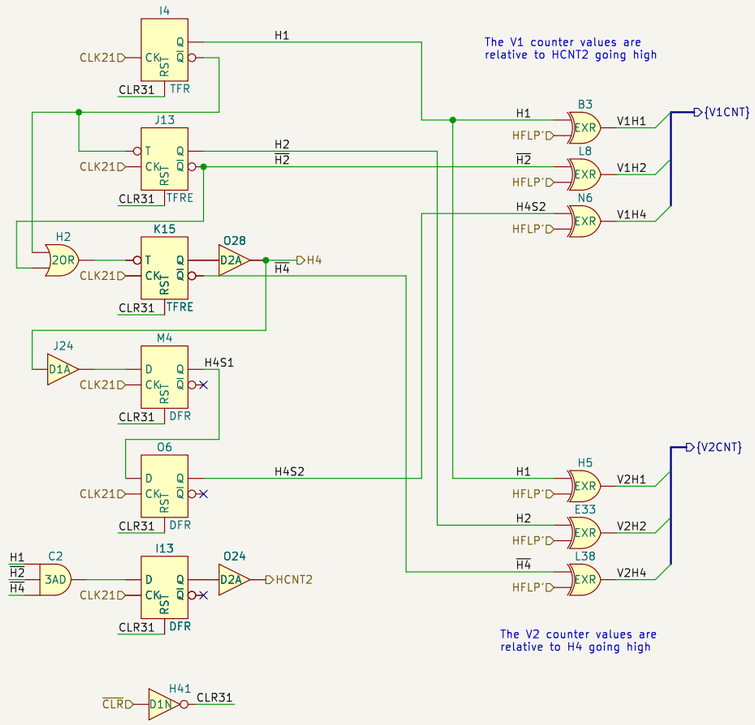


Ulf Skutnabba, twitter: @skutis77

Sheet: /
File: 007781.kicad_sch

Title: Konami 007781

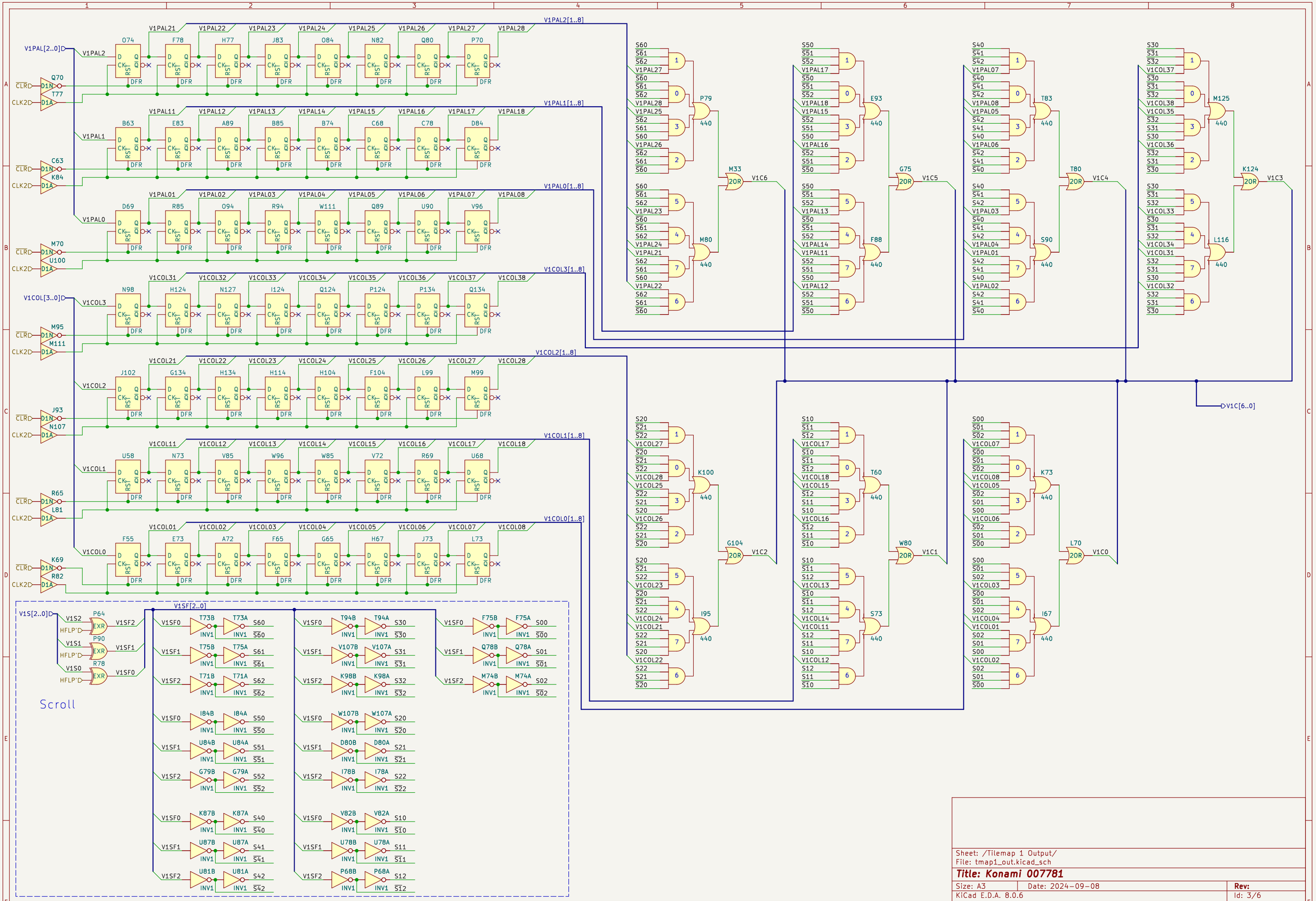
Size: A3	Date: 2024-09-08	**Rev:**
KiCad E.D.A. 8.0.6		Id: 1/6



Sheet: /Pixel Counters/
File: pixel_counters.kicad_sch

Title: Konami 007781

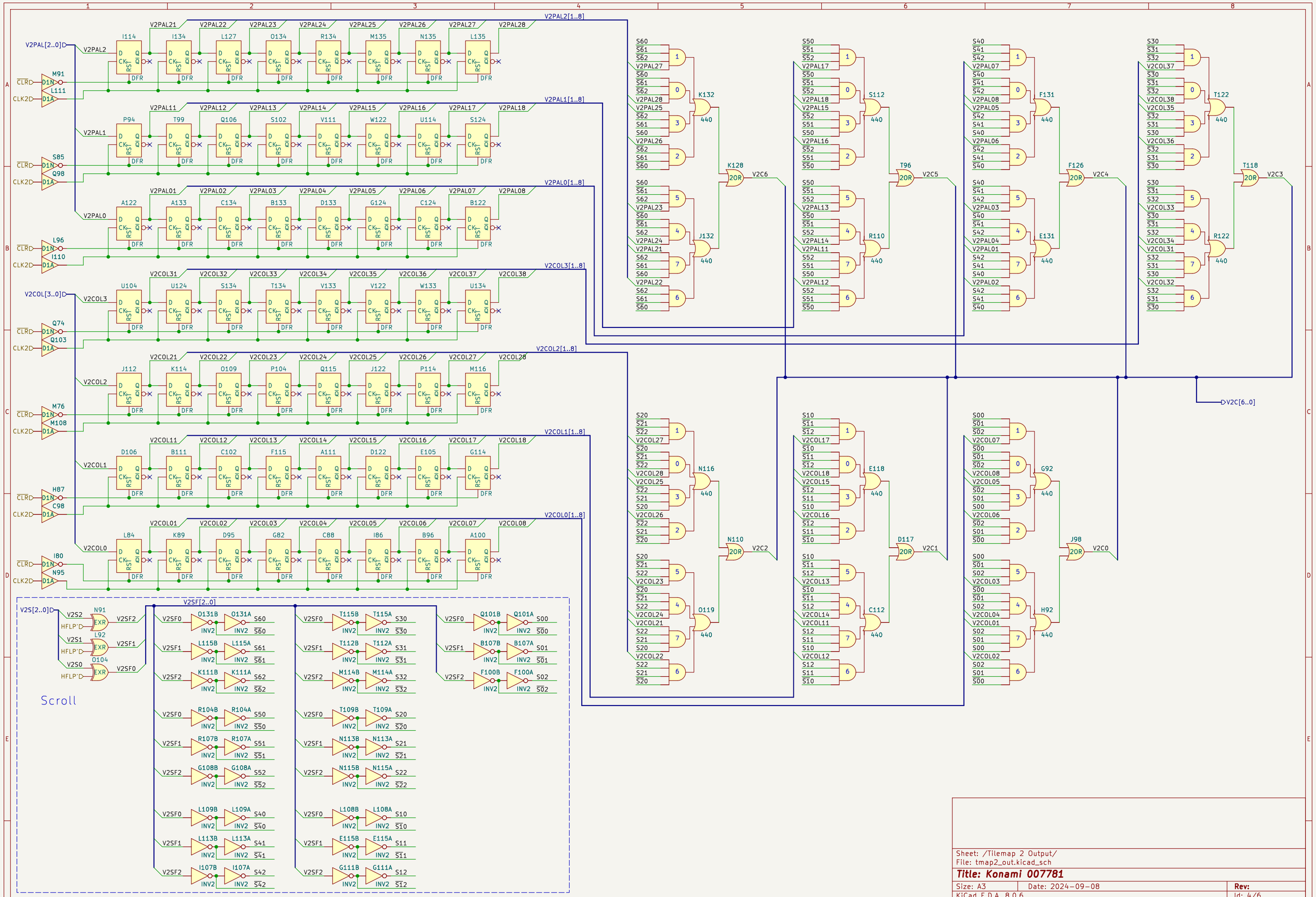
Size: A3	Date: 2024-09-08	Rev:
KiCad E.D.A. 8.0.6		Id: 2/6



Sheet: /Tilemap 1 Output/
File: tmap1_out.kicad_sch

Title: Konami 007781

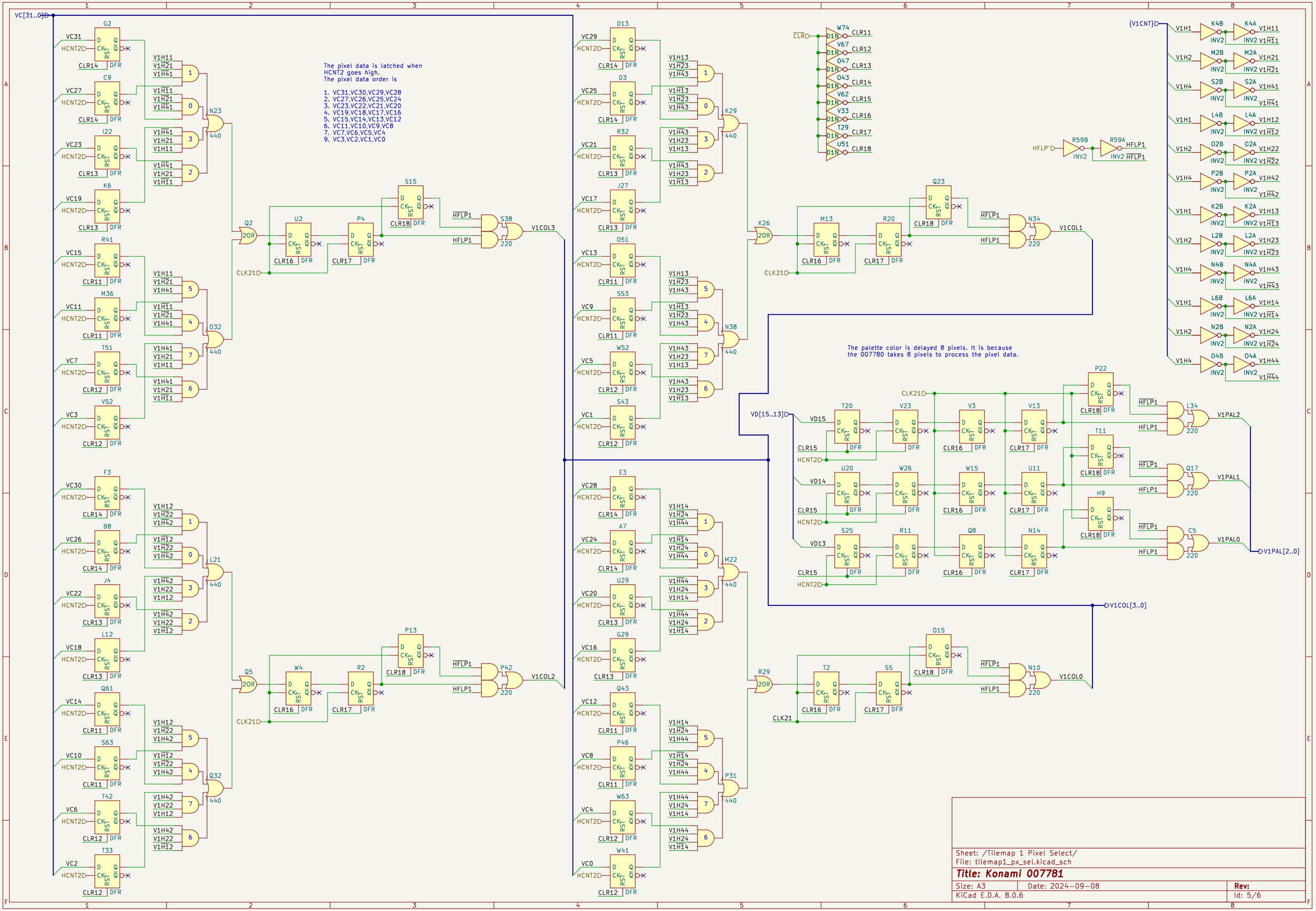
Size: A3	Date: 2024-09-08	Rev:
KiCad E.D.A. 8.0.6		Id: 3/6



Sheet: /Tilemap 2 Output/
File: tmap2_out.kicad_sch

Title: Konami 007781

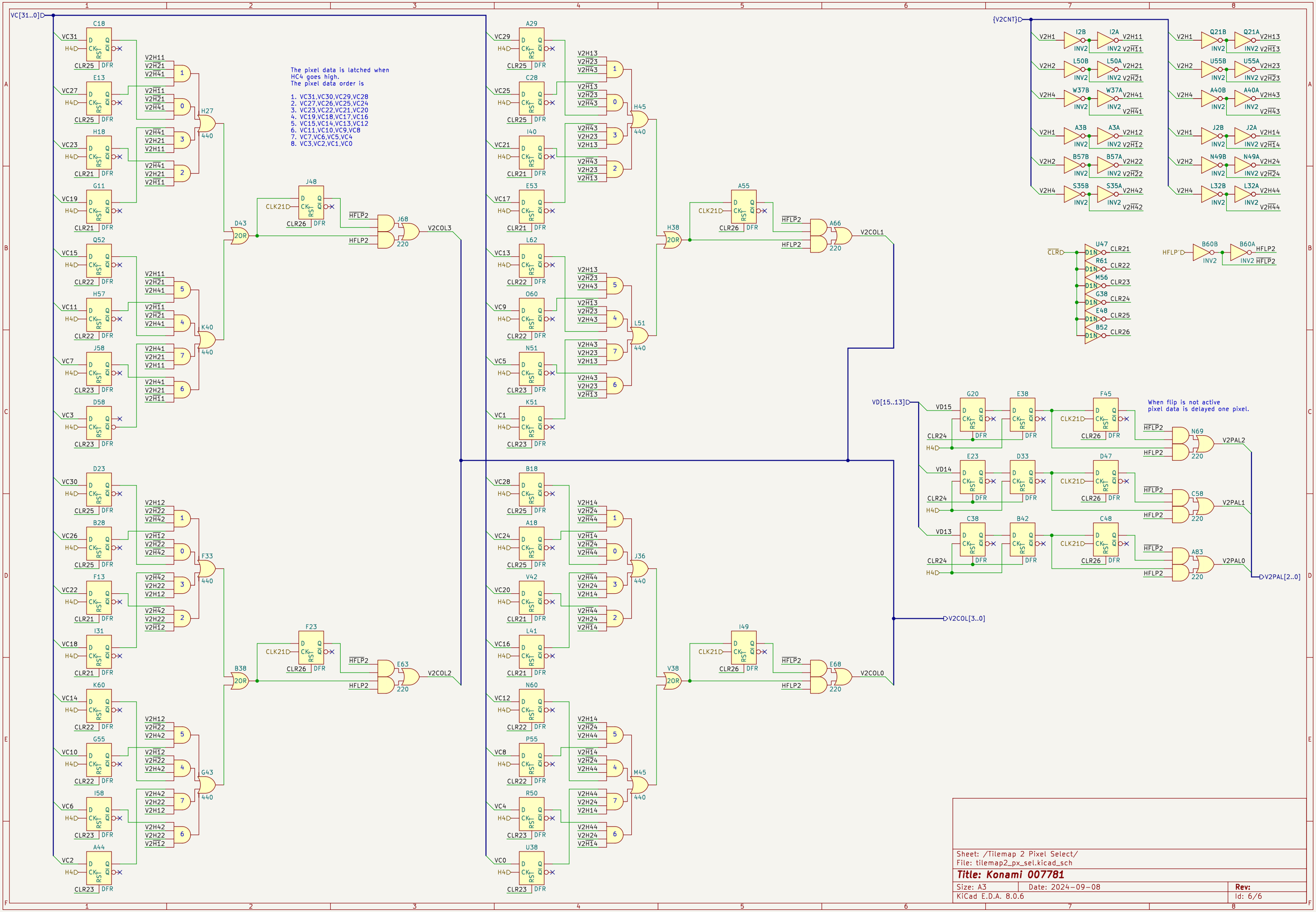
Size: A3	Date: 2024-09-08	Rev:
KiCad E.D.A. 8.0.6		Id: 4/6



Sheet: /Tilemap 1 Pixel Select/
File: tilemap1_px_sel.kicad_sch

Title: Konami 007781

Size: A3	Date: 2024-09-08	Rev:
KiCad E.D.A. 8.0.6		Id: 5/6



Sheet: /Tilemap 2 Pixel Select/
File: tilemap2_px_sel.kicad_sch

Title: Konami 007781

Size: A3	Date: 2024-09-08	Rev:
KiCad E.D.A. 8.0.6		Id: 6/6