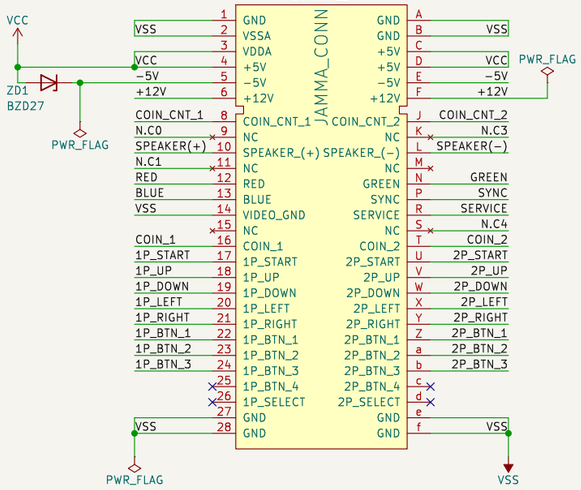
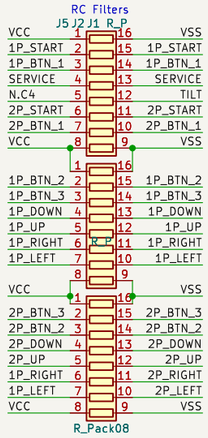
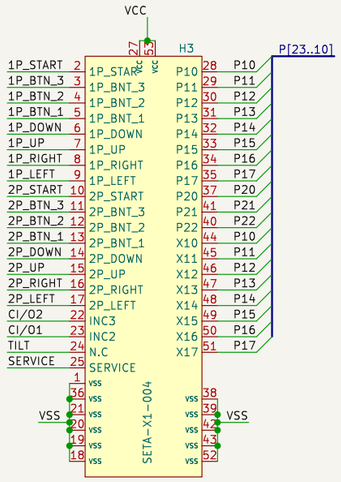
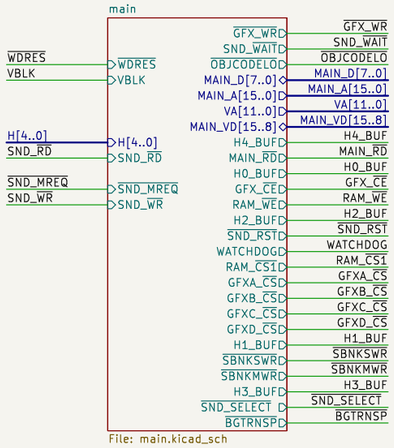
JM1

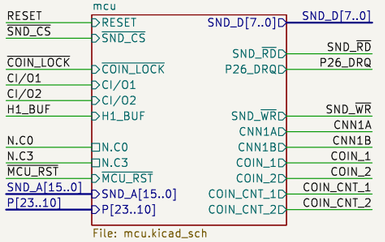


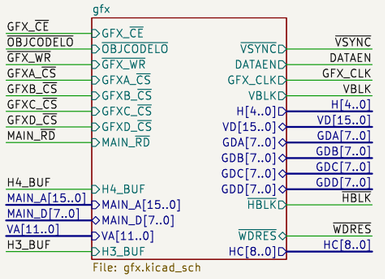
CABINET I/O

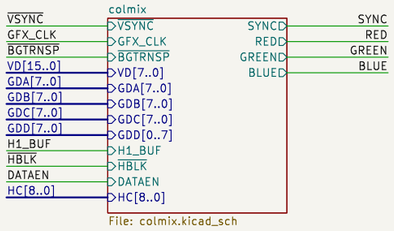


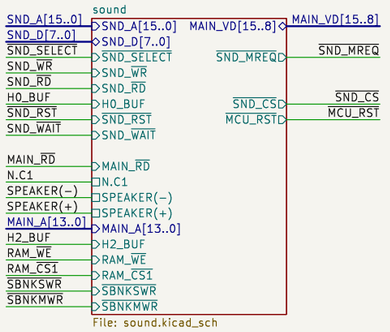










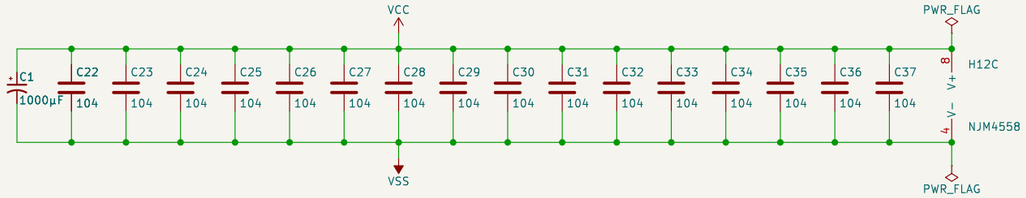


JOTEGO

Sheet: /
File: exterm.kicad_sch

Title: EXTERMINATION

Size: A3	Date: 29/08/2022	Rev: José Tejada G.
KiCad E.D.A. 8.0.6		Id: 1/10



H5E
74LS02

B7C
74LS74

B4C
74LS74

B3C
74LS74

B2E
74LS08

G13G
74LS04

C6E
74LS32

B6E
74LS08

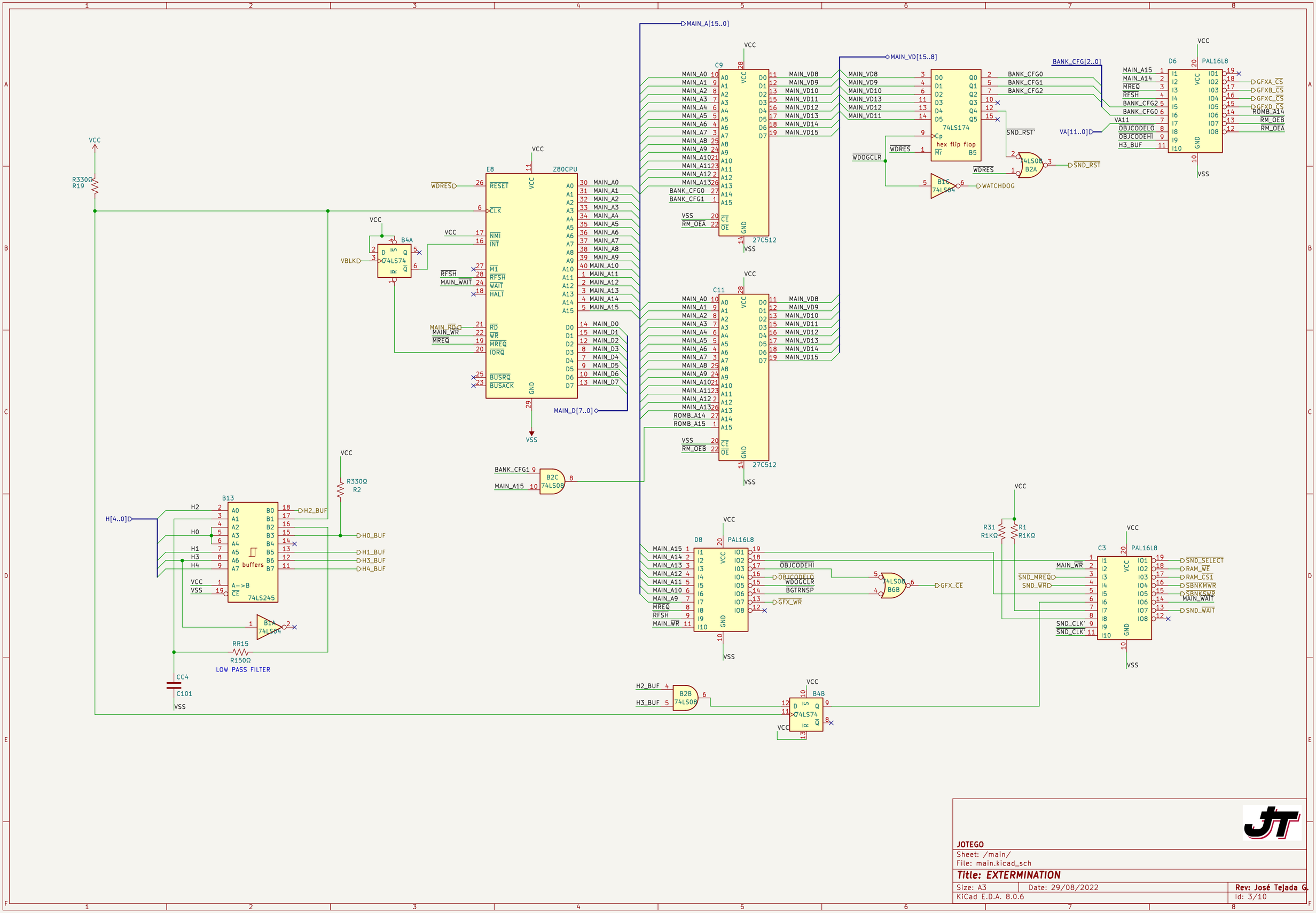
B1G
74LS04

JOTEGO

Sheet: /capacitors/
File: capacitors.kicad_sch

Title: EXTERMINATION

Size: A3	Date: 29/08/2022	**Rev: José Tejada G.**
KiCad E.D.A. 8.0.6		Id: 2/10



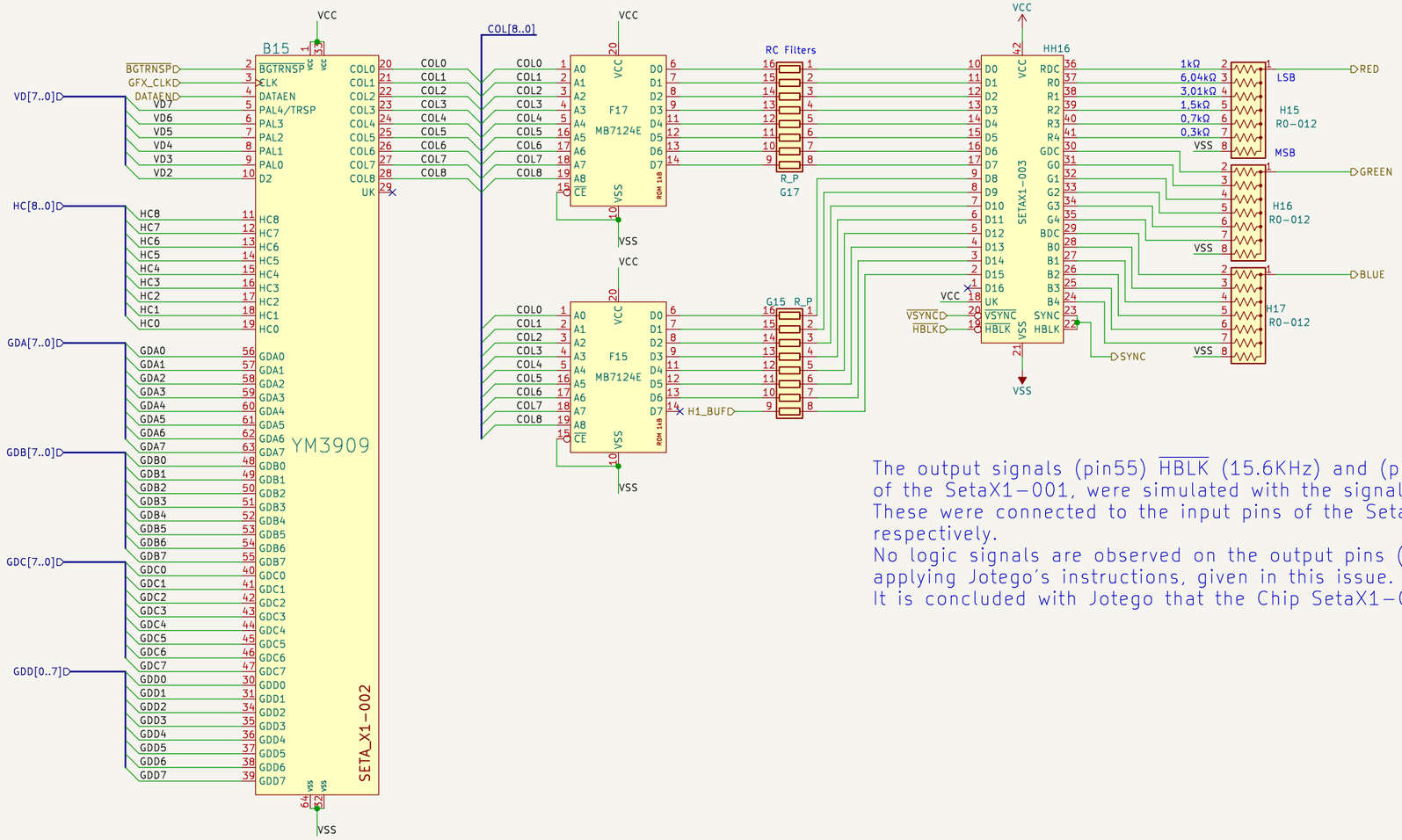
JOTEGO

Sheet: /main/

File: main.kicad_sch

Title: EXTERMINATION

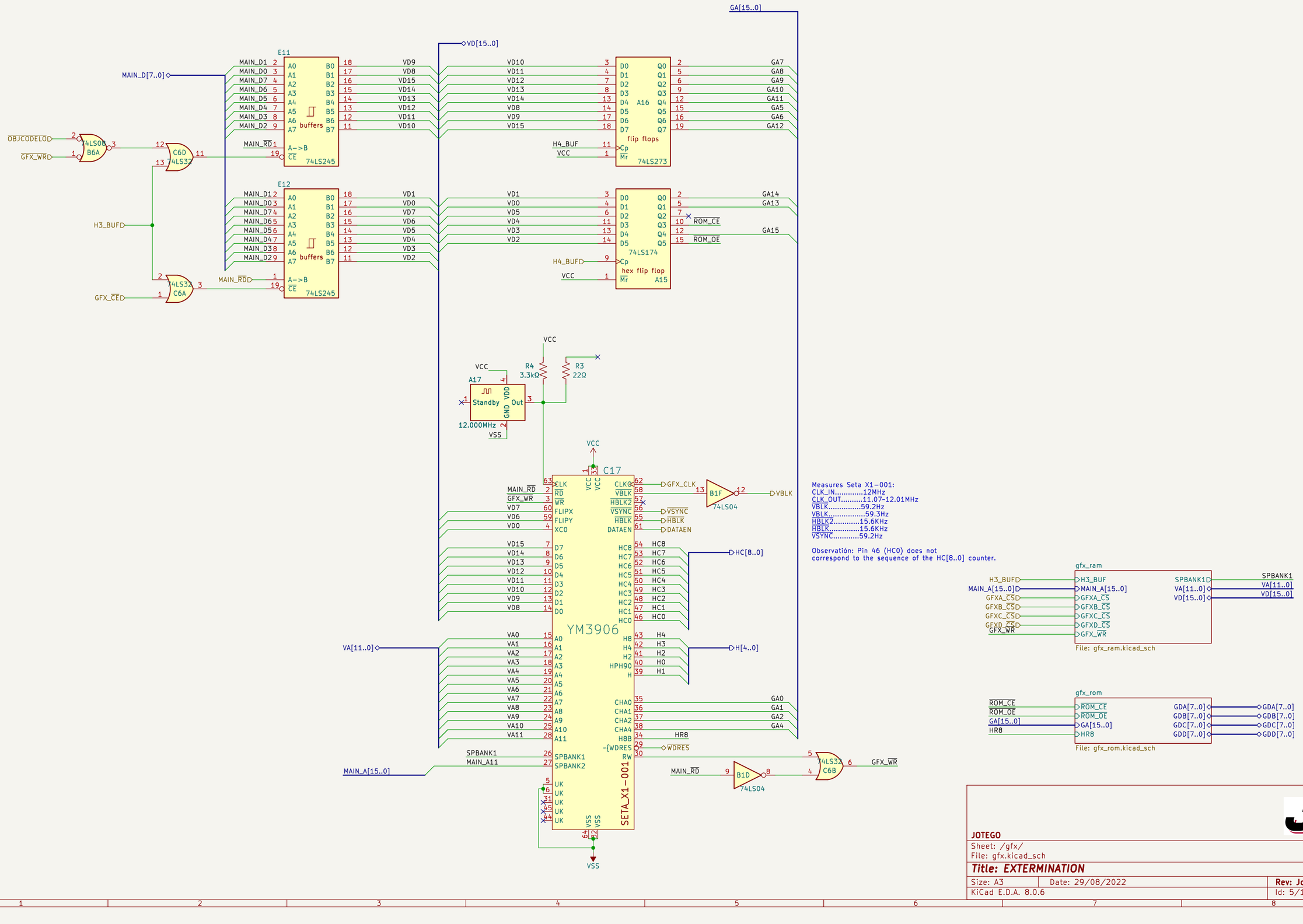
Size: A3	Date: 29/08/2022	Rev: José Tejada G.
KiCad E.D.A. 8.0.6		Id: 3/10

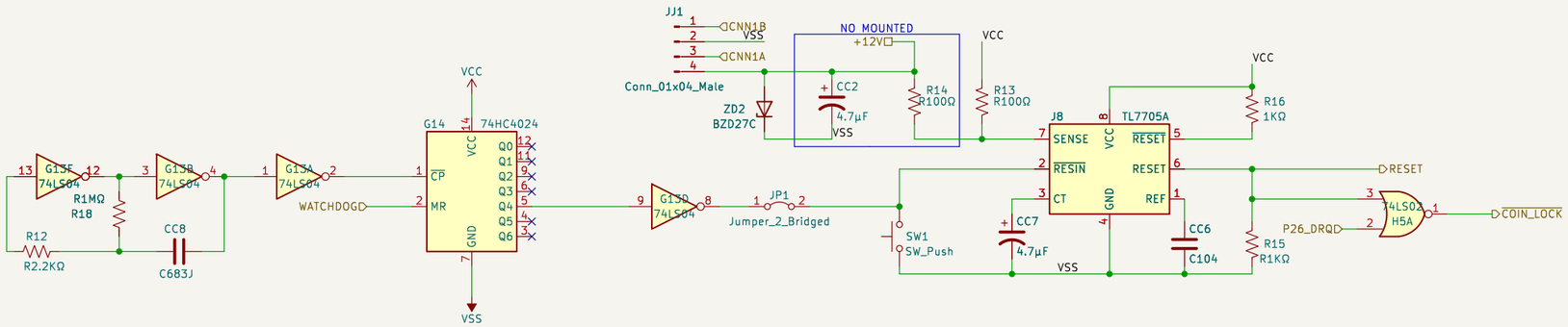


The output signals (pin55) $\overline{\text{HBLK}}$ (15.6KHz) and (pin56) $\overline{\text{VSYNC}}$ (59.2 Hz) of the SetaX1−001, were simulated with the signal generator and an inverter. These were connected to the input pins of the SetaX01−003 (pin 19 − 20), respectively.
No logic signals are observed on the output pins (22−23) HBLK − SYNC, applying Jotego's instructions, given in this issue.
It is concluded with Jotego that the Chip SetaX1−001 is broken.

JOTEGO

Sheet: /colmix/		
File: colmix.kicad_sch		
Title: EXTERMINATION		
Size: A3	Date: 29/08/2022	**Rev: José Tejada G.**
KiCad E.D.A. 8.0.6		Id: 4/10


GA[15..0]
VD[15..0]
E11
E12
MAIN_D[7..0]
MAIN_D1
MAIN_D0
MAIN_D7
MAIN_D6
MAIN_D5
MAIN_D4
MAIN_D3
MAIN_D2
A0 A1 A2 A3 A4 A5 A6 A7
B0 B1 B2 B3 B4 B5 B6 B7
buffers
MAIN_RD
A->B
CE
74LS245
VD9 VD8 VD15 VD14 VD13 VD12 VD11 VD10
VD1 VD0 VD7 VD6 VD5 VD4 VD3 VD2
OBJCODELO
GFX_WR
74LS08
B6A
C6D
74LS32
H3_BUF
GFX_CE
C6A
D0 D1 D2 D3 D4 D5 D6 D7
Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
A16
flip flops
H4_BUF
VCC
Cp
Mr
74LS273
GA7 GA8 GA9 GA10 GA11 GA5 GA6 GA12
74LS174
hex flip flop
A15
ROM_CE
ROM_OE
GA14 GA13 GA15
R4
3.3kΩ
R3
22Ω
A17
Standby
VDD
GND
Out
12.000MHz
VSS
C17
CLK
RD
WR
FLIPX
FLIPY
XC0
VCC
GFX_CLK
VBLK
HBLK2
VSYNC
HBLK
DATAEN
B1F
74LS04
HC8 HC7 HC6 HC5 HC4 HC3 HC2 HC1 HC0
HC[8..0]
YM3906
VA[11..0]
VA0 VA1 VA2 VA3 VA4 VA5 VA6 VA7 VA8 VA9 VA10 VA11
H8 H4 H2 HPH90 H
H4 H3 H2 H0 H1
H[4..0]
CHA0 CHA1 CHA2 CHA4 H8B
GA0 GA1 GA2 GA4 HR8
~{WDRES}
WDRES
RW
SPBANK1
SPBANK2
MAIN_A11
MAIN_A[15..0]
UK
SETA_X1-001
B1D
74LS32
C6B
GFX_WR
Measures Seta X1-001:
CLK_IN.....12MHz
CLK_OUT.....11.07-12.01MHz
VBLK.....59.2Hz
VBLK.....59.3Hz
HBLK2.....15.6KHz
HBLK.....15.6KHz
VSYNC.....59.2Hz
Observatión: Pin 46 (HC0) does not
correspond to the sequence of the HC[8..0] counter.
gfx_ram
H3_BUF
MAIN_A[15..0]
GFXA_CS
GFXB_CS
GFXC_CS
GFXD_CS
GFX_WR
SPBANK1
VA[11..0]
VD[15..0]
File: gfx_ram.kicad_sch
gfx_rom
ROM_CE
ROM_OE
GA[15..0]
HR8
GDA[7..0]
GDB[7..0]
GDC[7..0]
GDD[7..0]
File: gfx_rom.kicad_sch
JOTEGO
Sheet: /gfx/
File: gfx.kicad_sch
Title: EXTERMINATION
Size: A3
Date: 29/08/2022
Rev: José Tejada G.
KiCad E.D.A. 8.0.6
Id: 5/10

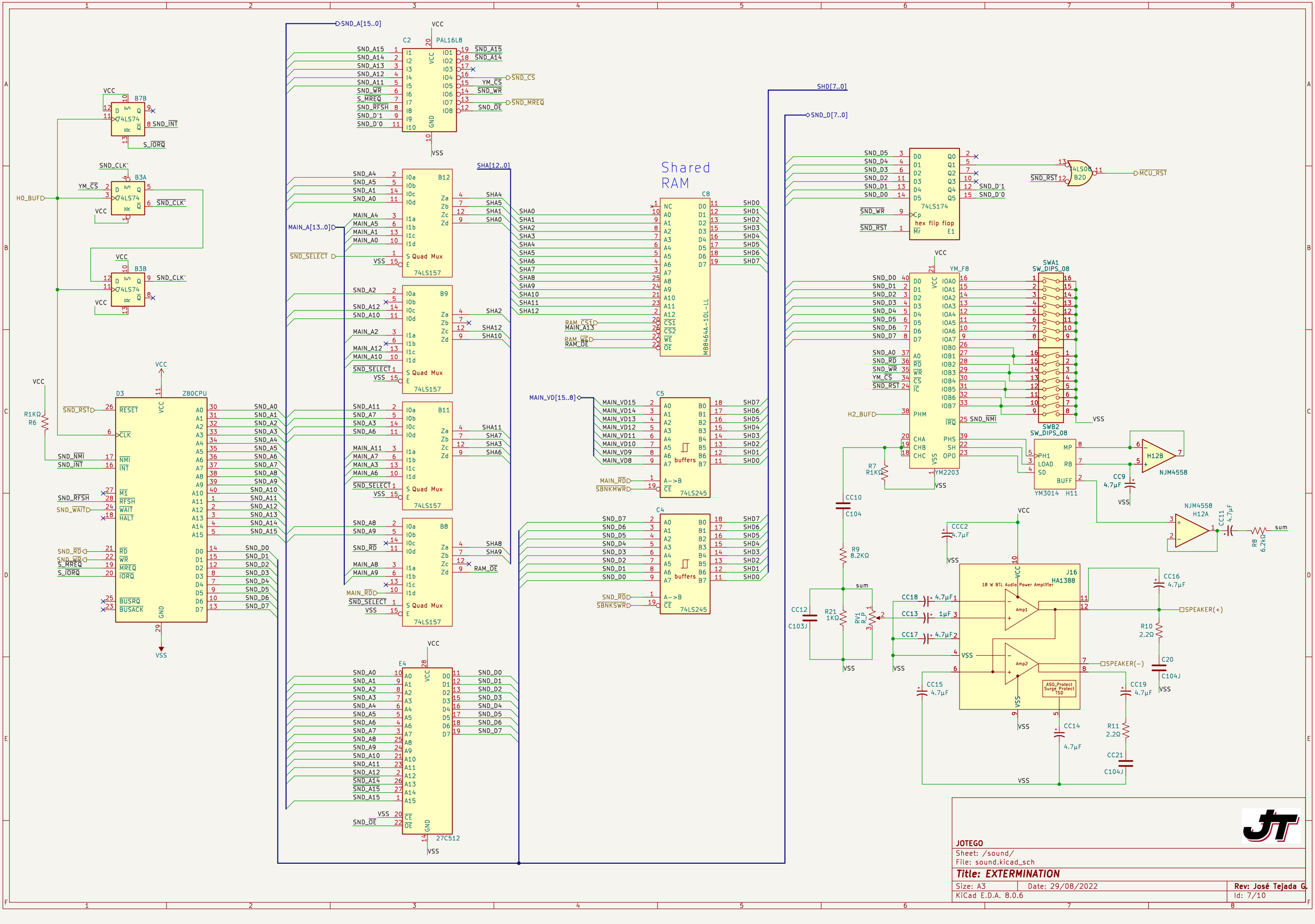


JOTEGO

Sheet: /watchdog/
File: watchdog.kicad_sch

Title: EXTERMINATION

Size: A3	Date: 29/08/2022	**Rev: José Tejada G.**
KiCad E.D.A. 8.0.6		Id: 6/10



JOTEGO

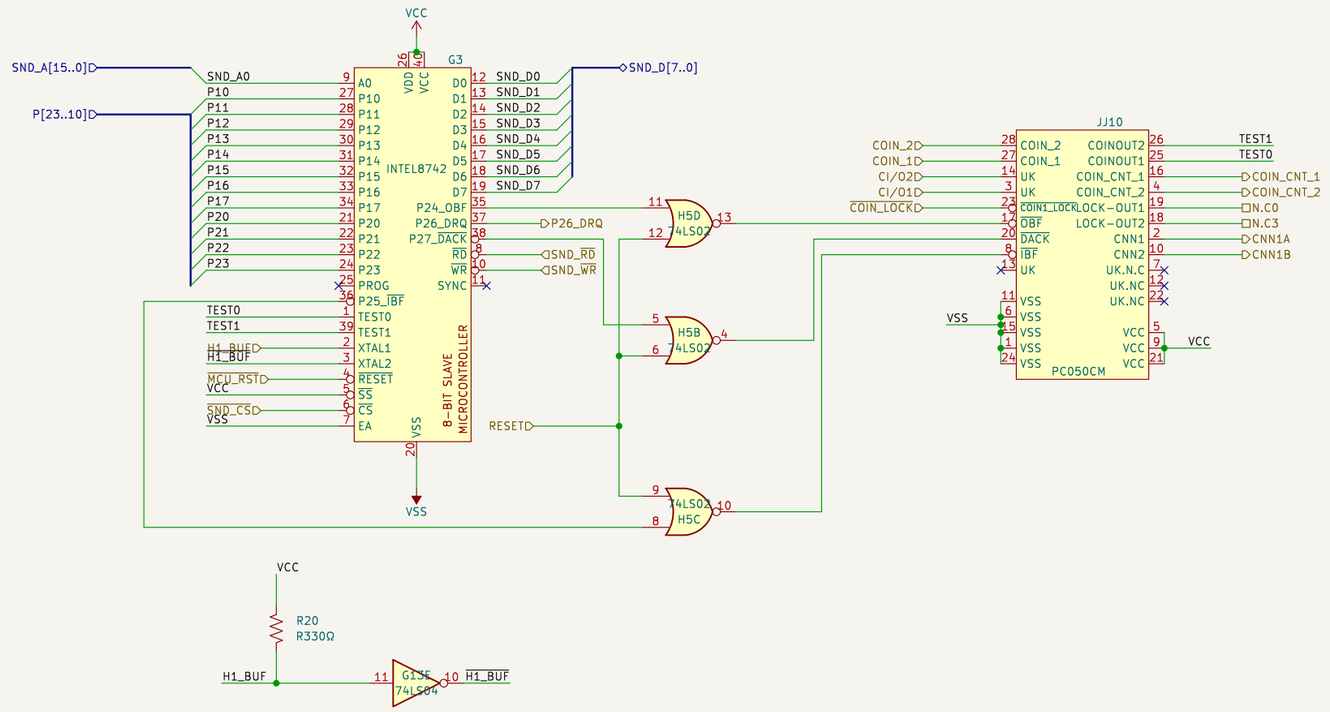
Sheet: /sound/

File: sound.kicad_sch

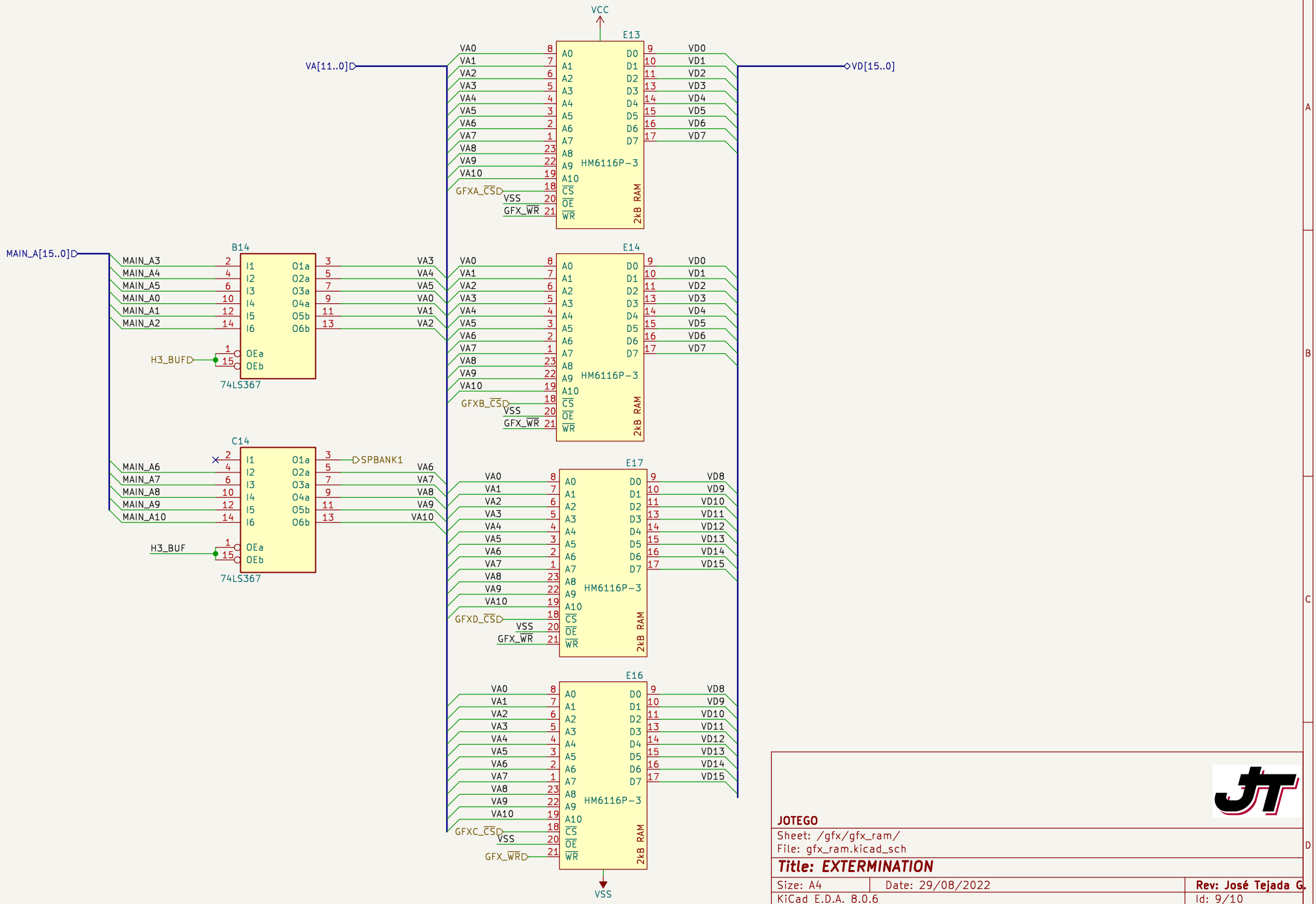
Title: EXTERMINATION

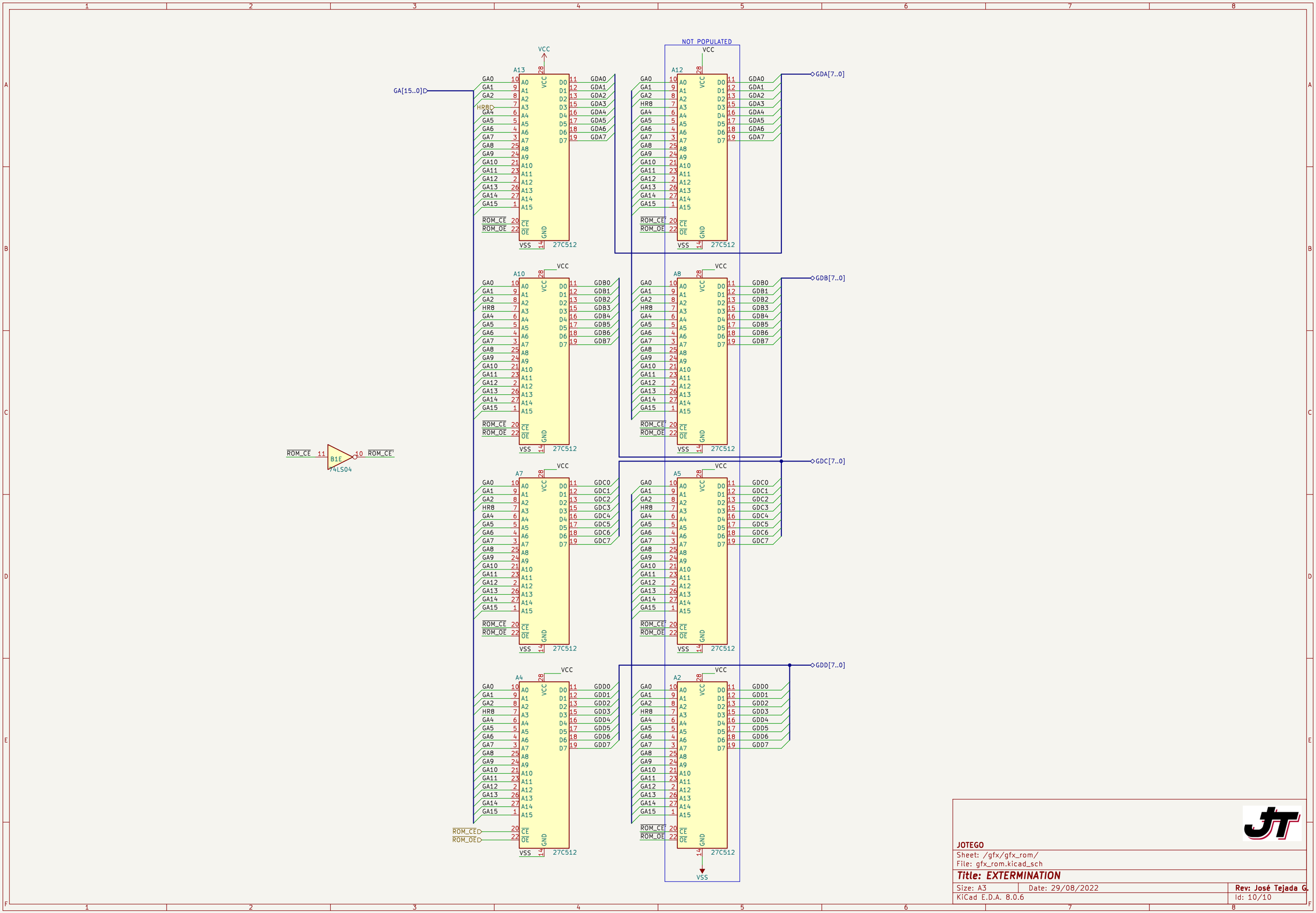
Size: A3 | Date: 29/08/2022 | Rev: José Tejada G.

KiCad E.D.A. 8.0.6 | Id: 7/10



JOTEGO		
Sheet: /mcu/		
File: mcu.kicad_sch		
Title: EXTERMINATION		
Size: A3	Date: 29/08/2022	**Rev: José Tejada G.**
KiCad E.D.A. 8.0.6		Id: 8/10


VCC
VA[11..0]
VD[15..0]
E13
E14
E17
E16
HM6116P-3
2kB RAM
GFXA_CS
GFXB_CS
GFXD_CS
GFXC_CS
GFX_WR
GFX_WRD
VSS
B14
C14
74LS367
H3_BUF
MAIN_A[15..0]
MAIN_A3
MAIN_A4
MAIN_A5
MAIN_A0
MAIN_A1
MAIN_A2
MAIN_A6
MAIN_A7
MAIN_A8
MAIN_A9
MAIN_A10
SPBANK1
JOTEGO
Sheet: /gfx/gfx_ram/
File: gfx_ram.kicad_sch
Title: EXTERMINATION
Size: A4
Date: 29/08/2022
KiCad E.D.A. 8.0.6
Rev: José Tejada G.
Id: 9/10


NOT POPULATED
VCC
A13
A12
A10
A8
A7
A5
A4
A2
GA[15..0]
GDA[7..0]
GDB[7..0]
GDC[7..0]
GDD[7..0]
HR8
ROM_CE
ROM_OE
VSS
27C512
B1E
74LS04
ROM_CE'
JOTEGO
Sheet: /gfx/gfx_rom/
File: gfx_rom.kicad_sch
Title: EXTERMINATION
Size: A3
Date: 29/08/2022
Rev: José Tejada G.
KiCad E.D.A. 8.0.6
Id: 10/10