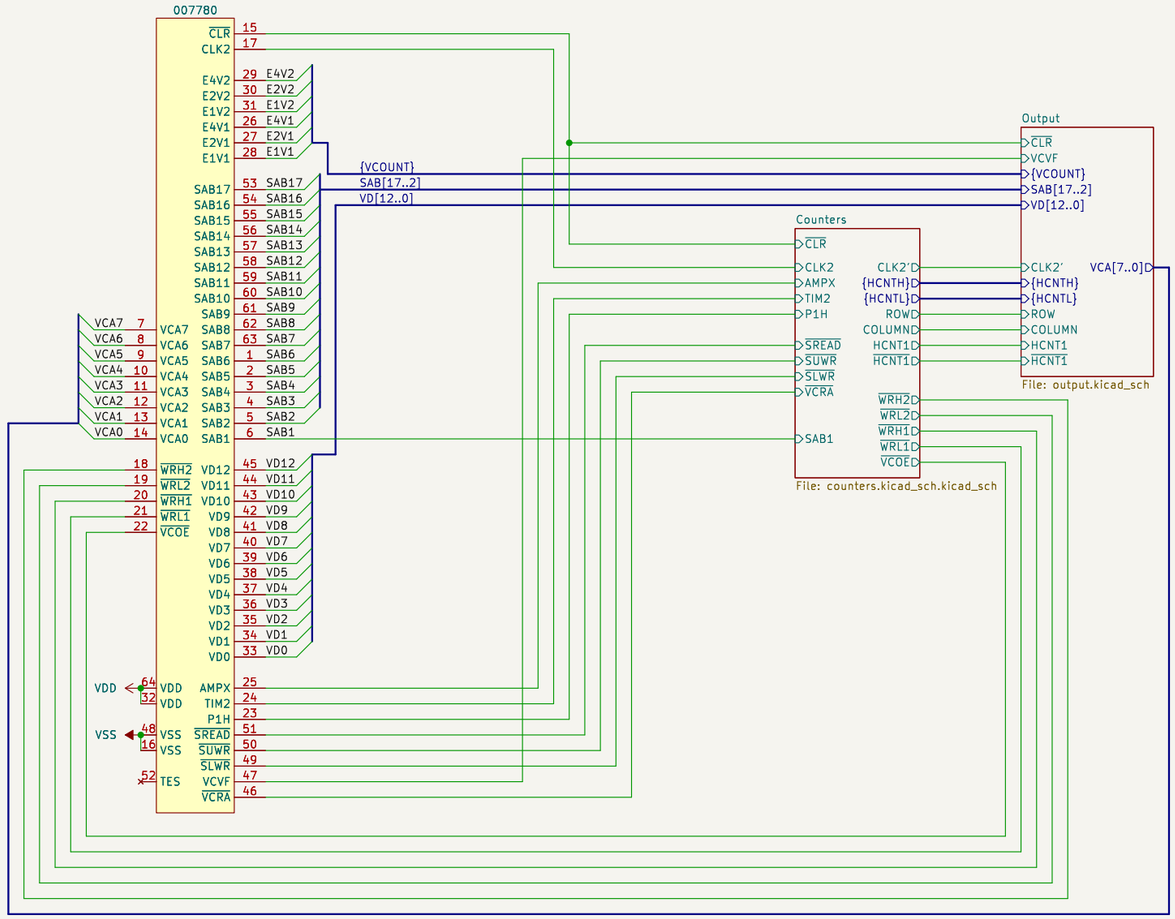
The Schematics have been analyzed from
a die picture by InfosecDJ.
The chip is identified as:

Fujitsu
673174U
C 1985

It is a C850AVB, MB673174 device
from the AVB-CMOS series.
- 852 Basic Cells
- 12 Columns, 71 Rows

Note: compared to the other devices from
the AVB series the VDD and VSS rails are flipped.
When analysed the picture has been flipped and rotated
to help identify cells.



Ulf Skutnabba, twitter: @skutis77

Sheet: /
File: 007780.kicad_sch

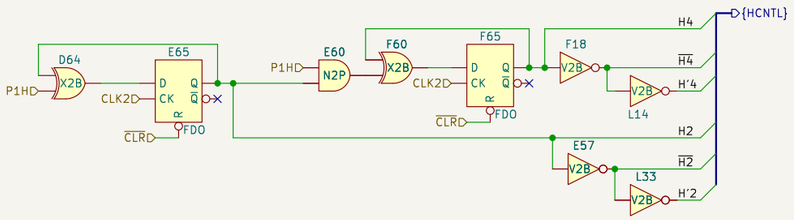
Title: Konami 007780

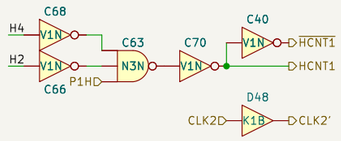
Size: A3	Date: 2024-07-28	Rev:
KiCad E.D.A. 8.0.6		Id: 1/3

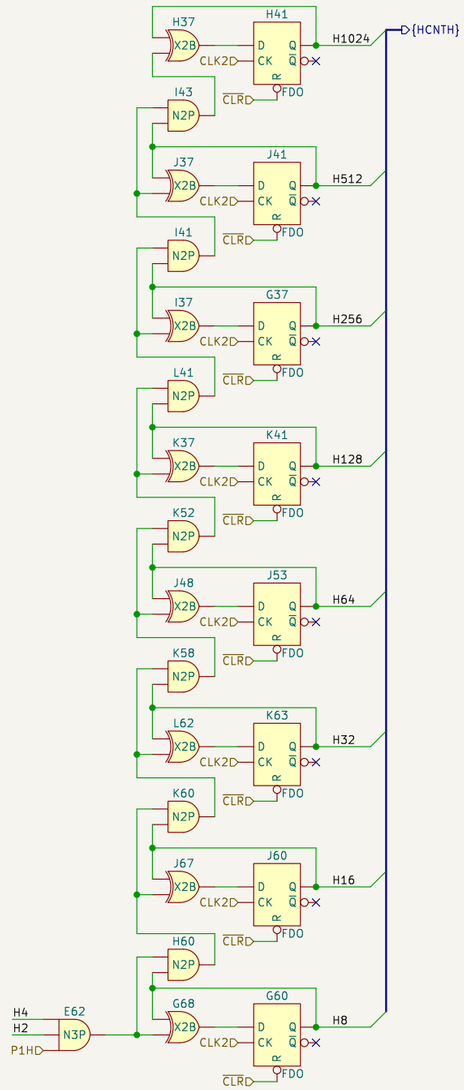
Horizontal clock P1H and $\overline{CLR}$ initiates the timing of the 007780. H2 and H4 are also generated which creates a 3-bit counter, HCNT, which controls the timing of the device. There are 2^3 = 8 different counter values: 0..7.

HCNT 0,1 Render Tilemap 1
HCNT 2,3 Render Tilemap 2
HCNT 4,5 Idle, writing to page 0
HCNT 6,7 CPU read/write cycle

TIM2 is active low during HCNT cycles 6 and 7.
When HCNT is 4 or 5 then row address = 0. The column address is incremented by one for each HCNT cycle. Is this used to not wear out the DRAM modules?







Sheet: /Counters/
File: counters.kicad_sch.kicad_sch

Title: Konami 007780

Size: A3 | Date: 2024-07-28 | **Rev:**
KiCad E.D.A. 8.0.6 | Id: 2/3

VD[12:5] = CA[7:0], row address
{VD[4:0],4V,2V,1V} = CA[7:0], column address

SAB[17:10] = CA[7:0], row address
SAB[9:2] = CA[7:0], column address

Tilemap 1 data latched when HCNT goes to 1.

Tilemap 2 data latched when HCNT goes to 4.

VCA[7..0]

{VCOUNT}

Sheet: /Output/	
File: output.kicad_sch	
Title: Konami 007780	
Size: A3	Date: 2024-07-28
KiCad E.D.A. 8.0.6	Id: 3/3
Rev:	