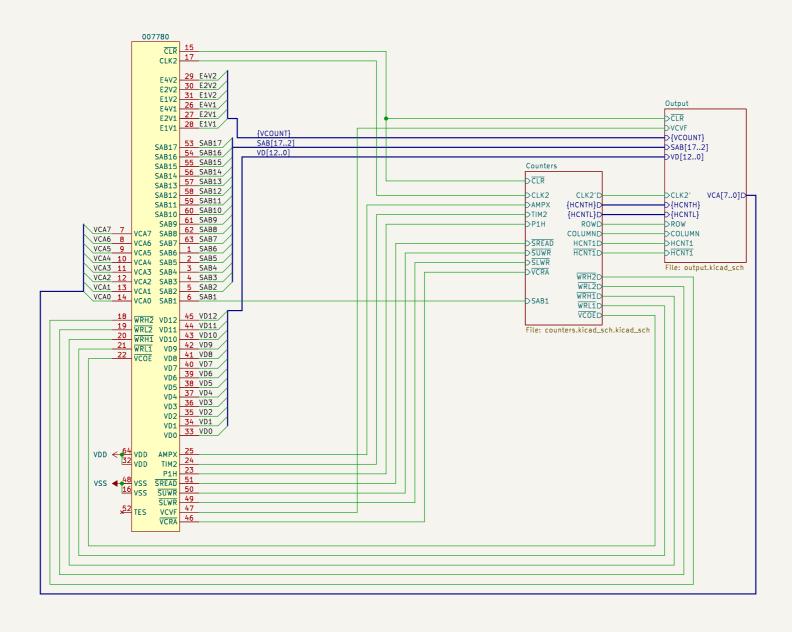
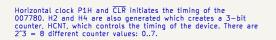
The Schematics have been analyzed from a die picture by InfosecDJ.
The chip is identified as:

It is a C850AVB, MB673174 device from the AVB-CMOS series. - 852 Basic Cells - 12 Columns, 71 Rows

Note: compared to the other devices from the AVB series the VDD and VSS rails are flipped. When analysed the picture has been flipped and rotated to help identify cells.



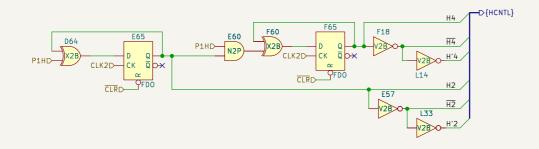
Ulf Skutnabba, twitter: @skutis77 Sheet: / File: 007780.kicad\_sch Title: Konami 007780 Size: A3 Date: 2024-07-28 KiCad E.D.A. 8.0.6

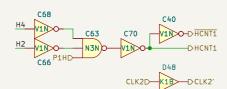


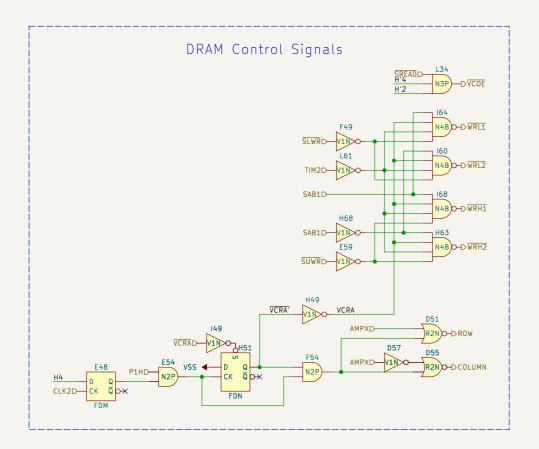
HCNT 0,1 Render Tilemap 1 HCNT 2,3 Render Tilemap 2

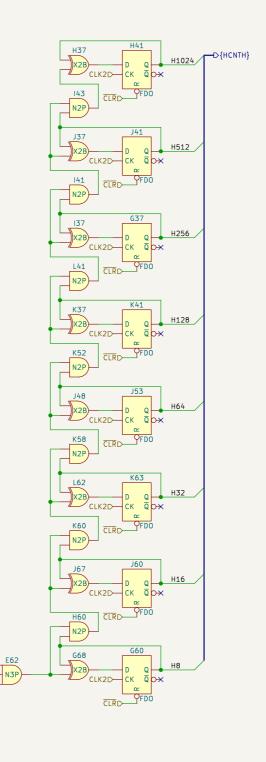
HCNT 4,5 Idle, writing to page HCNT 6.7 CPU read/write cycle

TIM2 is active low during HCNT cycles 6 and 7.
When HCNT is 4 or 5 then row address = 0. The column address
is incremented by one for each HCNT cycle. Is this used to
not wear out the DRAM modules?









| Sheet: /Counters/<br>File: counters.kicad_sch.kicad_sch |                  |                  |         |    |
|---|------------------|------------------|---------|----|
| Title: Kona   | ami 007780       |                  |         |    |
| Size: A3  | Date: 2024-07-28 | Date: 2024-07-28 |         |    |
| KiCad E.D.A. 8.0.6                                      |                  |                  | ld: 2/3 | ], |
|   | 7                |                  | - Ω     |    |

