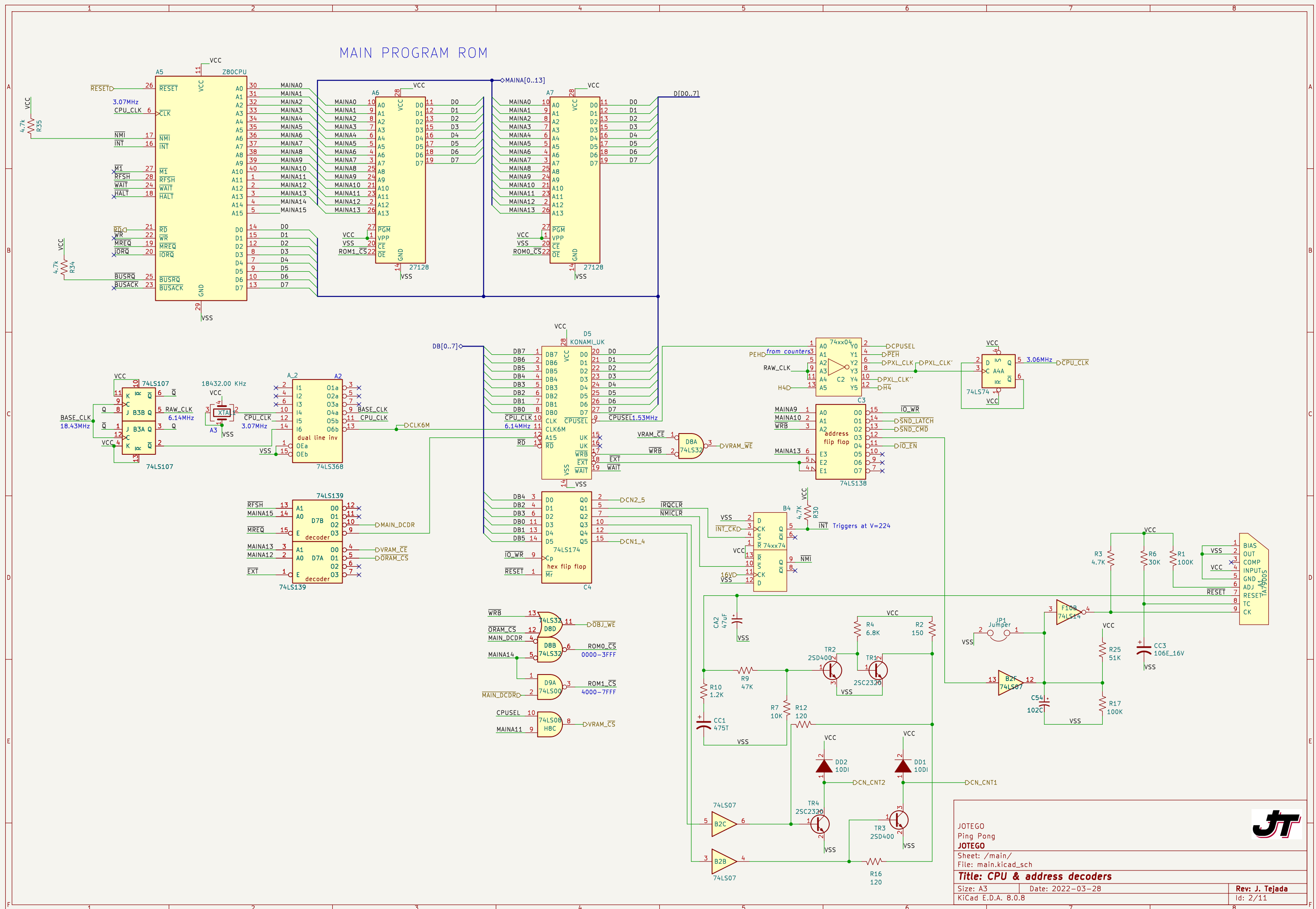


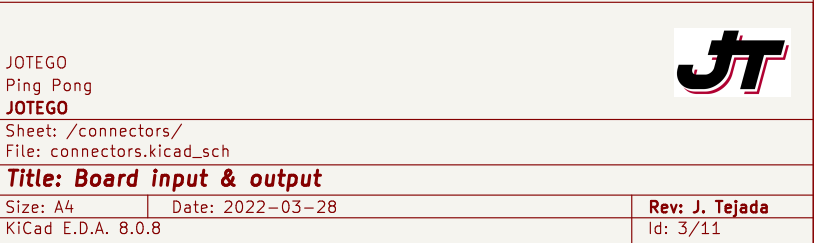
JOTEGO
Ping Pong
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Sheet: /
File: pingpong.kicad_sch
Title: Ping Pong

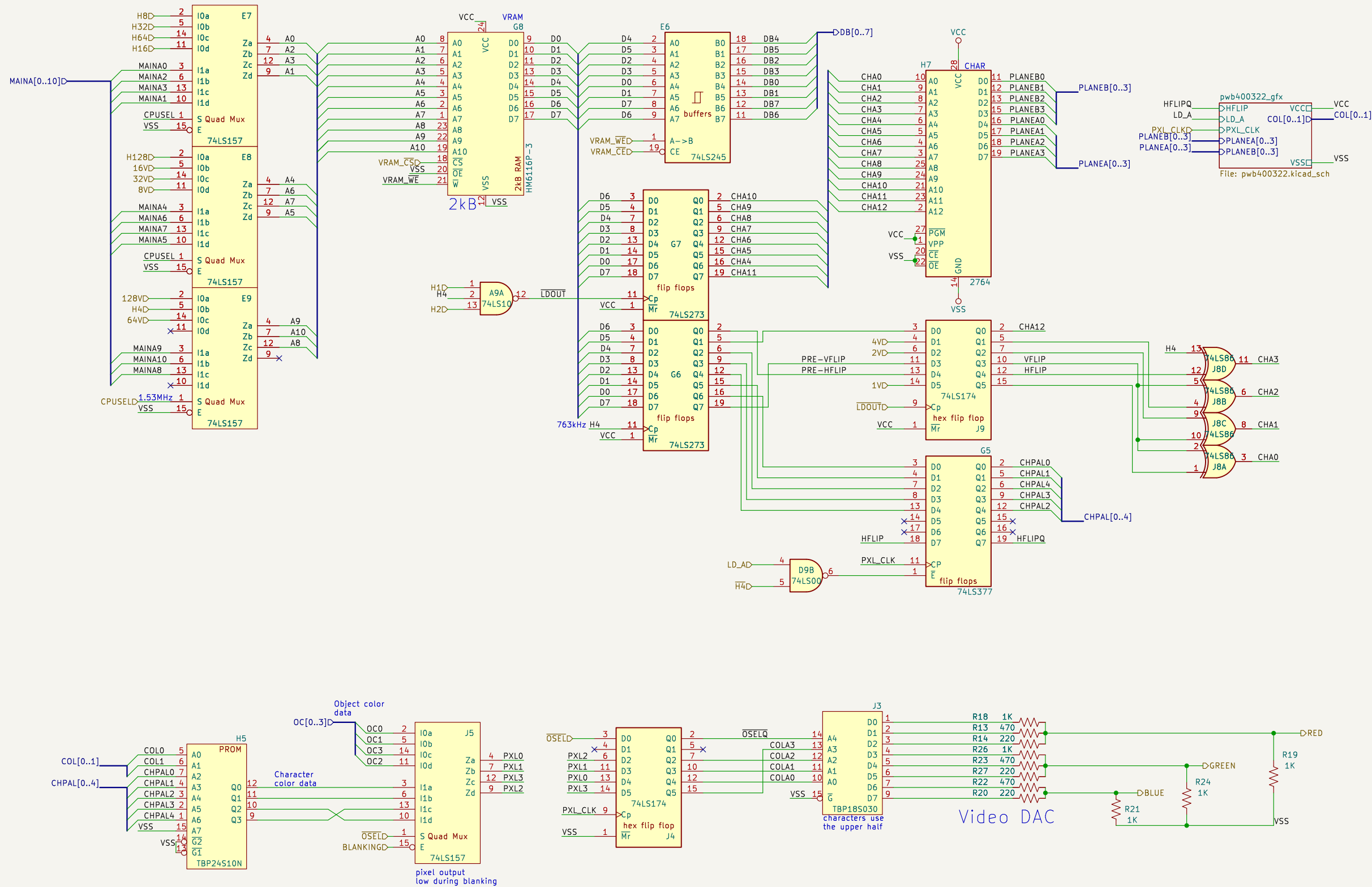


GX555

Size: A4 Date: 2022-03-28 Rev: J. Tejada
KiCad E.D.A. 8.0.8 Id: 1/11









This is a small board soldered to a DIP-28 footprint. It appears twice in the design

PWB-400322

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Sheet: /gfx/pwb400322_gfx/
File: pwb400322.kicad_sch

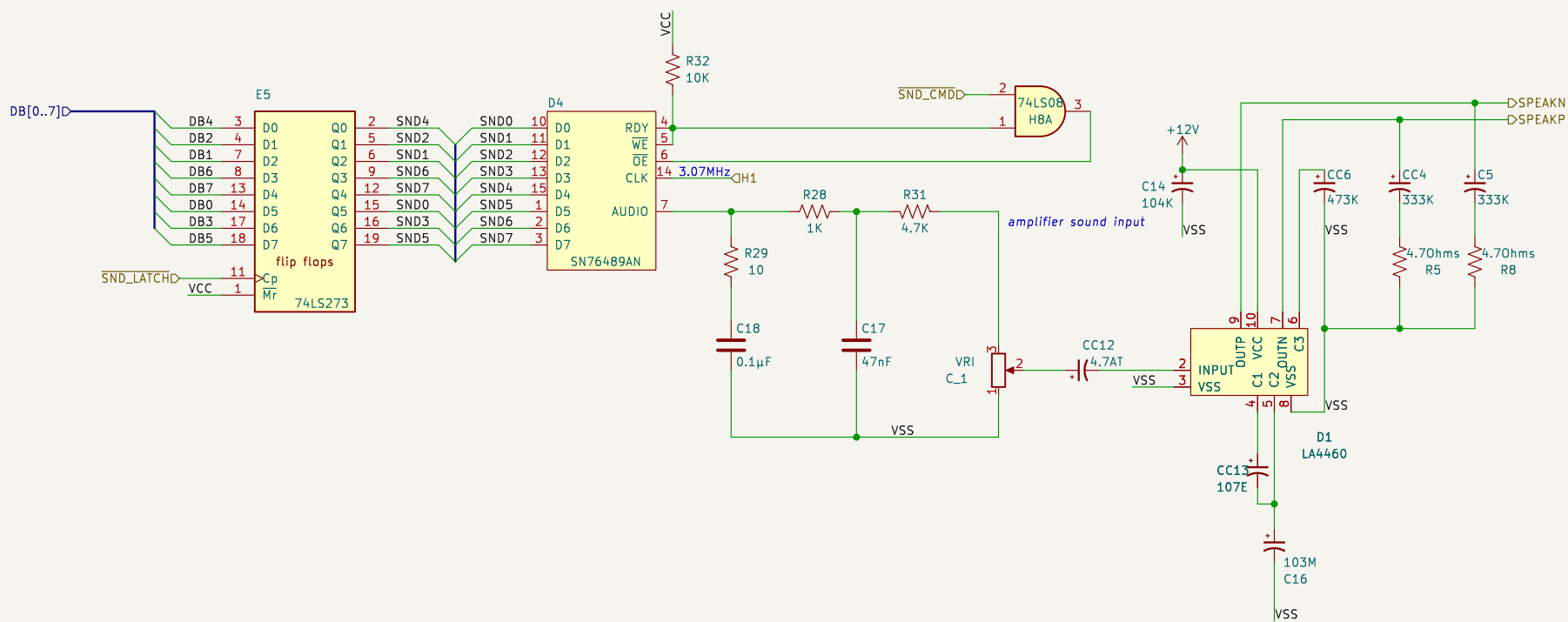
Title: Pixel shift register

Size: A4 Date: 2022-03-28

KiCad E.D.A. 8.0.8

Rev: J. Tejada

Id: 5/11



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Sheet: /sound/
File: sound.kicad_sch

Title: Sound generator

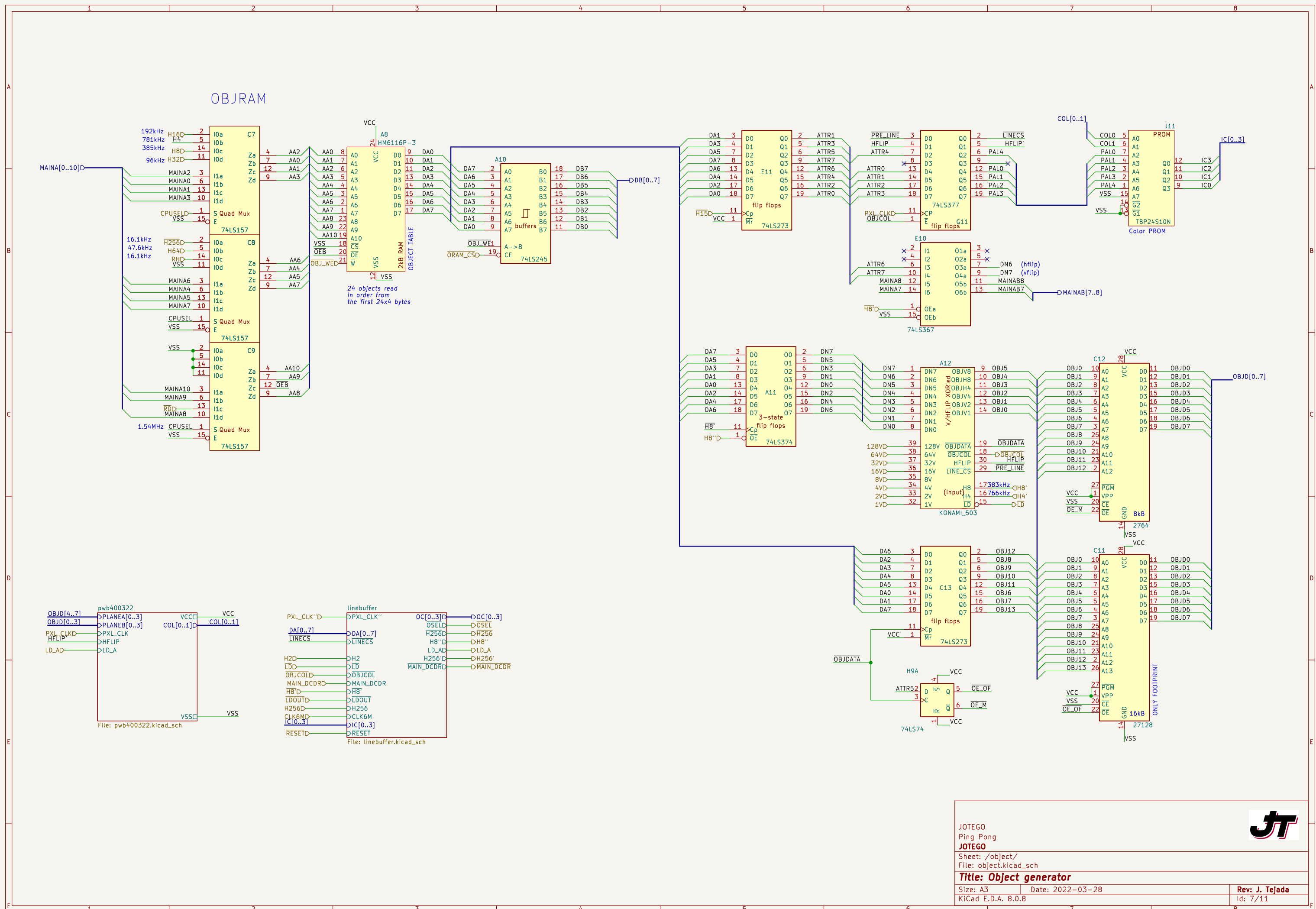
Size: A4 Date: 2022-03-28

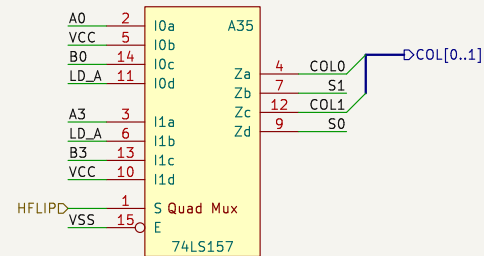
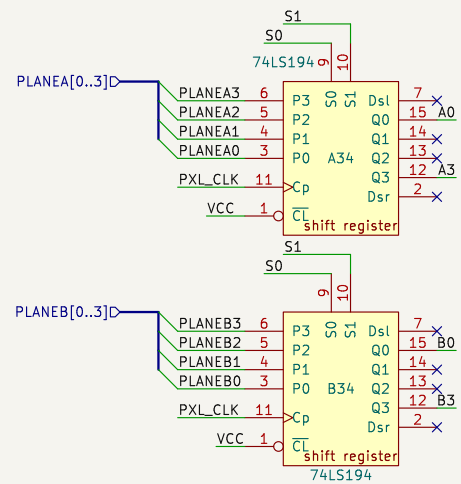
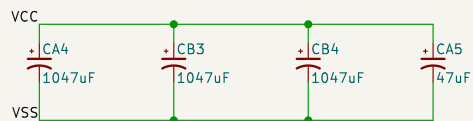
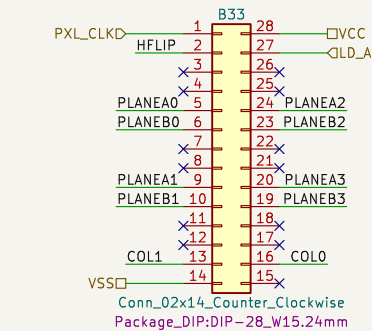
KiCad E.D.A. 8.0.8

Rev: J. Tejada

Id: 6/11








This is a small board soldered to a DIP-28 footprint. It appears twice in the design

PWB-400322

JOTEGO Ping Pong JOTEGO		
Sheet: /object/pwb400322/ File: pwb400322.kicad_sch		
Title: Pixel shift register		
Size: A4	Date: 2022-03-28	Rev: J. Tejada
KiCad E.D.A. 8.0.8	Id: 8/11	



Title: Double line buffer



Horizontal Counter

The Horizontal Counter uses two 74LS161 counters. The first counter (C6) is clocked by H1D (3.06MHz) and has its Q0-Q3 outputs connected to H2, H4, H8, and H16. The second counter (D6) is clocked by PXL_CLK'D (6.17MHz) and has its Q0-Q3 outputs connected to H32, H64, H128, and H256. The H256 signal is used to generate the right half of the screen (RH) and the horizontal sync (HS) signal. The HS signal is generated by an AND gate (H11B) and is used to generate the horizontal sync (HS) and the horizontal blanking (HB) signal.

Vertical Counter

The Vertical Counter uses two 74LS161 counters. The first counter (G10) is clocked by VSS and has its Q0-Q3 outputs connected to 4kHz, 2kHz, 1kHz, and 16V. The second counter (G9) is clocked by VSS and has its Q0-Q3 outputs connected to 32V, 64V, 128V, and 256V. The 256V signal is used to generate the vertical sync (VS) and the vertical blanking (VB) signal. The VS signal is generated by an AND gate (A9B) and is used to generate the vertical sync (VS) and the vertical blanking (VB) signal.

74LS139 Decoder

The 74LS139 decoder is used to generate the game state signals (H8', H4', H15). It has three inputs (A1, A0, E) and four outputs (00, 01, 02, 03). The inputs are connected to H8', H4', and H1D. The outputs are connected to H8', H4', and H15.

Game State Signals

The game state signals are generated by the 74LS139 decoder and are used to control the game. The signals are H8', H4', and H15. H8' is the horizontal sync signal, H4' is the horizontal blanking signal, and H15 is the horizontal sync signal.

Horizontal Sync and Blanking

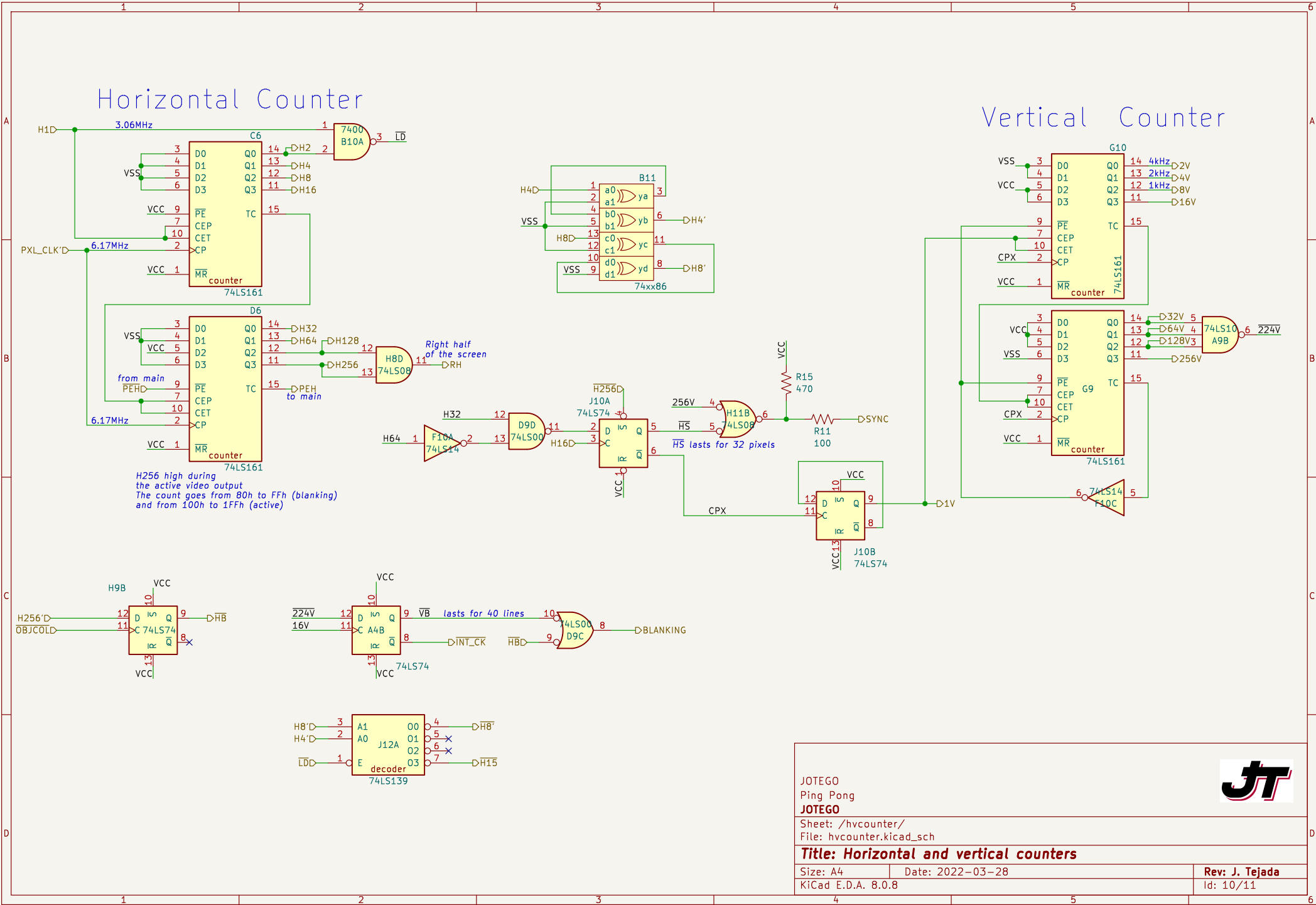
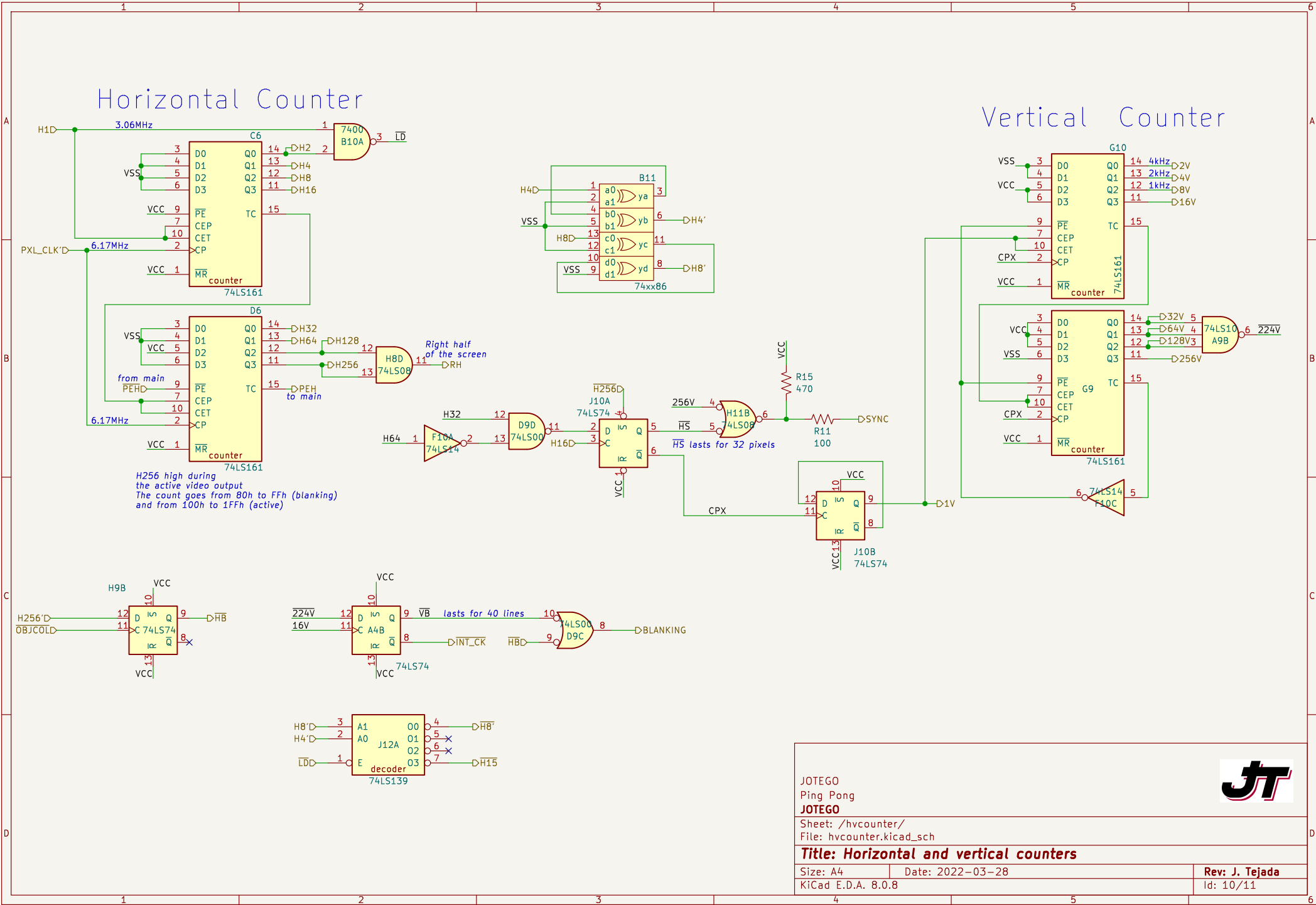
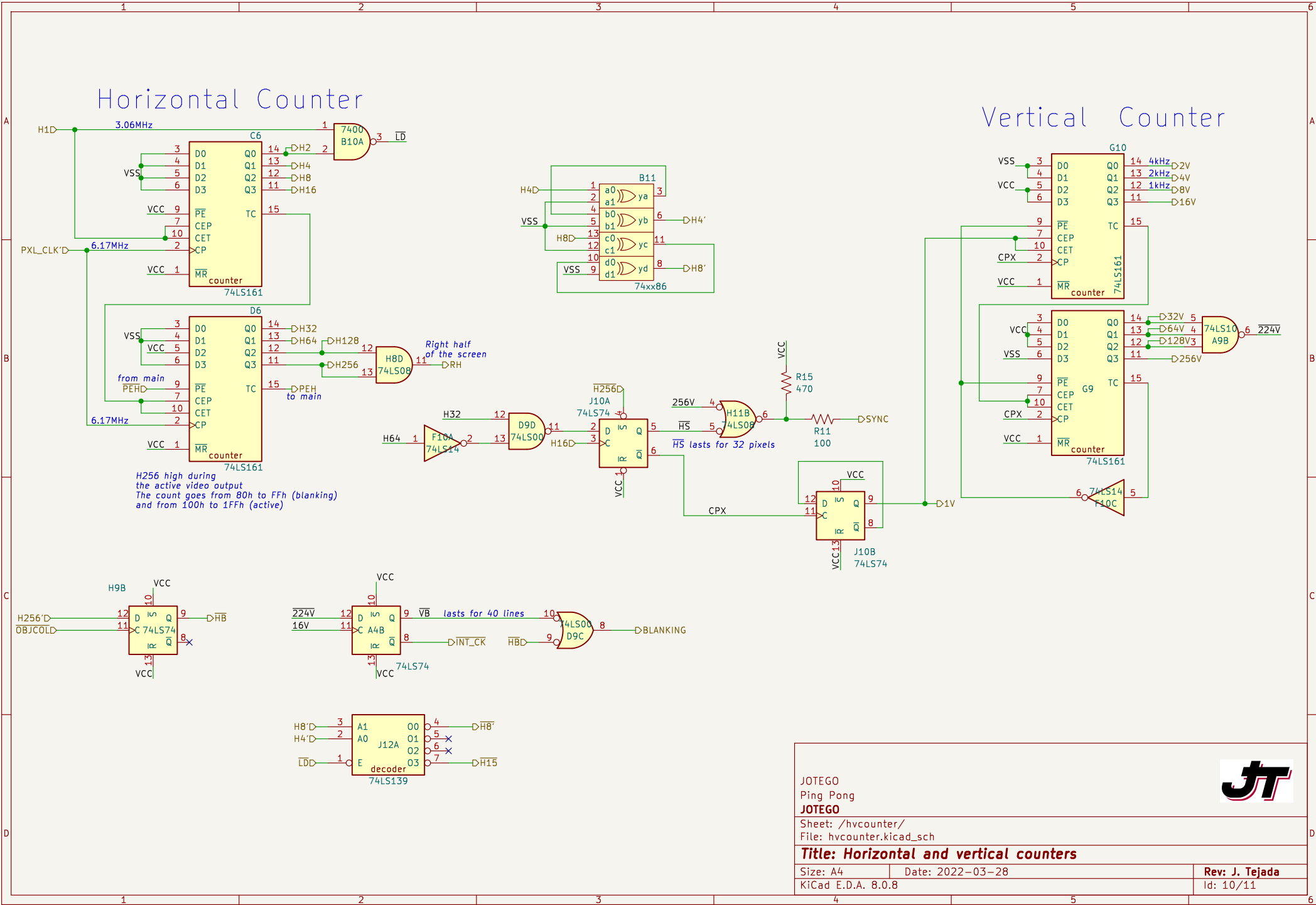
The horizontal sync and blanking signals are generated by the Horizontal Counter. The horizontal sync (HS) signal is generated by an AND gate (H11B) and is used to generate the horizontal sync (HS) and the horizontal blanking (HB) signal. The horizontal blanking (HB) signal is generated by an AND gate (H9B) and is used to generate the horizontal blanking (HB) signal.

Vertical Sync and Blanking

The vertical sync and blanking signals are generated by the Vertical Counter. The vertical sync (VS) signal is generated by an AND gate (A9B) and is used to generate the vertical sync (VS) and the vertical blanking (VB) signal. The vertical blanking (VB) signal is generated by an AND gate (A4B) and is used to generate the vertical blanking (VB) signal.

Legend

- 74LS161: Counter
- 74LS139: Decoder
- 74LS10: NAND gate
- 74LS74: D flip-flop
- 74LS00: NAND gate
- 74LS08: AND gate
- 74LS04: Inverter
- 74LS01: SR flip-flop
- 74LS02: NOR gate
- 74LS03: OR gate
- 74LS05: Inverter
- 74LS06: Inverter
- 74LS07: Inverter
- 74LS09: Inverter
- 74LS10: NAND gate
- 74LS11: NAND gate
- 74LS12: NAND gate
- 74LS13: NAND gate
- 74LS14: Inverter
- 74LS15: Inverter
- 74LS16: Inverter
- 74LS17: Inverter
- 74LS18: Inverter
- 74LS19: Inverter
- 74LS20: NAND gate
- 74LS21: NAND gate
- 74LS22: NAND gate
- 74LS23: NAND gate
- 74LS24: NAND gate
- 74LS25: NAND gate
- 74LS26: NAND gate
- 74LS27: NAND gate
- 74LS28: NAND gate
- 74LS29: NAND gate
- 74LS30: NAND gate
- 74LS31: NAND gate
- 74LS32: NAND gate
- 74LS33: NAND gate
- 74LS34: NAND gate
- 74LS35: NAND gate
- 74LS36: NAND gate
- 74LS37: NAND gate
- 74LS38: NAND gate
- 74LS39: NAND gate
- 74LS40: NAND gate
- 74LS41: NAND gate
- 74LS42: NAND gate
- 74LS43: NAND gate
- 74LS44: NAND gate
- 74LS45: NAND gate
- 74LS46: NAND gate
- 74LS47: NAND gate
- 74LS48: NAND gate
- 74LS49: NAND gate
- 74LS50: NAND gate
- 74LS51: NAND gate
- 74LS52: NAND gate
- 74LS53: NAND gate
- 74LS54: NAND gate
- 74LS55: NAND gate
- 74LS56: NAND gate
- 74LS57: NAND gate
- 74LS58: NAND gate
- 74LS59: NAND gate
- 74LS60: NAND gate
- 74LS61: NAND gate
- 74LS62: NAND gate
- 74LS63: NAND gate
- 74LS64: NAND gate
- 74LS65: NAND gate
- 74LS66: NAND gate
- 74LS67: NAND gate
- 74LS68: NAND gate
- 74LS69: NAND gate
- 74LS70: NAND gate
- 74LS71: NAND gate
- 74LS72: NAND gate
- 74LS73: NAND gate
- 74LS74: D flip-flop
- 74LS75: D flip-flop
- 74LS76: D flip-flop
- 74LS77: D flip-flop
- 74LS78: D flip-flop
- 74LS79: D flip-flop
- 74LS80: D flip-flop
- 74LS81: D flip-flop
- 74LS82: D flip-flop
- 74LS83: D flip-flop
- 74LS84: D flip-flop
- 74LS85: D flip-flop
- 74LS86: D flip-flop
- 74LS87: D flip-flop
- 74LS88: D flip-flop
- 74LS89: D flip-flop
- 74LS90: D flip-flop
- 74LS91: D flip-flop
- 74LS92: D flip-flop
- 74LS93: D flip-flop
- 74LS94: D flip-flop
- 74LS95: D flip-flop
- 74LS96: D flip-flop
- 74LS97: D flip-flop
- 74LS98: D flip-flop
- 74LS99: D flip-flop

[illegible]



JOTEGO
Ping Pong
JOTEGO



Sheet: /capacitors/
File: capacitors.kicad_sch

Title: Decoupling capacitors

Size: A4 Date: 2022-03-28
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Rev: J. Tejada
Id: 11/11