



CP2A PAG. 19 SCH	MAIN_A[150] MAIN_DB[70] DBJCLK6 OBJCLK12 CRCS IDS OBJCS OBJCS OBJREG SYSRES OBJCHA VBLANK XSYNC RD	objects MAIN_A[120] MAIN_DB[70] >OBJCLK6 >OBJCLK12 >CRCS >DS >OBJCS >OBJCS >OBJCS >SYSRES >OBJCHA >VBLANK >XSYNC >RD	PAL[40]D PRI[40]D OCOL[30]D SHD[10]D CPUD	PAL[40 PRI[40 OCOL[30 SHD[10
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	scroll		
MAIN_A[150]	→MAIN_A[150]	APAL[20]D	APAL[20]
MAIN_DB[70]			BPAL[20]
SCRCLK	♦MAIN_DB[70]	BPAL[20]D	BC0L[30]
VBLK		BCOL[30]D	FPAL[20]
RD	->VBLK	FPAL[20]D	ACOL[30]
SYSRES	→RD	ACOL[30]D	FC0L[30]
VRAMCS	SYSRES	FC0L[30]D	OBJCLK12
RMRD	->VRAM <mark>CS</mark>	OBJCLK12D	OBJCLK6
KIIKD	->RMRD	OBJCLK6D	XSYNC
		XSYNCD	MRESET
		MRESETD	PE
		PED	SNDRES
		SNDRESD	PQ
		PQD	CPURES
		CPURES D	HSYNC
		HSYNCD	
		VBLANK D	VBLANK
		HBLANKD	HBLANK
		JP3D	<u>JP3</u>
		ĪNĪD	INT
		FIROD	FIRQ
		NMID	NMI
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MAIN_A[150]	>MAIN_A[40]	<u>UWR</u> D	UWR
MAIN_DB[70]	→ MAIN_DB[70]	LWRD	LWR
AFR	DAFR	COIN CNT 1D	COIN_CNT_2
HIPCS	DHIPCS	COIN_CNT_2D	COIN_CNT_1
WR	-DWR	SCRCLKD	SCRCLK
AS	DAS	INTO	INT
10 <u>CS</u>	>10 <u>cs</u>	IRQEND	IRQEN
CPURES	CPURES	EEPDID	EEPDI
ccu cs	->ccu cs	WOCOD	WOC0
CCUCK	->ccuck	WOC1D	WOC1
VLDI	- DVLDI	MSCHGD	MSCHG
HLDI	- DHLDI	FEPCSD	EEPCS
+12V	+12V	EEPCLKD	EEPCLK
	F	COIN1D	COIN_1
		COIN2D	COIN_2
		OBJCHAD	OBJCHA
		RMRDD	RMRD
		BRAMBKD	BRAMBK
		INITD	INIT
		SYSRESD	SYSRES
		SOUNDOND	SOUNDON
		SOUNDREGD	SOUNDREG
		VBLKD	VBLK
		CR CS D	CRCS
		ĀFRD	ĀFR
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These schematics cover the missing pages in the original ones published by the maker. Signal names existing in the original pages have been preserved. New signal names try to follow the maker style or are taken from similar schematics of the same maker.

www.patreon.com/jotego github.com/jotego/jtcores/tree/master/cores/simson/sch/vendetta JOTEGO KONAMI PWB352292A

Sheet: / File: vendetta.kicad_sch Title: Vendetta

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