007783

ORA12 74 — ORA12   AB13 — 4 AB13
ORA11 73 — ORA11   AB12 — 5 AB12
ORA10 72 — ORA10   AB11 — 6 AB11
ORA9 71 — ORA9   AB10 — 7 AB10
ORA8 70 — ORA8   AB9 — 8 AB9
ORA7 69 — ORA7   AB8 — 9 AB8
ORA6 68 — ORA6   AB7 — 10 AB7
ORA5 67 — ORA5   AB6 — 11 AB6
ORA4 66 — ORA4   AB5 — 12 AB5
ORA3 65 — ORA3   AB4 — 13 AB4
ORA2 62 — ORA2   AB3 — 14 AB3
ORA1 61 — ORA1   AB2 — 15 AB2
ORA0 60 — ORA0   AB1 — 16 AB1

CRW3 35 — CRW3   SAB13 — 17 SAB13
CRW2 34 — CRW2   SAB12 — 18 SAB12
CRW1 33 — CRW1   SAB11 — 19 SAB11
CRW0 32 — CRW0   SAB10 — 20 SAB10
                    SAB9 — 23 SAB9
48 — OOE   SAB8 — 24 SAB8
47 — ORUWR   SAB7 — 25 SAB7
46 — ORLWR   SAB6 — 26 SAB6
36 — DMA   SAB5 — 27 SAB5
                    SAB4 — 28 SAB4
                    SAB3 — 29 SAB3
                    SAB2 — 30 SAB2
                    SAB1 — 31 SAB1

                    OD7 — 45 OD7
                    OD6 — 44 OD6
                    OD5 — 42 OD5
                    OD4 — 41 OD4
                    OD3 — 40 OD3
                    OD2 — 39 OD2
                    OD1 — 38 OD1
                    OD0 — 37 OD0

TIM — 3
TIM3 — 84
DMAON — 2
OCRA — 81
SUWR — 82
SLWR — 83
MREAD — 79
SREAD — 80
MUWR — 75
MLWR — 76
MOCS — 77
SOCS — 78

DMC — 57
OSC — 56
OBFI — 55
OFC — 54
FBRF — 53
OCEN — 52
CLR — 51 CLR
CLK2 — 50 CLK2
BFLG — 49

TES2 — 59
TES1 — 58

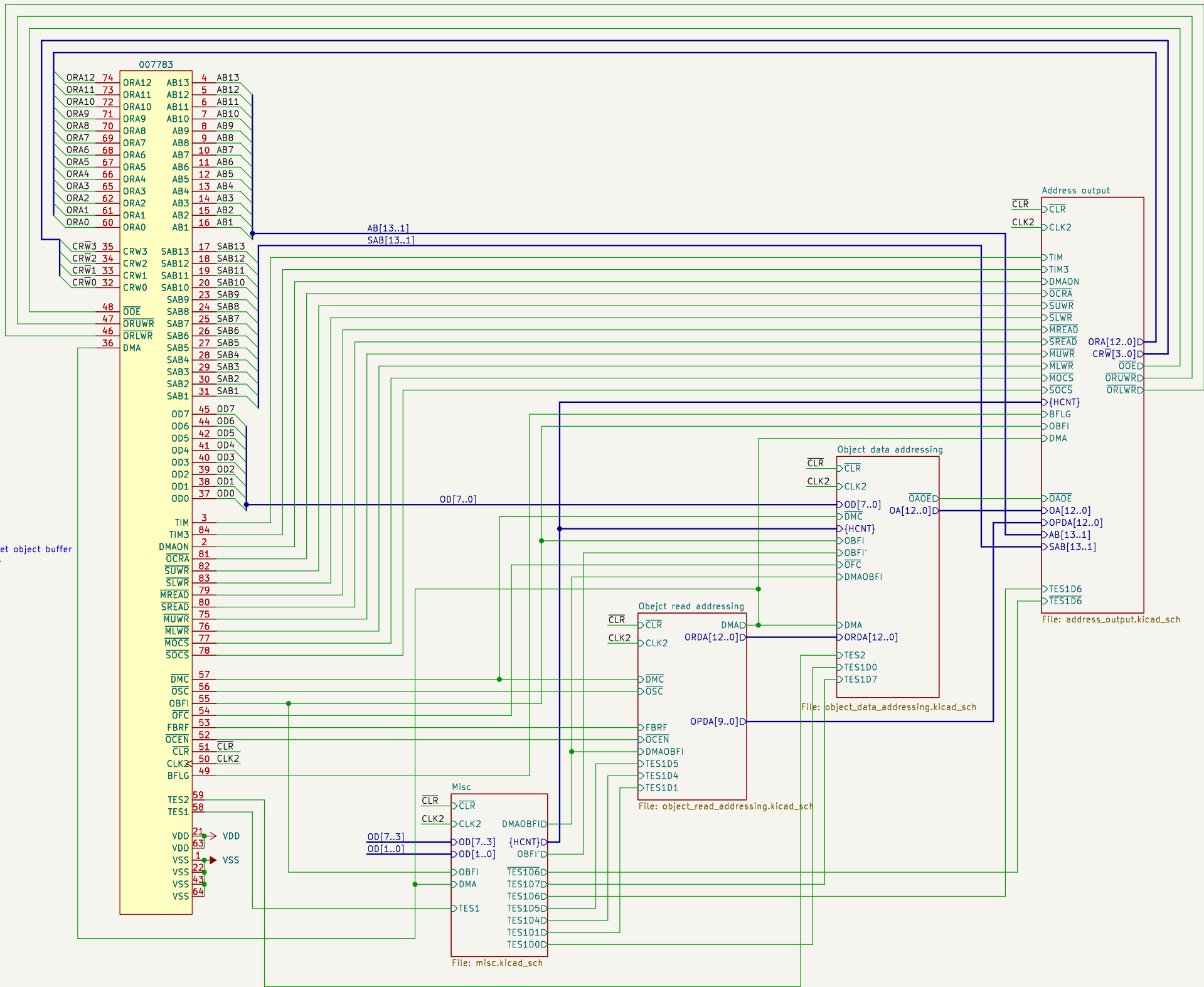VDD — 21 / 63 ▷ VDD
VSS — 1 / 22 / 43 / 64 ▷ VSS

1. OBFI: (OBJBUFINIT) zeros are written to 1800h..1AFFh.
2. DMA: OA[12:0] active.
   a) 8 words are read from addresses 0000h..0007h, 0028h..002Fh,...,17E0h..17E7h
      by the sprite data parser 007784 and if the sprite is enabled with BEFLAG
      they are written to the buffer OBJBUF.

OBJRAM
0000h..17E7h   Unprocessed data
1800h..1BFFh   Processed data

WD0	WD1	WD2	WD3	WD4	WD5	WD6	WD7	WD0	WD1	WD2	WD3
0000	0001	0002	0003	0004	0005	0006	0007	BA1	BA2	BA3	BA4

OBJBUF, Buffer Address
BA1 : OA[12:0] = 1800 + OD''[7:0] << 2
BA2 : OA[12:0] = BA1 + 1
BA3 : OA[12:0] = BA1 + 2
BA4 : OA[12:0] = BA1 + 3

OBFI	H8	OA		OAOE	
1	X	{3'b110,OWRA[9:0]}		1	Writes to 1800h..1BFFh, reset object buffer
0	0	ORDA[12:0]		0	Read data from object RAM.
0	1	{3'b110,OD''[7:0],OWRA[2:1]}		1	Writes to 1800h..1BFFh

Address output
CLR ▷ CLR
CLK2 ▷ CLK2
▷ TIM
▷ TIM3
▷ DMAON
▷ OCRA
▷ SUWR
▷ SLWR
▷ MREAD
▷ SREAD   ORA[12..0]
▷ MUWR   CRW[3..0]
▷ MLWR   OOED
▷ MOCS   ORUWRD
▷ SOCS   ORLWRD
▷{HCNT}
▷ BFLG
▷ OBFI
▷ DMA
File: address_output.kicad_sch

Object data addressing
CLR ▷ CLR
CLK2 ▷ CLK2
▷ OD[7..0]
▷ DMC
▷{HCNT}
▷ OBFI   OAOED
▷ OBFI'   OA[12..0]D
▷ OFC
▷ DMAOBFI
File: object_data_addressing.kicad_sch

Obejct read addressing
CLR ▷ CLR   DMAD
CLK2 ▷ CLK2   ORDA[12..0]D
▷ DMA
▷ DMC
▷ OSC   TES2
▷ FBRF   TES1D0
▷ OCEN   TES1D7
▷ DMAOBFI
▷ TES1D5
▷ TES1D4   OPDA[9..0]D
▷ TES1D1
File: object_read_addressing.kicad_sch

Misc
CLR ▷ CLR
CLK2 ▷ CLK2   DMAOBFID
OD[7..3] ▷ OD[7..3]   {HCNT}D
OD[1..0] ▷ OD[1..0]   OBFI'D
▷ OBFI   TES1D6D
▷ DMA   TES1D7D
▷ TES1   TES1D6D
                  TES1D5D
                  TES1D4D
                  TES1D1D
                  TES1D0D
File: misc.kicad_sch

AB[13..1]
SAB[13..1]
OD[7..0]

OAOE
OA[12..0]
OPDA[12..0]
AB[13..1]
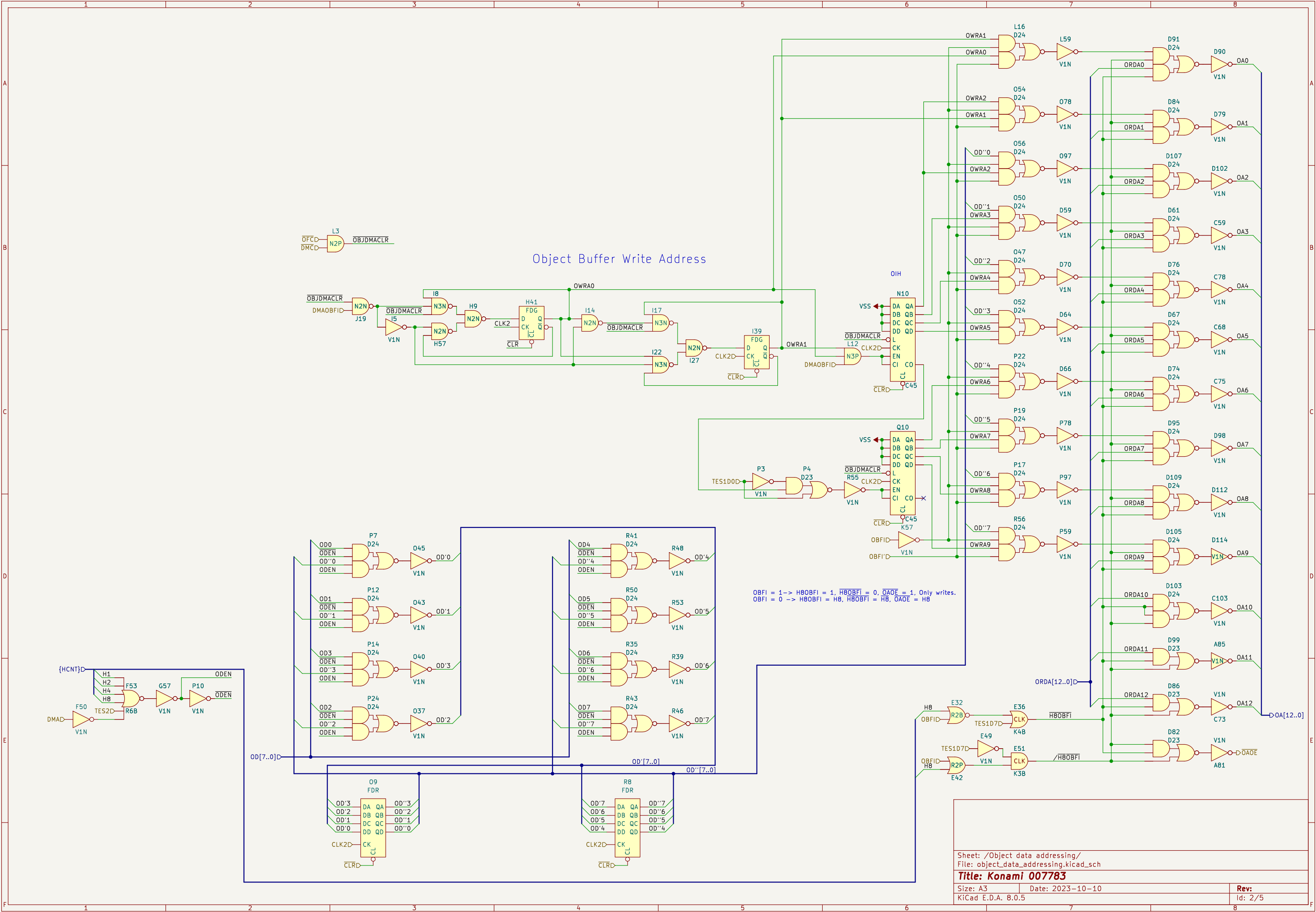SAB[13..1]
TES1D6
TES1D6

Ulf Skutnabba, twitter: @skutis77
Sheet: /
File: 007783.kicad_sch
Title: Konami 007783
Size: A3   Date: 2023-10-10   Rev:
KiCad E.D.A. 8.0.5   Id: 1/5

Object Buffer Write Address

OBFI = 1 -> H8OBFI = 1, $\overline{H8OBFI}$ = 0, $\overline{OAOE}$ = 1, Only writes.
OBFI = 0 -> H8OBFI = H8, $\overline{H8OBFI}$ = $\overline{H8}$, $\overline{OAOE}$ = H8

Sheet: /Object data addressing/
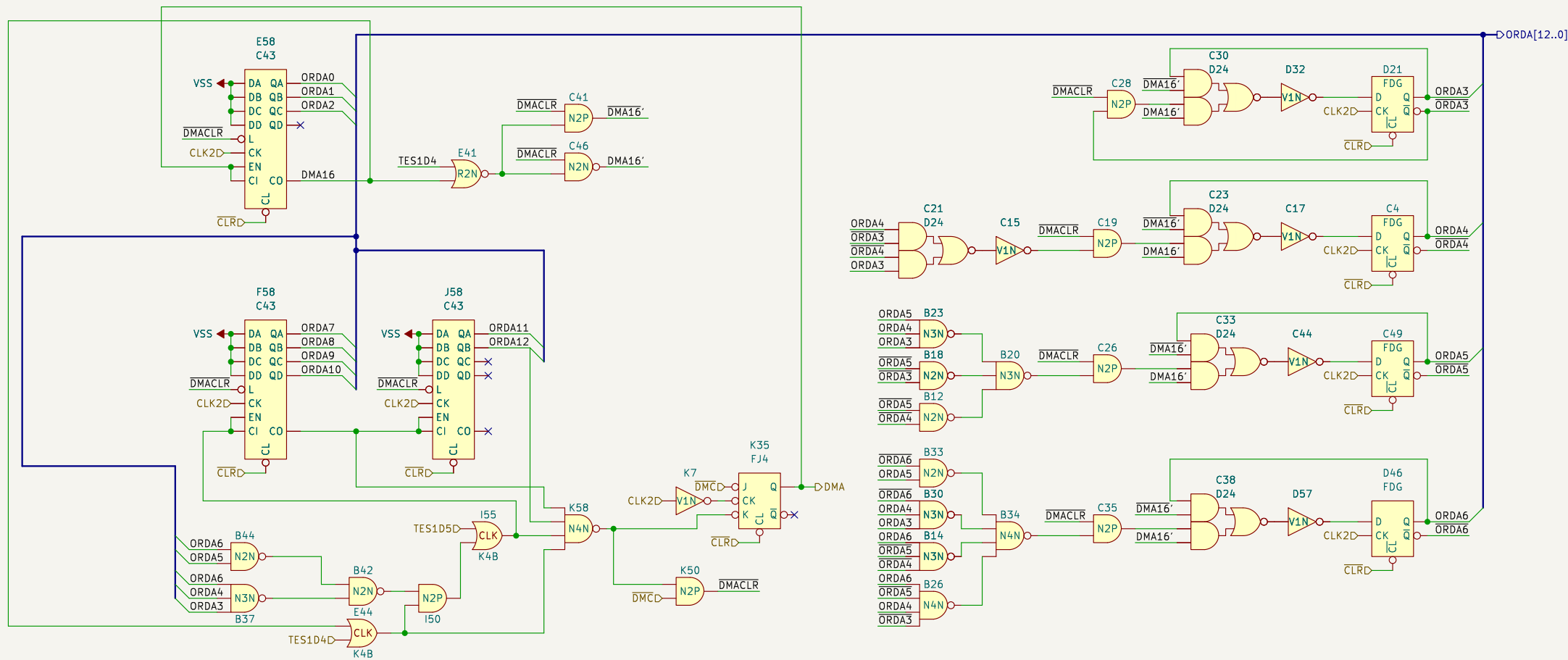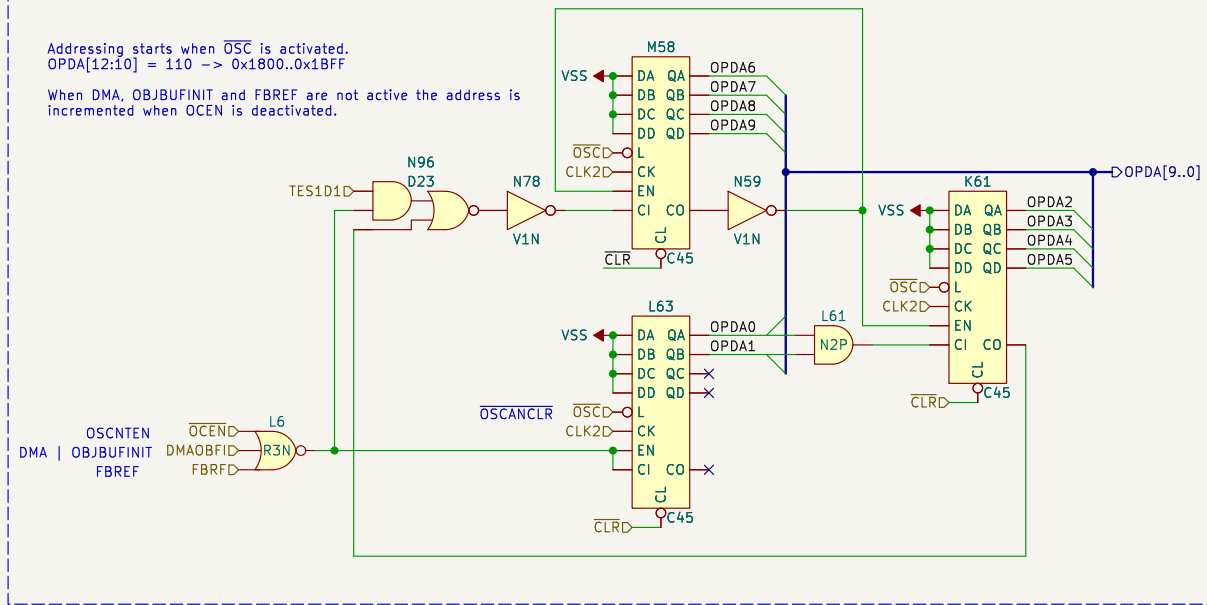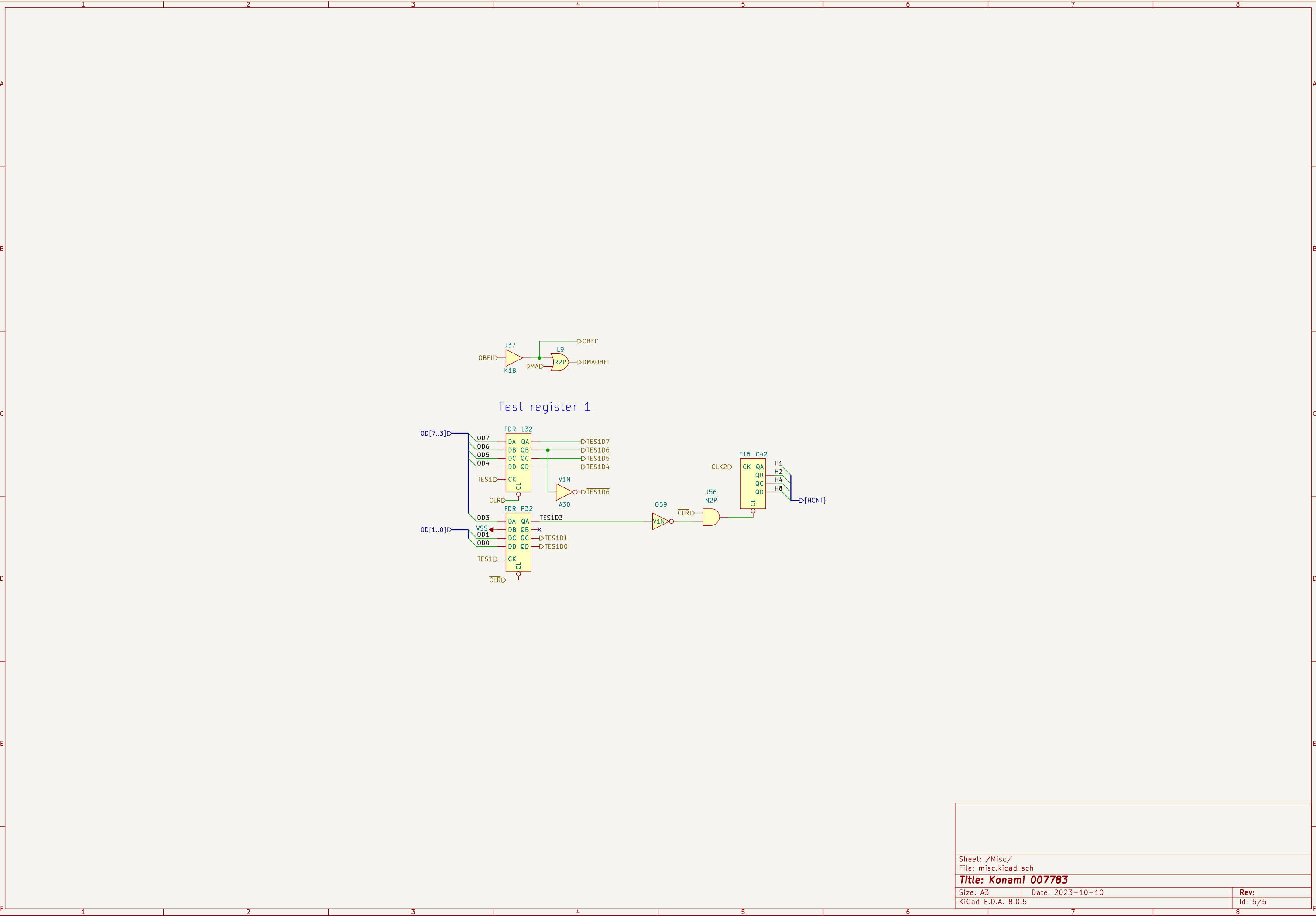File: object_data_addressing.kicad_sch

Title: Konami 007783

Size: A3   Date: 2023-10-10   Rev:
KiCad E.D.A. 8.0.5   Id: 2/5

Object Read Addressing

Parsed Object Data Addressing

Addressing starts when $\overline{OSC}$ is activated.
OPDA[12:10] = 110 -> 0x1800..0x1BFF

When DMA, OBJBUFINIT and FBREF are not active the address is incremented when OCEN is deactivated.

OSCNTEN
DMA | OBJBUFINIT
FBREF

ORDA[12..0]

OPDA[9..0]

OBFI'

J37
OBFI
K1B

L9
DMA
R2P
DMAOBFI

Test register 1

FDR L32
OD[7..3]
OD7 DA QA TES1D7
OD6 DB QB TES1D6
OD5 DC QC TES1D5
OD4 DD QD TES1D4
TES1 CK
CLR CL

V1N
A30 TES1D6

F16 C42
CLK2 CK QA H1
QB H2
QC H4
QD H8
CL {HCNT}

FDR P32
OD3 DA QA TES1D3
VSS DB QB
OD[1..0]
OD1 DC QC TES1D1
OD0 DD QD TES1D0
TES1 CK
CLR CL

O59
V1N
CLR
N2P
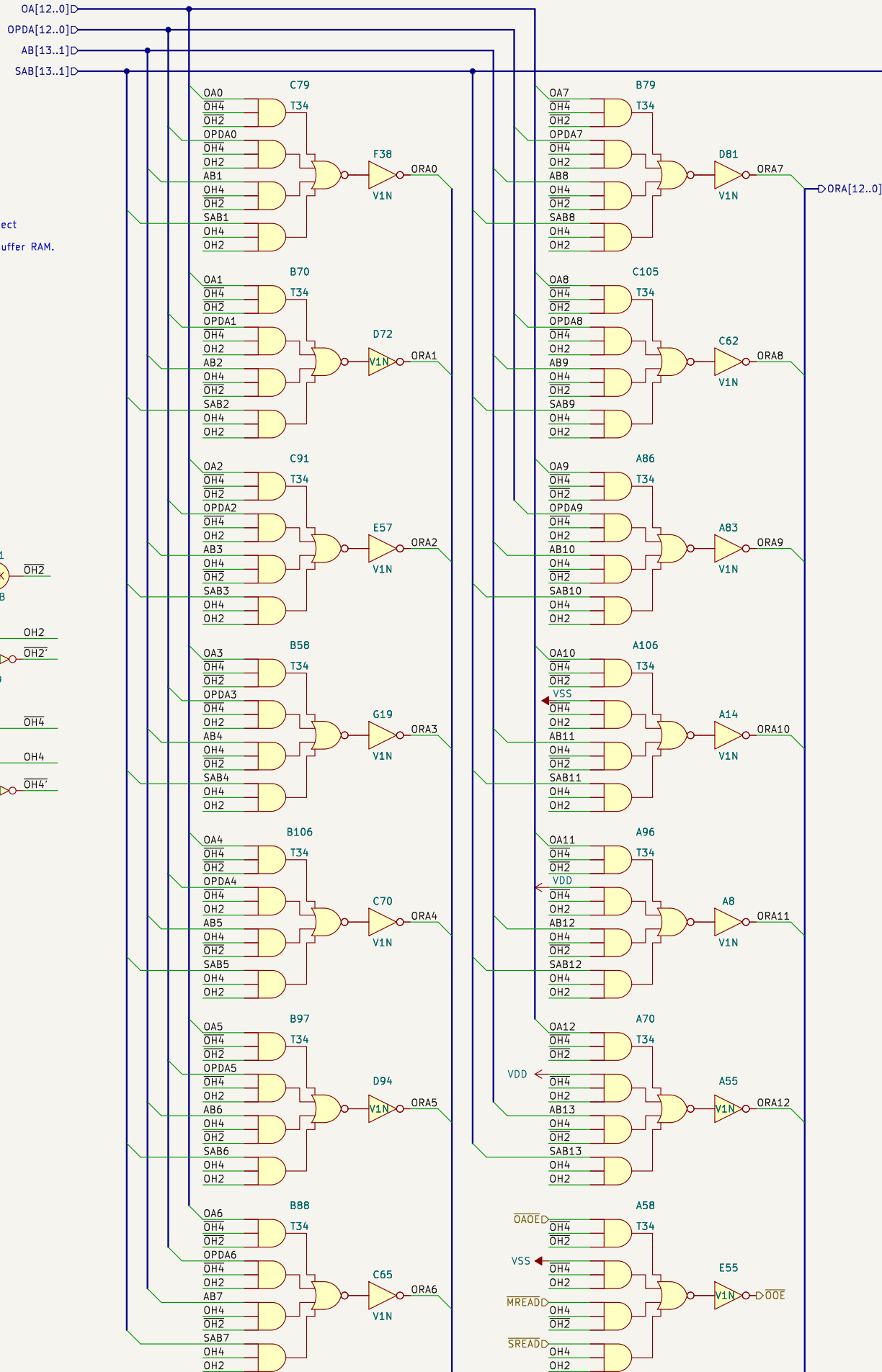J56

OA[12..0]
OPDA[12..0]
AB[13..1]
SAB[13..1]

Four time slots available all the time for addressing.
0: – OBJBUFINIT high: Writing zeros to all data in the Object
       Data Buffer.
     – DMA high: Data copying from Object RAM to Object Buffer RAM.
1: Parsed object data copy to the frame buffers.
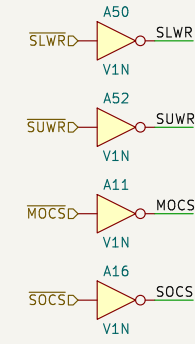2: Master CPU access
3: Slave CPU access

OBFI	DMA	OH2	$\overline{OH2}$	OH4	$\overline{OH4}$
1	X	0	1	0	1
X	1	0	1	0	1

OBFI
DMA

E30 R2N   A25 N2B   A31 CLK $\overline{OH2}$
H2   K3B
                      $\overline{TES1D6}$

A35 N2P   A45 CLK   A9 V1N $\overline{OH2}$
H2   K4B $\overline{OH2}$'
           TES1D6

A38 N2B   A42 CLK $\overline{OH4}$
           K4B
H2   TES1D6

A22 N2P   A19 CLK   E8 V1N $\overline{OH4}$'
H4   K3B   OH4
           $\overline{TES1D6}$

{HCNT}

OA0 $\overline{OH4}$ $\overline{OH2}$ OPDA0 $\overline{OH4}$ $\overline{OH2}$ AB1 $\overline{OH4}$ $\overline{OH2}$ SAB1 $\overline{OH4}$ $\overline{OH2}$ C79 T34   F38 V1N   ORA0
OA1 ... OPDA1 ... AB2 ... SAB2 ...   B70 T34   D72 V1N   ORA1
OA2 ... OPDA2 ... AB3 ... SAB3 ...   C91 T34   E57 V1N   ORA2
OA3 ... OPDA3 ... AB4 ... SAB4 ...   B58 T34   G19 V1N   ORA3
OA4 ... OPDA4 ... AB5 ... SAB5 ...   B106 T34 C70 V1N   ORA4
OA5 ... OPDA5 ... AB6 ... SAB6 ...   B97 T34   D94 V1N   ORA5
OA6 ... OPDA6 ... AB7 ... SAB7 ...   B88 T34   C65 V1N   ORA6

OA7 ... OPDA7 ... AB8 ... SAB8 ...   B79 T34   DB1 V1N   ORA7
OA8 ... OPDA8 ... AB9 ... SAB9 ...   C105 T34 C62 V1N   ORA8
OA9 ... OPDA9 ... AB10 ... SAB10 ... A86 T34   A83 V1N   ORA9
OA10 ... VSS ... AB11 ... SAB11 ...   A106 T34 A14 V1N   ORA10
OA11 ... VDD ... AB12 ... SAB12 ...   B106 T34 A8 V1N   ORA11
OA12 ... VDD ... AB13 ... SAB13 ...   A70 T34   A55 V1N   ORA12

ORA[12..0]

$\overline{OAOE}$ $\overline{OH4}$ $\overline{OH2}$ VSS $\overline{MREAD}$ $\overline{SREAD}$ A58 T34   E55 V1N $\overline{OOE}$

CPU Read/Write logic

$\overline{SLWR}$ A50 V1N SLWR
$\overline{SUWR}$ A52 V1N SUWR
$\overline{MOCS}$ A11 V1N MOCS
$\overline{SOCS}$ A16 V1N SOCS

Object Character RAM
Read/Write logic

SLWR SAB1   R87 R3B $\overline{CRW0}$
SUWR SAB1   R58 R3B $\overline{CRW1}$
A57 R2N
TIM3   OCRA
SLWR   Q80 R3B $\overline{CRW2}$
SAB1   Q84 V1N
SUWR   Q58 R3B $\overline{CRW3}$
$\overline{CRW}$[3..0]
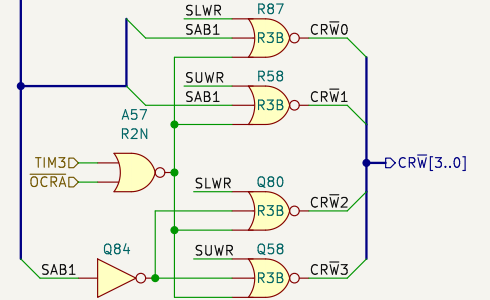
Object RAM Read/Write logic

SOCS SLWR $\overline{OH4}$ $\overline{OH2}$ B68 N4N
$\overline{MLWR}$ A6 V1N   MOCS $\overline{OH4}$ $\overline{OH2}$'   B2 N4N   B55 N2N   B50 CLK K3B   D40 R2N $\overline{ORLWR}$

BEFLAG & DMA & DMAON
BFLG   H8 H2   E11 N8B   E3 N2N   D4 CLK K3B
E20 FDG   DMA $\overline{OH4}$' $\overline{OH2}$'
DMAON D Q   D10 BD3   CLK2
OBFI CK $\overline{Q}$ VDD
$\overline{CLR}$
OBFI   E5 D24 $\overline{OH4}$' $\overline{OH2}$'
OBFI & DMAON

SOCS SUWR $\overline{OH4}$ $\overline{OH2}$ A68 N4N
$\overline{MUWR}$ A3 V1N   MOCS $\overline{OH4}$ $\overline{OH2}$'   B5 N4N   B57 N2N   B46 CLK K3B   D36 R2N $\overline{ORUWR}$
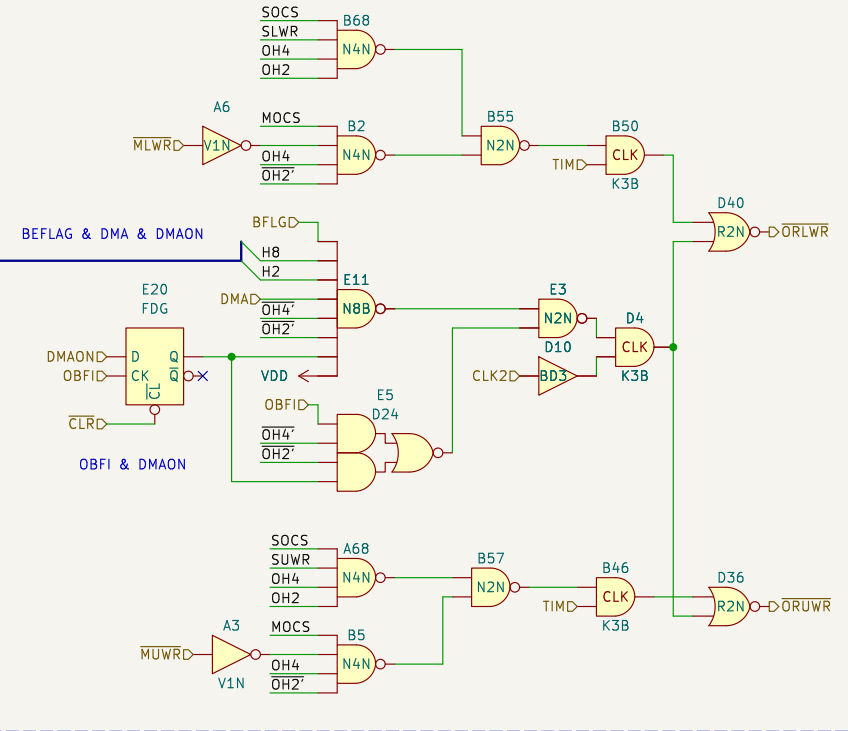
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File: address_output.kicad_sch
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KiCad E.D.A. 8.0.5   Id: 6/5