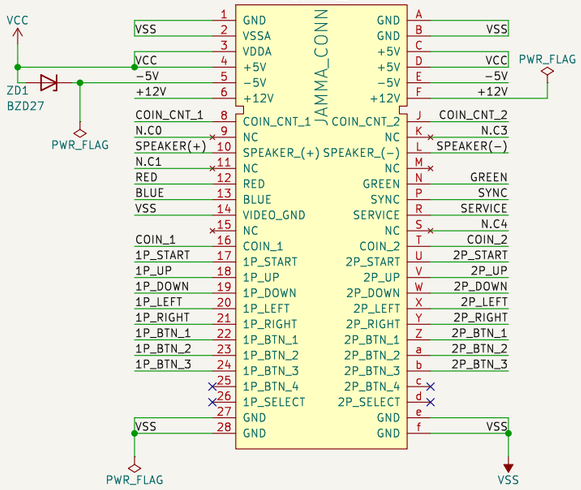
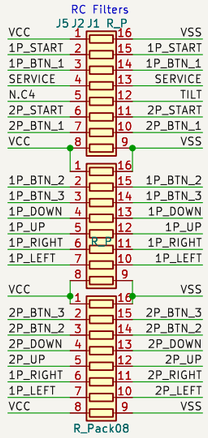
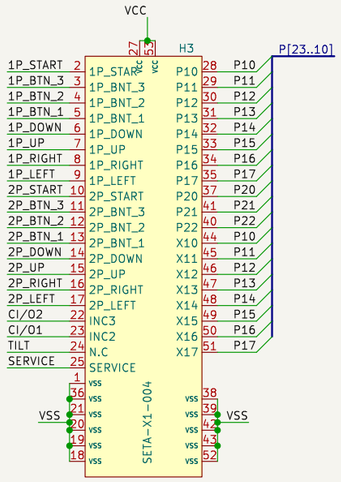
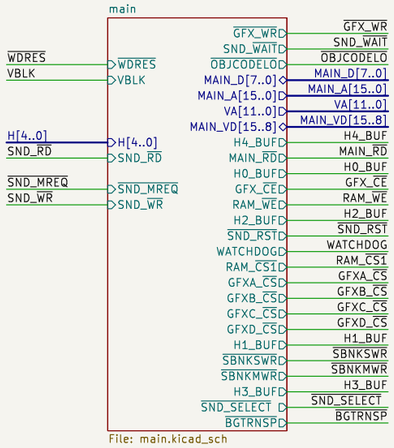
JM1

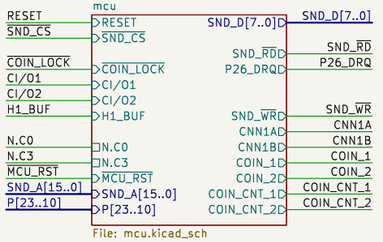


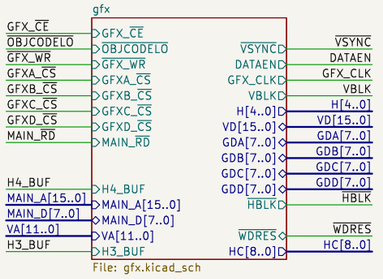
CABINET I/O

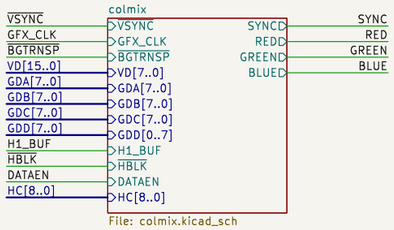


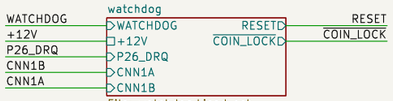


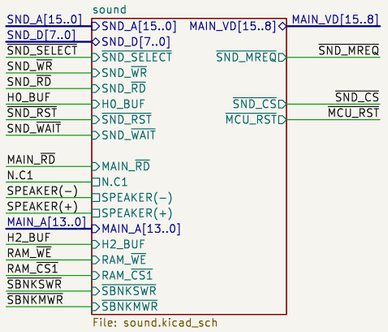












JOTEGO

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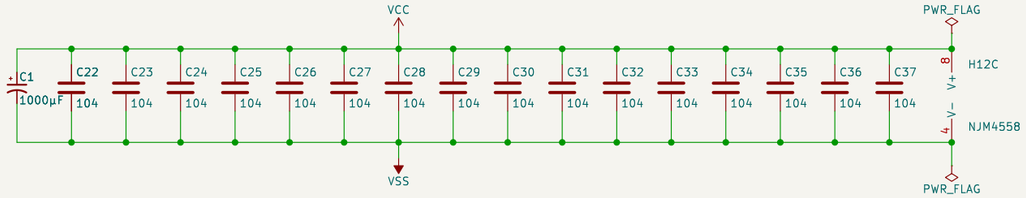
Title: EXTERMINATION

Size: A3	Date: 29/08/2022	Rev: José Tejada G.
KiCad E.D.A. 8.0.6		Id: 1/10



H5E
74LS02

B7C
74LS74

B4C
74LS74

B3C
74LS74

B2E
74LS08

G13G
74LS04

C6E
74LS32

B6E
74LS08

B1G
74LS04

JOTEGO

Sheet: /capacitors/
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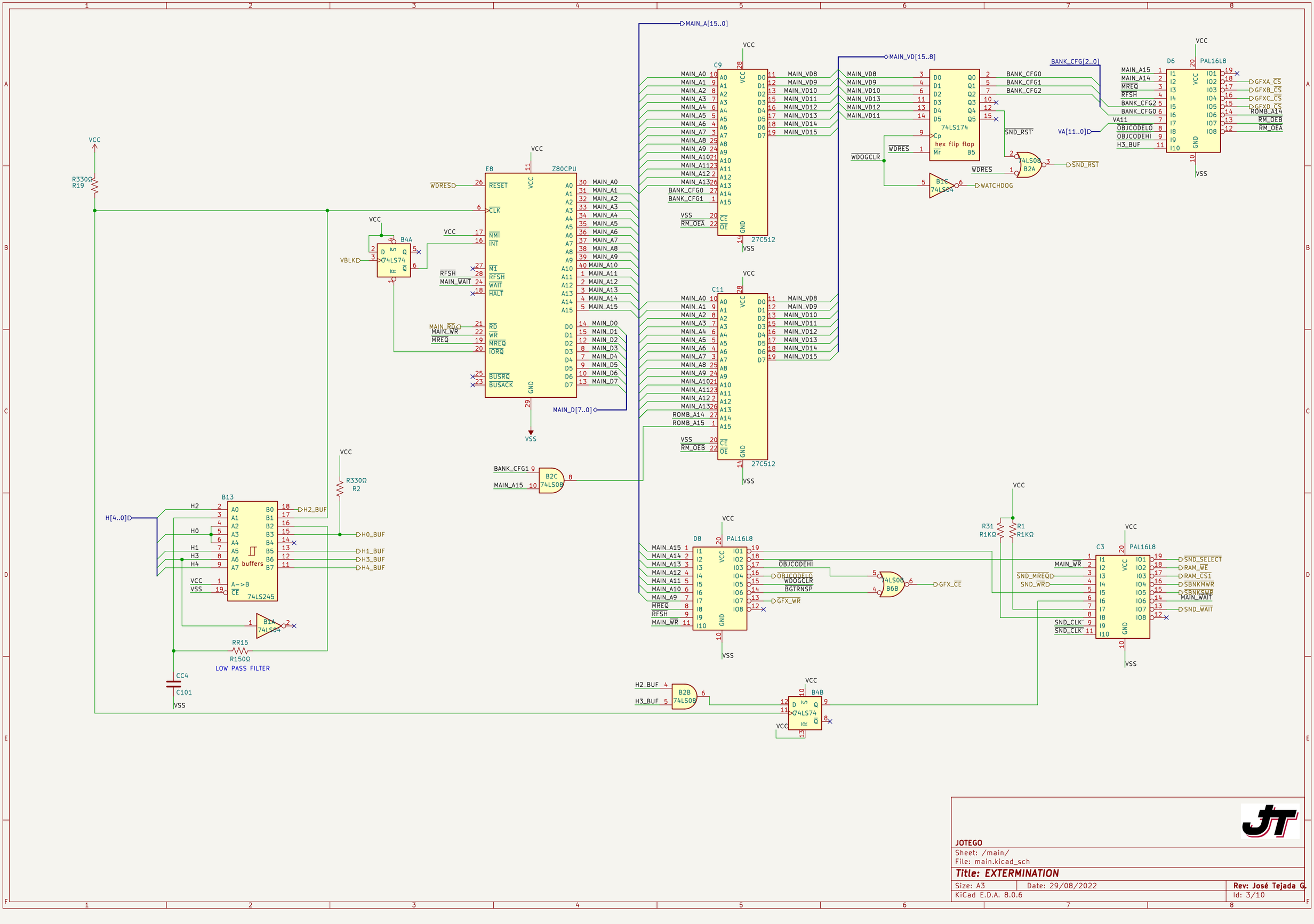
Size: A3	Date: 29/08/2022	**Rev: José Tejada G.**
KiCad E.D.A. 8.0.6		Id: 2/10



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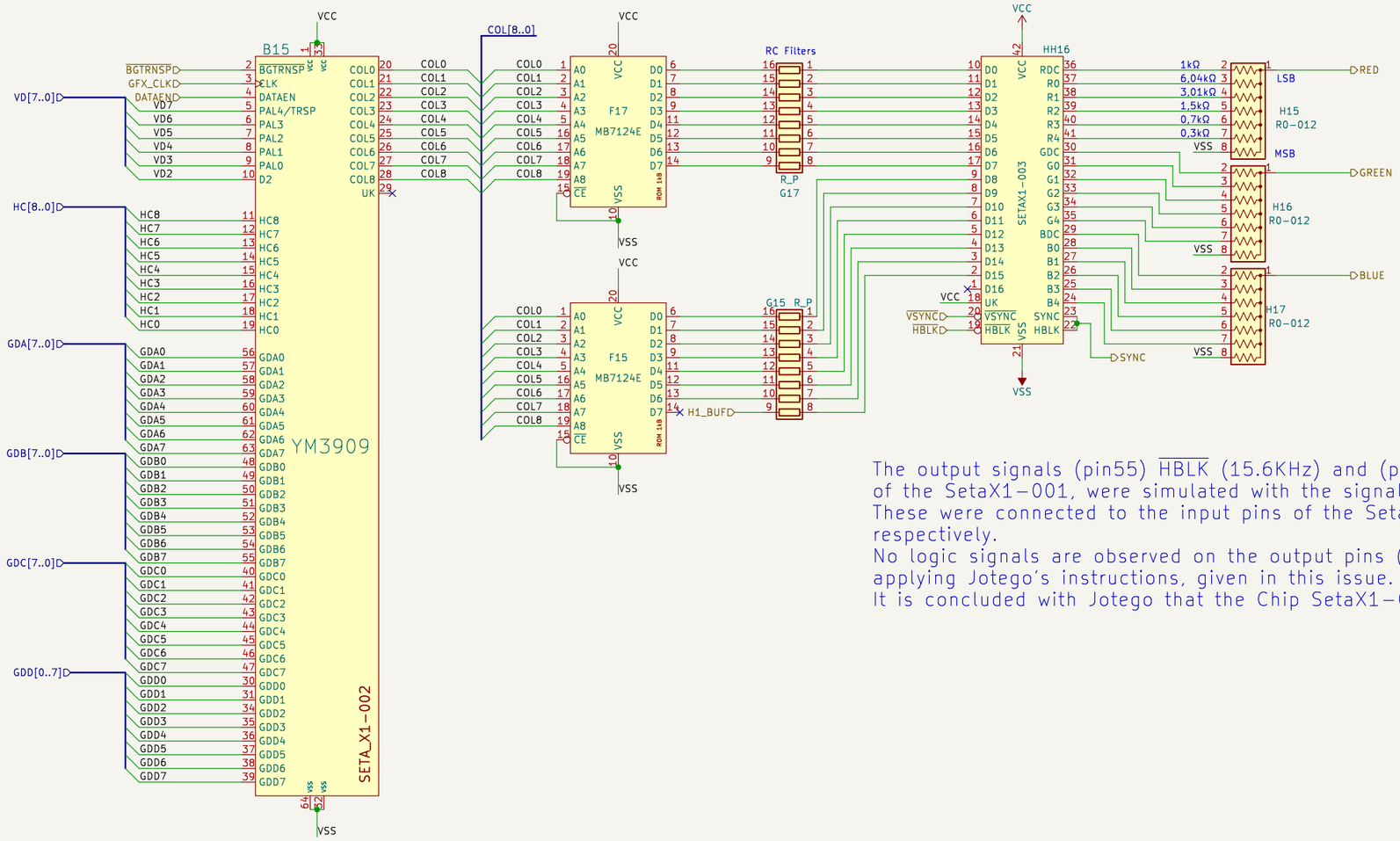
Size: A3	Date: 29/08/2022
KiCad E.D.A. 8.0.6	Id: 3/10
	Rev: José Tejada G.



The output signals (pin55) $\overline{\text{HBLK}}$ (15.6KHz) and (pin56) $\overline{\text{VSYNC}}$ (59.2 Hz) of the SetaX1−001, were simulated with the signal generator and an inverter. These were connected to the input pins of the SetaX01−003 (pin 19 − 20), respectively.
No logic signals are observed on the output pins (22−23) HBLK − SYNC, applying Jotego's instructions, given in this issue.
It is concluded with Jotego that the Chip SetaX1−001 is broken.

JOTEGO

Sheet: /colmix/		
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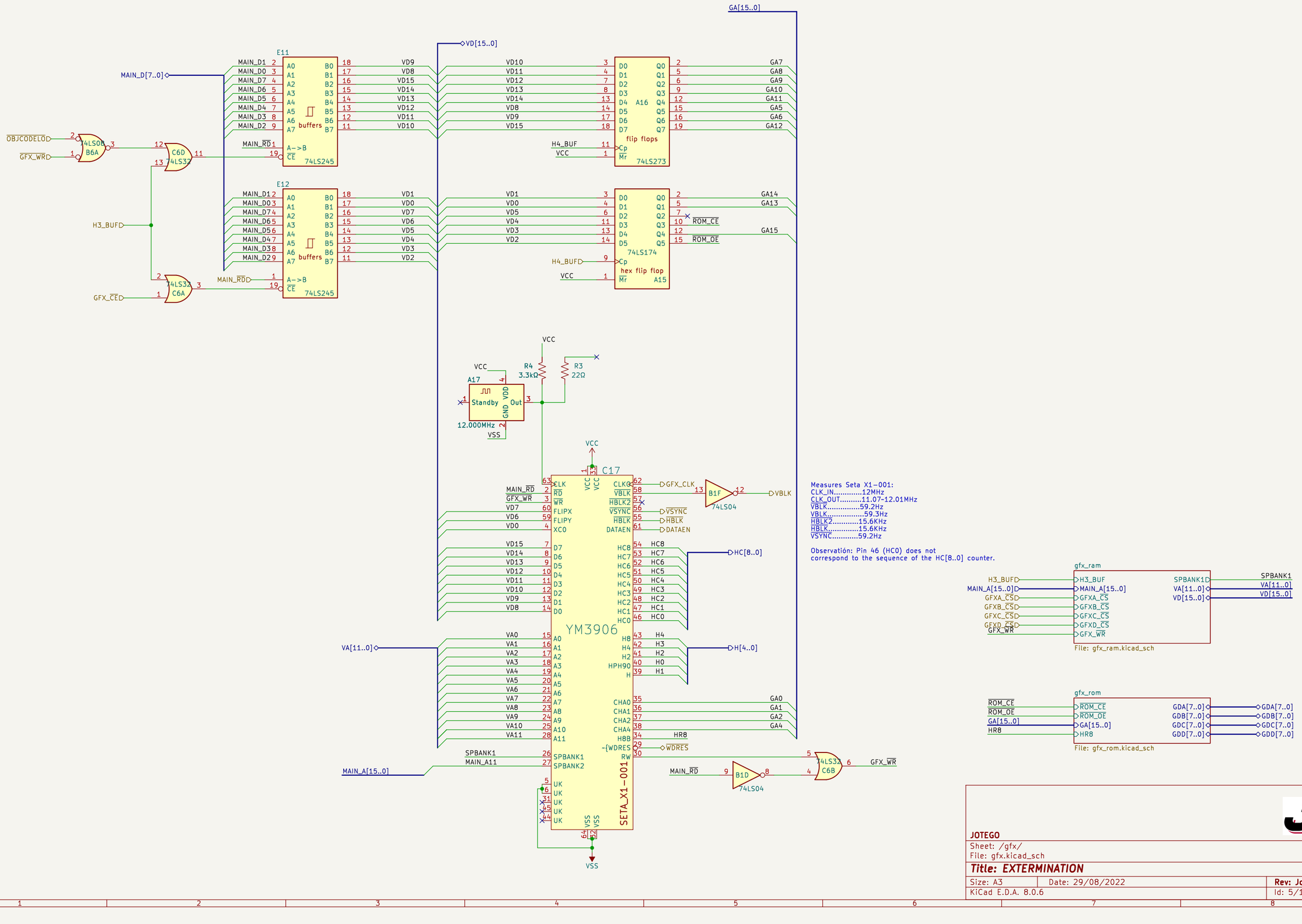
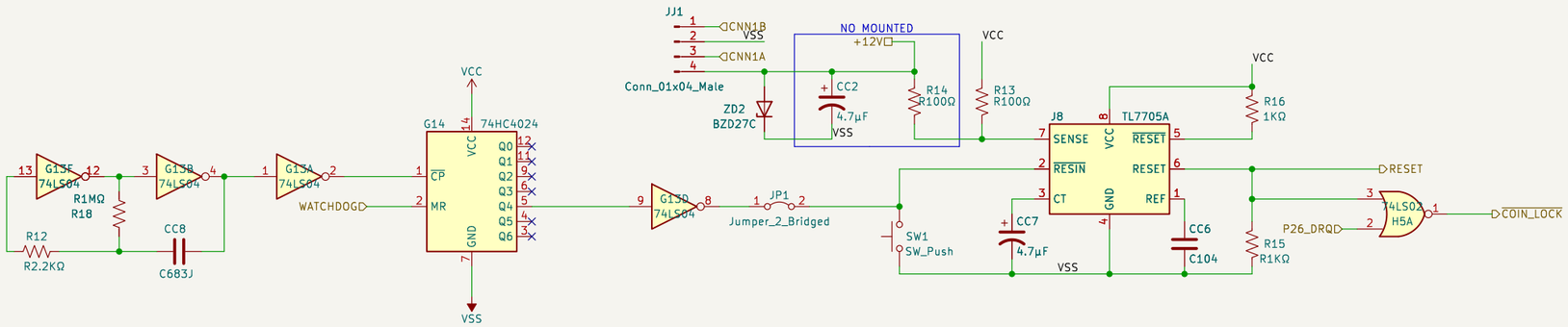
Size: A3	Date: 29/08/2022	**Rev: José Tejada G.**
KiCad E.D.A. 8.0.6		Id: 4/10


GA[15..0]
VD[15..0]
MAIN_D[7..0]
E11
E12
buffers
A->B
74LS245
flip flops
74LS273
74LS174
hex flip flop
OBJCODELO
GFX_WR
H3_BUF
GFX_CE
74LS08
B6A
C6D
74LS32
C6A
H4_BUF
VCC
R4
3.3kΩ
R3
22Ω
A17
Standby
VDD
GND
Out
12.000MHz
VSS
C17
YM3906
SETA_X1-001
GFX_CLK
VBLK
VSYNC
HBLK
DATAEN
HC[8..0]
H[4..0]
VA[11..0]
SPBANK1
MAIN_A11
MAIN_A[15..0]
HR8
B1F
B1D
74LS04
C6B
Measures Seta X1-001:
CLK_IN.....12MHz
CLK_OUT.....11.07-12.01MHz
VBLK.....59.2Hz
VBLK.....59.3Hz
HBLK2.....15.6KHz
HBLK.....15.6KHz
VSYNC.....59.2Hz
Observatión: Pin 46 (HC0) does not
correspond to the sequence of the HC[8..0] counter.
gfx_ram
File: gfx_ram.kicad_sch
gfx_rom
File: gfx_rom.kicad_sch
JOTEGO
Sheet: /gfx/
File: gfx.kicad_sch
Title: EXTERMINATION
Size: A3
Date: 29/08/2022
Rev: José Tejada G.
KiCad E.D.A. 8.0.6
Id: 5/10



JOTEGO

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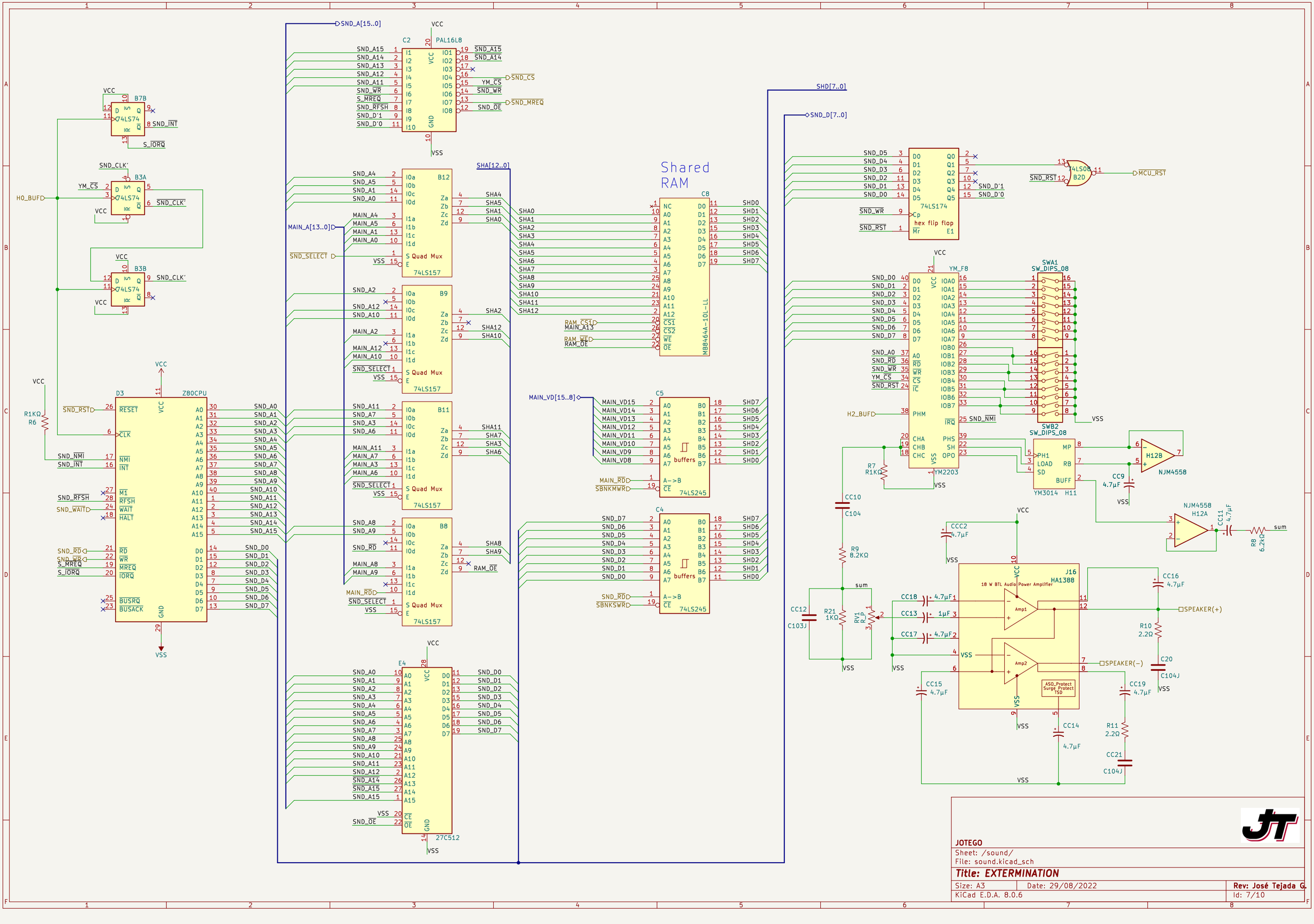
Size: A3	Date: 29/08/2022	**Rev: José Tejada G.**
KiCad E.D.A. 8.0.6		Id: 6/10


SND_A[15..0]
VCC
C2
PAL16L8
SND_A15
SND_A14
SND_A13
SND_A12
SND_A11
SND_WR
S_MREQ
SND_RFSH
SND_D'1
SND_D'0
SND_A15
SND_A14
YM_CS
SND_WR
SND_CS
SND_MREQ
SND_OE
VSS
B7B
74LS74
SND_INT
S_IORQ
SND_CLK'
B3A
YM_CS
H0_BUFF
B3B
SHA[12..0]
Shared
RAM
C8
MB8464A-10L-LL
RAM_CS1
MAIN_A13
RAM_WE
RAM_OE
MAIN_A[13..0]
SND_SELECT
74LS157
MAIN_VD[15..8]
C5
C4
buffers
74LS245
MAIN_RD
SBNKMWR
SBNKSWR
SHD[7..0]
SND_D[7..0]
74LS174
hex flip flop
SND_RST
MCU_RST
74LS08
B2D
YM_F8
SWA1
SW_DIPS_08
SWB2
H2_BUFF
SND_NMI
YM2203
YM3014
H11
H12B
NJM4558
H12A
CC9
4.7µF
CC10
C104
R9
8.2KΩ
sum
R8
6.2KΩ
CC11
CCC2
J16
HA1388
18 W BTL Audio Power Amplifier
Amp1
Amp2
SPEAKER(+)
SPEAKER(−)
CC16
CC18
CC13
1µF
CC17
CC12
C103J
R21
1KΩ
RV1
R10
2.2Ω
C20
C104J
CC15
CC19
CC14
R11
CC21
ASO_Protect
Surge Protect
TSD
R7
R1KΩ
R1KΩ
R6
D3
Z80CPU
RESET
CLK
NMI
INT
M1
RFSH
WAIT
HALT
MREQ
IORQ
BUSRQ
BUSACK
SND_RD
SND_WR
SND_MREQ
SND_IORQ
SND_RFSH
SND_WAIT
E4
27C512
JOTEGO
Sheet: /sound/
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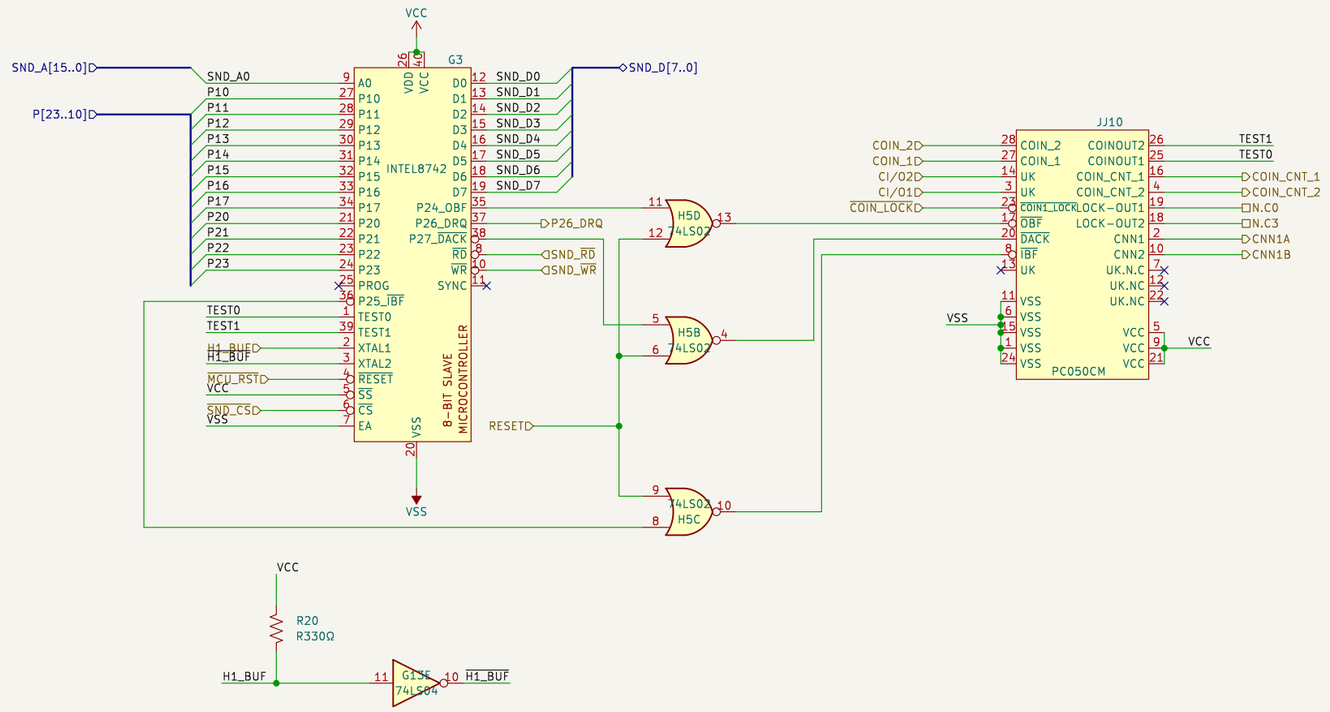
Title: EXTERMINATION
Size: A3
Date: 29/08/2022
Rev: José Tejada G.
KiCad E.D.A. 8.0.6
Id: 7/10



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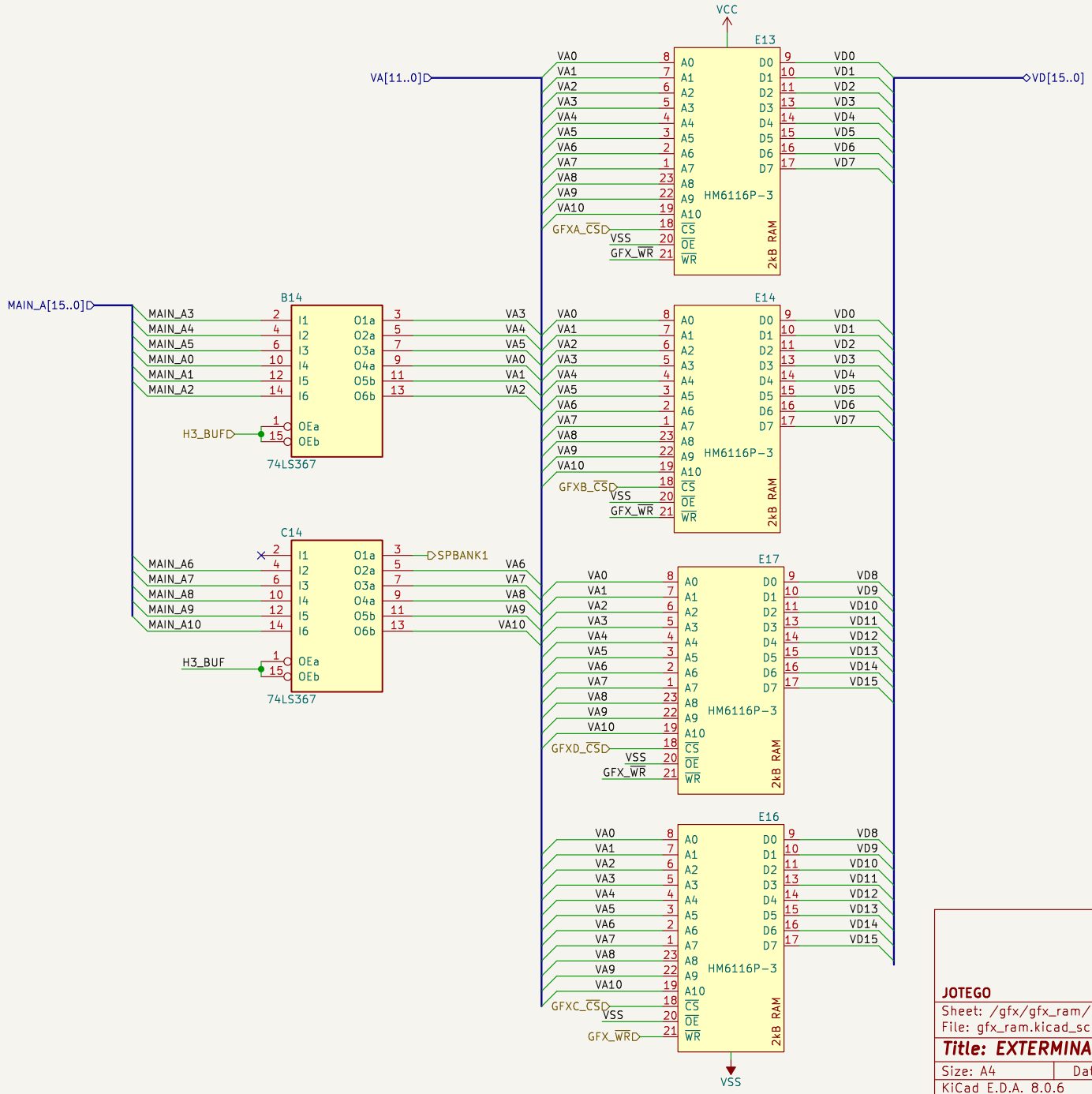
Size: A3	Date: 29/08/2022	**Rev: José Tejada G.**
KiCad E.D.A. 8.0.6		Id: 8/10



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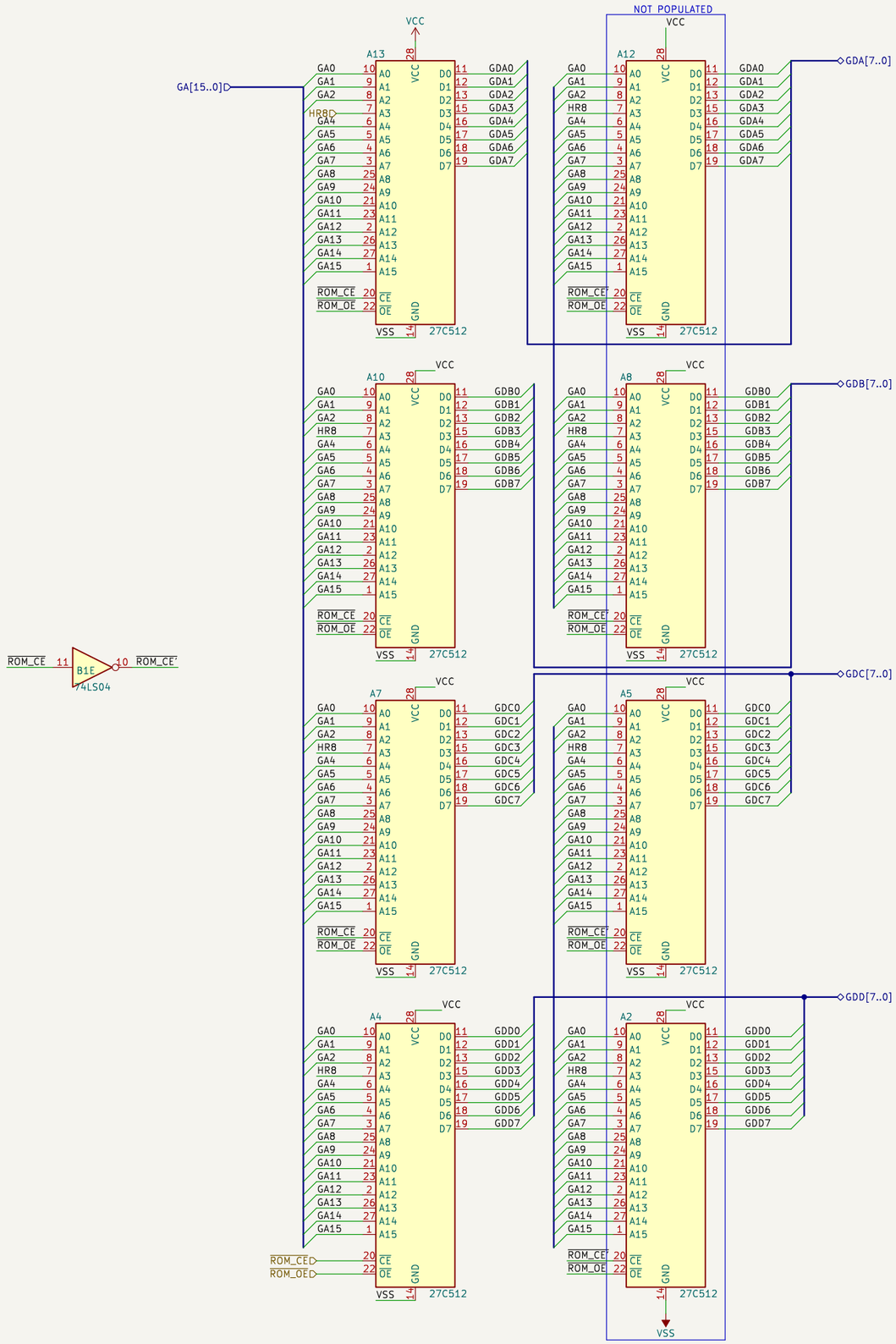
Size: A4	Date: 29/08/2022	**Rev: José Tejada G.**
KiCad E.D.A. 8.0.6		Id: 9/10



JOTEGO

Sheet: /gfx/gfx_rom/
File: gfx_rom.kicad_sch

Title: EXTERMINATION

Size: A3	Date: 29/08/2022	**Rev: José Tejada G.**
KiCad E.D.A. 8.0.6		Id: 10/10