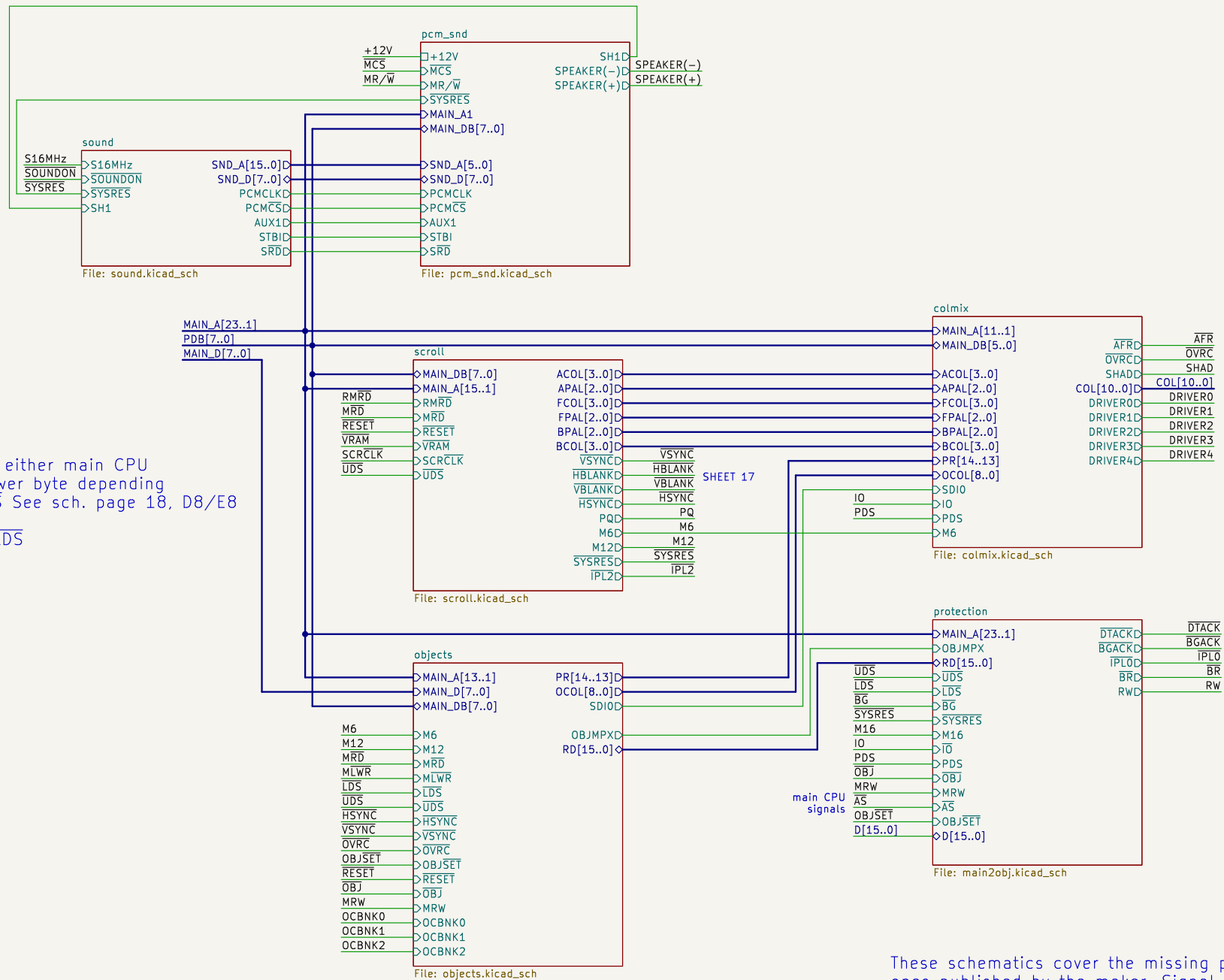


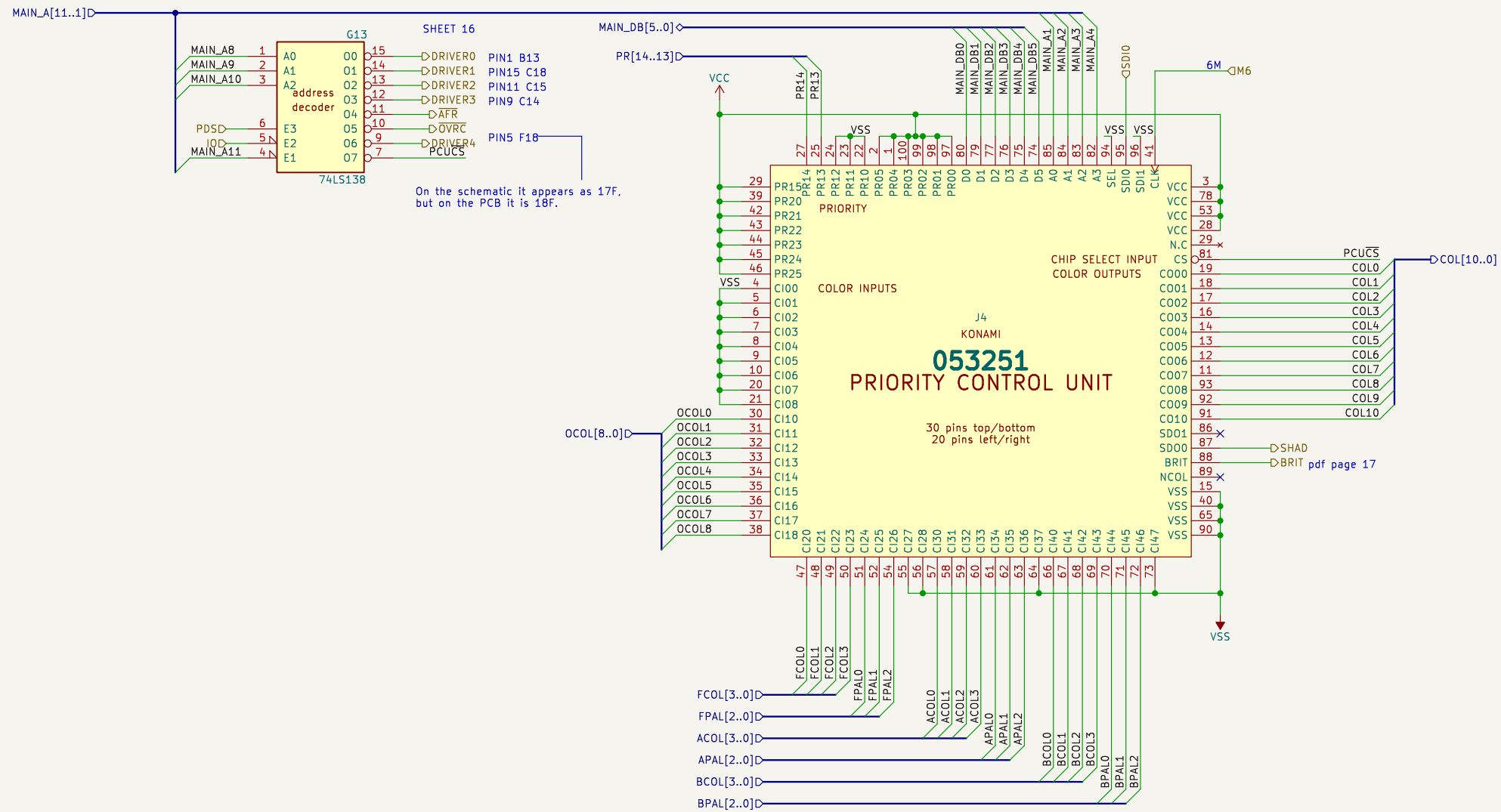
PDB[7:0] is either main CPU
upper or lower byte depending
on UDS/LDS See sch. page 18, D8/E8

$PDS = \overline{UDS} \& \overline{LDS}$



These schematics cover the missing pages in the original ones published by the maker. Signal names existing in the original pages have been preserved. New signal names try to follow the maker style or are taken from similar schematics of the same maker.





SHEET 02



