

1151

B

1151

C



C

D

E

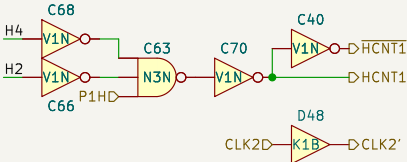
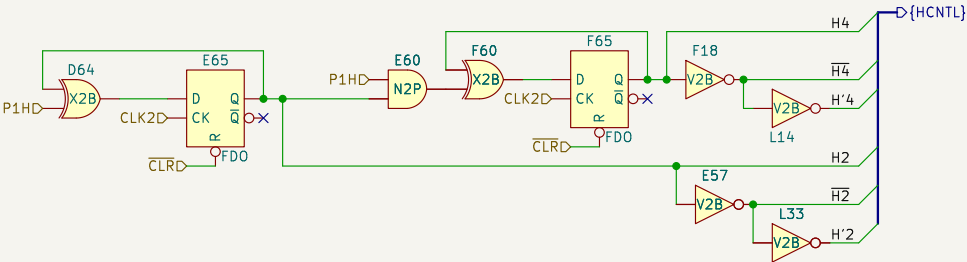
**F**

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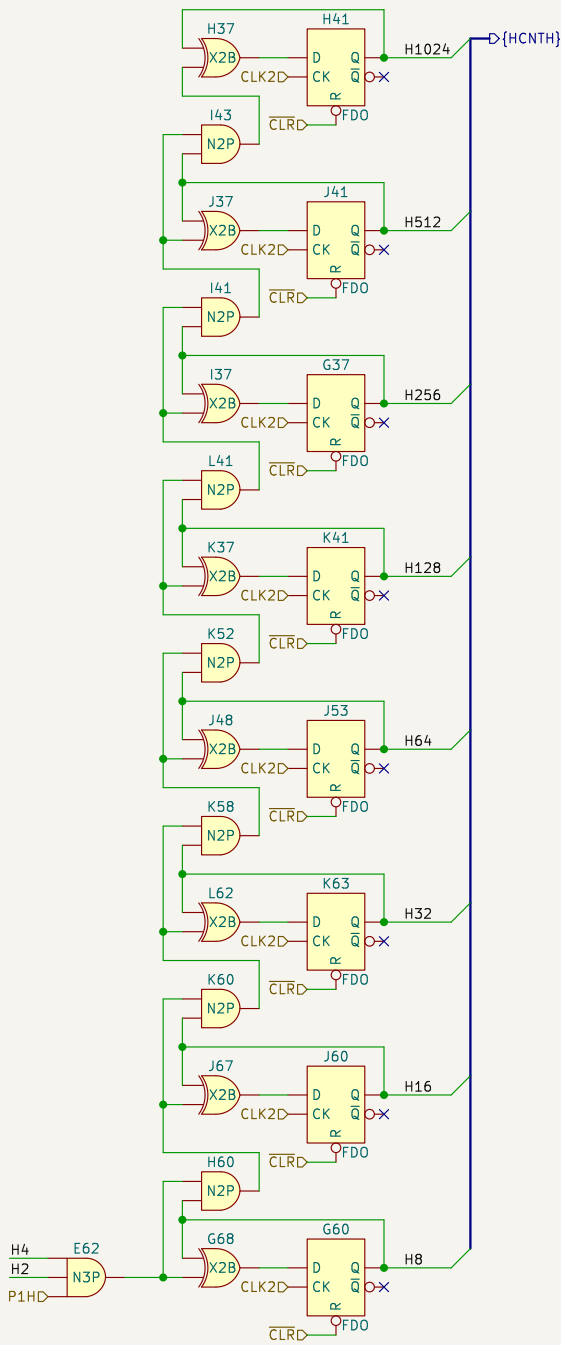
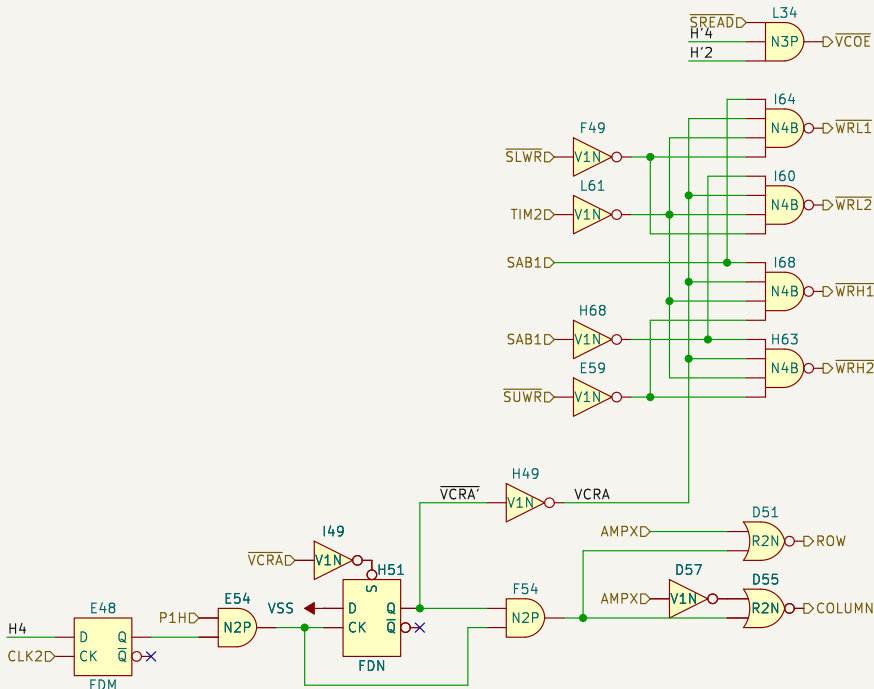
Horizontal clock P1H and  $\overline{\text{CLR}}$  initiates the timing of the 007780. H2 and H4 are also generated which creates a 3-bit counter, HCNT, which controls the timing of the device. There are  $2^3 = 8$  different counter values: 0..7.

HCNT 0,1 Render Tilemap 1  
HCNT 2,3 Render Tilemap 2  
HCNT 4,5 Idle, writing to page 0  
HCNT 6,7 CPU read/write cycle

TIM2 is active low during HCNT cycles 6 and 7.  
When HCNT is 4 or 5 then row address = 0. The column address is incremented by one for each HCNT cycle. Is this used to not wear out the DRAM modules?



### DRAM Control Signals



Sheet: /Counters/  
File: counters.kicad\_sch.kicad\_sch

**Title: Konami 007780**

Size: A3 Date: 2024-07-28

KiCad E.D.A. 8.0.4

Rev:

Id: 2/3

