

Course Name: Embedded Systems Design

Course Number and Section: 14:332:493:02

Homework #3

Submitted by: Angie Flores - af770

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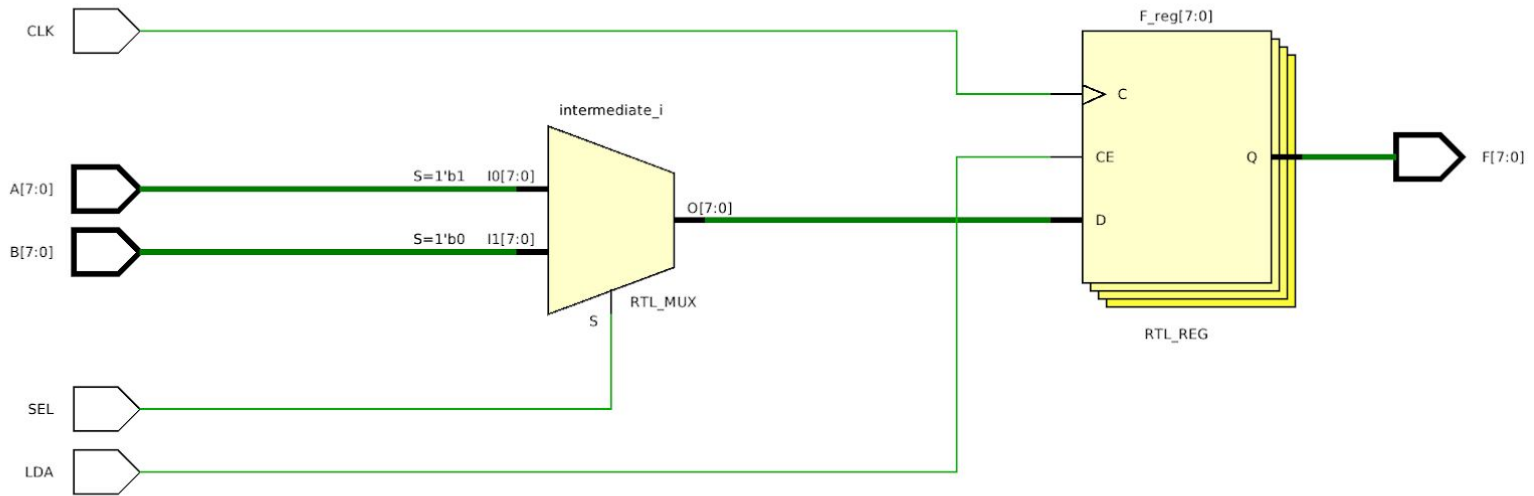
CHAPTER 7

• EXERCISE 1

VHDL Code:

```
1  library ieee;
2      use ieee.std_logic_1164.all;
3      use ieee.numeric_std.all;
4
5  entity entidad is
6      port(
7
8          A,B : in std_logic_vector(7 downto 0);
9          SEL, CLK, LDA : in std_logic;
10         F: out std_logic_vector(7 downto 0)
11
12     );
13 end entidad;
14
15 architecture behavior of entidad is
16
17     signal intermediate : std_logic_vector(7 downto 0);
18
19 begin
20     r:process(CLK)
21     begin
22         if (rising_edge(CLK)) then
23             if (LDA = '1') then
24                 F <= intermediate;
25             end if;
26         end if;
27     end process;
28
29     with SEL select
30     intermediate<=A when '1',
31                 B when '0',
32                 (others => '0') when others;
33
34 end behavior;
```

RTL in Vivado:

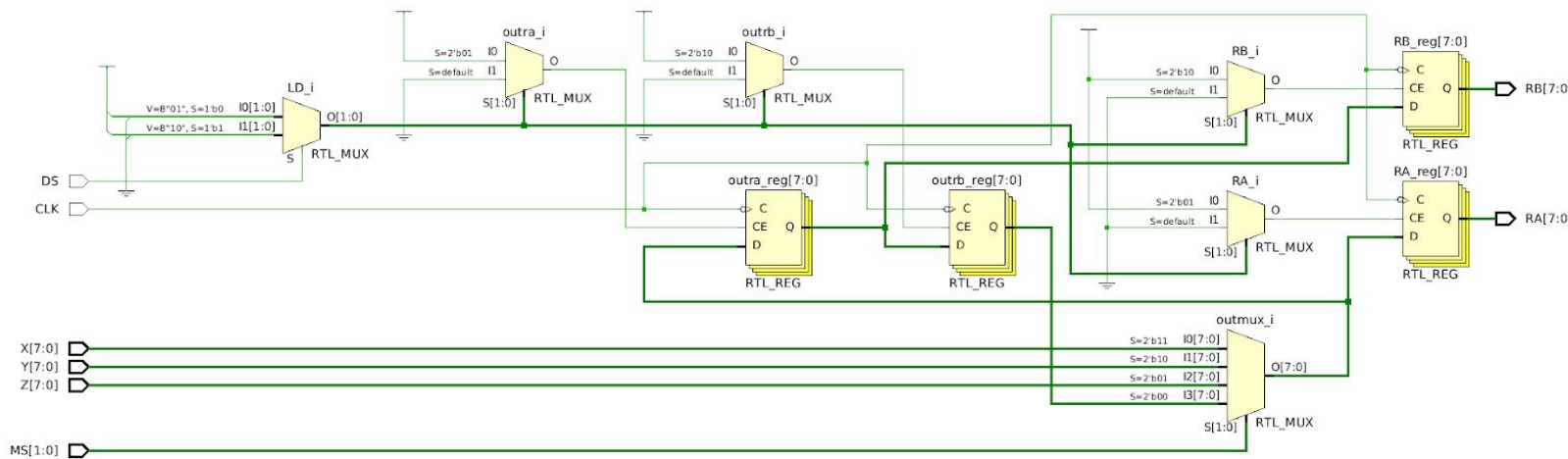


● EXERCISE 2

VHDL Code:

```
1  library ieee;
2      use ieee.std_logic_1164.all;
3      use ieee.numeric_std.all;
4
5  entity entidad is
6      port(
7
8          X,Y,Z : in std_logic_vector(7 downto 0);
9          MS: in std_logic_vector(1 downto 0);
10         CLK, DS : in std_logic;
11         RA, RB: out std_logic_vector(7 downto 0)
12
13     );
14 end entidad;
15
16 architecture behavior of entidad is
17
18     signal outmux, outra, outrb : std_logic_vector(7 downto 0);
19     signal LD: std_logic_vector(1 downto 0);
20
21 begin
22     registera: process(CLK)
23     begin
24         if (falling_edge(CLK)) then
25             if (LD="01") then
26                 outra <= outmux;
27                 RA <= outmux;
28             end if;
29         end if;
30     end process;
31
32     registerb: process(CLK)
33     begin
34         if (falling_edge(CLK)) then
35             if (LD="10") then
36                 outrb <= outra;
37                 RB <= outra;
38             end if;
39         end if;
40     end process;
41
42     dec:process(DS)
43     begin
44         case DS is
45             when '0' => LD <= "01";
46             when '1' => LD <= "10";
47             when others => LD <= "00";
48         end case;
49     end process;
50
51     with MS select
52     outmux <= X when "11",
53             Y when "10",
54             Z when "01",
55             outra when "00",
56             "00000000" when others;
57
58 end behavior;
```

RTL in Vivado:



● EXERCISE 3

VHDL Code:

```
1  library ieee;
2      use ieee.std_logic_1164.all;
3      use ieee.numeric_std.all;
4
5  entity entidad is
6      port(
7
8          X , Y : in std_logic_vector(7 downto 0);
9          LDA,LDB,S1,S0,CLK: in std_logic;
10         RB: out std_logic_vector(7 downto 0)
11
12     );
13 end entidad;
14
15 architecture behavior of entidad is
16
17     signal outmux1, outmux2, outra, outrb : std_logic_vector(7 downto 0);
18
19 begin
20     registera: process(CLK)
21     begin
22         if (rising_edge(CLK)) then
23             if (LDA='1') then
24                 outra <= outmux1;
25             end if;
26         end if;
27     end process;
28
29     registerb: process(CLK)
30     begin
31         if (rising_edge(CLK)) then
32             if (LDB='1') then
33                 outrb <= outmux2;
34                 RB <= outmux2;
35             end if;
36         end if;
37     end process;
38
39     with S1 select
40         outmux1 <= X when '1',
41                 outrb when '0',
42                 "00000000" when others;
43
44
45     with S0 select
46         outmux2 <= outra when '1',
47                 Y when '0',
48                 "00000000" when others;
49
50 end behavior;
```

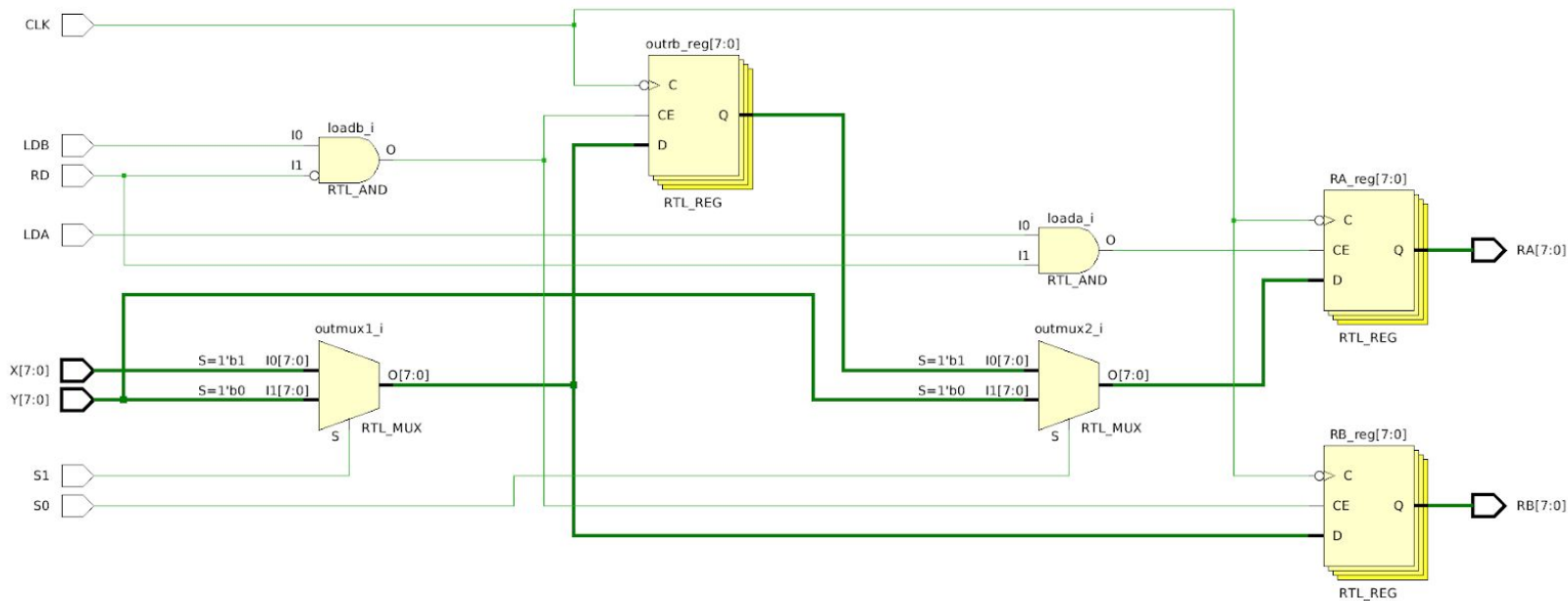
RTL in Vivado:

● EXERCISE 4

VHDL Code:

```
1  library ieee;
2      use ieee.std_logic_1164.all;
3      use ieee.numeric_std.all;
4
5  entity entidad is
6      port(
7
8          X , Y : in std_logic_vector(7 downto 0);
9          RD, LDA,LDB,S1,S0,CLK: in std_logic;
10         RA, RB: out std_logic_vector(7 downto 0)
11
12     );
13 end entidad;
14
15 architecture behavior of entidad is
16
17     signal outmux1, outmux2, outrb : std_logic_vector(7 downto 0);
18     signal loada,loadb : std_logic;
19
20 begin
21     registera: process(CLK)
22     begin
23         if (falling_edge(CLK)) then
24             if (loada='1') then
25                 RA <= outmux2;
26             end if;
27         end if;
28     end process;
29
30     registerb: process(CLK)
31     begin
32         if (falling_edge(CLK)) then
33             if (loadb='1') then
34                 outrb <= outmux1;
35                 RB <= outmux1;
36             end if;
37         end if;
38     end process;
39
40     loadb <= LDB AND NOT(RD);
41     loada <= LDA AND RD;
42
43     with S0 select
44     outmux2 <= outrb when '1',
45              Y when '0',
46              "00000000" when others;
47
48     with S1 select
49     outmux1 <= X when '1',
50              Y when '0',
51              "00000000" when others;
52
53 end behavior;
```


RTL in Vivado:

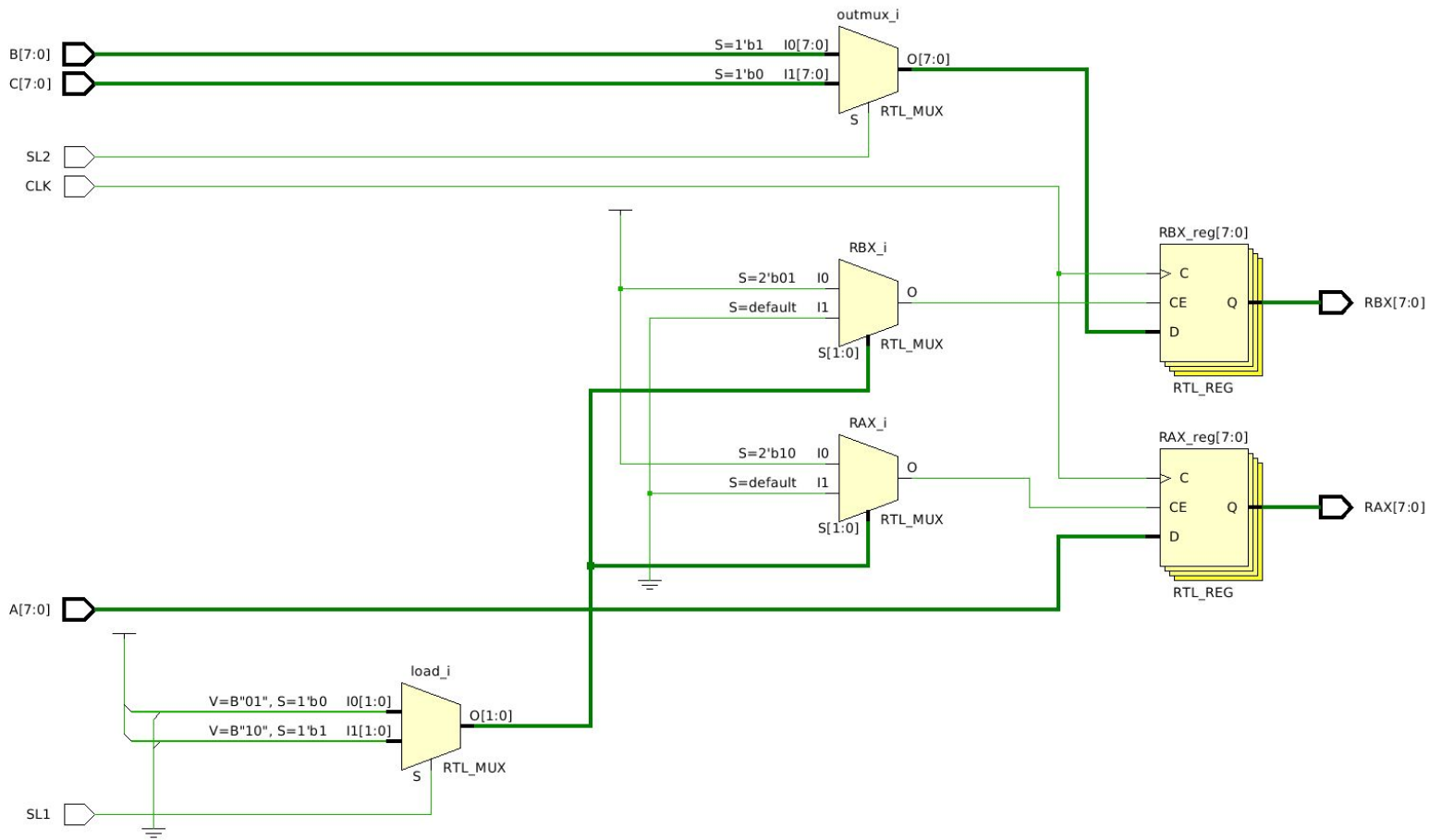


• EXERCISE 5

VHDL Code:

```
1  library ieee;
2      use ieee.std_logic_1164.all;
3      use ieee.numeric_std.all;
4
5  entity entidad is
6      port(
7
8          A, B,C: in std_logic_vector(7 downto 0);
9          SL1, SL2, CLK: in std_logic;
10         RAX,RBX: out std_logic_vector(7 downto 0)
11     );
12 end entidad;
13
14 architecture behavior of entidad is
15
16     signal outmux:std_logic_vector(7 downto 0);
17     signal load:std_logic_vector(1 downto 0);
18
19 begin
20     registera: process(CLK)
21     begin
22         if (rising_edge(CLK)) then
23             if (load="10") then
24                 RAX <= A;
25             end if;
26         end if;
27     end process;
28
29     registerb: process(CLK)
30     begin
31         if (rising_edge(CLK)) then
32             if (load="01") then
33                 RBX <= outmux;
34             end if;
35         end if;
36     end process;
37
38     dec:process(SL1)
39     begin
40         case SL1 is
41             when '0' => load <= "01";
42             when '1' => load <= "10";
43             when others => load <= "00";
44         end case;
45     end process;
46
47     with SL2 select
48     outmux <= B when '1',
49             C when '0',
50             "00000000" when others;
51
52 end behavior;
```

RTL in Vivado:



● EXERCISE 6

VHDL Code:

```
1  library ieee;
2      use ieee.std_logic_1164.all;
3      use ieee.numeric_std.all;
4
5  entity entidad is
6      port(
7
8          A, B,C: in std_logic_vector(7 downto 0);
9          SEL1, SEL2, CLK: in std_logic;
10         RAP, RBP: out std_logic_vector(7 downto 0)
11     );
12 end entidad;
13
14 architecture behavior of entidad is
15
16     signal outmux:std_logic_vector(7 downto 0);
17     signal load:std_logic_vector(1 downto 0);
18
19 begin
20     registra: process(CLK)
21     begin
22         if (rising_edge(CLK)) then
23             if (load="10") then
24                 RAP <= outmux;
25             end if;
26         end if;
27     end process;
28
29     registerb: process(CLK)
30     begin
31         if (rising_edge(CLK)) then
32             if (load="01") then
33                 RBP <= C;
34             end if;
35         end if;
36     end process;
37
38     dec:process(SEL2)
39     begin
40         case SEL2 is
41             when '0' => load <= "01";
42             when '1' => load <= "10";
43             when others => load <= "00";
44         end case;
45     end process;
46
47     with SEL1 select
48     outmux <= A when '1',
49              B when '0',
50              "00000000" when others;
51
52 end behavior;
```

RTL in Vivado:

