Course Name: Embedded Systems Design

Course Number and Section: 14:332:493:02

Lab 1 - Clocks, Counters and Buttons

Submitted by: Angie Flores - af770

Date Submitted: 02/27/2020

Purpose:

- ***What is the intent of the lab? (To design, test, or implement a/an xyz?)***

The intent of this lab is to design, test and implement a counter controlled by buttons and switches, to see a descending or ascending counting in the LEDs of the Zybo board.

For each part of the Lab:

<u>Part 1:</u>

- ***Theory of Operation:***

  ➔ ***How will or should the circuit behave?***

The circuit should behave like a new clock, where the output is going to be a one clock cycle ON every 500 ms, it will behave like a chirp.

  ➔ ***What do you expect to happen?***

I expect the LED0 to blink every 500 ms, since the output div has a spike every 500 ms, the new speed is 2 HZ.

- ***Schematic Diagram (as desired)***

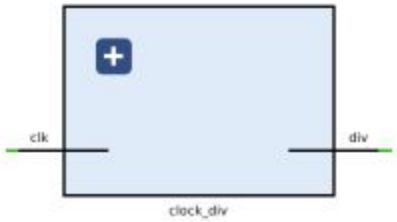


Figure 1.2: clk_div block diagram

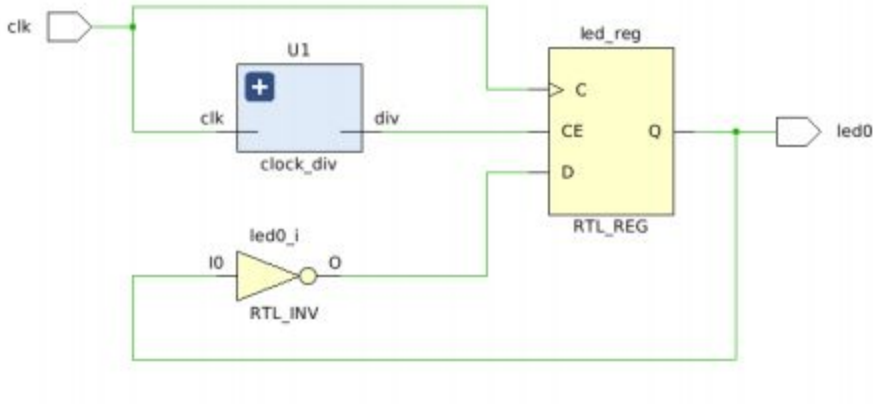
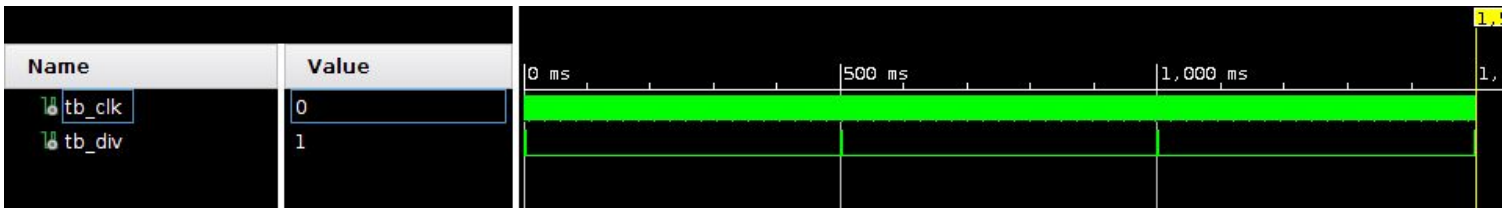


Figure 1.3: divider_top block diagram

- ***Testing/Simulation***

  ➔ **Screenshots of simulation result/waveforms**

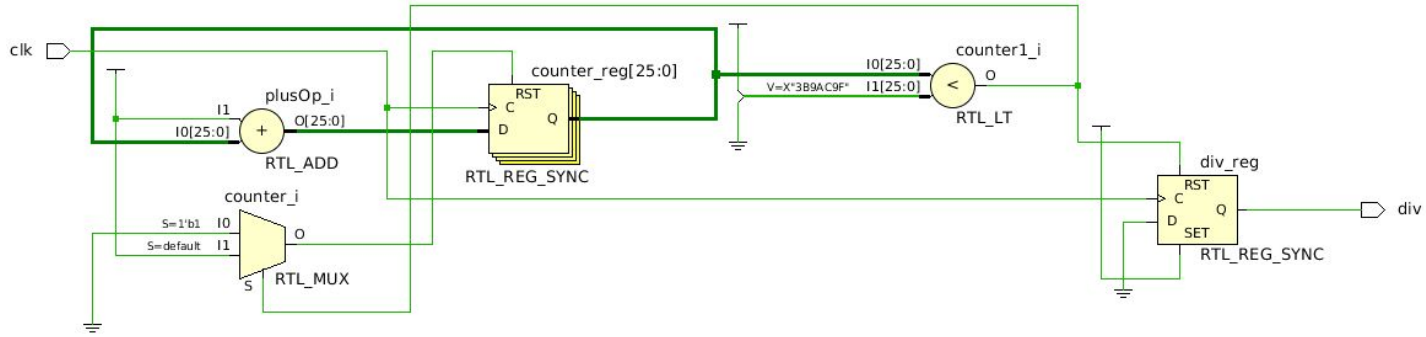
Simulation for clk_div: (There are spikes every 500 ms) :



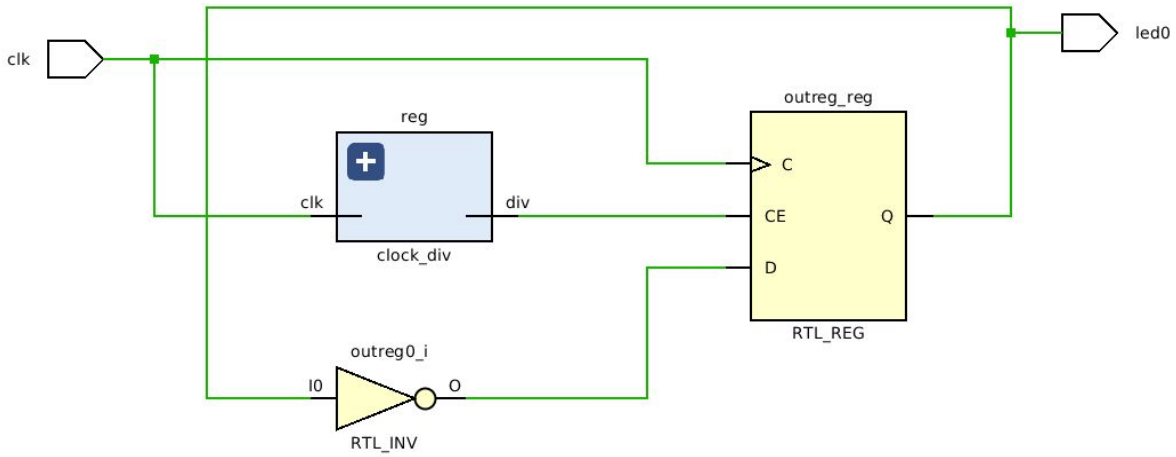
- ***Implementation***

  ➔ ***Vivado Elaboration Schematic***

Schematic for clk_div:

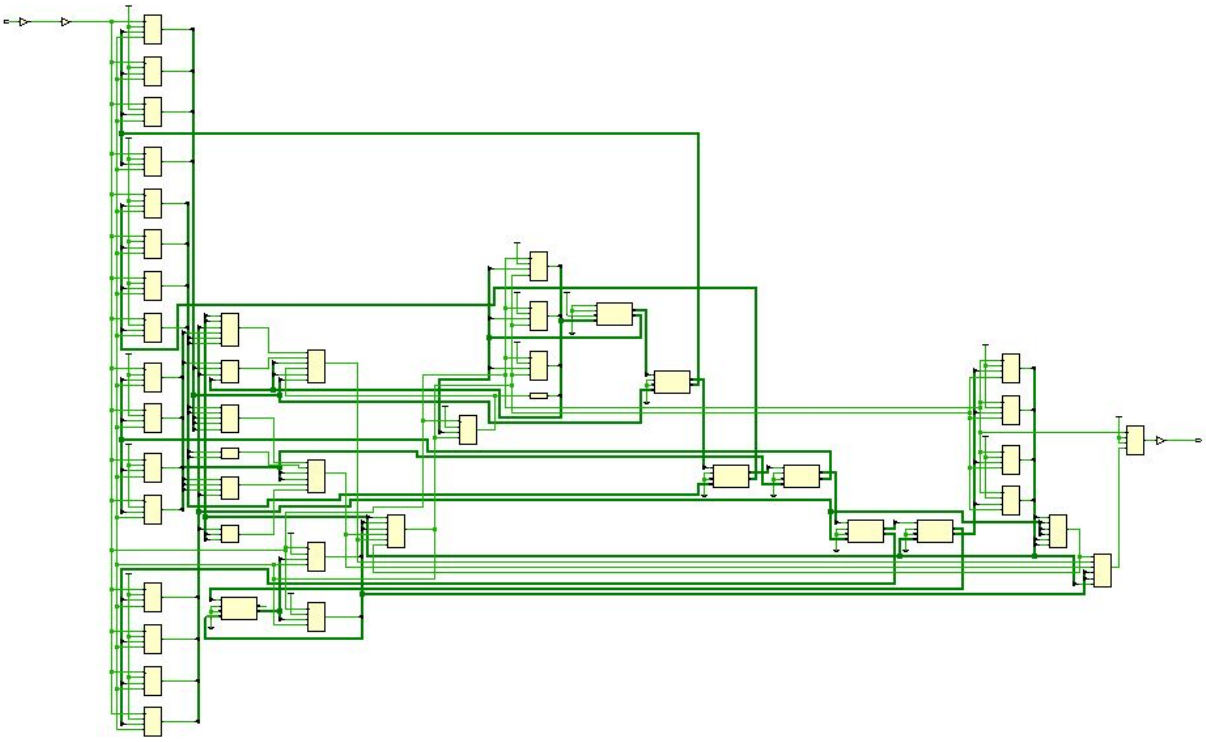


Schematic for divider_top:

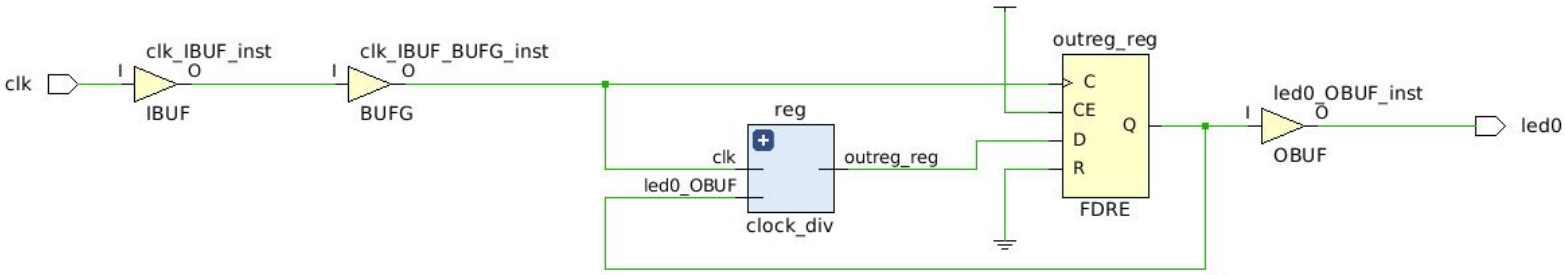


➔ ***Vivado Synthesis Schematic***

Synthesis Schematic for clk_div:



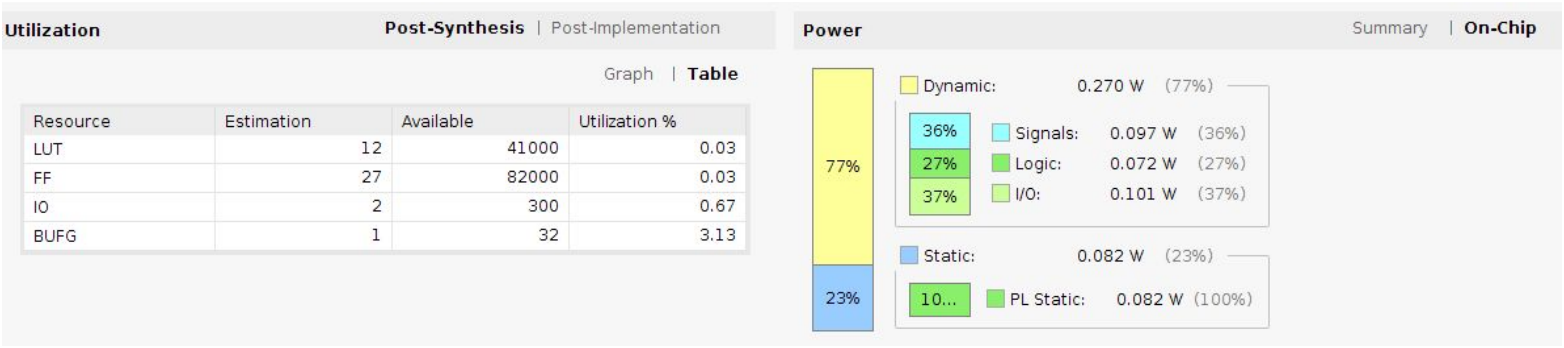
Synthesis Schematic for divider_top:



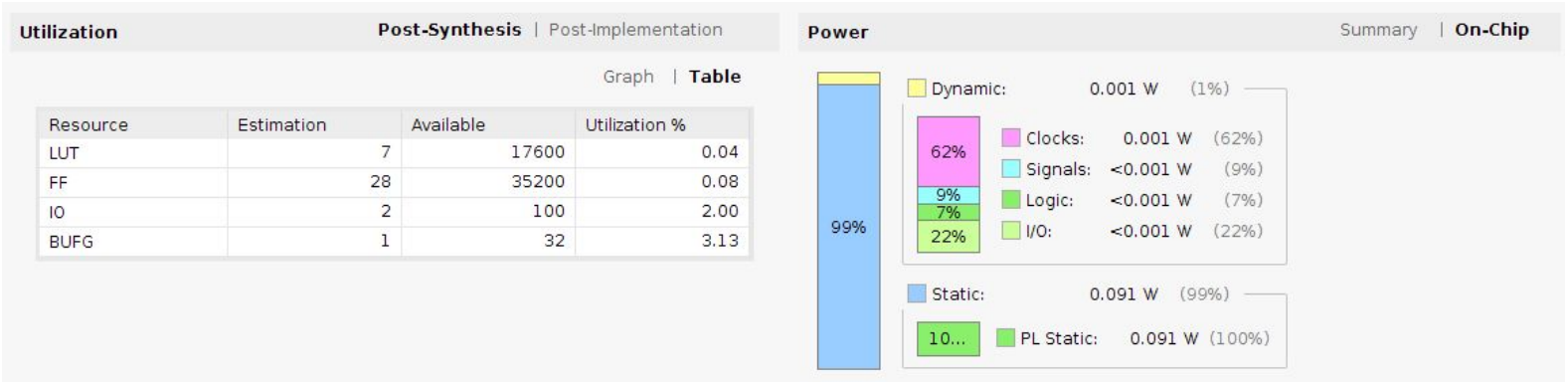
➔ ***Vivado Project Summary Images***

- ❖ ***Post Synthesis Utilization Table***
- ❖ ***On– Chip Power Graphs***

For clk_div:



For divider_top:



➔ ***Explain what you had to put in your constraint (.xdc) file and why***

I had to uncomment the LED0 line, so it can work.

Part 2:

- ***Theory of Operation:***

  ➔ ***How will or should the circuit behave?***

After 20 ms, the output of dbnc should be 1, and before that should be 0, if the input button is 1, it is a debounce circuit.

  ➔ ***What do you expect to happen?***

I expect the button signal to go through 2 shift registers and get the output 1 after 20 ms.

- ***Schematic Diagram (as desired)***

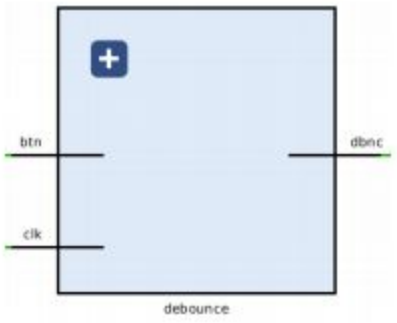
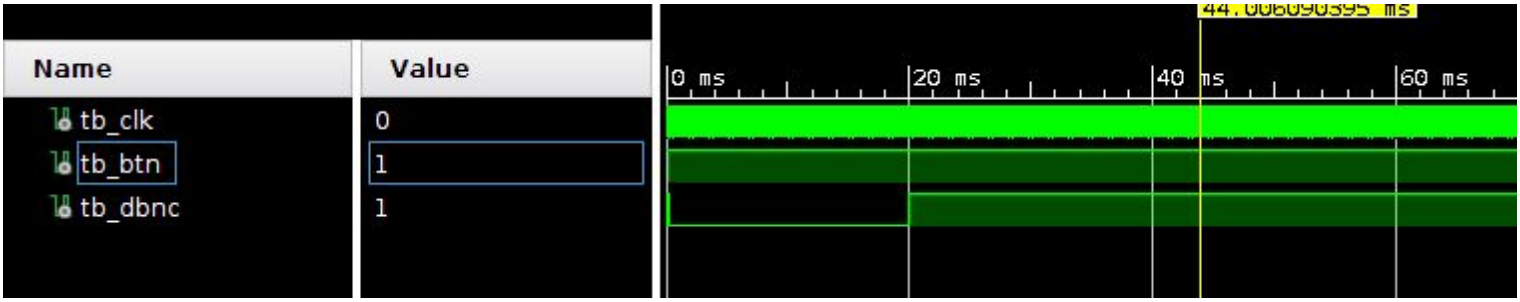


Figure 1.6: debounce block diagram

- ***Testing/Simulation***

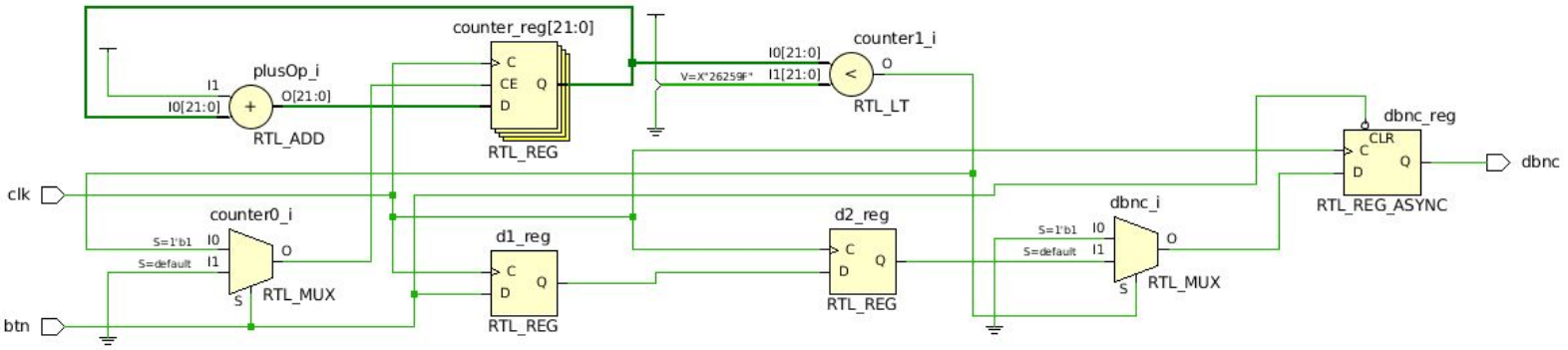
  ➔ **Screenshots of simulation result/waveforms**

Simulation of debounce:

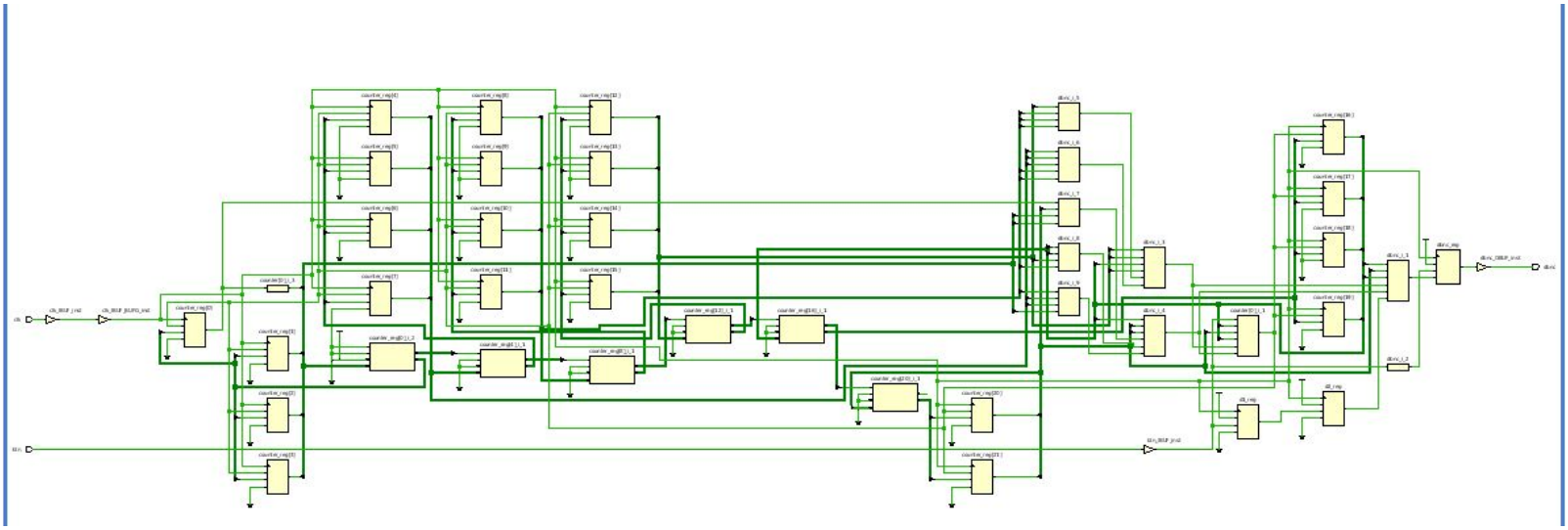


- ***Implementation***

  ➔ ***Vivado Elaboration Schematic***



➔ ***Vivado Synthesis Schematic***



➔ ***Vivado Project Summary Images***

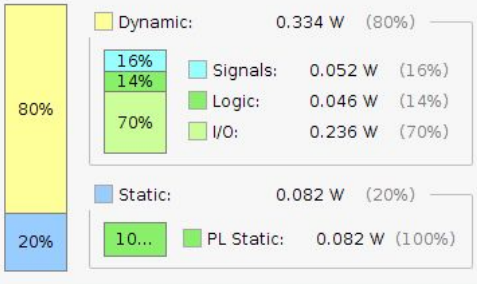
- ❖ ***Post Synthesis Utilization Table***
- ❖ ***On – Chip Power Graphs***

Utilization **Post-Synthesis** | Post-Implementation

Graph | **Table**

Resource	Estimation	Available	Utilization %
LUT	11	41000	0.03
FF	25	82000	0.03
IO	3	300	1.00
BUFG	1	32	3.13

Power Summary | **On-Chip**



➔ ***Explain what you had to put in your constraint (.xdc) file and why***

I didn't use it for this part.

<u>Part 3:</u>

- ***Theory of Operation:***

  ➔ ***How will or should the circuit behave?***

The circuit should behave like a counter, count until value, through the commands of the inputs.

➔ ***What do you expect to happen?***

I expect to have my output count to count until the value, load the value in the val pin when ld is 1 and updn load in the value when dir pin is 1.

- ***Schematic Diagram (as desired)***

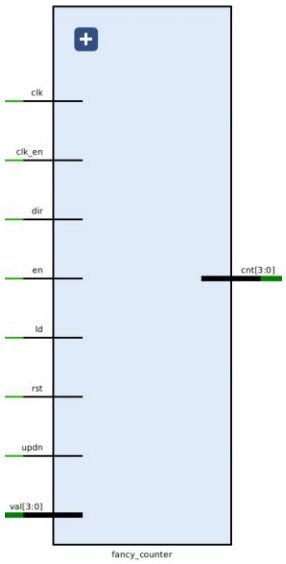
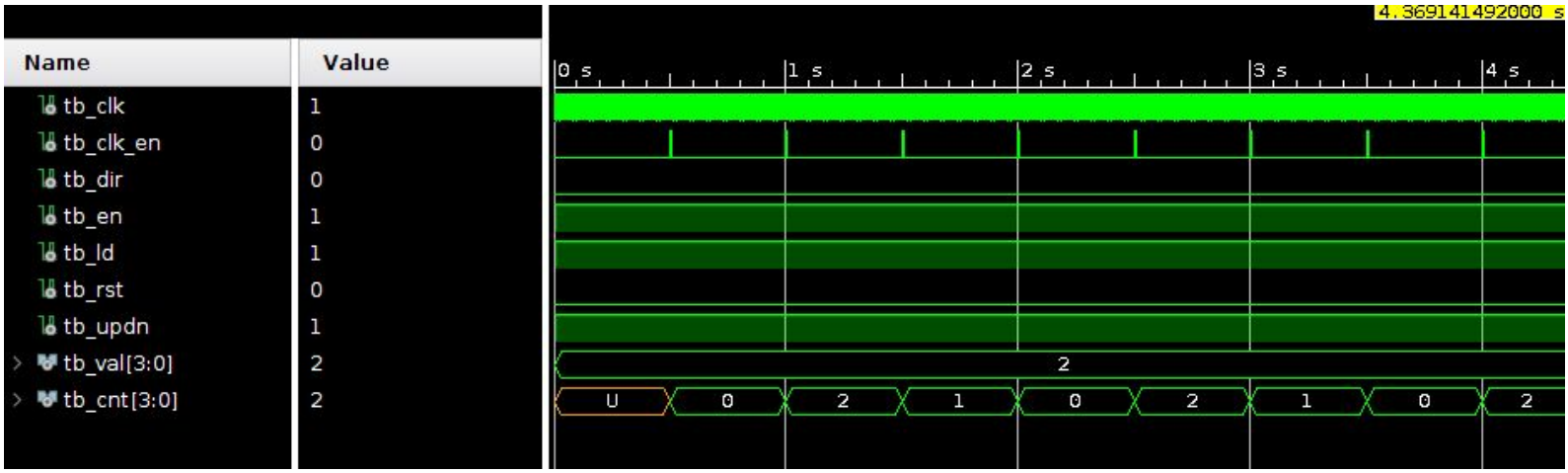


Figure 1.7: fancy_counter block diagram

- ***Testing/Simulation***

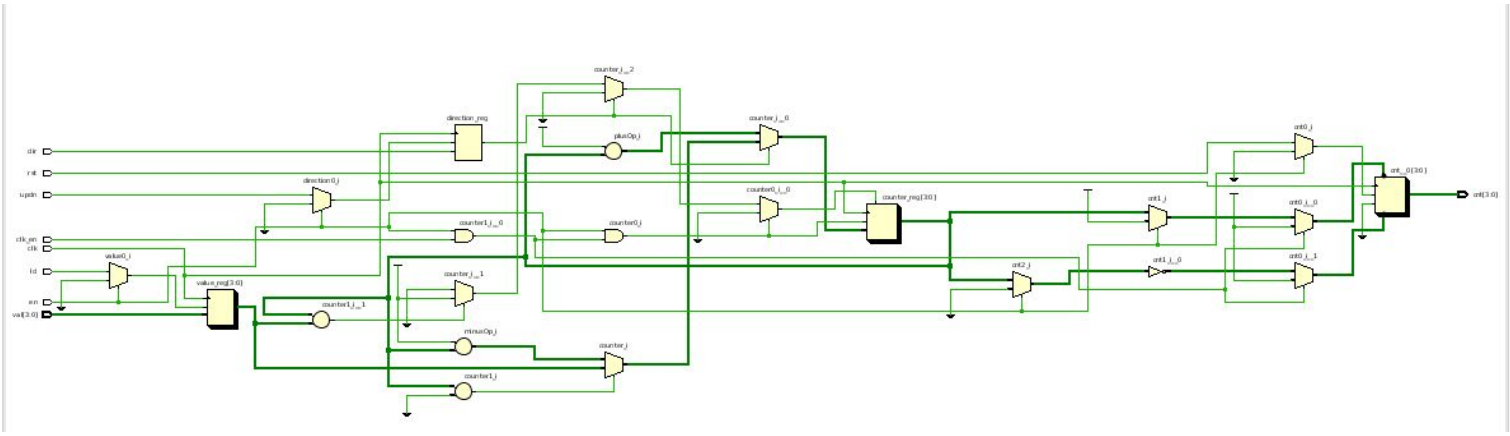
  ➔ **Screenshots of simulation result/waveforms**

Simulation of fancy_counter:

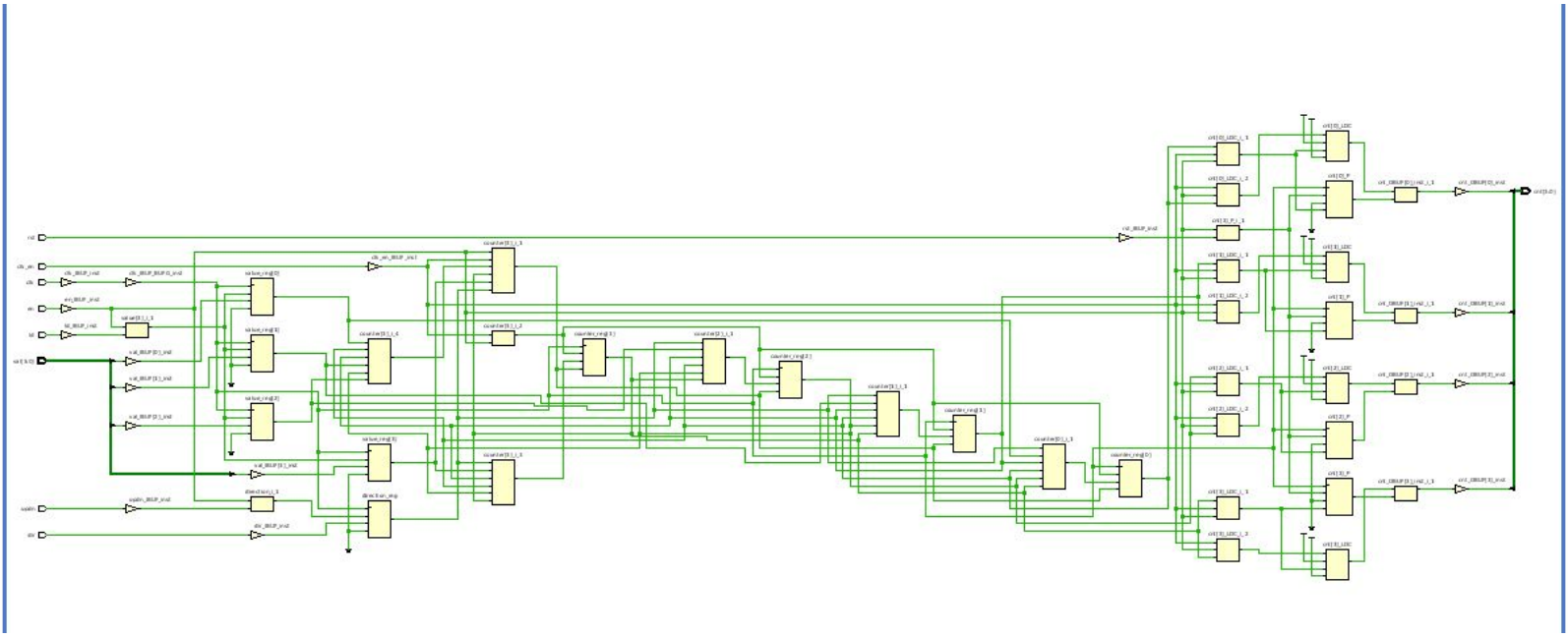


- ***Implementation***

  ➔ ***Vivado Elaboration Schematic***



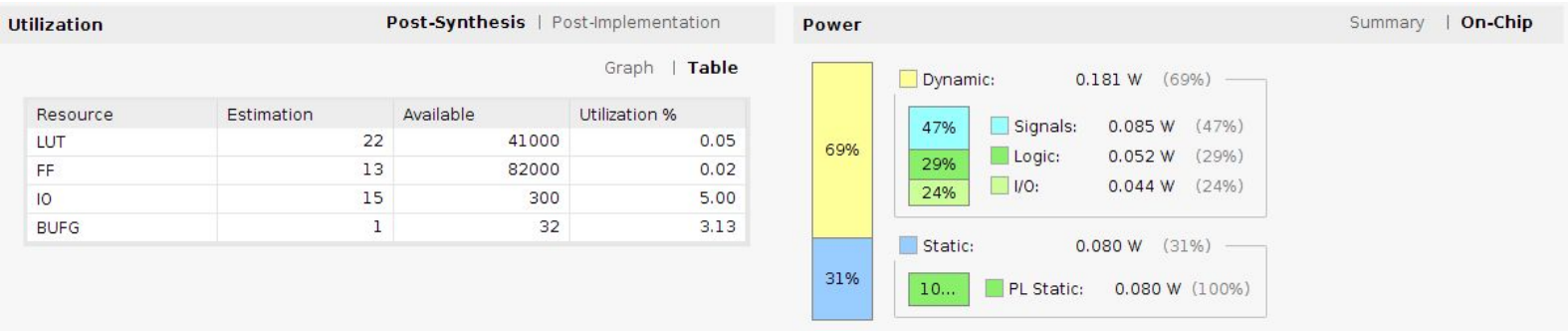
  ➔ ***Vivado Synthesis Schematic***



➔ ***Vivado Project Summary Images***

❖ ***Post Synthesis Utilization Table***

❖ ***On – Chip Power Graphs***



➔ ***Explain what you had to put in your constraint (.xdc) file and why***

I didn't use it for this part.

<u>Part 4:</u>

- ***Theory of Operation:***

  ➔ ***How will or should the circuit behave?***

The circuit should blink like a counter in the LEDs while the button 1 is pressed, since that is the enable button, get the value load and resetted through button 2 & 3.

➔ ***What do you expect to happen?***

I expect my circuit to call my other functions and my output to give the numbers from up to down or down to up depending on my direction pin, and my buttons pressed.

- ***Schematic Diagram (as desired)***

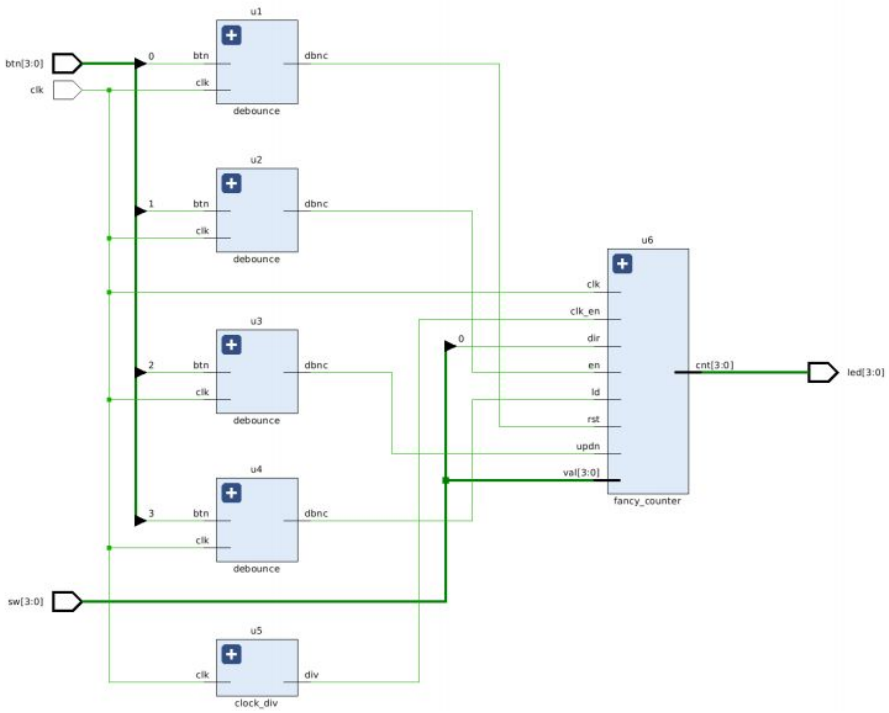
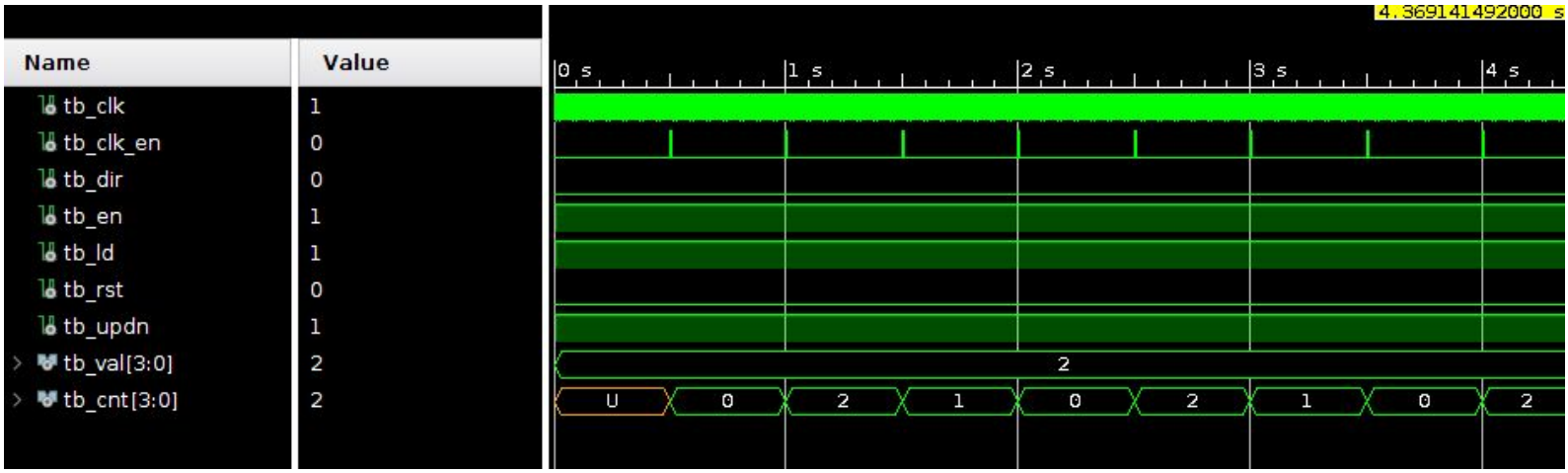


Figure 1.8: counter_top block diagram

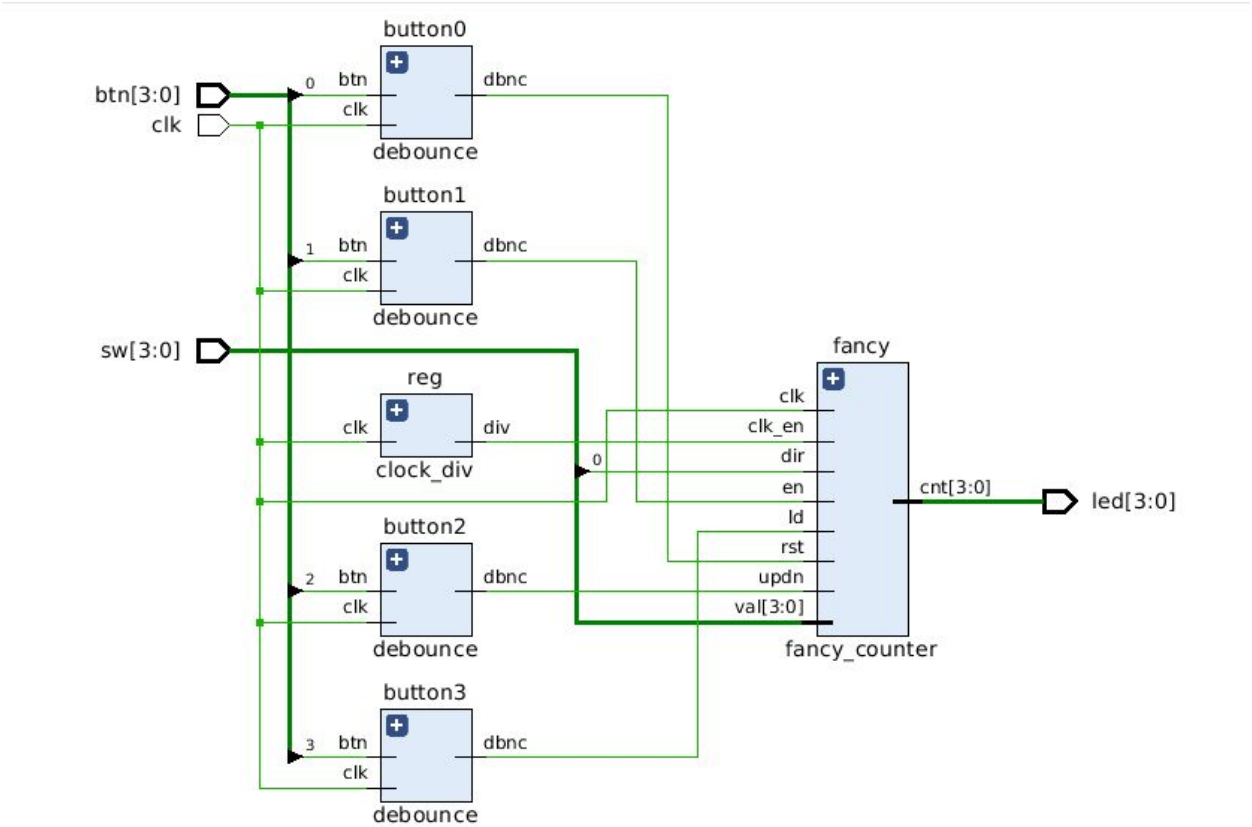
- ***Testing/Simulation***

  ➔ **Screenshots of simulation result/waveforms**

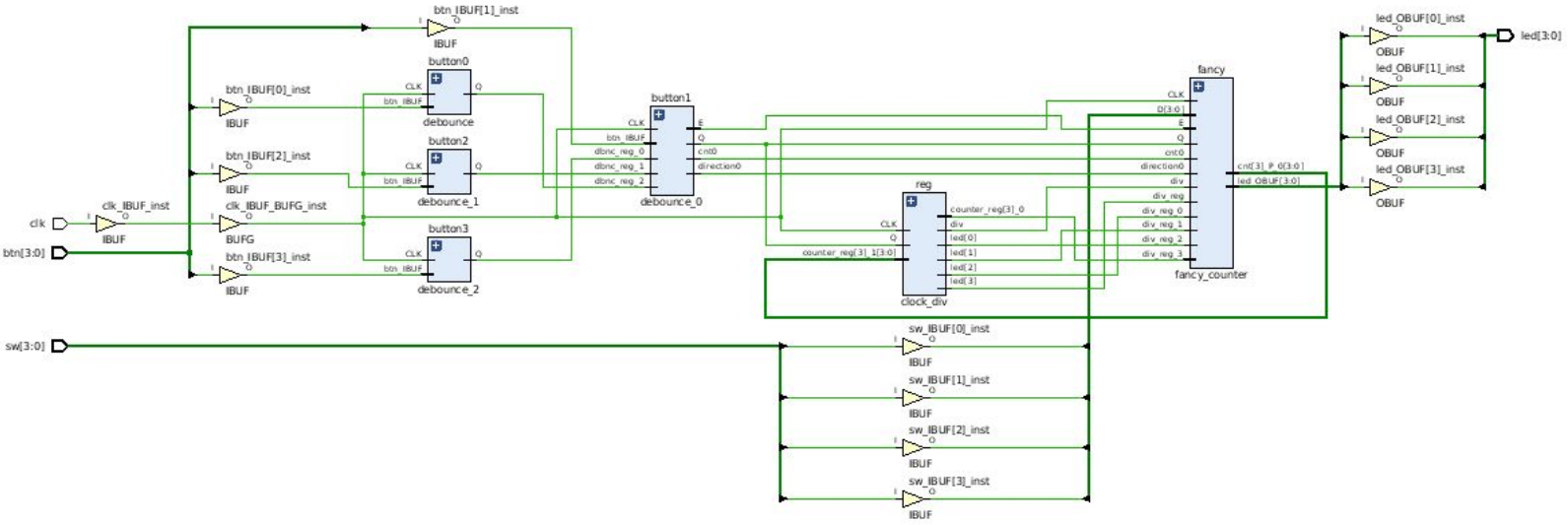


- ***Implementation***

  ➔ ***Vivado Elaboration Schematic***



➔ ***Vivado Synthesis Schematic***



➔ ***Vivado Project Summary Images***

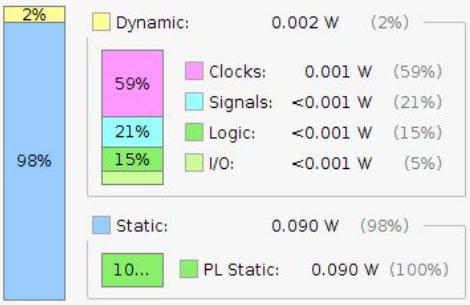
- ❖ ***Post Synthesis Utilization Table***
- ❖ ***On – Chip Power Graphs***

Utilization Post-Synthesis | **Post-Implementation**

Graph | **Table**

Resource	Utilization	Available	Utilization %
LUT	73	17600	0.41
FF	140	35200	0.40
IO	13	100	13.00
BUFG	1	32	3.13

Power Summary | **On-Chip**



➔ ***Explain what you had to put in your constraint (.xdc) file and why***

I had to uncomment the LED0 line, so it can work.

Discussion:

- ***Answer to specific Lab Manual questions:***

<u>Part 1:</u>

1. ***How much do we need to divide our input by to get from 125 MHz to 2 Hz?***

We need to divide the input in 62500000 countings to get to 2 Hz.

2. ***How many bits are required to store a counter that can count up to the value obtained in Q1.1?***

I will need 26 bits to fit the number 62500000.

<u>Part 2:</u>

1. ***What is the value of the button when it is pressed for the Zybo?***

The value of the button when it is pressed is the value of VCC3V3, which digitally would be 1.

2. ***If we want our debounce time to be 20 ms, and our system clock is 125 MHz, how many ticks do we need a steady '1' to be read for it to count as a '1' ?)***

To get a steady '1' , 2500000 ticks are needed to be read for it to count as a '1'.

3. ***How many bits are required for a counter that can go that high?***

To get the number 2500000, 22 bits are required to get that high.

- ***Observations/Discoveries***

  ➔ ***What did you learn?***

I learned how to make a counter using buttons and switches, how to use the registers to count in bits, and divide the clock at a different speed.

- ***Questions/Follow Up***

  ➔ ***Which concepts do you feel like you completely understand?***

I completely understand now the concept of a clock cycle and the use of the registers as D flip flops, to do countings.

  ➔ ***Any concept you're unsure of?***

I am unsure of the concept of the Chip Power Graph and the Utilization Table, what exactly they are for.