



Reference 90nm Mixed Mode Technology

Design Rule Manual May 2007

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Revision History

| Date | Version | Details |
|------------|---------|--|
| 29-Sept-06 | 1.1 | Document remodeled Added diff – poly spacing rules. Added gate – gate spacing rules. |
| 21-May-07 | 1.2 | Updated change of values for DAC layout. Added new section 0 and 9. Added subsections on MOM cap, junction varactor, serpentine resistor and added new rules. |

0 General Information

0.1 CAD Layer numbers

| Layer | Layer number ¹ | Layer | Layer number |
|---------|---------------------------|-------------|--------------|
| nwell | 1 | varmarker | 31 |
| diff | 2 | rmdmy | 32 |
| poly | 3 | medvtn | 33 |
| pplus | 4 | medvtp | 34 |
| nplus | 5 | diff18 | 35 |
| rpoly | 6 | diff33 | 36 |
| cont | 7 | lowvtn | 37 |
| m1 | 8 | lowvtp | 38 |
| m1text | 9 | highvtn | 39 |
| m2 | 10 | highvtp | 40 |
| m2text | 11 | polytext | 41 |
| m3 | 12 | bjtdummy | 49 |
| m3text | 13 | iplayer | 63 |
| m4 | 14 | psub | 64 |
| m4text | 15 | pindummy | 65 |
| v1 | 16 | rtermmarker | 66 |
| v2 | 17 | ctmdmy | 67 |
| v3 | 18 | momdmy | 68 |
| exclude | 19 | rfdmy | 69 |
| mtcap | 20 | boundary | 127 |
| mbcap | 21 | | |
| dnw | 22 | | |
| nwdmy | 23 | | |
| rpdmy | 24 | | |
| diode | 25 | | |
| nat | 26 | | |
| diff25 | 27 | | |
| rmarker | 28 | | |
| hrimp | 29 | | |
| inddmy | 30 | | |

¹ The layer numbers here are same as the mask number. These names/numbers are used in the “techLayers” and “layerRules” section of the Copernicus technology files.

0.2 Layer purposes

| Data type name | Data type/ purpose no. | Data type name | Data type/ purpose no. |
|----------------|------------------------|----------------|------------------------|
| dmy0 | 0 | waterMark | 63 |
| dmy1 | 1 | dummy | 127 |
| dmy2 | 2 | | |
| dmy3 | 3 | | |
| dmy4 | 4 | | |

0.3 Grid and DBU

| Rule | Description | | Design Value (μm) |
|---------------------------------------|---|---|-------------------|
| 0.21 | Manufacturing grid resolution | = | 0.005 |
| View type units for Copernicus editor | | | |
| 0.22 | Database unit per user unit for maskLayout (in microns) | = | 1000 |
| 0.23 | Database unit per user unit for schematic (in microns) | = | 160 |
| 0.24 | Database unit per user unit for schematic Symbol (in microns) | = | 160 |
| 0.25 | The maskGrid, cadGrid and drcGrid | = | 0.005 |

1 Mosfet Design Rules

1.1 Reference Rules

| Rule | Description | | Design Value (μm) |
|--------|---|---|-------------------|
| 1.1 | Polysilicon spacing to Contact (for N NM Model Device) | ≥ | 0.08 |
| 1.2 | Polysilicon spacing to Contact (for NA Model Device) | ≥ | 0.08 |
| 1.3 | Polysilicon spacing to Contact (for N25 NM25 Model Device) | ≥ | 0.15 |
| 1.4 | Polysilicon spacing to Contact (for NA25 Model Device) | ≥ | 0.15 |
| 1.5 | Polysilicon spacing to Contact (for P25 PM25 Model Device) | ≥ | 0.15 |
| 1.6 | Polysilicon spacing to Contact (for P PM Model Device) | ≥ | 0.08 |
| 1.7 | Gate (Polysilicon over Diffusion) minimum spacing to Gate | ≥ | 0.15 |
| 1.8 | Enclosure of Gate within Implant | ≥ | 0.13 |
| 1.9 | Enclosure of Diffusion within Native Oxide | ≥ | 0.28 |
| 1.10 | Enclosure of Diffusion within 25Volt (DIFF25) | ≥ | 0.30 |
| 1.11 | Active Diffusion (touching Polysilicon) spacing to Active Diffusion | ≥ | 0.13 |
| 1.12 | Polysilicon to diffusion spacing (N NL NH) | ≥ | 0.10 |
| 1.13 | Polysilicon to diffusion spacing (for NA Model Device) | ≥ | 0.15 |
| 1.14 | Polysilicon to diffusion spacing (N25 N18 N33) | ≥ | 0.15 |
| 1.15 | Polysilicon to diffusion spacing (for NM25 NA25 Model Device) | ≥ | 0.15 |
| 1.16 | Polysilicon to diffusion spacing (P25 P18 P33) | ≥ | 0.15 |
| 1.17 | Polysilicon to diffusion spacing (P PL) | ≥ | 0.10 |
| 1.17.1 | Polysilicon to diffusion spacing (PH NM) | ≥ | 0.11 |
| 1.18 | Spacing between native oxide and diffusion layer | ≥ | 0.20 |
| 1.19 | Enclosure of gate with 25Volt(DIFF25) | ≥ | 0.35 |
| 1.20 | Extension of poly beyond diffusion layer (end cap) of standard MOS | ≥ | 0.13 |

| | | | |
|------|--|---|------|
| 1.21 | Extension of poly beyond diffusion layer (end cap) of native MOS | ≥ | 0.22 |
| 1.22 | Extension of poly beyond diffusion layer (end cap) of HV MOS | ≥ | 0.22 |
| 1.23 | Poly to Pdiff Spacing | ≥ | 0.12 |
| 1.24 | Poly to Ndiff Spacing | ≥ | 0.12 |
| 1.25 | Pplus to Ndiff Spacing | ≥ | 0.02 |
| 1.26 | Nplus to Pdiff Spacing | ≥ | 0.02 |
| 1.27 | Maximum finger width | ≤ | 10 |
| 1.28 | Maximum folds | ≤ | 100 |
| 1.29 | Maximum multiples | ≤ | 100 |
| 1.30 | Minimum poly to contact spacing in source | = | 0.08 |
| 1.31 | Minimum poly to contact spacing in drain | = | 0.08 |
| 1.32 | Maximum poly to contact spacing in source | ≤ | 10 |
| 1.33 | Maximum poly to contact spacing in drain | ≤ | 10 |
| 1.34 | Maximum tap spacing | ≤ | 10 |
| 1.35 | Minimum area of a poly hole formed in MOSFET | ≥ | 0.2 |
| 1.41 | Gate to contact spacing for Non-Dogbone Structure (N P) | ≥ | 0.12 |
| 1.83 | Gate to Gate spacing(N , NL , NH) | ≥ | 0.15 |
| 1.84 | Gate to Gate spacing(NA) | ≥ | 0.15 |
| 1.85 | Gate to Gate spacing(NA25 NA18 NA33) | ≥ | 0.35 |
| 1.86 | Gate to Gate spacing(N25 N18 N33 NM25) | ≥ | 0.35 |
| 1.87 | Gate to Gate spacing(P PL PH PM) | ≥ | 0.15 |
| 1.88 | Gate to Gate spacing(P25 P18 P33) | ≥ | 0.35 |

1.2 DNW MOSFET Design Rules

| Rule | Description | | Design Value (μm) |
|-------|---|---|-------------------|
| 1.89 | Minimum Width of Gate (NDN) | ≥ | 0.12 |
| 1.90 | Maximum Width of Gate (NDN) | ≤ | 900 |
| 1.91 | Minimum Width of Gate (NDN25) | ≥ | 0.5 |
| 1.92 | Maximum Width of Gate (NDN25) | ≤ | 900 |
| 1.93 | Minimum Length of Gate (NDN) | ≥ | 0.1 |
| 1.94 | Maximum Length of Gate (NDN) | ≤ | 900 |
| 1.95 | Minimum Length of Gate (NDN25) | ≥ | 0.28 |
| 1.96 | Maximum Length of Gate (NDN25) | ≤ | 900 |
| 1.97 | Gate to contact spacing for Non-Dogbone Structure(NDN) | ≥ | 0.08 |
| 1.98 | Ggate to contact spacing for Non-Dogbone Structure(NDN25) | ≥ | 0.15 |
| 1.105 | Gate to Gate spacing(NDN) | ≥ | 0.15 |
| 1.112 | Gate to Gate spacing(NDN25) | ≥ | 0.35 |
| 1.113 | Polysilicon spacing to Contact (for NDN Model Device) | ≥ | 0.11 |
| 1.114 | Polysilicon spacing to Contact (for NDN25 Model Device) | ≥ | 0.15 |
| 1.115 | Polysilicon to diffusion spacing (for NDN Model Device) | ≥ | 0.10 |
| 1.116 | Polysilicon to diffusion spacing (for NDN25 Model Device) | ≥ | 0.15 |

1.3 Tap related rules

| | | | |
|-------|---|---|------|
| 1.121 | Source/Drain contact to tap diffusion spacing | ≥ | 0.06 |
| 1.122 | Tap contact to MOS diffusion spacing | ≥ | 0.06 |
| 1.123 | PPLUS enclosure of DIFF in a pwell strap | ≥ | 0.02 |
| 1.124 | NPLUS enclosure of DIFF in an Nwell strap | ≥ | 0.02 |

1.4 N18 N33 NA18 NA33 NH NL P18 P33 PL PH NM NM25 PM Design Rules

| Rule | Description | | Design Value (μm) |
|-------------|---------------------------------------|---|--------------------------|
| 1.117 | PolySilicon to Contact Spacing (N18) | ≥ | 0.15 |
| 1.118 | PolySilicon to Contact Spacing (N33) | ≥ | 0.15 |
| 1.119 | PolySilicon to Contact Spacing (NA18) | ≥ | 0.15 |
| 1.120 | PolySilicon to Contact Spacing (NA33) | ≥ | 0.15 |
| 1.121 | PolySilicon to Contact Spacing (P33) | ≥ | 0.15 |
| 1.122 | PolySilicon to Contact Spacing (P18) | ≥ | 0.15 |
| 1.123 | PolySilicon to Contact Spacing (NM) | ≥ | 0.08 |
| 1.124 | PolySilicon to Contact Spacing (NL) | ≥ | 0.11 |
| 1.125 | PolySilicon to Contact Spacing (NH) | ≥ | 0.11 |
| 1.126 | PolySilicon to Contact Spacing (NM25) | ≥ | 0.15 |
| 1.127 | PolySilicon to Contact Spacing (PM) | ≥ | 0.08 |
| 1.129 | PolySilicon to Contact Spacing (PL) | ≥ | 0.11 |
| 1.130 | PolySilicon to Contact Spacing (PH) | ≥ | 0.11 |
| 1.132 | Gate minimum width (P18) | ≥ | 0.4 |
| 1.133 | Gate maximum width (P18) | ≤ | 900 |
| 1.134 | Gate minimum width (PL) | ≥ | 0.3 |
| 1.135 | Gate maximum width (PL) | ≤ | 900 |
| 1.136 | Gate minimum width (PM) | ≥ | 0.3 |
| 1.137 | Gate maximum width (PM) | ≤ | 900 |
| 1.138 | Gate minimum width (P33) | ≥ | 0.4 |
| 1.139 | Gate maximum width (P33) | ≤ | 900 |
| 1.140 | Gate minimum width (PH) | ≥ | 0.3 |
| 1.141 | Gate maximum width (PH) | ≤ | 900 |

Synopsys Reference Design Rules

| | | | |
|-------|---------------------------|--------|------|
| 1.142 | Gate minimum length (P18) | \geq | 0.28 |
| 1.143 | Gate maximum length (P18) | \leq | 900 |
| 1.144 | Gate minimum length (PL) | \geq | 0.15 |
| 1.145 | Gate maximum length (PL) | \leq | 20 |
| 1.146 | Gate minimum length (PM) | \geq | 0.15 |
| 1.147 | Gate maximum length (PM) | \leq | 20 |
| 1.148 | Gate minimum length (P33) | \geq | 0.28 |
| 1.149 | Gate maximum length (P33) | \leq | 900 |
| 1.150 | Gate minimum length (PH) | \geq | 0.15 |
| 1.151 | Gate maximum length (PH) | \leq | 20 |
| 1.152 | Gate minimum width (NM) | \geq | 0.3 |
| 1.153 | Gate maximum width (NM) | \leq | 900 |
| 1.155 | Gate minimum width (N18) | \geq | 0.4 |
| 1.156 | Gate maximum width (N18) | \leq | 900 |
| 1.157 | Gate minimum width (NA18) | \geq | 0.5 |
| 1.158 | Gate maximum width (NA18) | \leq | 900 |
| 1.159 | Gate minimum width (NL) | \geq | 0.3 |
| 1.161 | Gate maximum width (NL) | \leq | 900 |
| 1.162 | Gate minimum width (N33) | \geq | 0.4 |
| 1.163 | Gate maximum width (N33) | \leq | 900 |
| 1.164 | Gate minimum width (NA33) | \geq | 0.5 |
| 1.165 | Gate maximum width (NA33) | \leq | 900 |
| 1.166 | Gate minimum width (NH) | \geq | 0.3 |
| 1.167 | Gate maximum width (NH) | \leq | 900 |
| 1.168 | Gate minimum width (NM25) | \geq | 0.4 |
| 1.169 | Gate maximum width (NM25) | \leq | 900 |

Synopsys Reference Design Rules

| | | | |
|-------|---|--------|------|
| 1.171 | Gate minimum length (NM) | \geq | 0.15 |
| 1.172 | Gate maximum length (NM) | \leq | 20 |
| 1.173 | Gate minimum length (NM25) | \geq | 0.28 |
| 1.174 | Gate maximum length (NM25) | \leq | 900 |
| 1.175 | Gate minimum length (N18) | \geq | 0.28 |
| 1.176 | Gate maximum length (N18) | \leq | 900 |
| 1.177 | Gate minimum length (NA18) | \geq | 1.2 |
| 1.178 | Gate maximum length (NA18) | \leq | 900 |
| 1.179 | Gate minimum length (NL) | \geq | 0.15 |
| 1.180 | Gate maximum length (NL) | \leq | 20 |
| 1.181 | Gate minimum length (N33) | \geq | 0.28 |
| 1.182 | Gate maximum length (N33) | \leq | 900 |
| 1.183 | Gate minimum length (NA33) | \geq | 1.2 |
| 1.184 | Gate maximum length (NA33) | \leq | 900 |
| 1.185 | Gate minimum length (NH) | \geq | 0.15 |
| 1.186 | Gate maximum length (NH) | \leq | 20 |
| 1.187 | Enclosure of Diffusion within 18Volt (DIFF18) | \geq | 0.30 |
| 1.188 | Enclosure of Diffusion within 33Volt (DIFF33) | \geq | 0.30 |
| 1.889 | Polysilicon to diffusion spacing (NM PM) | \geq | 0.11 |
| 1.891 | Medium Vt to N/P Diff Enclosure | \geq | 0.22 |
| 1.892 | Low Vt to N/P Gate Enclosure | \geq | 0.12 |
| 1.893 | High Vt to N/P Gate Enclosure | \geq | 0.12 |

1.5 PMOS Design Rules

| Rule | Description | | Design Value (μm) |
|------|--------------------------------------|---|-------------------|
| 1.12 | Minimum Width of gate (P) | ≥ | 0.12 |
| 1.13 | Maximum Width of gate (P) | ≤ | 900 |
| 1.14 | Minimum Width of gate (P18 P25 P33) | ≥ | 0.4 |
| 1.15 | Maximum Width of gate (P18 P25 P33) | ≤ | 900 |
| 1.16 | Minimum Length of gate (P) | ≥ | 0.1 |
| 1.17 | Maximum Length of gate (P) | ≤ | 20 |
| 1.18 | Minimum Length of gate (P18 P25 P33) | ≥ | 0.28 |
| 1.19 | Maximum Length of gate (P18 P25 P33) | ≤ | 900 |

1.6 NMOS Design Rules

| Rule | Description | | Design Value (μm) |
|------|--|---|-------------------|
| 1.20 | Minimum Width of gate (N) | ≥ | 0.12 |
| 1.21 | Maximum Width of gate (N) | ≤ | 900 |
| 1.22 | Minimum Width of gate (N18 N25 N33) | ≥ | 0.4 |
| 1.23 | Maximum Width of gate (N18 N25 N33) | ≤ | 900 |
| 1.24 | Minimum Width of gate (NA) | ≥ | 0.5 |
| 1.25 | Maximum Width of gate (NA) | ≤ | 900 |
| 1.26 | Minimum Width of gate (NA18 NA25 NA33) | ≥ | 0.5 |
| 1.27 | Maximum Width of gate (NA18 NA25 NA33) | ≤ | 900 |
| 1.28 | Minimum Length of gate (N) | ≥ | 0.1 |
| 1.29 | Maximum Length of gate (N) | ≤ | 20 |

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| | | | |
|------|---|--------|------|
| 1.30 | Minimum Length of gate (N18 N25 N33) | \geq | 0.28 |
| 1.31 | Maximum Length of gate (N18 N25 N33) | \leq | 900 |
| 1.32 | Minimum Length of gate (NA) | \geq | 0.2 |
| 1.33 | Maximum Length of gate (NA) | \leq | 20 |
| 1.34 | Minimum Length of gate (NA18 NA25 NA33) | \geq | 1.2 |
| 1.35 | Maximum Length of gate (NA18 NA25 NA33) | \leq | 900 |

2 RESISTOR Design Rules

| Rule | Description | | Design Value (μm) |
|--------|--|---|-------------------|
| 2.1 | Minimum Width (for RNPOLY device) | ≥ | 0.15 |
| 2.1.1 | Minimum Width (for RNPOLYS device) | ≥ | 0.15 |
| 2.2 | Minimum Width (for RPPOLY device) | ≥ | 0.18 |
| 2.2.1 | Minimum Width (for RPPOLYS device) | ≥ | 0.12 |
| 2.3 | Minimum Width (for RNDIFF device) | ≥ | 0.16 |
| 2.3.1 | Minimum Width (for RNDIFFS device) | ≥ | 0.14 |
| 2.4 | Minimum Width (for RPDIFF device) | ≥ | 0.18 |
| 2.4.1 | Minimum Width (for RPDIFFS device) | ≥ | 0.14 |
| 2.5 | Minimum Width (for HRNPOLY device) | ≥ | 1.2 |
| 2.6 | Minimum Width (for HRPPOLY device) | ≥ | 1.3 |
| 2.7 | Minimum Length (for RNPOLY device) | ≥ | 0.8 |
| 2.8 | Minimum Length (for RPPOLY device) | ≥ | 1.0 |
| 2.9 | Minimum Length (for RNDIFF device) | ≥ | 2.0 |
| 2.10 | Minimum Length (for RPDIFF device) | ≥ | 2.0 |
| 2.7.1 | Minimum Length (for RNPOLYS device) | ≥ | 0.8 |
| 2.8.1 | Minimum Length (for RPPOLYS device) | ≥ | 0.6 |
| 2.9.1 | Minimum Length (for RNDIFFS device) | ≥ | 0.7 |
| 2.10.1 | Minimum Length (for RPDIFFS device) | ≥ | 0.5 |
| 2.11 | Minimum Length (for HRNPOLY device) | ≥ | 1.2 |
| 2.12 | Minimum Length (for HRPPOLY device) | ≥ | 1.3 |
| 2.13 | Resistor Maximum Length for all models | ≤ | 1000 |
| 2.14 | Resistor maximum Width for all models | ≤ | 100 |

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| | | | |
|------|--|---|------|
| 2.16 | Minimum Enclosure of RPOLY within Poly | ≥ | 0.5 |
| 2.17 | Minimum Enclosure of RPOLY within Diffusion | ≥ | 0.8 |
| 2.18 | Minimum Enclosure of Resistor Diffusion within Implant | ≥ | 0.2 |
| 2.19 | Minimum NPLUS RPOLY overlap | ≥ | 0.18 |
| 2.20 | Minimum PPLUS RPOLY overlap | ≥ | 0.18 |
| 2.21 | Minimum Enclosure of POLY within hr-implant | ≥ | 0.23 |
| 2.22 | Minimum HRIMP Spacing | ≥ | 0.2 |
| 2.23 | Minimum recommended width of non metal resistors | ≥ | 2.0 |
| 2.24 | Minimum recommended width of metal resistors | ≥ | 1.0 |
| 2.25 | Minimum Width (for metal1 device) | ≥ | 0.1 |
| 2.26 | Minimum Width (for metal2 device) | ≥ | 0.15 |
| 2.27 | Minimum Width (for metal3 device) | ≥ | 0.15 |
| 2.28 | Minimum Width (for metal4 device) | ≥ | 0.15 |
| 2.29 | Minimum Length (for metal1 device) | ≥ | 0.1 |
| 2.30 | Minimum Length (for metal2 device) | ≥ | 0.15 |
| 2.31 | Minimum Length (for metal3 device) | ≥ | 0.15 |
| 2.32 | Minimum Width (for metal4 device) | ≥ | 0.15 |
| 2.33 | Number of squares (for RNPOLY device) | = | 1 |
| 2.34 | Number of squares (for RNPOLYS device) | = | 1 |
| 2.35 | Number of squares (for RPPOLY device) | = | 1 |
| 2.36 | Number of squares (for RPPOLYS device) | = | 1 |
| 2.37 | Number of squares (for RNDIFF device) | = | 1 |
| 2.38 | Number of squares (for RNDIFFS device) | = | 1 |
| 2.39 | Number of squares (for RPDIFF device) | = | 1 |
| 2.40 | Number of squares (for RPDIFFS device) | = | 1 |
| 2.41 | Number of squares (for HRNPOLY device) | = | 1 |

| | | | |
|------|---|---|-------|
| 2.42 | Number of squares (for HRPPOLY device) | = | 1 |
| 2.43 | Number of squares (for RNWELL device) | = | 5 |
| 2.44 | Number of squares (for RNWDIFF device) | = | 5 |
| 2.45 | Number of squares (for METAL1 device) | = | 1 |
| 2.46 | Number of squares (for METAL2 device) | = | 1 |
| 2.47 | Number of squares (for METAL3 device) | = | 1 |
| 2.48 | Number of squares (for METAL4 device) | = | 1 |
| 2.51 | Sheet Resistance (for RNPOLY device) | = | 402.1 |
| 2.52 | Sheet Resistance (for RNPOLYS device) | = | 20.0 |
| 2.53 | Sheet Resistance (for RPPOLY device) | = | 390.0 |
| 2.54 | Sheet Resistance (for RPPOLYS device) | = | 15.0 |
| 2.55 | Sheet Resistance (for RNDIFF device) | = | 25.0 |
| 2.56 | Sheet Resistance (for RNDIFFS device) | = | 10.5 |
| 2.57 | Sheet Resistance (for RPDIFF device) | = | 40.0 |
| 2.58 | Sheet Resistance (for RPDIFFS device) | = | 30.0 |
| 2.59 | Sheet Resistance (for HRNPOLY device) | = | 700.0 |
| 2.60 | Sheet Resistance (for HRPPOLY device) | = | 800.0 |
| 2.61 | Sheet Resistance (for RNWELL device) | = | 330.0 |
| 2.62 | Sheet Resistance (for RNWDIFF device) | = | 550.0 |
| 2.63 | Sheet Resistance (for METAL1 device) | = | 0.115 |
| 2.64 | Sheet Resistance (for METAL2 device) | = | 0.086 |
| 2.65 | Sheet Resistance (for METAL3 device) | = | 0.086 |
| 2.66 | Sheet Resistance (for METAL4 device) | = | 0.04 |
| 2.67 | End Resistance (for RNPOLY device) | = | 2.0 |
| 2.68 | End Resistance (for RNPOLYS device) | = | 0.0 |
| 2.69 | End Resistance (for RPPOLY device) | = | 3.0 |

| | | | |
|------|--------------------------------------|---|-------|
| 2.70 | End Resistance (for RPPOLYS device) | = | 0.0 |
| 2.71 | End Resistance (for RNDIFF device) | = | 2.5 |
| 2.72 | End Resistance (for RNDIFFS device) | = | 0.0 |
| 2.73 | End Resistance (for RPDIFF device) | = | 3.5 |
| 2.74 | End Resistance (for RPDIFFS device) | = | 0.0 |
| 2.75 | End Resistance (for HRNPOLY device) | = | 6.0 |
| 2.76 | End Resistance (for HRPPOLY device) | = | 7.0 |
| 2.77 | End Resistance (for RNWELL device) | = | 0.0 |
| 2.78 | End Resistance (for RNWDIFF device) | = | 0.0 |
| 2.79 | End Resistance (for METAL1 device) | = | 0.0 |
| 2.80 | End Resistance (for METAL2 device) | = | 0.0 |
| 2.81 | End Resistance (for METAL3 device) | = | 0.0 |
| 2.82 | End Resistance (for METAL4 device) | = | 0.0 |
| 2.83 | Delta Width (for RNPOLY device) | = | 0.02 |
| 2.84 | Delta Width (for RNPOLYS device) | = | -0.02 |
| 2.85 | Delta Width (for RPPOLY device) | = | 0.03 |
| 2.86 | Delta Width (for RPPOLYS device) | = | -0.03 |
| 2.87 | Delta Width (for RNDIFF device) | = | 0.05 |
| 2.88 | Delta Width (for RNDIFFS device) | = | -0.01 |
| 2.89 | Delta Width (for RPDIFF device) | = | 0.04 |
| 2.90 | Delta Width (for RPDIFFS device) | = | -0.03 |
| 2.91 | Delta Width (for HRNPOLY device) | = | 0.09 |
| 2.92 | Delta Width (for HRPPOLY device) | = | 0.09 |
| 2.93 | Delta Width (for RNWELL device) | = | 0.2 |
| 2.94 | Delta Width (for RNWDIFF device) | = | 0.3 |
| 2.95 | Delta Width (for METAL1 device) | = | 0.023 |

| | | | |
|-------|--|---|-------|
| 2.96 | Delta Width (for METAL2 device) | = | 0.006 |
| 2.97 | Delta Width (for METAL3 device) | = | 0.015 |
| 2.98 | Delta Width (for METAL4 device) | = | 0.009 |
| 2.99 | Delta Length (for RNPOLY device) | = | 0.04 |
| 2.100 | Delta Length (for RNPOLYS device) | = | 0.0 |
| 2.101 | Delta Length (for RPPOLY device) | = | 0.04 |
| 2.102 | Delta Length (for RPPOLYS device) | = | 0.0 |
| 2.103 | Delta Length (for RNDIFF device) | = | 0.01 |
| 2.104 | Delta Length (for RNDIFFS device) | = | 0.0 |
| 2.105 | Delta Length (for RPDIFF device) | = | 0.01 |
| 2.106 | Delta Length (for RPDIFFS device) | = | 0.0 |
| 2.107 | Delta Length (for HRNPOLY device) | = | 0.06 |
| 2.108 | Delta Length (for HRPPOLY device) | = | 0.066 |
| 2.109 | Delta Length (for RNWELL device) | = | 0.0 |
| 2.110 | Delta Length (for RNWDIFF device) | = | 0.0 |
| 2.111 | Delta Length (for METAL1 device) | = | 0.0 |
| 2.112 | Delta Length (for METAL2 device) | = | 0.0 |
| 2.113 | Delta Length (for METAL3 device) | = | 0.0 |
| 2.114 | Delta Length (for METAL4 device) | = | 0.0 |
| 2.116 | Lower limit for resistor spacing | ≥ | 0.01 |
| 2.117 | Higher limit for resistor spacing | ≤ | 9.0 |
| 2.118 | Distance from the RPOLY region to related N-well region | ≥ | 0.18 |
| 2.119 | Minimum extension of the diffusion region beyond N-well region | ≥ | 0.6 |
| 2.120 | Enclosure of n-plus region by N-well region | ≥ | 0.18 |
| 2.122 | Minimum distance from the RPOLY region to contact which is inside SAB hole | ≥ | 0.40 |
| 2.123 | Minimum overlap of RPOLY region over N-well region | ≥ | 0.50 |

| | | | |
|-------|---|---|------|
| 2.125 | Enclosure by n-well layer with the P type diffusion for N-well type resistors | ≥ | 0.23 |
| 2.126 | Nplus Enclosure of POLY | ≥ | 0.25 |
| 2.127 | Pplus Enclosure of POLY | ≥ | 0.25 |
| 2.128 | Minimum enclosure of RMARKER layer with POLY | ≥ | 0.22 |

2.1 Serpentine resistor rules

| Rule | Description | | Design Value (μm) |
|-------|---|---|-------------------|
| 2.301 | Minimum Width (for RPOLY RPOLYH RPOLYRF RPOLYHRF RPOLYC RPOLYHC device) | ≥ | 0.09 |
| 2.302 | Minimum Length (for RPOLY RPOLYH RPOLYRF RPOLYHRF RPOLYC RPOLYHC device) | ≥ | 4.0 |
| 2.303 | Maximum Width (for RPOLY RPOLYH RPOLYRF RPOLYHRF RPOLYC RPOLYHC device) | ≥ | 100 |
| 2.304 | Maximum Length (for RPOLY RPOLYH RPOLYRF RPOLYHRF RPOLYC RPOLYHC device) | ≥ | 1000 |
| 2.305 | Number of squares (for RPOLYH RPOLYHC device) | = | 5 |
| 2.306 | Sheet resistance (for RPOLYH RPOLYHRF RPOLYHC devices) | = | 1200 |
| 2.307 | Sheet resistance (for RPOLY RPOLYRF RPOLYC devices) | = | 50.0 |
| 2.308 | Delta length (for RPOLY RPOLYRF RPOLYC devices) | = | 0.247 |
| 2.309 | Delta width (for RPOLYH RPOLYHRF RPOLYHC devices) | = | 0.20 |
| 2.310 | End resistance (for RPOLY device) | = | 2.0 |
| 2.311 | End resistance (for RPOLYH device) | = | 2.5 |
| 2.312 | End resistance (for RPOLYC device) | = | 3.0 |
| 2.313 | End resistance (for RPOLYHC device) | = | 3.5 |
| 2.314 | End resistance (for RPOLYRF device) | = | 6.0 |
| 2.315 | End resistance (for RPOLYHRF device) | = | 7.0 |
| 2.316 | Maximum number of turns in Serpentine resistors | ≤ | 20 |
| 2.317 | Minimum spacing (for RPOLY RPOLYRF RPOLYC devices) | ≥ | 0.5 |

Synopsys Reference Design Rules

| | | | |
|-------|--|---|------|
| 2.318 | Minimum spacing (for RPOLYH RPOLYHRF RPOLYHC devices) | ≥ | 0.75 |
| 2.319 | PPLUS Poly2 ² enclosure with contact | ≥ | 0.3 |
| 2.320 | PPLUS Poly2 spacing with contact | ≥ | 0.35 |
| 2.321 | Poly2 contact enclosure | ≥ | 0.05 |
| 2.322 | Precision Width of RPOLYH device | = | 2 |
| 2.323 | Precision Width of RPOLYHC device | = | 2 |

² Poly rules from the technology are used in place of Poly2 rules, since poly2 is absent in Reference 90nm kit

3 DIODE Design Rules

| Rule | Description | | Design Value (μm) |
|------|--|---|-------------------|
| 3.1 | Minimum Width (All N+/PWELL device) | ≥ | 1.1 |
| 3.2 | Minimum Length (All N+/PWELL device) | ≥ | 1.1 |
| 3.3 | Minimum Width (All P+/NWELL device) | ≥ | 1.1 |
| 3.4 | Minimum Length (All P+/NWELL device) | ≥ | 1.1 |
| 3.5 | Maximum Width (All N+/PWELL device) | ≤ | 100 |
| 3.6 | Maximum Length (All N+/PWELL device) | ≤ | 100 |
| 3.7 | Maximum Width (All P+/NWELL device) | ≤ | 100 |
| 3.8 | Maximum Length (All P+/NWELL device) | ≤ | 100 |
| 3.9 | Minimum Width (NWELL/PSUB Device) | ≥ | 1.1 |
| 3.10 | Maximum Width (NWELL/PSUB Device) | ≤ | 100 |
| 3.11 | Minimum Length (NWELL/PSUB Device) | ≥ | 1.1 |
| 3.12 | Maximum Length (NWELL/PSUB Device) | ≤ | 100 |
| 3.13 | Minimum Width (DNWDIODE Model Device) | ≥ | 3.0 |
| 3.14 | Minimum Length (DNWDIODE Model Device) | ≥ | 3.0 |
| 3.15 | Maximum Width (DNWDIODE Model Device) | ≤ | 100 |
| 3.16 | Maximum Length (DNWDIODE Model Device) | ≤ | 100 |
| 3.17 | Maximum width of M1 (Wide metal value) | ≤ | 15 |
| 3.18 | NWELL enclosure of N type diffusion | ≥ | 0.23 |
| 3.19 | NWELL enclosure of P type diffusion | ≥ | 0.23 |

4 CAPACITOR Design Rules

4.1 MIM Capacitor rules

| Rule | Description | | Design Value (μm) |
|------|---|---|-------------------|
| 4.1 | Minimum width of a Capacitor top plate (MTCAP) | ≥ | 1 |
| 4.2 | Maximum width of a Capacitor plate | ≤ | 100 |
| 4.3 | Enclosure of Via within the Capacitor layer | ≥ | 0.24 |
| 4.4 | Enclosure of Capacitor layer within M3 | ≥ | 0.30 |
| 4.5 | Enclosure of (Via within Capacitor layer) within M4 (top metal) | ≥ | 0.06 |
| 4.6 | Area capacitance | = | 1.0274e-15 |
| 4.7 | Fringe capacitance | = | 0.1685e-15 |
| 4.9 | Capacitor Via minimum Width | ≥ | 0.13 |
| 4.10 | Top Metal width inside CTM | ≥ | 0.33 |
| 4.11 | Top Metal spacing inside CTM or Top Metal spacing | ≥ | 0.15 |
| 4.12 | Top Metal Via Enclose | ≥ | 0.06 |
| 4.13 | Bottom metal via Enclose | ≥ | 0.2 |
| 4.14 | CTMDMY Enclosure of CBM | ≥ | 0.1 |
| 4.15 | CTM Cap Via Enclosure | ≥ | 0.24 |
| 4.16 | CTM to CTM spacing | ≥ | 0.8 |
| 4.17 | CTM Cap Via Spacing | ≥ | 0.3 |
| 4.18 | Capacitor Bottom plate Via Spacing | ≥ | 0.8 |
| 4.19 | Bottom plate CTM Enclose | ≥ | 0.4 |
| 4.20 | Slot Width for underground metal shield | ≥ | 0.21 |
| 4.21 | Slot Separation of for underground metal shield | ≥ | 0.21 |
| 4.22 | Shield Hanger width to accommodate one via | = | 0.21 |
| 4.23 | Shield via minimum Width | ≥ | 0.13 |

| | | | |
|------|--|--------|-------|
| 4.24 | Shield via minimum spacing | \geq | 0.15 |
| 4.25 | Shield metal via end of line enclosure | \geq | 0.04 |
| 4.26 | Delta length for MIM cap | = | 0 |
| 4.27 | Delta width for MIM cap | = | 0 |
| 4.28 | CMIM constant | = | 0 |
| 4.29 | Minimum length (CMIM device) | \geq | 1.0 |
| 4.30 | Maximum length (CMIM device) | \leq | 100.0 |
| 4.31 | Minimum width (CMIM device) | \geq | 1.0 |
| 4.32 | Maximum width (CMIM device) | \leq | 100.0 |

4.2 MOM Capacitor rules

| Rule | Description | | Design Value (μm) |
|------|---|--------|--------------------------------|
| 4.40 | Distance from horizontal end to first vertical finger | \geq | 1.0 |
| 4.41 | Distance from vertical end to first horizontal finger | \leq | 1.0 |
| 4.42 | Minimum number of vertical fingers | \geq | 6 |
| 4.43 | Maximum number of vertical fingers | \leq | 288 |
| 4.44 | Minimum number of horizontal fingers | \geq | 6 |
| 4.45 | Maximum number of horizontal fingers | \leq | 288 |
| 4.46 | Minimum spacing between fingers | \geq | 0.18 |
| 4.47 | Maximum spacing between fingers | \leq | 0.28 |
| 4.48 | Minimum thickness | \geq | 0.18 |
| 4.49 | Maximum thickness | \leq | 0.28 |

5 VARACTOR Design Rules

5.1 MOS varactor rules

| Rule | Description | | Design Value (μm) |
|------|---|---|-------------------|
| 5.1 | Minimum Length (for NVAR1 device) | ≥ | 0.20 |
| 5.2 | Minimum Length (for NVAR2 device) | ≥ | 0.50 |
| 5.3 | Minimum Length (for PVAR1 device) | ≥ | 0.20 |
| 5.4 | Minimum Length (for PVAR2 device) | ≥ | 0.50 |
| 5.5 | Maximum Length (for NVAR1 device) | ≤ | 50 |
| 5.6 | Maximum Length (for NVAR2 device) | ≤ | 50 |
| 5.7 | Maximum Length (for PVAR1 device) | ≤ | 50 |
| 5.8 | Maximum Length (for PVAR2 device) | ≤ | 50 |
| 5.9 | Minimum Width (for NVAR1 device) | ≥ | 0.5 |
| 5.10 | Minimum Width (for NVAR2 device) | ≥ | 1.5 |
| 5.11 | Minimum Width (for PVAR1 device) | ≥ | 0.5 |
| 5.12 | Minimum Width (for PVAR2 device) | ≥ | 1.50 |
| 5.13 | Maximum Width (for NVAR1 device) | ≤ | 50 |
| 5.14 | Maximum Width (for NVAR2 device) | ≤ | 50 |
| 5.15 | Maximum Width (for PVAR1 device) | ≤ | 50 |
| 5.16 | Maximum Width (for PVAR2 device) | ≤ | 50 |
| 5.17 | Minimum Poly Contact to Diffusion spacing | ≥ | 0.12 |
| 5.18 | Minimum Enclosure of Diffusion within VARMARKER layer | ≥ | 0.22 |
| 5.19 | Minimum Enclosure of Poly within VARMARKER layer | ≥ | 0.22 |
| 5.20 | Minimum Diffusion contact to Poly (for NVAR1 device) | ≥ | 0.08 |
| 5.21 | Minimum Diffusion contact to Poly (for NVAR2 device) | ≥ | 0.13 |
| 5.22 | Minimum Diffusion contact to Poly (for PVAR1 device) | ≥ | 0.13 |

| | | | |
|------|--|--------|----------|
| 5.23 | Minimum Diffusion contact to Poly (for PVAR2 device) | \geq | 0.13 |
| 5.24 | Area capacitance (device NVAR1) | = | 2.1e-03 |
| 5.25 | Length capacitance (device NVAR1) | = | 2.5e-10 |
| 5.26 | Width capacitance (device NVAR1) | = | 4.1e-10 |
| 5.27 | Area capacitance (device PVAR1) | = | 2.1e-03 |
| 5.28 | Length capacitance (device PVAR1) | = | 2.5e-10 |
| 5.29 | Width capacitance (device PVAR1) | = | 4.1e-10 |
| 5.30 | Area capacitance (device NVAR2) | = | 1.25e-03 |
| 5.31 | Length capacitance (device NVAR2) | = | 2.5e-10 |
| 5.32 | Width capacitance (device NVAR2) | = | 4e-10 |
| 5.33 | Area capacitance (device PVAR2) | = | 1.25e-03 |
| 5.34 | Length capacitance (device PVAR2) | = | 2.5e-10 |
| 5.35 | Width capacitance (device PVAR2) | = | 4e-10 |

5.2 Junction varactor rules

| Rule | Description | | Design Value (μm) |
|------|--------------------------------------|--------|--------------------------------|
| 5.51 | Minimum length (XJVAR model device) | \geq | 1.0 |
| 5.52 | Maximum length (XJVAR model device) | \leq | 1.0 |
| 5.53 | Minimum width (XJVAR model device) | \geq | 10.0 |
| 5.54 | Maximum width (XJVAR model device) | \leq | 50.0 |
| 5.55 | Minimum length (VARDIO model device) | \geq | 5.0 |
| 5.56 | Maximum length (VARDIO model device) | \leq | 50.0 |
| 5.57 | Minimum width (VARDIO model device) | \geq | 10.0 |
| 5.58 | Maximum width (VARDIO model device) | \leq | 50.0 |

Synopsys Reference Design Rules

| | | | |
|------|--|--------|----|
| 5.59 | Minimum number of rows (XJVAR model device) | \geq | 5 |
| 5.60 | Maximum number of rows (XJVAR model device) | \leq | 20 |
| 5.61 | Minimum number of rows (XJVAR model device) | \geq | 1 |
| 5.62 | Maximum number of rows (XJVAR model device) | \leq | 20 |

6 INDUCTOR Design Rules

| Rule | Description | | Design Value (μm) |
|------|--|---|-------------------|
| 6.1 | Minimum Radius (for SYNSTD Model) | ≥ | 40 |
| 6.2 | Maximum Radius (for SYNSTD Model) | ≤ | 120 |
| 6.3 | Minimum number of Turns (for SYNSTD Model) | ≥ | 0.5 |
| 6.4 | Maximum number of Turns (for SYNSTD Model) | ≤ | 7.5 |
| 6.5 | Minimum Radius (for INDSYM Model) | ≥ | 45 |
| 6.6 | Maximum Radius (for INDSYM Model) | ≤ | 140 |
| 6.7 | Minimum number of Turns (for INDSYM Model) | ≥ | 1 |
| 6.8 | Maximum number of Turns (for INDSYM Model) | ≤ | 8 |
| 6.9 | Minimum Radius (for INDSYMCT Model) | ≥ | 45 |
| 6.10 | Maximum Radius (for INDSYMCT Model) | ≤ | 150 |
| 6.11 | Minimum number of Turns (for INDSYMCT Model) | ≥ | 1 |
| 6.12 | Maximum number of Turns (for INDSYMCT Model) | ≤ | 7 |
| 6.13 | Fixed Width1 of inductor metal (SYNSTD) ³ | = | "5u" |
| 6.14 | Fixed Width2 of inductor metal (SYNSTD) | = | "9u" |
| 6.15 | Fixed Width3 of inductor metal (SYNSTD) | = | "12u" |
| 6.16 | Fixed Width4 of inductor metal (SYNSTD) | = | "20u" |
| 6.18 | Fixed Width1 of inductor metal (INDSYM) | = | "9u" |
| 6.19 | Fixed Width2 of inductor metal (INDSYM) | = | "12u" |
| 6.20 | Fixed Width3 of inductor metal (INDSYM) | = | "20u" |
| 6.21 | Fixed Width1 of inductor metal (INDSYMCT) | = | "9u" |
| 6.22 | Fixed Width2 of inductor metal (INDSYMCT) | = | "12u" |

³ These rules are found in the CDF array as cyclic options.

Synopsys Reference Design Rules

| | | | |
|------|---|---|-------|
| 6.23 | Fixed Width3 of inductor metal (INDSYMCT) | = | “20u” |
| 6.50 | Minimum space of thick metal under INDDMY | ≥ | 1.5 |
| 6.51 | Maximum space of thick metal under INDDMY | ≤ | 3.0 |
| 6.52 | Enclosure of Inductor device (Metal) within INDDMY | ≥ | 45 |
| 6.53 | Enclosure of Via within last Metal | ≥ | 0.30 |
| 6.54 | Enclosure of Via within last Metal (End of line) | ≥ | 0.45 |
| 6.55 | metal island region width for inductor | ≥ | 18 |
| 6.56 | island width of inductor | ≥ | 3 |
| 6.57 | island to island spacing in metal island area | ≥ | 3 |
| 6.58 | enclosure of inductor dummy layer with substrate pickup | ≥ | 2.5 |
| 6.59 | Split metal1 width in inductor | = | 3.0 |
| 6.60 | enclosure of SAB with diffusion layer in inductor | ≥ | 0.5 |
| 6.61 | spacing between island layer and filler poly layer | ≥ | 0.5 |
| 6.62 | width of poly used for filling metal island area | = | 2.0 |

**Note:

All the above design rules (6.x) are applicable within the INDDMY layer only.

All the above design rules (5.x) are applicable within the VARMARKER layer only.

7 Mask Layers Design Rules

| Rule | Description | | Design Value (μm) |
|------|--------------------------------|---|-------------------|
| 7.1 | Minimum Width for NWELL | ≥ | 0.55 |
| 7.2 | Minimum Spacing for NWELL | ≥ | 0.55 |
| 7.3 | Minimum area of NWELL | ≥ | 1.2 |
| 7.4 | Minimum Enclosed area of NWELL | ≥ | 1.2 |
| 7.5 | Minimum Width for DIFF | ≥ | 0.09 |
| 7.6 | Minimum Spacing for DIFF | ≥ | 0.09 |
| 7.7 | Minimum area of DIFF | ≥ | 0.05 |
| 7.8 | Minimum Enclosed area of DIFF | ≥ | 0.065 |
| 7.9 | Minimum Width for POLY | ≥ | 0.09 |
| 7.10 | Minimum Spacing for POLY | ≥ | 0.09 |
| 7.11 | Minimum area of POLY | ≥ | 0.05 |
| 7.12 | Minimum Enclosed area of POLY | ≥ | 0.09 |
| 7.13 | Minimum Width for PPLUS | ≥ | 0.2 |
| 7.14 | Minimum Spacing for PPLUS | ≥ | 0.1 |
| 7.15 | Minimum area of PPLUS | ≥ | 0.08 |
| 7.16 | Minimum Enclosed area of PPLUS | ≥ | 0.11 |
| 7.17 | Minimum Width for NPLUS | ≥ | 0.2 |
| 7.18 | Minimum Spacing for NPLUS | ≥ | 0.1 |
| 7.19 | Minimum area of NPLUS | ≥ | 0.08 |
| 7.20 | Minimum Enclosed area of NPLUS | ≥ | 0.11 |

| Rule | Description | | Design Value (μm) |
|------|--------------------------------|---|-------------------|
| 7.21 | Minimum width for RPOLY | ≥ | 0.34 |
| 7.22 | Minimum Spacing for RPOLY | ≥ | 0.34 |
| 7.23 | Minimum Area of RPOLY | ≥ | 0.85 |
| 7.24 | Minimum Enclosed Area of RPOLY | ≥ | 0.85 |
| 7.25 | Minimum Width for Contact (CO) | ≥ | 0.09 |
| 7.26 | Minimum Spacing for CO | ≥ | 0.1 |
| 7.27 | Minimum width for M1 | ≥ | 0.1 |
| 7.28 | Maximum Width for M1 | ≤ | 1000 |
| 7.29 | Minimum Spacing for M1 | ≥ | 0.1 |
| 7.30 | Minimum area of M1 | ≥ | 0.04 |
| 7.31 | Minimum enclosed area of M1 | ≥ | 0.3 |
| 7.32 | Minimum width for M2 | ≥ | 0.15 |
| 7.33 | Maximum Width for M2 | ≤ | 1000 |
| 7.34 | Minimum Spacing for M2 | ≥ | 0.15 |
| 7.35 | Minimum area of M2 | ≥ | 0.06 |
| 7.36 | Minimum enclosed area of M2 | ≥ | 0.3 |
| 7.37 | Minimum width for M3 | ≥ | 0.15 |
| 7.38 | Maximum Width for M3 | ≤ | 1000 |
| 7.39 | Minimum Spacing for M3 | ≥ | 0.15 |
| 7.40 | Minimum area of M3 | ≥ | 0.06 |
| 7.41 | Minimum enclosed area of M3 | ≥ | 0.3 |
| 7.42 | Minimum width for M4 | ≥ | 0.15 |
| 7.43 | Maximum Width for M4 | ≤ | 1000 |

Synopsys Reference Design Rules

| | | | |
|-------|--|---|-------|
| 7.44 | Minimum Spacing for M4 | ≥ | 0.15 |
| 7.45 | Minimum area of M4 | ≥ | 0.06 |
| 7.46 | Minimum enclosed area of M4 | ≥ | 0.3 |
| 7.47 | Minimum width for VIA1 | ≥ | 0.13 |
| 7.48 | Minimum spacing for VIA1 | ≥ | 0.15 |
| 7.49 | Minimum width for VIA2 | ≥ | 0.13 |
| 7.50 | Minimum spacing for VIA2 | ≥ | 0.15 |
| 7.51 | Minimum width for VIA3 | ≥ | 0.13 |
| 7.52 | Minimum spacing for VIA3 | ≥ | 0.15 |
| 7.53 | Minimum Enclosure of Contact within POLY | ≥ | 0.05 |
| 7.54 | Minimum Enclosure of Contact within M1 | ≥ | 0.005 |
| 7.55 | Minimum Spacing from NWELL to DIFF | ≥ | 0.22 |
| 7.56 | Minimum Enclosure of DIFF within NWELL | ≥ | 0.23 |
| 7.57 | Minimum Enclosure of POLY within RPOLY | ≥ | 0.22 |
| 7.58 | Minimum Spacing from contact to RPOLY | ≥ | 0.22 |
| 7.59 | Minimum Enclosure of NWELL within NWRES | ≥ | 0.2 |
| 7.60 | Minimum Enclosure of PPLUS within NWELL | ≥ | 0.0 |
| 7.61 | Minimum Spacing from POLY to DIFF | ≥ | 0.045 |
| 7.62 | Minimum Enclosure of DIFF within POLY (N P) | ≥ | 0.13 |
| 7.621 | Minimum Enclosure of DIFF within POLY (NM NL NH PM PL PH) | ≥ | 0.16 |
| 7.622 | Minimum Enclosure of DIFF within POLY (N25 NA NA25 N18 NA18 N33 NA33 NM25 P18 P25 P33) | ≥ | 0.22 |
| 7.63 | Minimum Spacing from DIFF to CO | ≥ | 0.1 |
| 7.64 | Minimum Enclosure of CO within DIFF | ≥ | 0.05 |
| 7.65 | Minimum Spacing from POLY to CO | ≥ | 0.08 |
| 7.66 | Minimum Enclosure of CO within POLY | ≥ | 0.05 |
| 7.67 | Minimum Enclosure of CO within PPLUS | ≥ | 0.06 |

Synopsys Reference Design Rules

| | | | |
|------|--|---|-------|
| 7.68 | Minimum Enclosure of CO within NPLUS | ≥ | 0.06 |
| 7.69 | PPLUS should not overlap NPLUS (can abut) | - | - |
| 7.70 | Minimum Enclosure of Contact within M1 | ≥ | 0.005 |
| 7.71 | Minimum End of Line Enclosure of Contact within M1 | ≥ | 0.04 |
| 7.72 | Minimum Enclosure of VIA1 within M1 | ≥ | 0.01 |
| 7.73 | Minimum End of Line Enclosure of VIA1 within M1 | ≥ | 0.04 |
| 7.74 | Minimum Enclosure of VIA1 within M2 | ≥ | 0.01 |
| 7.75 | Minimum End of Line Enclosure of VIA1 within M2 | ≥ | 0.04 |
| 7.76 | Minimum Enclosure of VIA2 within M2 | ≥ | 0.01 |
| 7.77 | Minimum End of Line Enclosure of VIA2 within M2 | ≥ | 0.04 |
| 7.78 | Minimum Enclosure of VIA2 within M3 | ≥ | 0.01 |
| 7.79 | Minimum End of Line Enclosure of VIA2 within M3 | ≥ | 0.04 |
| 7.80 | Minimum Enclosure of VIA3 within M3 | ≥ | 0.01 |
| 7.81 | Minimum End of Line Enclosure of VIA3 within M3 | ≥ | 0.04 |
| 7.82 | Minimum Enclosure of VIA3 within M4 | ≥ | 0.01 |
| 7.83 | Minimum End of Line Enclosure of VIA3 within M4 | ≥ | 0.04 |
| 7.84 | Minimum Spacing from RPOLY to POLY | ≥ | 0.22 |
| 7.85 | Minimum Enclosure of POLY within RPOLY | ≥ | 0.22 |
| 7.86 | Minimum Spacing of CO to RPOLY | ≥ | 0.22 |
| 7.87 | Minimum Spacing of RPOLY to Diffusion | ≥ | 0.22 |
| 7.88 | Minimum Enclosure of Diffusion within RPOLY | ≥ | 0.22 |
| 7.89 | Minimum Spacing of PPLUS to DIFF | ≥ | 0.13 |
| 7.90 | Minimum Enclosure of DIFF within PPLUS | ≥ | 0.13 |

Synopsys Reference Design Rules

| | | | |
|------|---|---|------|
| 7.91 | Minimum Spacing of NPLUS to DIFF | ≥ | 0.13 |
| 7.92 | Minimum Enclosure of DIFF within NPLUS | ≥ | 0.13 |
| 7.94 | NPLUS space to PW strap | ≥ | 0.02 |
| 7.95 | CO space to DIFF | ≥ | 0.06 |
| 7.96 | Spacing between vias when there is an array of vias | ≥ | 0.17 |
| 7.97 | Spacing between contacts when there is an array of contacts | ≥ | 0.15 |
| 7.98 | Minimum end of line enclosure of POLY with CO | ≥ | 0.07 |
| 7.99 | Minimum end of line enclosure of DIFF with CO | ≥ | 0.07 |

8 Triple-Well (DNWELL) Design Rules

| Rule | Description | | Design Value (μm) |
|------|---|---|-------------------|
| 8.1 | Minimum width of DNWELL | ≥ | 2.80 |
| 8.2 | All DNWELL edges must be enclosed by NWELL | - | - |
| 8.3 | DNWELL spacing to DNWELL | ≥ | 4.40 |
| 8.4 | DNWELL overlap of NWELL (measured at the Inner edge of NWELL) | ≥ | 0.80 |
| 8.5 | Extension of NWELL over DNWELL (outer edge of NWELL) | ≥ | 1.40 |
| 8.6 | Extension of DNWELL over (P+ diffusion inside DNWELL) | ≥ | 0.25 |
| 8.7 | [N+ diffusion inside (DNWELL not NWELL)] spacing to NWELL | ≥ | 0.20 |
| 8.8 | NWELL hole minimum width | ≥ | 1.4 |
| 8.9 | NWELL to inner implant spacing | ≥ | 0.1 |
| 8.10 | NWELL overlap of Deep N well | ≥ | 0.8 |
| 8.11 | NWELL extension over deep N-well | ≥ | 1.4 |
| 8.12 | Minimum spacing between two DNW region | ≥ | 4.4 |
| 8.13 | RPOLY enclosure with NPLUS | ≥ | 0.05 |

9 Recommended rules⁴

| | | | |
|------|--|---|------|
| 9.01 | Minimum POLY to DIFF endcap/overlap recommended | ≥ | 0.2 |
| 9.02 | Minimum DIFF to POLY Enclosure recommended | ≥ | 0.2 |
| 9.03 | Minimum M1 to CO end of line enclosure recommended | ≥ | 0.06 |
| 9.04 | Minimum POLY to CO end of line enclosure recommended | ≥ | 0.07 |
| 9.05 | Minimum POLY to DIFF spacing recommended | ≥ | 0.14 |
| 9.06 | Minimum DIFF to CO enclosure recommended | ≥ | 0.10 |
| 2.23 | Minimum recommended width of non metal resistors | ≥ | 2.0 |
| 2.24 | Minimum recommended width of metal resistors | ≥ | 1.0 |

⁴ These rules are applicable to all the devices in the Reference kit like MOSFET, Resistor, Diode, Capacitor etc. These are also called as DFM rules.