VLSI Design

EECS 217

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06/11/2024

1. Schematic simulation

a. Project design requirements

Final Project
EECS217
Instructor: Dr. Kavianpour

Design 256 bits SRAM with the following characteristics:

1-The memory cell is based on the 6-transistor CMOS SR flip flop.
2- The memory cells are organized as 16 by two bytes rectangular array.
3- Row decoder addresses the 16 worldlines, while column decoder addresses each of the 2 bytes columns. Each row wordline is 16 bits (thus 2 bytes), and each column is 1 byte wide.
4- Use NAND design for these decoders.
5-Input/ouput signals swing between Gnd and Vdd and assume to be ideal steps.
6- Delays should be measured from the 50% point of the input waveform of the input, to the 50% of the outputs of either of the two decoders (whichever is slower).
7-The memory cell should be sized in such a way that the overall memory achieves the goals: performance, power, and area. Your cell design should first be based on proper operation in both *read* and *write* mode.
8- You do not need to include the sense amplifier or the tri-state driver in your design
9- Assume row word line load is 100fF and the column bit line load is 20pF. 10- Take only the capacitance of the bit- and wordlines into account. IGNORE the resistance. This will give you optimistic results but simplifies the analysis. You should, however, keep the resistance of the bit- and wordlines into account when you layout your cell. Long wires in polysilicon are not the right way to go. Poly-metal contacts also introduce resistance.

Fig. 1 Design requirements

b. Circuit Design

- **Memory Cell Circuit**

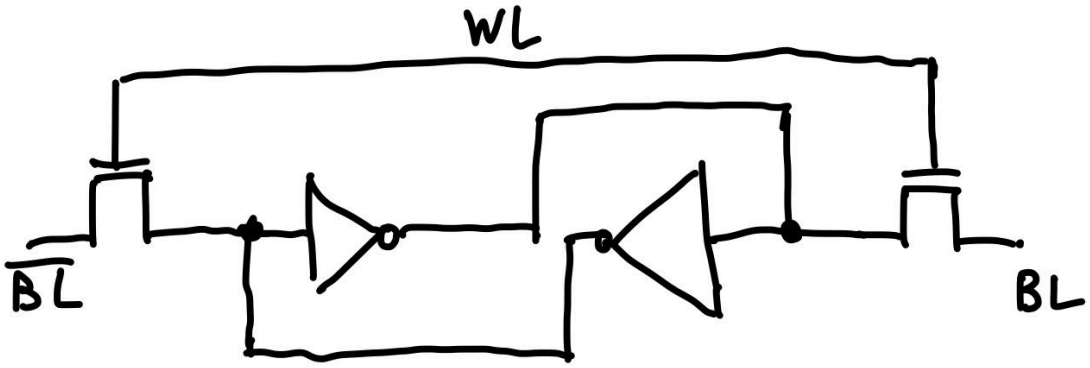

Fig. 2 Gate level design of Memory Cell

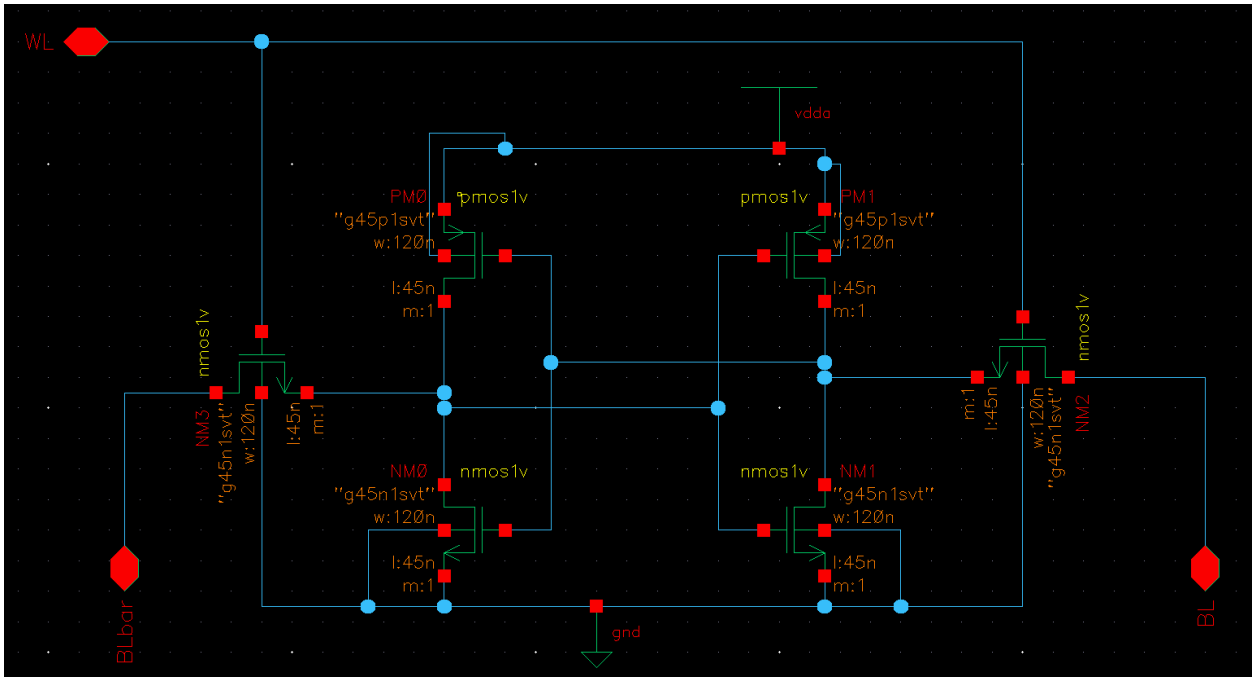

Fig. 3 Memory Cell Circuit

The circuit is shown in **Fig. 3** ,is a single memory cell circuit, whole SRAM include 16*16=256 memory cell

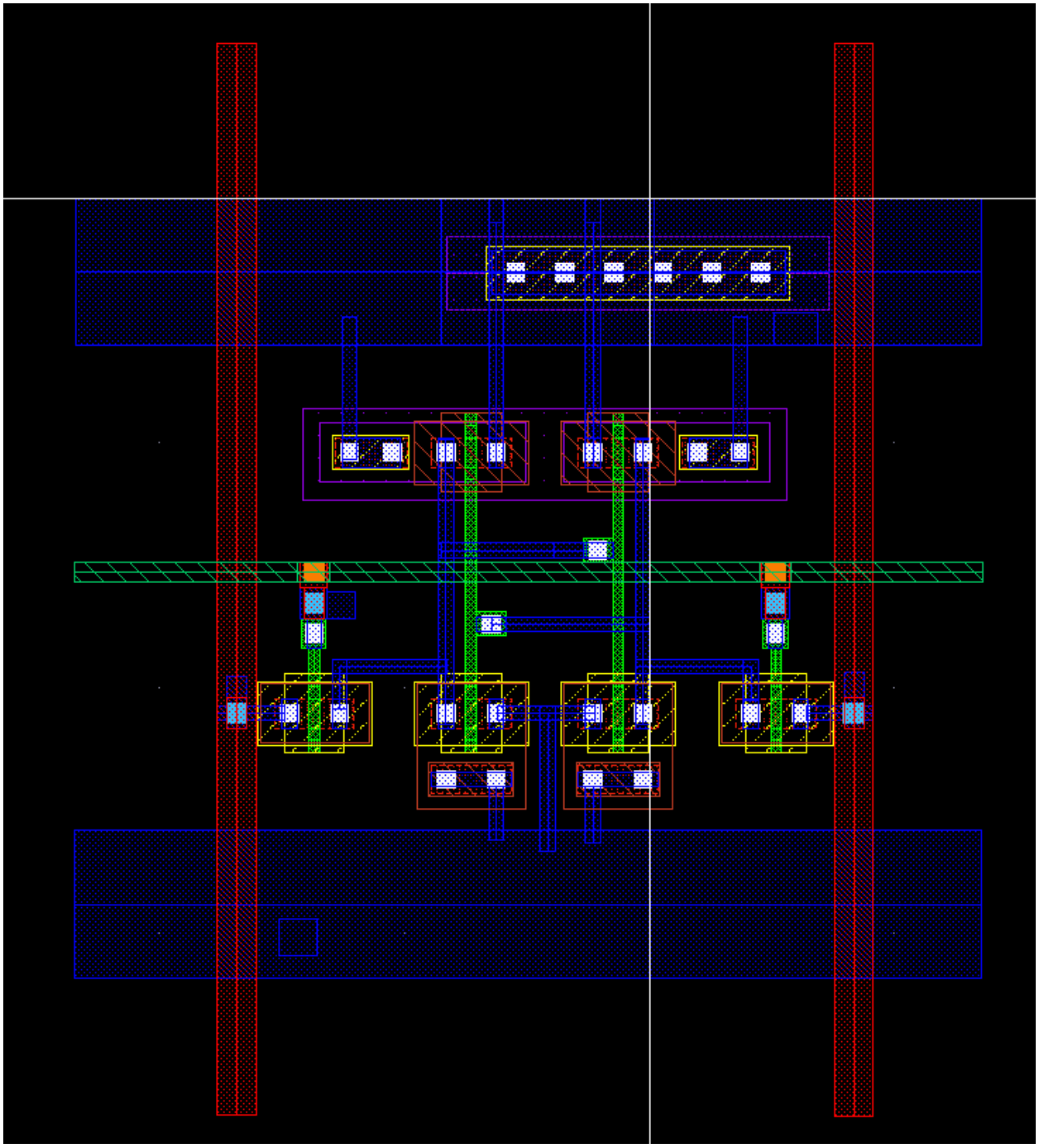

Fig. 4 Memory Cell Circuit Layout

The **Fig. 4** shown the layout of one memory cell.

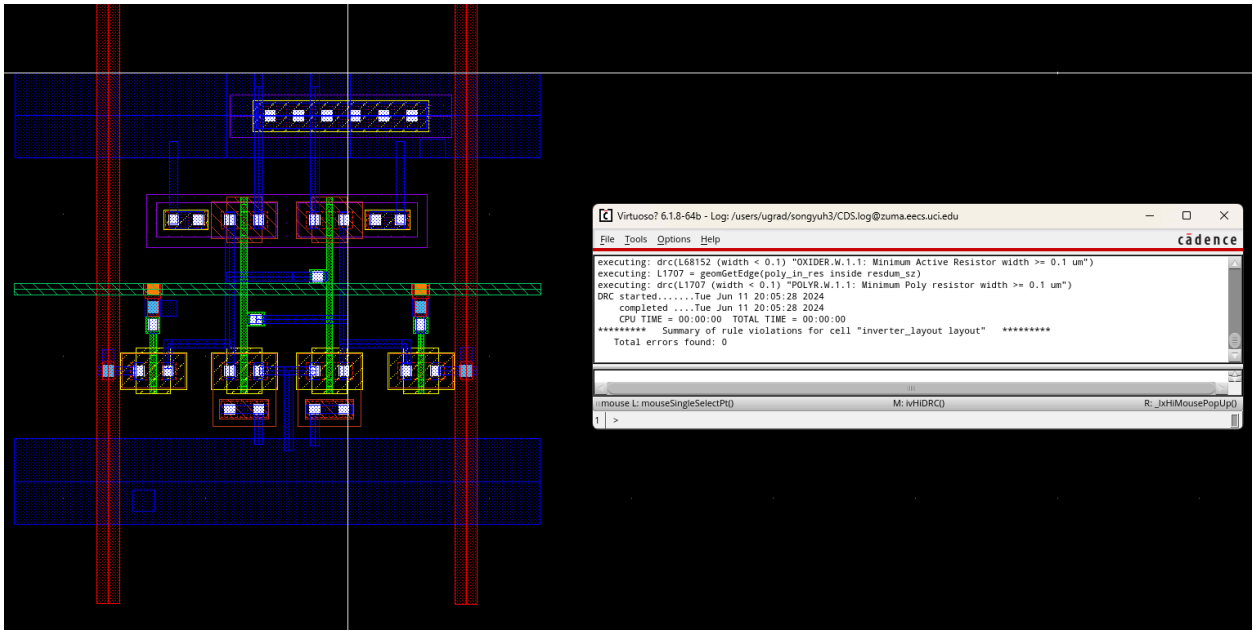

Fig. 5 Memory Cell Circuit Layout DRC Check

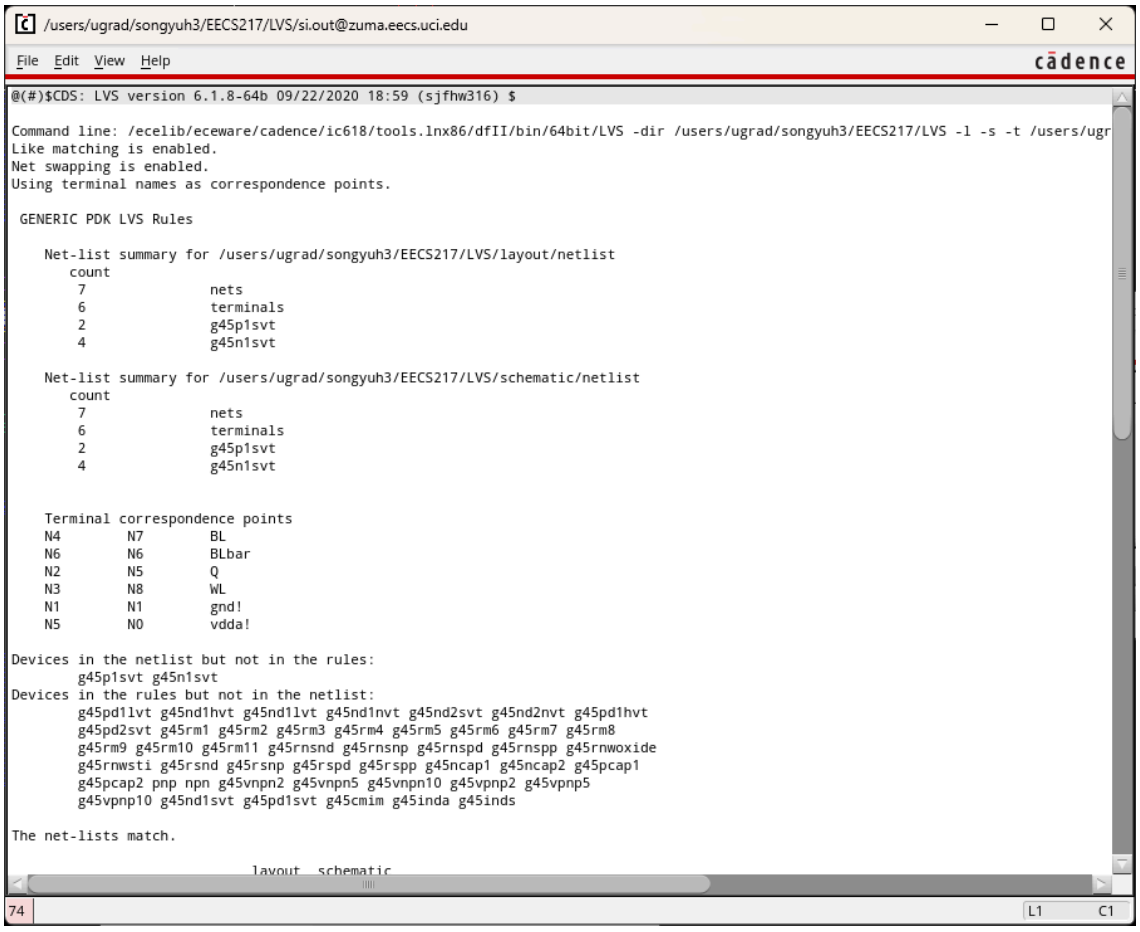

Fig. 6 Memory Cell Circuit Layout LVS Check

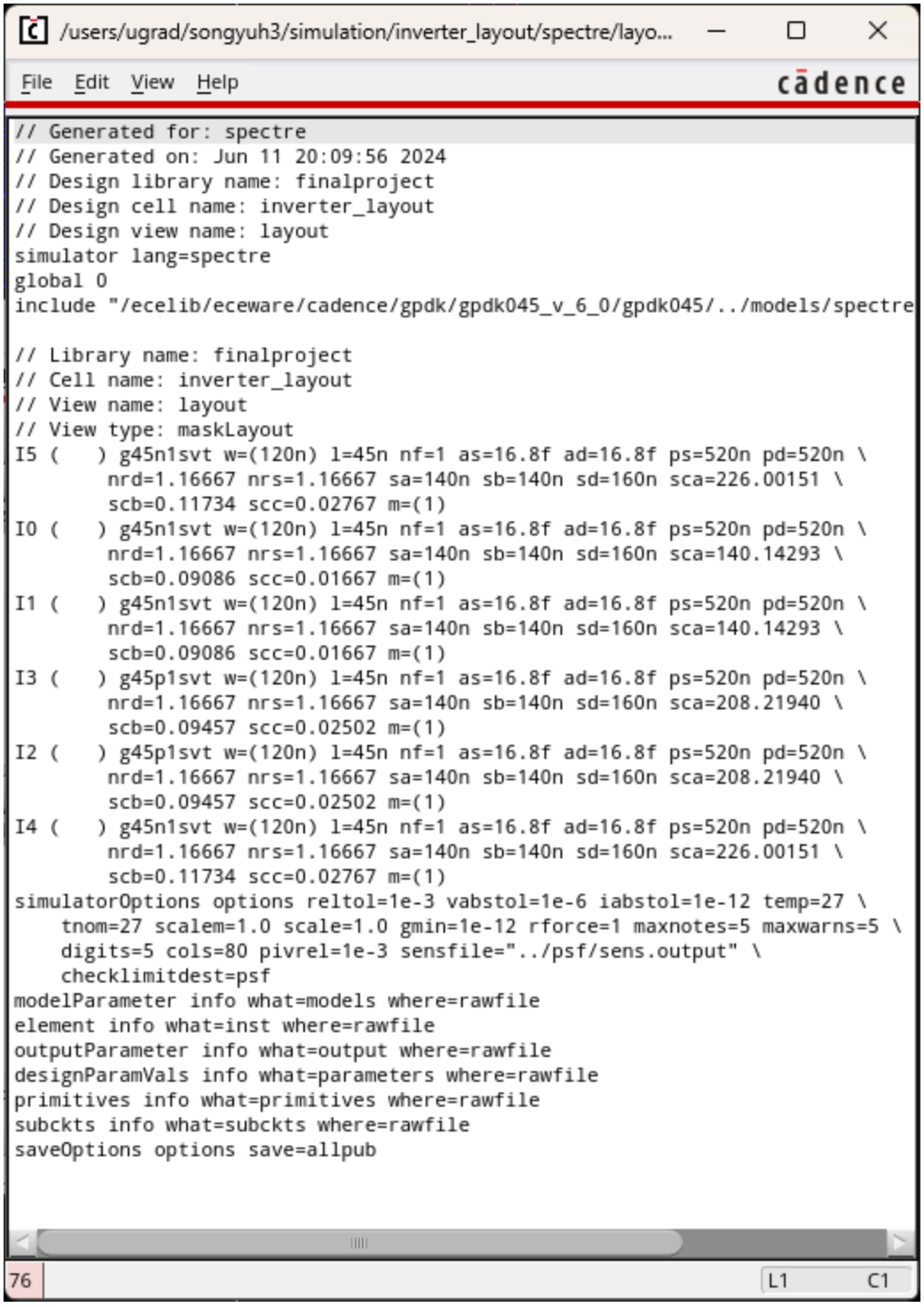

Fig. 7 Memory Cell Circuit Layout Netlist

- **Column Decoder Circuit**

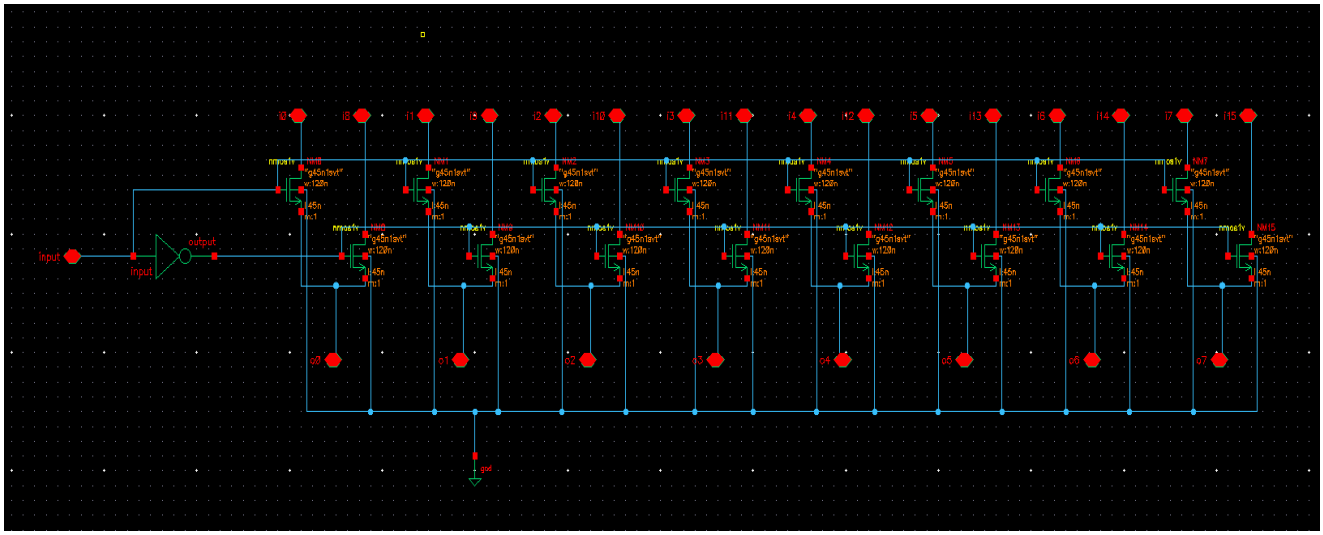

Fig. 8 Column Decoder Circuit

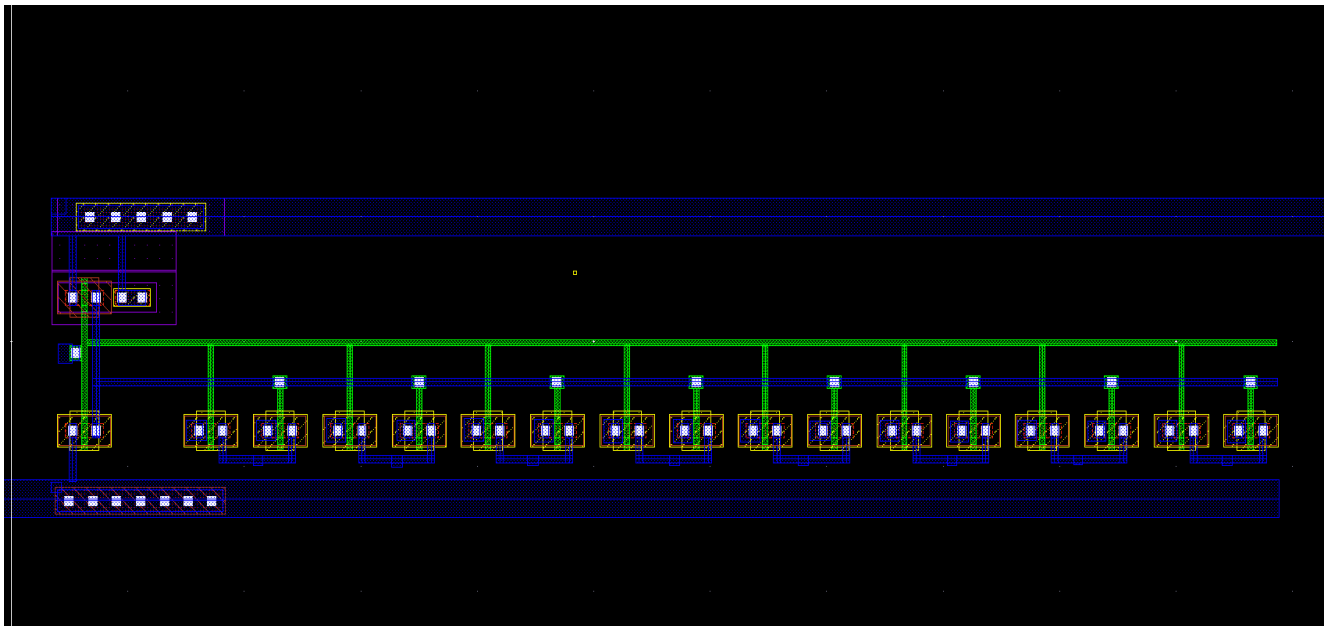

Fig. 9 Column Decoder Circuit Layout

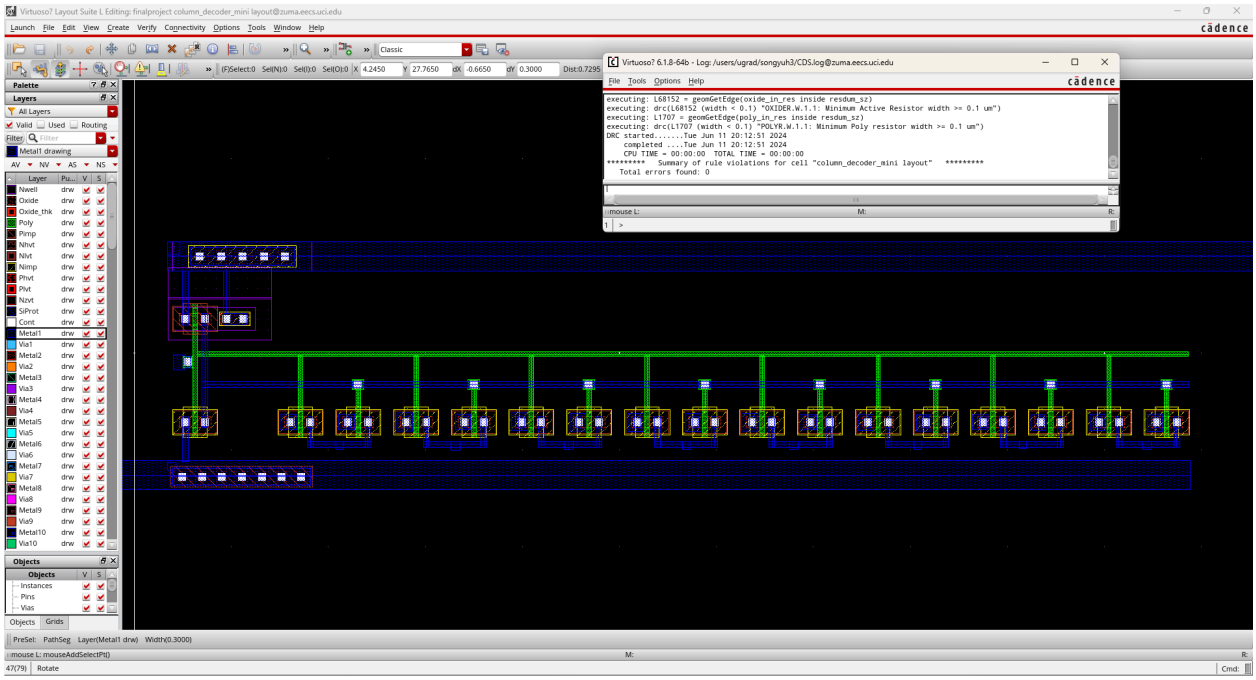

Fig. 10 Column Decoder Circuit Layout DRC Check

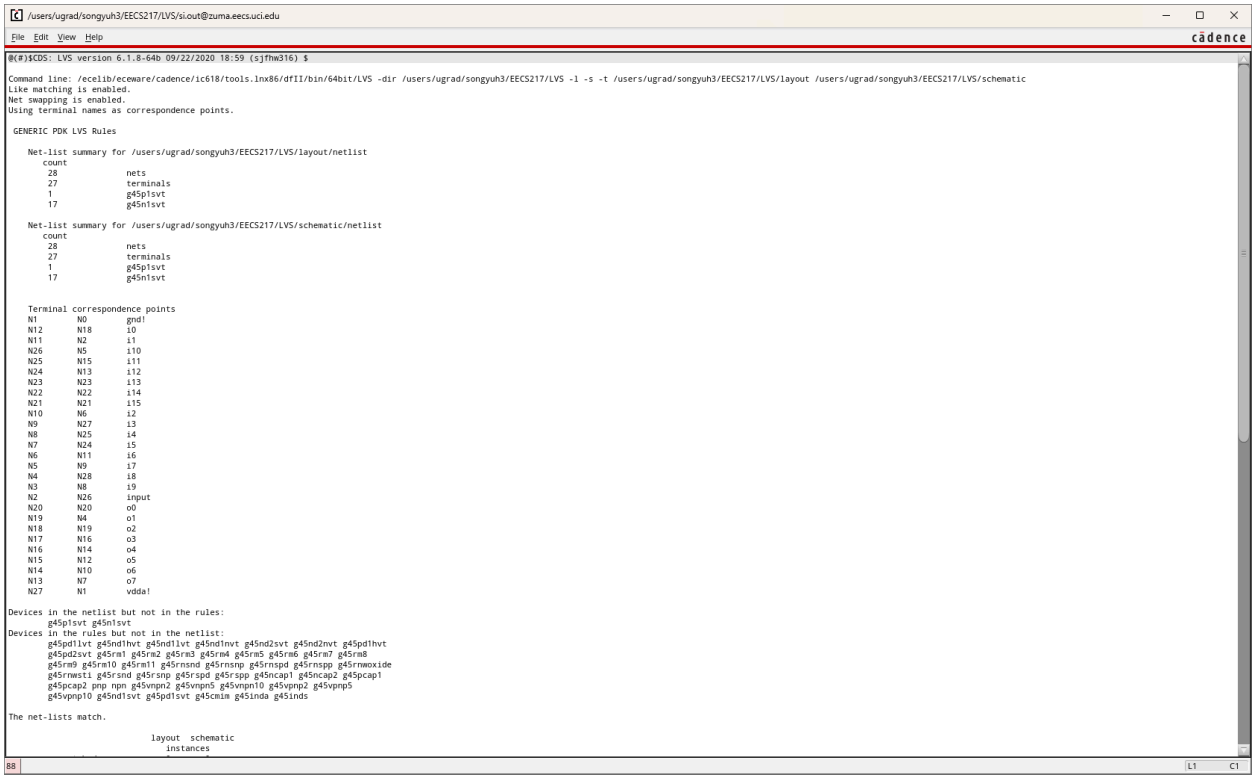

Fig. 11 Column Decoder Circuit Layout LVS Check

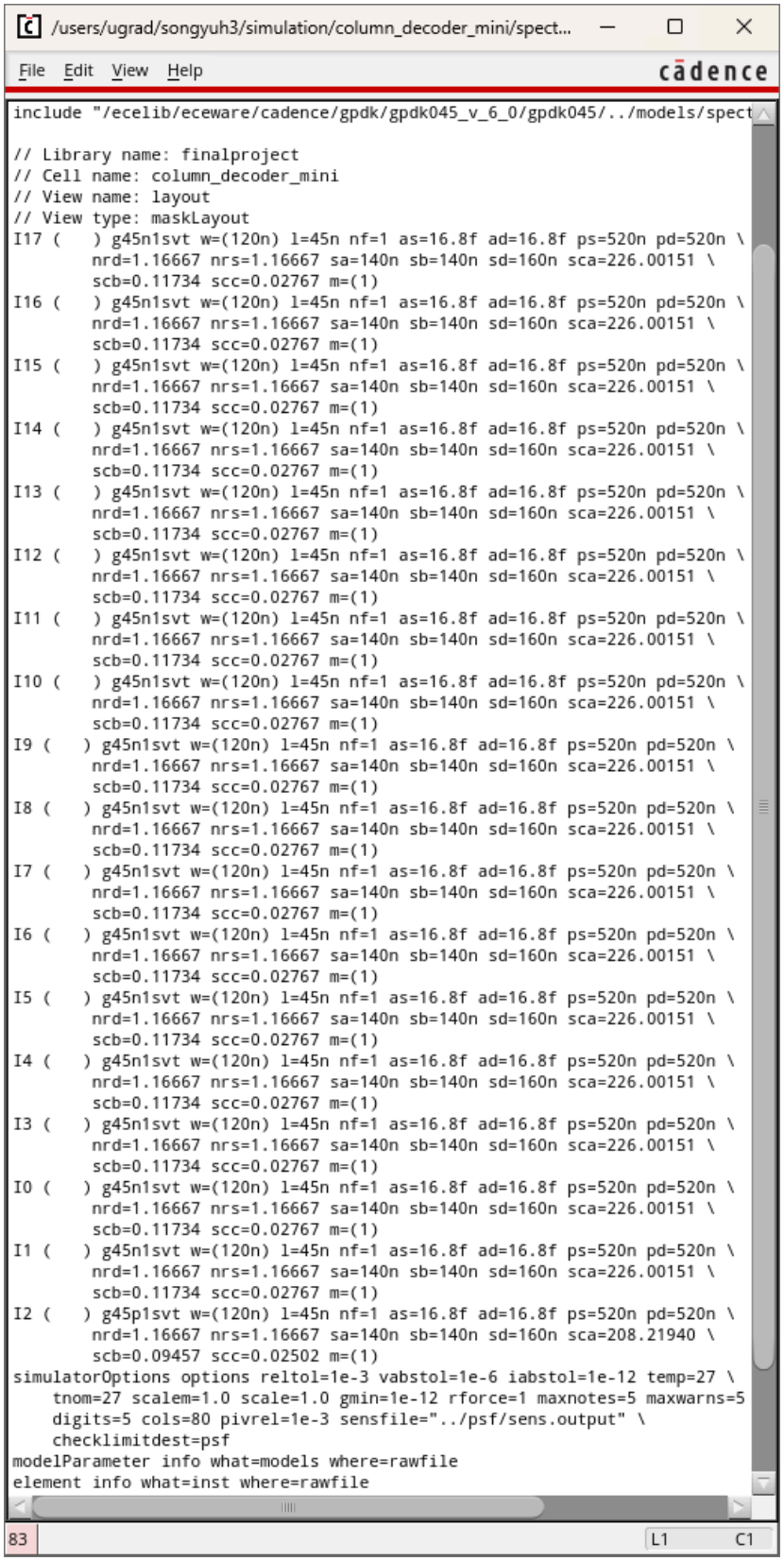

Fig. 12 Column Decoder Circuit Layout Netlist

- **Row Decoder Circuit**

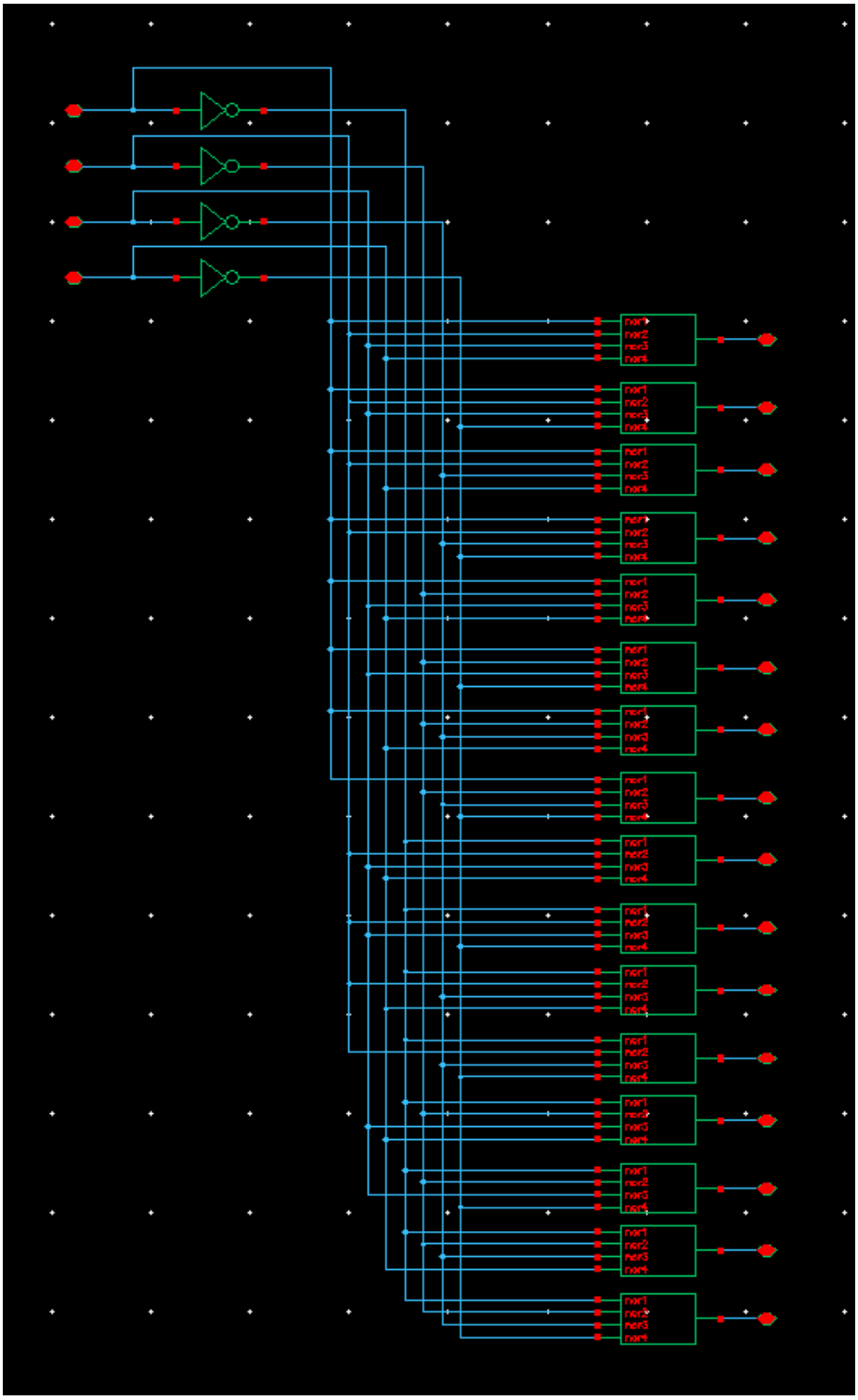

Fig. 13 Row Decoder Circuit

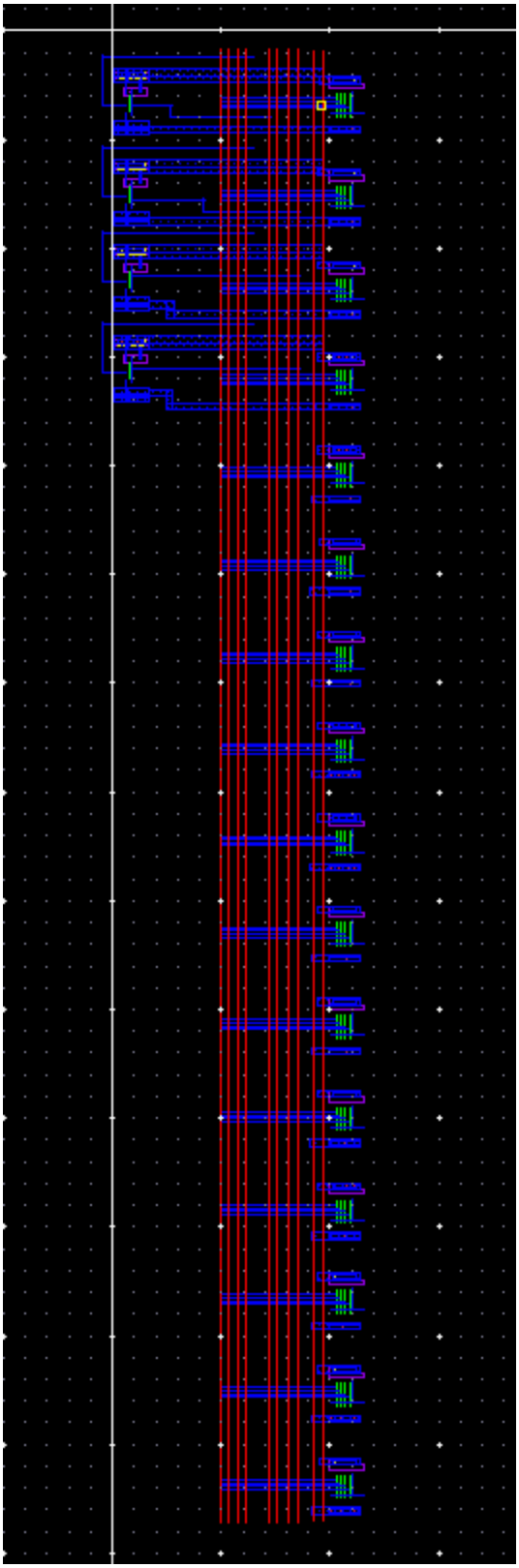

Fig. 14 Row Decoder Circuit Layout

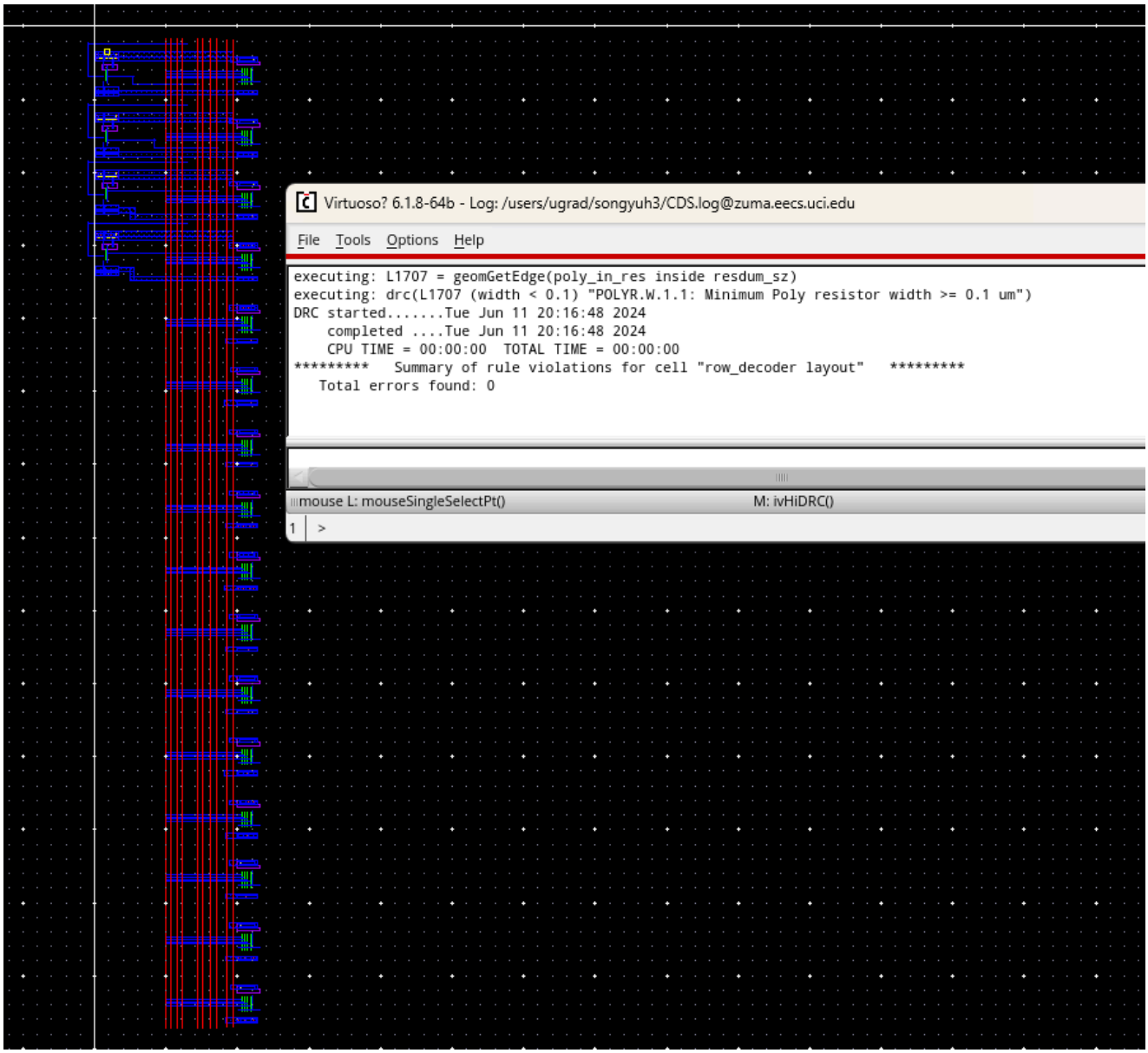

Fig. 15 Row Decoder Circuit Layout DRC Check

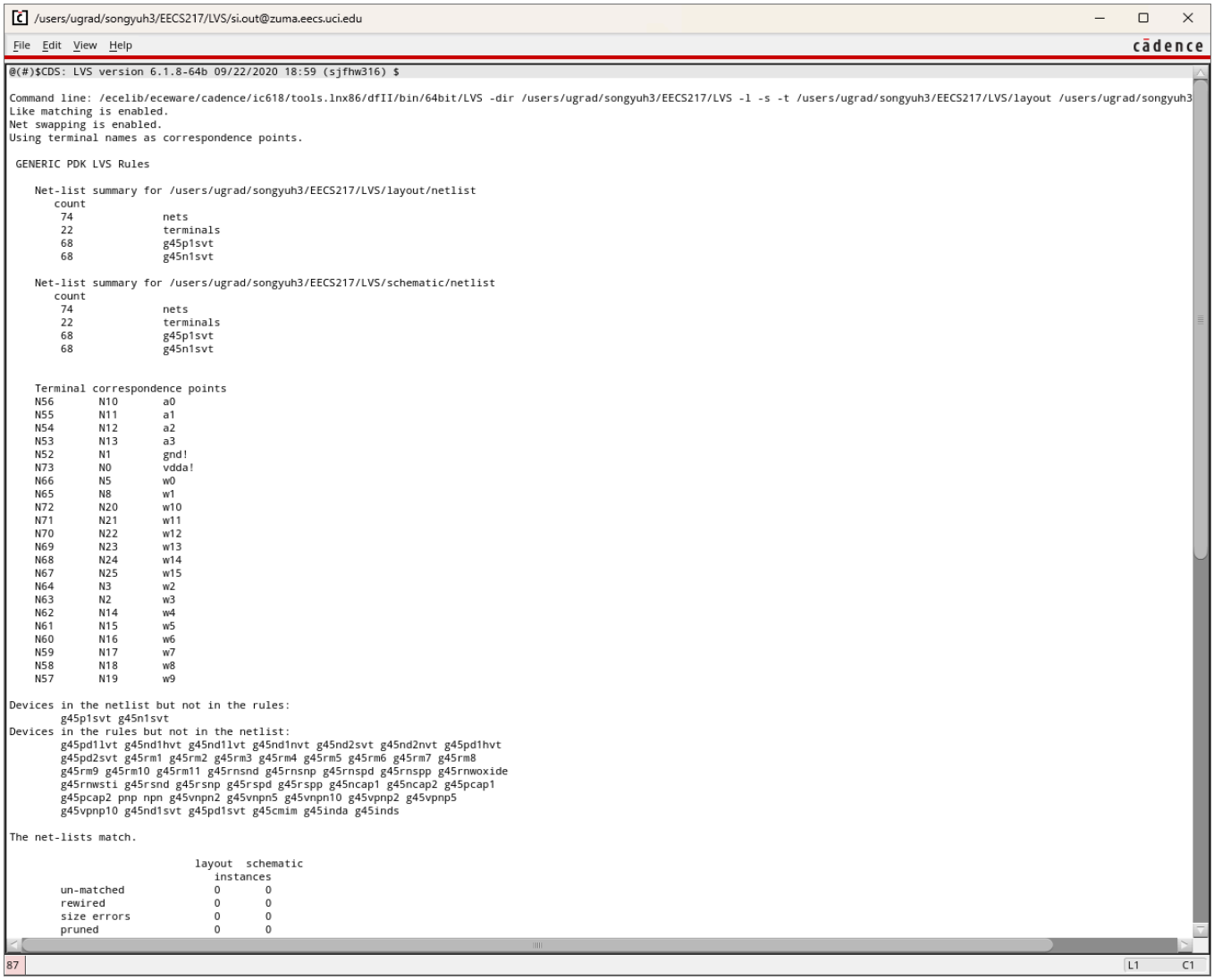

Fig. 16 Row Decoder Circuit Layout LVS Check

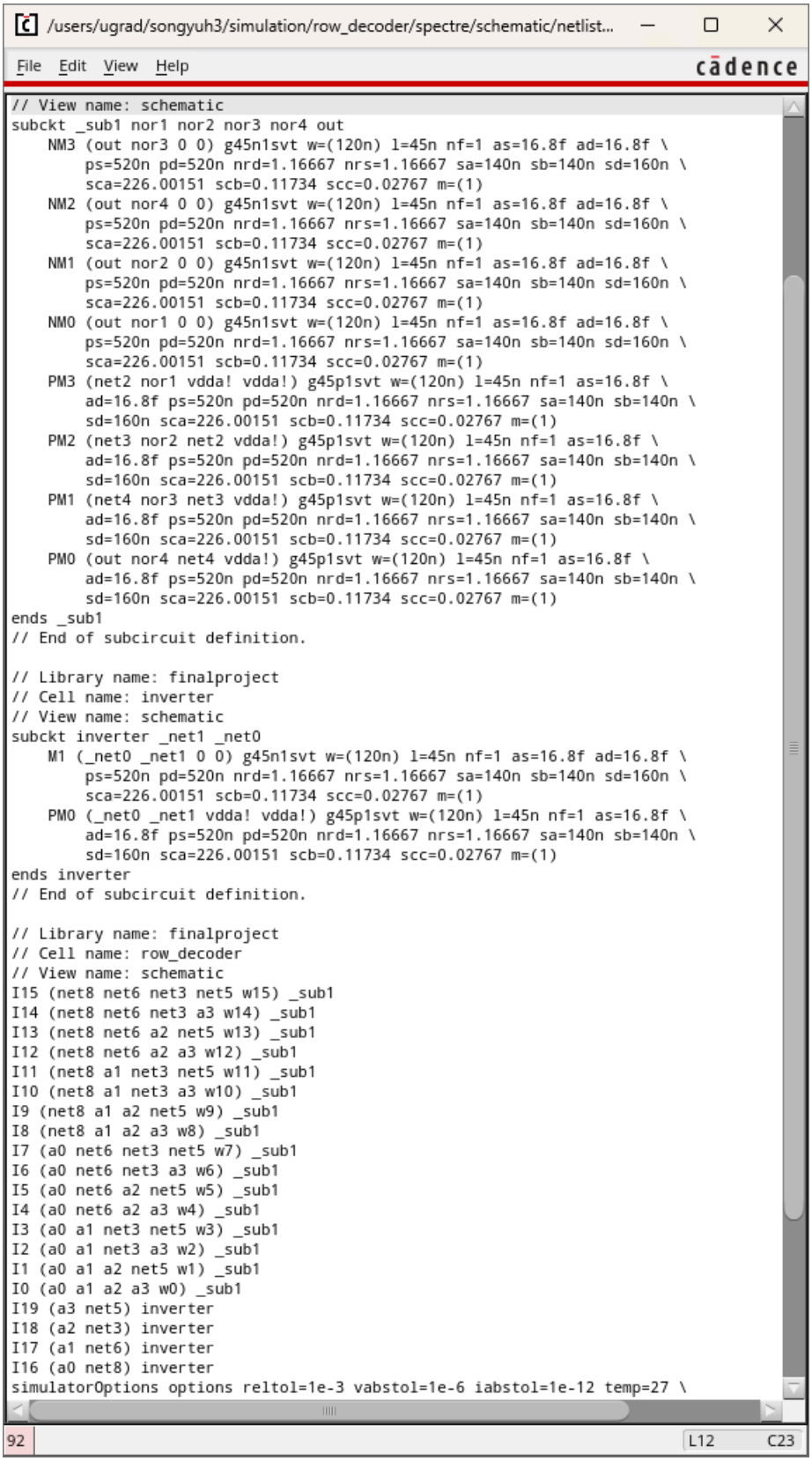

Fig. 17 Row Decoder Circuit Layout Netlist

c. Finished Circuit

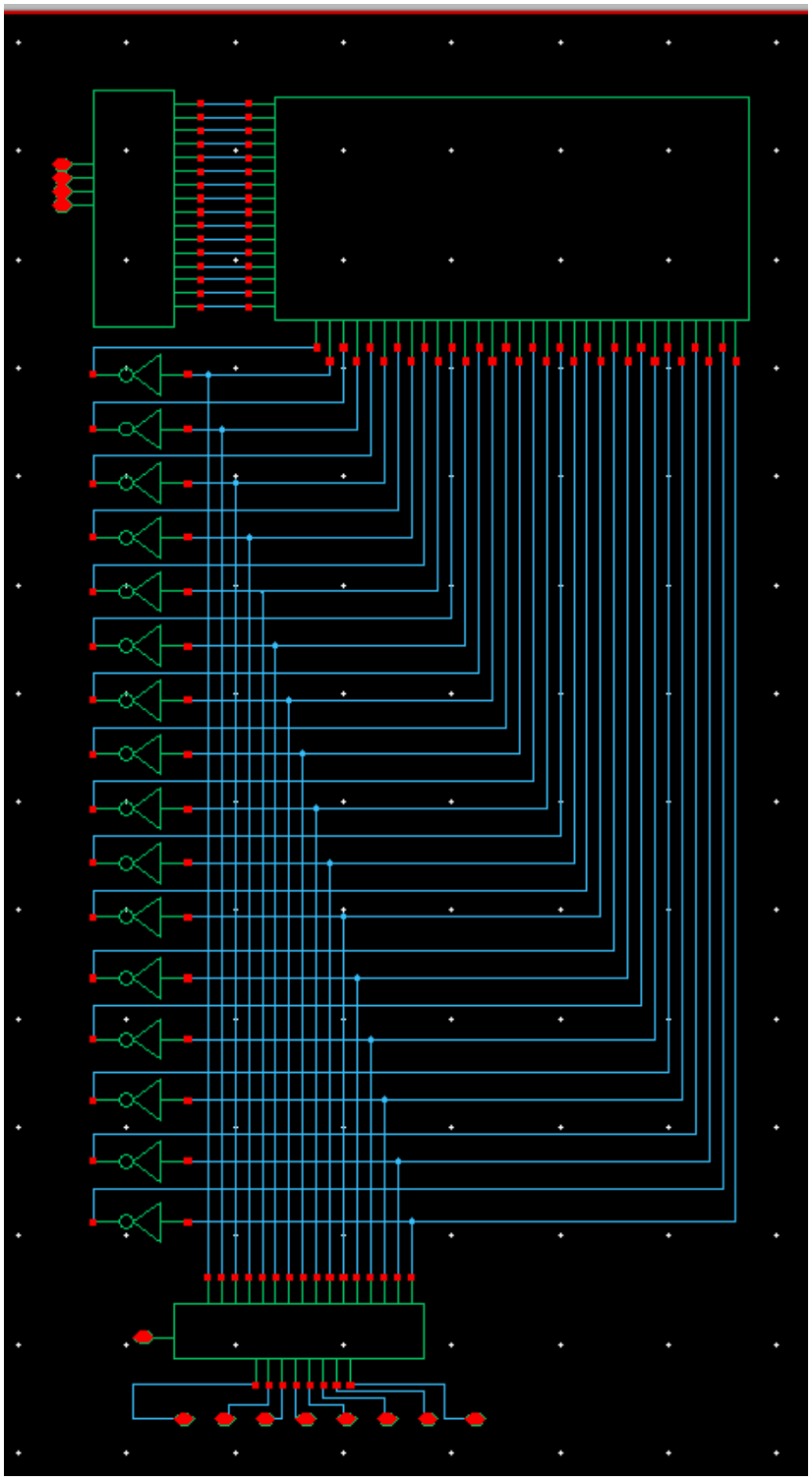

Fig. 18 Finished circuit

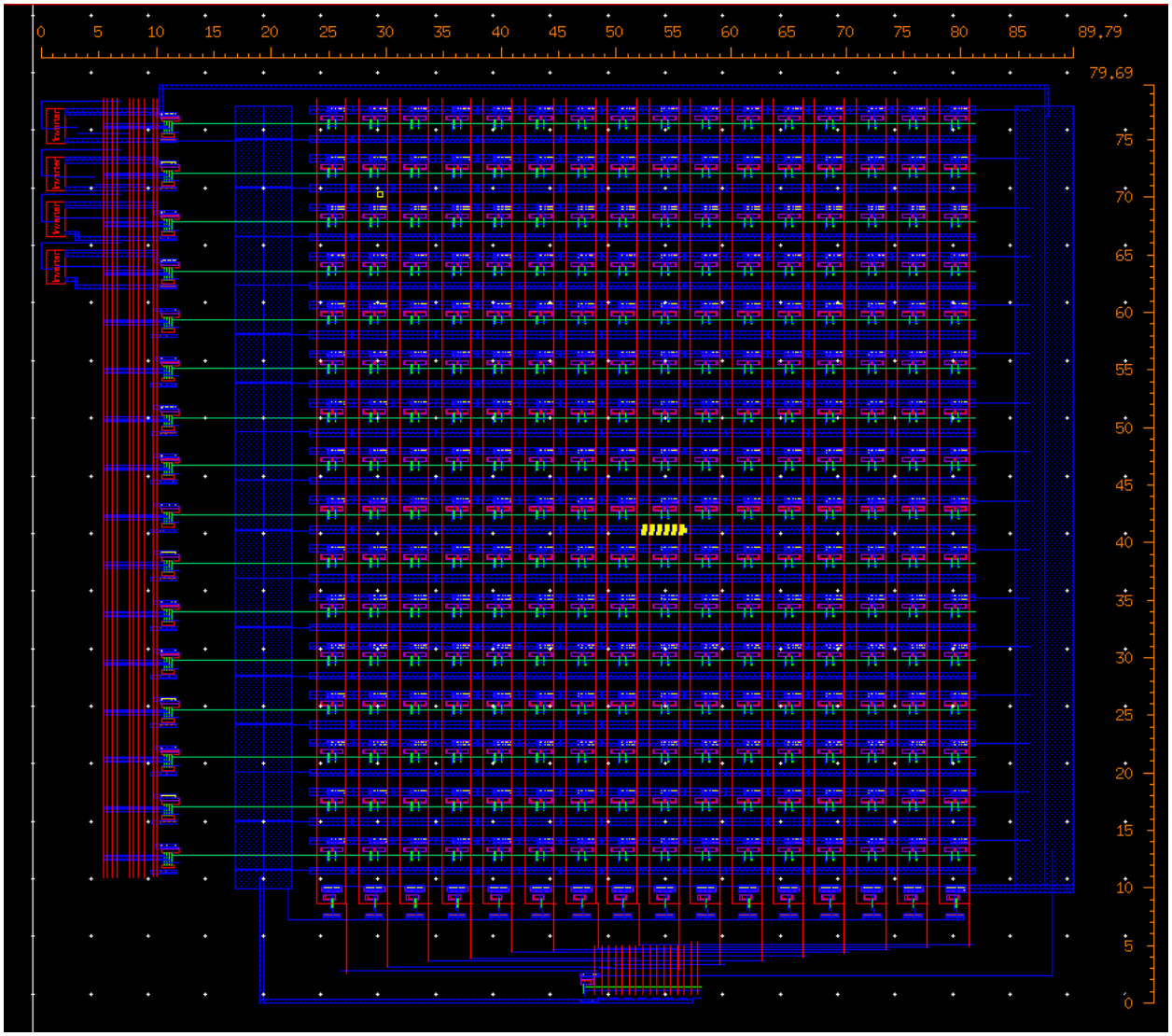

Fig. 19 Finished circuit Layout

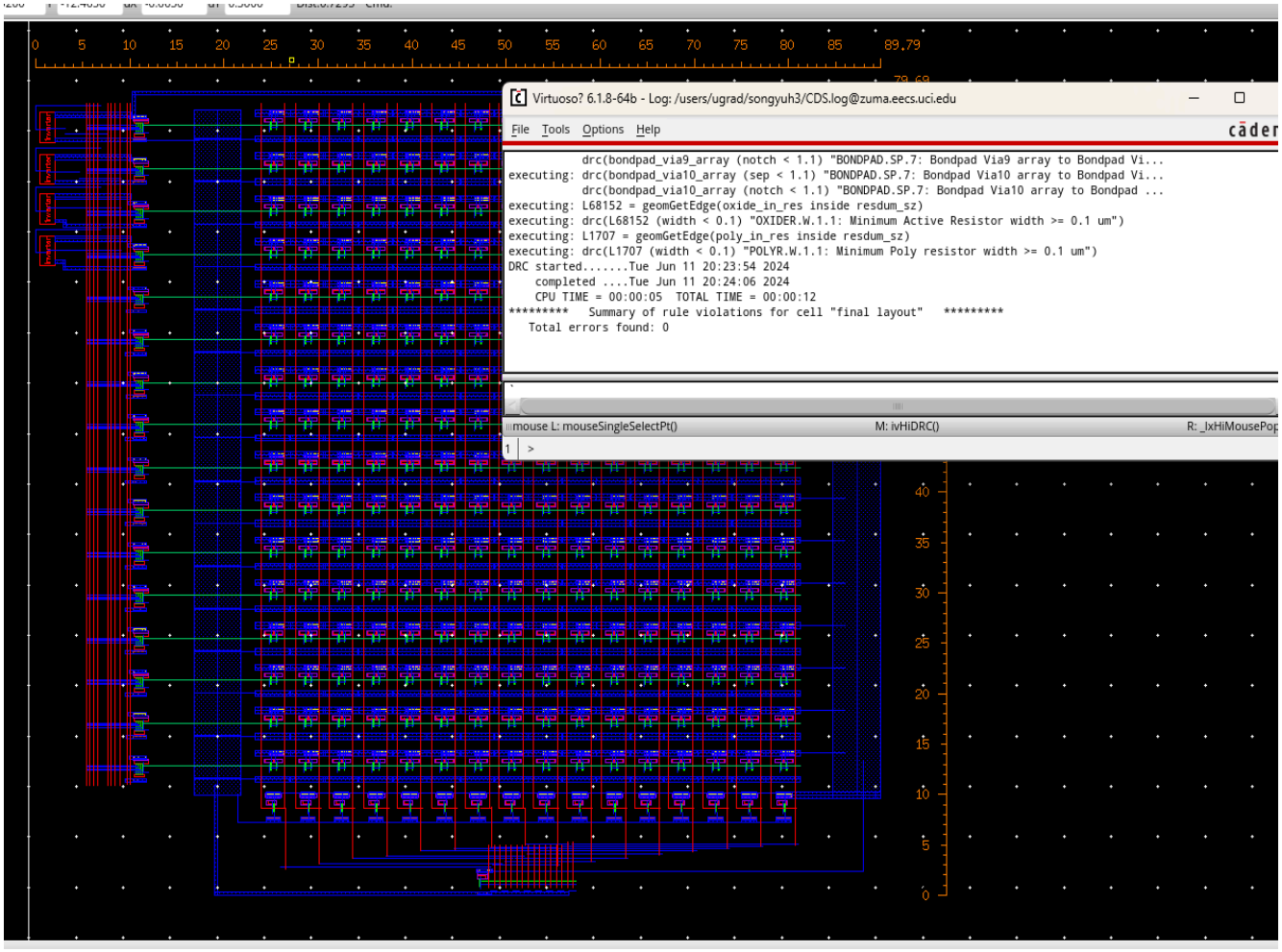

Fig. 20 Finished circuit Layout DRC Check

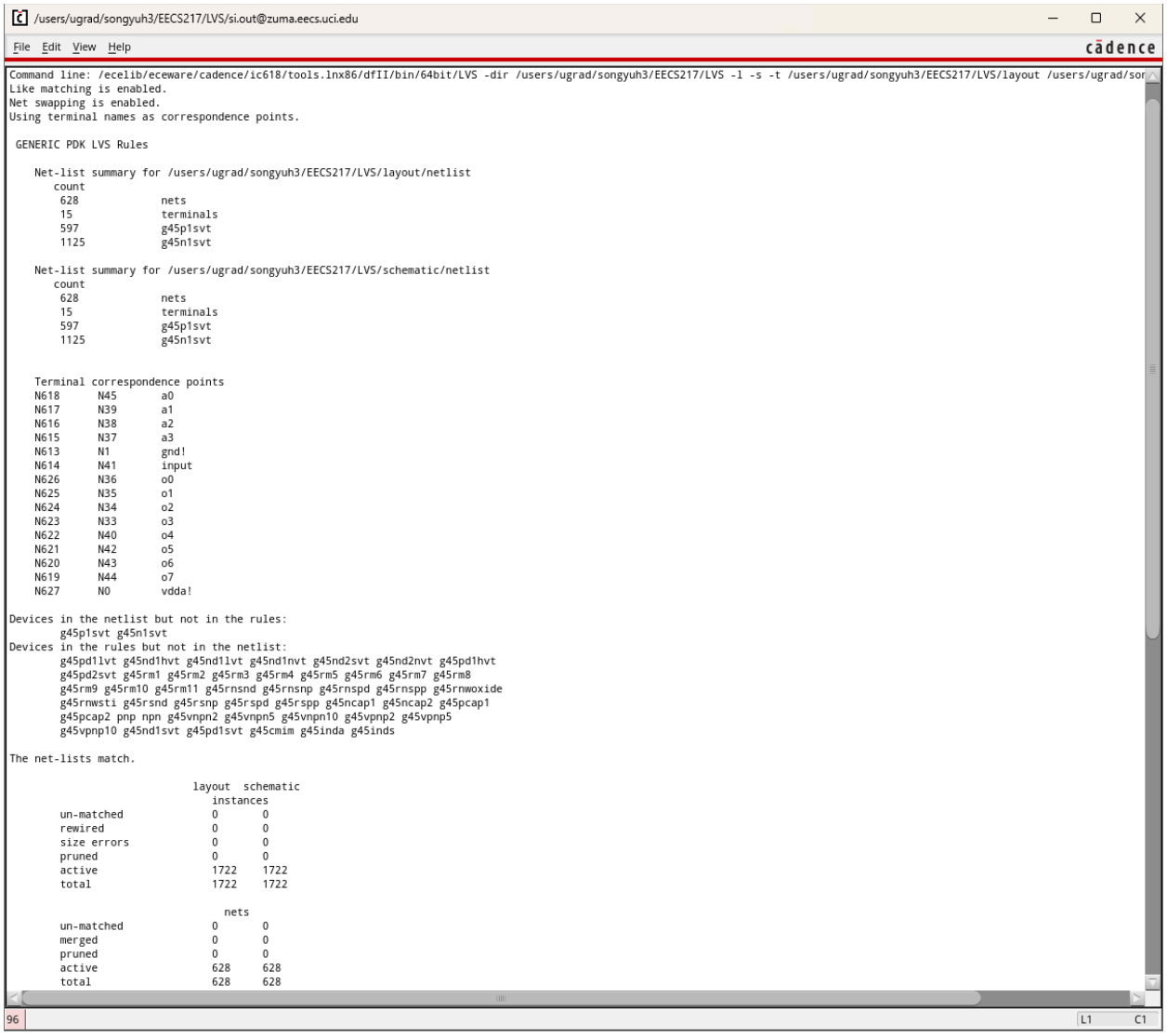

Fig. 21 Finished circuit Layout LVS Check

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// Cell name: SRAMcell
// View name: schematic
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        sca=226.00151 scb=0.11734 scc=0.02767 m=(1)
    NM2 (BL WL net1 0) g45n1svt w=(120n) l=45n nf=1 as=16.8f ad=16.8f \
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        sca=226.00151 scb=0.11734 scc=0.02767 m=(1)
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        ps=520n pd=520n nrd=1.16667 nrs=1.16667 sa=140n sb=140n sd=160n \
        sca=226.00151 scb=0.11734 scc=0.02767 m=(1)
    NM0 (net2 net1 0 0) g45n1svt w=(120n) l=45n nf=1 as=16.8f ad=16.8f \
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        sca=226.00151 scb=0.11734 scc=0.02767 m=(1)
    PM1 (net1 net2 vdda! vdda!) g45p1svt w=(120n) l=45n nf=1 as=16.8f \
        ad=16.8f ps=520n pd=520n nrd=1.16667 nrs=1.16667 sa=140n sb=140n \
        sd=160n sca=226.00151 scb=0.11734 scc=0.02767 m=(1)
    PM0 (net2 net1 vdda! vdda!) g45p1svt w=(120n) l=45n nf=1 as=16.8f \
        ad=16.8f ps=520n pd=520n nrd=1.16667 nrs=1.16667 sa=140n sb=140n \
        sd=160n sca=226.00151 scb=0.11734 scc=0.02767 m=(1)
ends SRAMcell
// End of subcircuit definition.

// Library name: finalproject
// Cell name: 16x16
// View name: schematic
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        bl2 bl3 bl4 bl5 bl6 bl7 bl8 bl9 blbar0 blbar1 blbar10 blbar11 \
        blbar12 blbar13 blbar15 blbar2 blbar214 blbar3 blbar4 blbar5 \
        blbar6 blbar7 blbar8 blbar9 w0 w1 w10 w11 w12 w13 w14 w15 w2 w3 w4
        w5 w6 w7 w8 w9
    I495 (bl0 blbar0 w8) SRAMcell
    I494 (bl0 blbar0 w12) SRAMcell
    I493 (bl0 blbar0 w14) SRAMcell
    I492 (bl0 blbar0 w15) SRAMcell
    I491 (bl8 blbar8 w15) SRAMcell
    I490 (bl12 blbar12 w15) SRAMcell
    I489 (bl15 blbar15 w15) SRAMcell
    I488 (bl14 blbar214 w15) SRAMcell
    I487 (bl13 blbar13 w15) SRAMcell
    I486 (bl11 blbar11 w15) SRAMcell
    I485 (bl10 blbar10 w15) SRAMcell
    I484 (bl9 blbar9 w15) SRAMcell
    I483 (bl4 blbar4 w15) SRAMcell
    I482 (bl7 blbar7 w15) SRAMcell
    I481 (bl6 blbar6 w15) SRAMcell
    I480 (bl5 blbar5 w15) SRAMcell
    I479 (bl3 blbar3 w15) SRAMcell
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99 L1 C1

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```
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    I367 (bl0 blbar0 w4) SRAMcell
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    I365 (bl0 blbar0 w7) SRAMcell
    I364 (bl8 blbar8 w7) SRAMcell
    I363 (bl12 blbar12 w7) SRAMcell
    I362 (bl15 blbar15 w7) SRAMcell
    I361 (bl14 blbar214 w7) SRAMcell
    I360 (bl13 blbar13 w7) SRAMcell
    I359 (bl11 blbar11 w7) SRAMcell
    I358 (bl10 blbar10 w7) SRAMcell
    I357 (bl9 blbar9 w7) SRAMcell
    I356 (bl4 blbar4 w7) SRAMcell
    I355 (bl7 blbar7 w7) SRAMcell
    I354 (bl6 blbar6 w7) SRAMcell
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    I352 (bl3 blbar3 w7) SRAMcell
    I351 (bl2 blbar2 w7) SRAMcell
    I350 (bl1 blbar1 w7) SRAMcell
    I349 (bl8 blbar8 w6) SRAMcell
    I348 (bl12 blbar12 w6) SRAMcell
    I347 (bl15 blbar15 w6) SRAMcell
    I346 (bl14 blbar214 w6) SRAMcell
    I345 (bl13 blbar13 w6) SRAMcell
    I344 (bl11 blbar11 w6) SRAMcell
    I343 (bl10 blbar10 w6) SRAMcell
    I342 (bl9 blbar9 w6) SRAMcell
    I341 (bl4 blbar4 w6) SRAMcell
    I340 (bl7 blbar7 w6) SRAMcell
    I339 (bl6 blbar6 w6) SRAMcell
    I338 (bl5 blbar5 w6) SRAMcell
    I337 (bl3 blbar3 w6) SRAMcell
    I336 (bl2 blbar2 w6) SRAMcell
    I335 (bl1 blbar1 w6) SRAMcell
    I334 (bl0 blbar0 w5) SRAMcell
    I333 (bl8 blbar8 w5) SRAMcell
    I332 (bl12 blbar12 w5) SRAMcell
    I331 (bl15 blbar15 w5) SRAMcell
    I330 (bl14 blbar214 w5) SRAMcell
    I329 (bl13 blbar13 w5) SRAMcell
    I328 (bl11 blbar11 w5) SRAMcell
    I327 (bl10 blbar10 w5) SRAMcell
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    I325 (bl4 blbar4 w5) SRAMcell
    I324 (bl7 blbar7 w5) SRAMcell
    I323 (bl6 blbar6 w5) SRAMcell
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    I318 (bl8 blbar8 w4) SRAMcell
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99 L1 C1

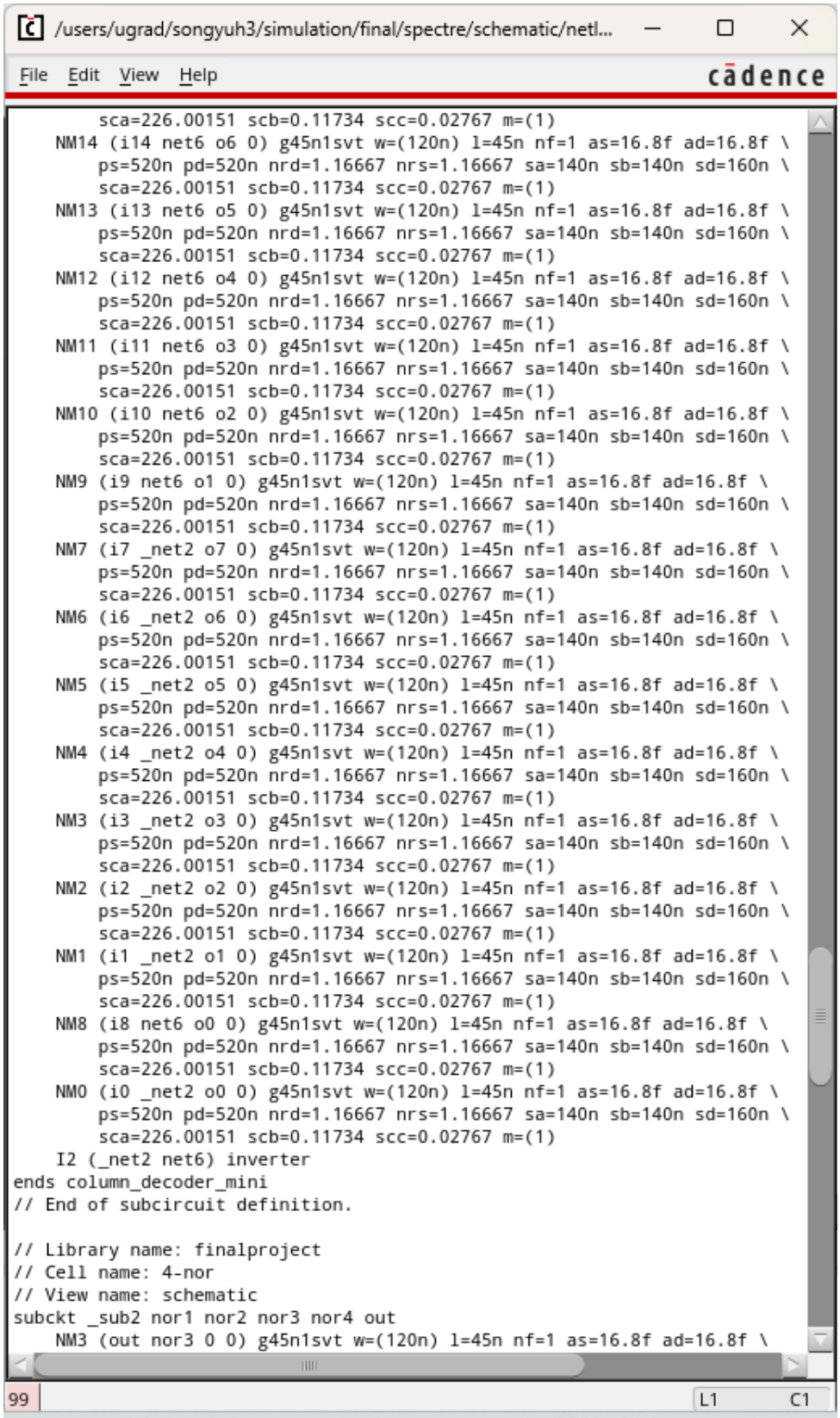


Fig. 22 Finished circuit Layout Netlist

d. Floor Plan of SRAM and dimension of each block

- SRAM dimension

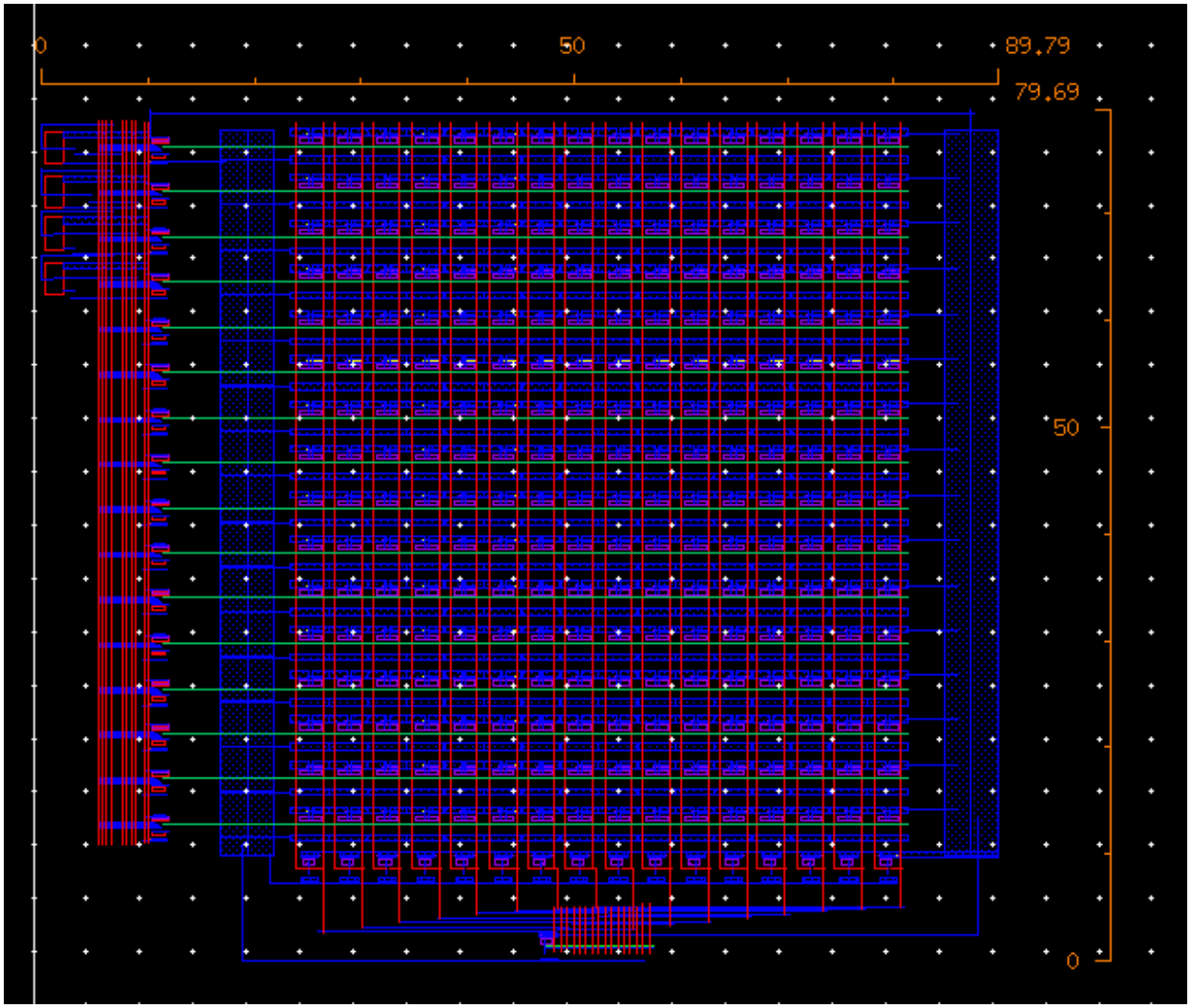


Fig. 23 Finished Circuit Layout Dimension

- Memory cell block dimension

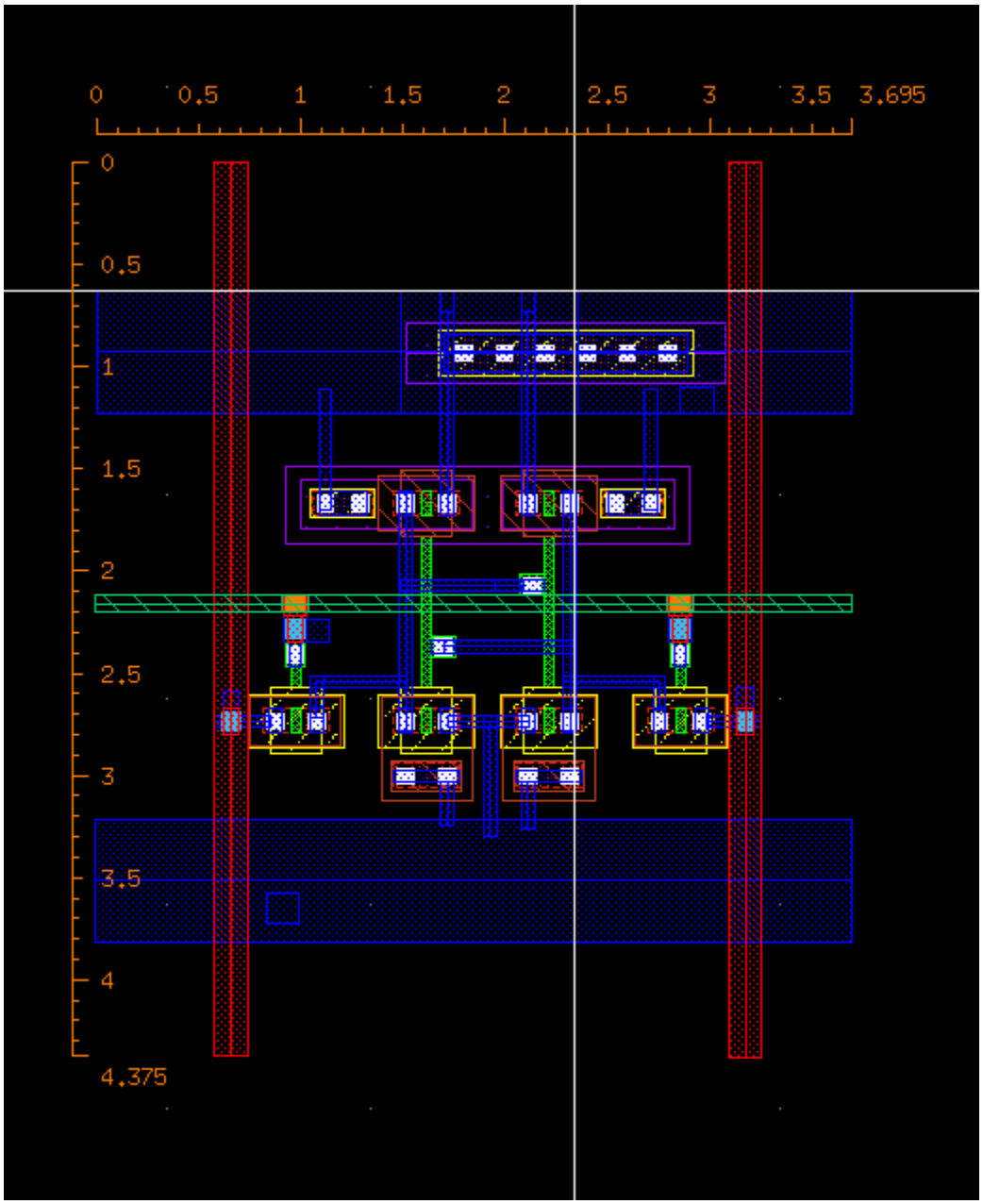


Fig. 24 Each memory cell dimension

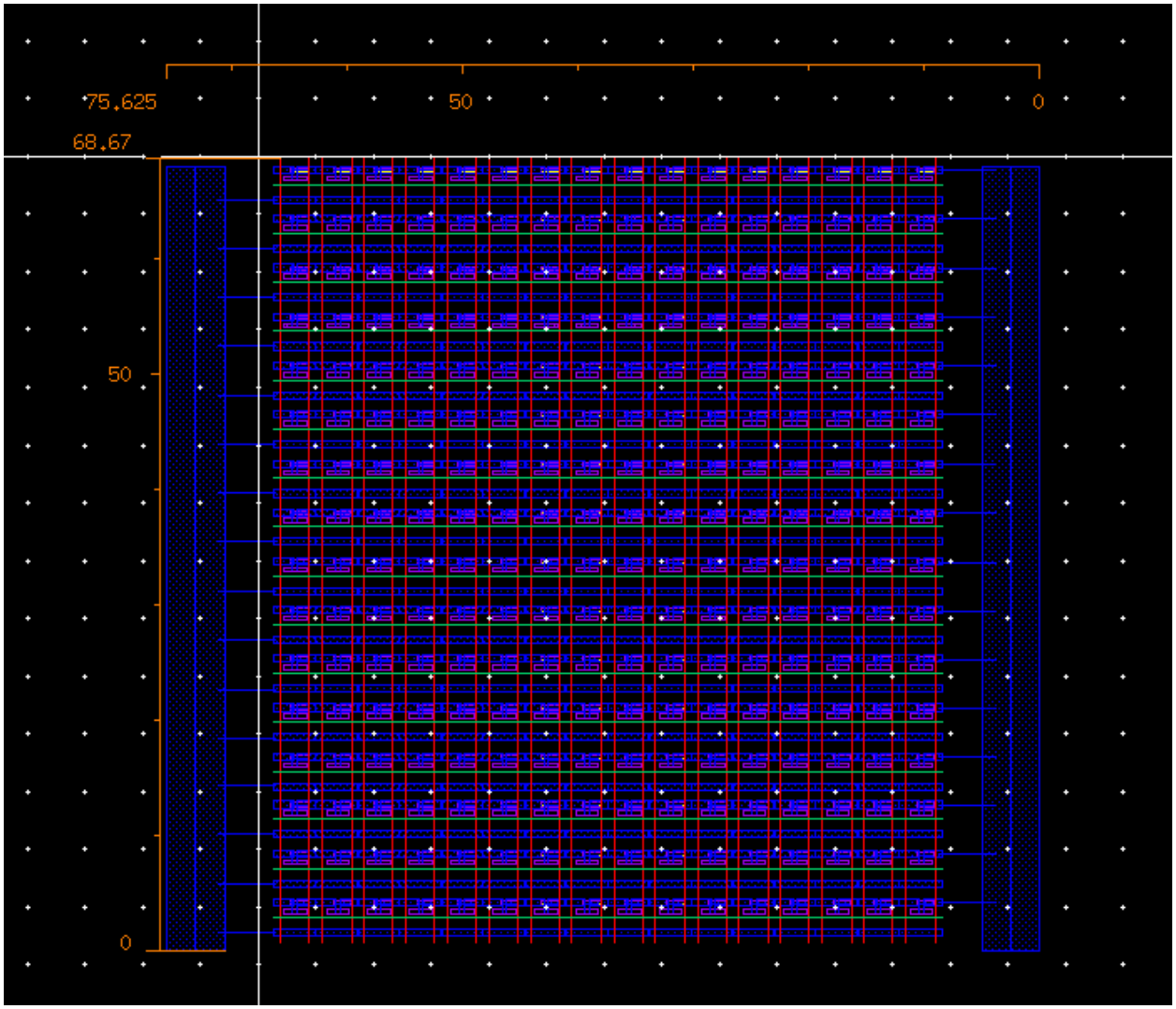


Fig. 25 16*16 memory cell block dimension

- Row decoder block dimension

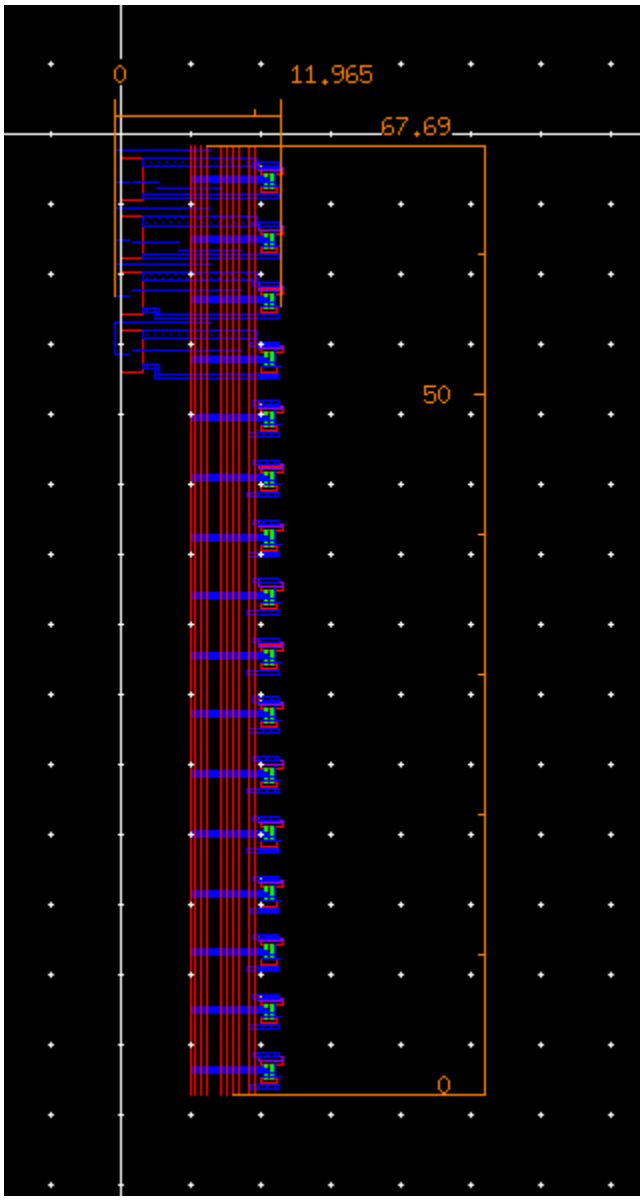


Fig. 26 Row decoder block dimension

- Column decoder block dimension

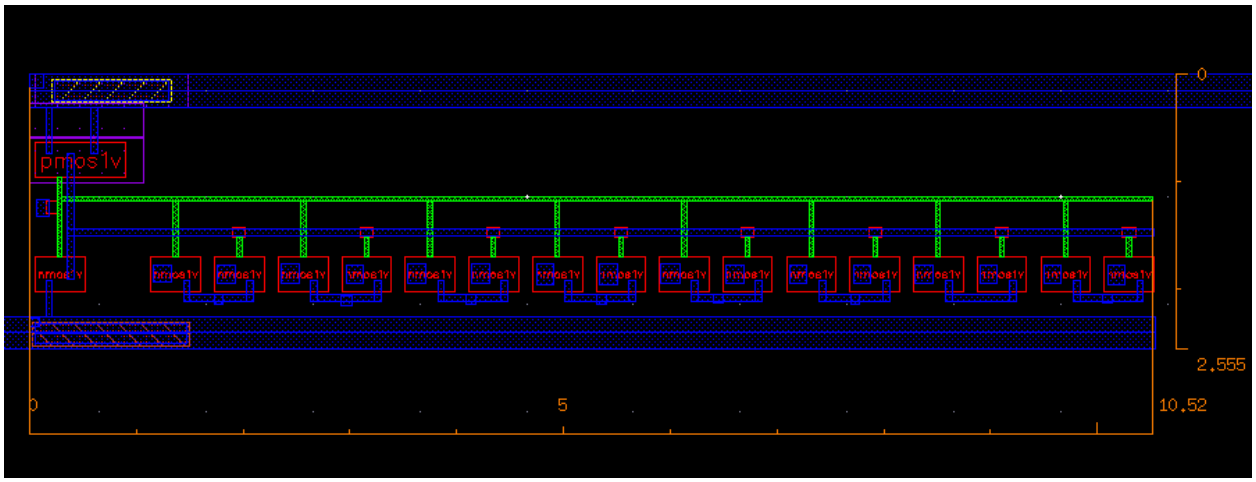


Fig. 27 Column decoder block dimension

2. Simulation result

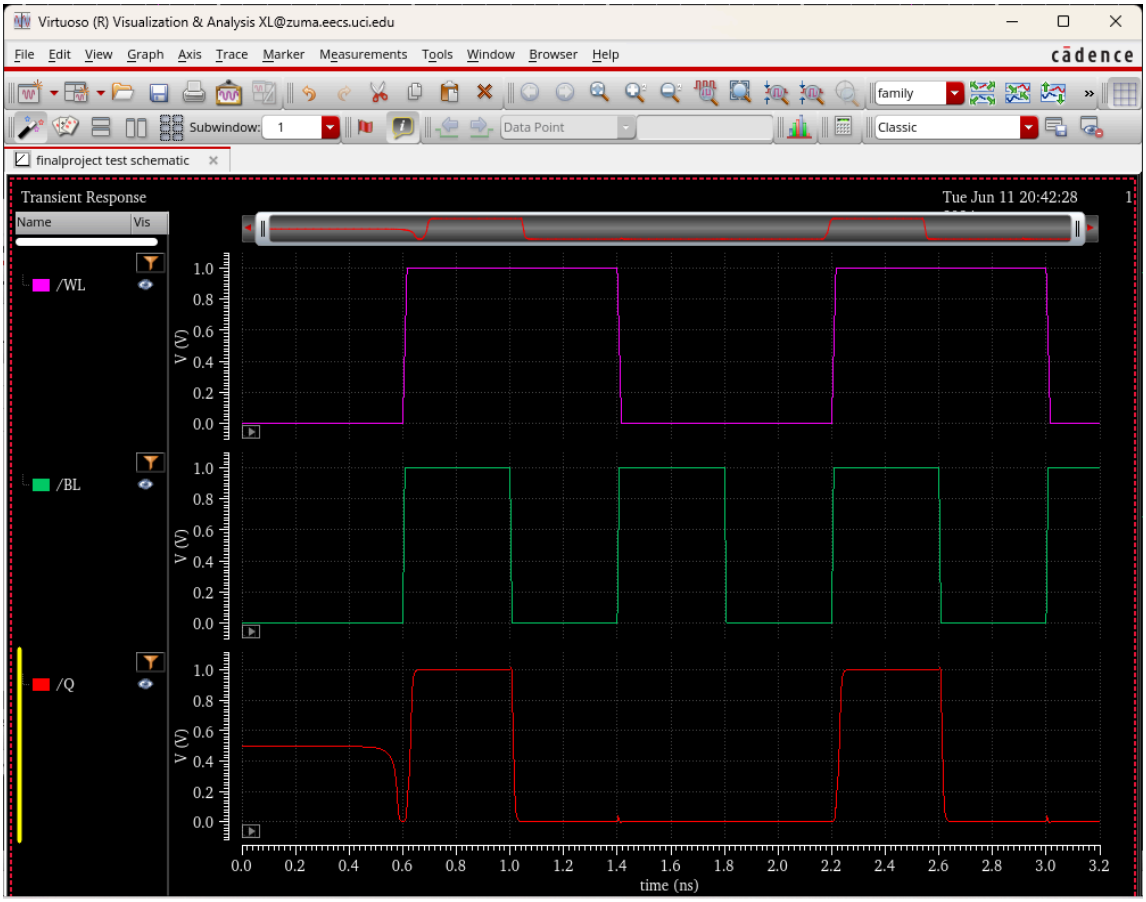


Fig. 28 Working waveform (1->0)

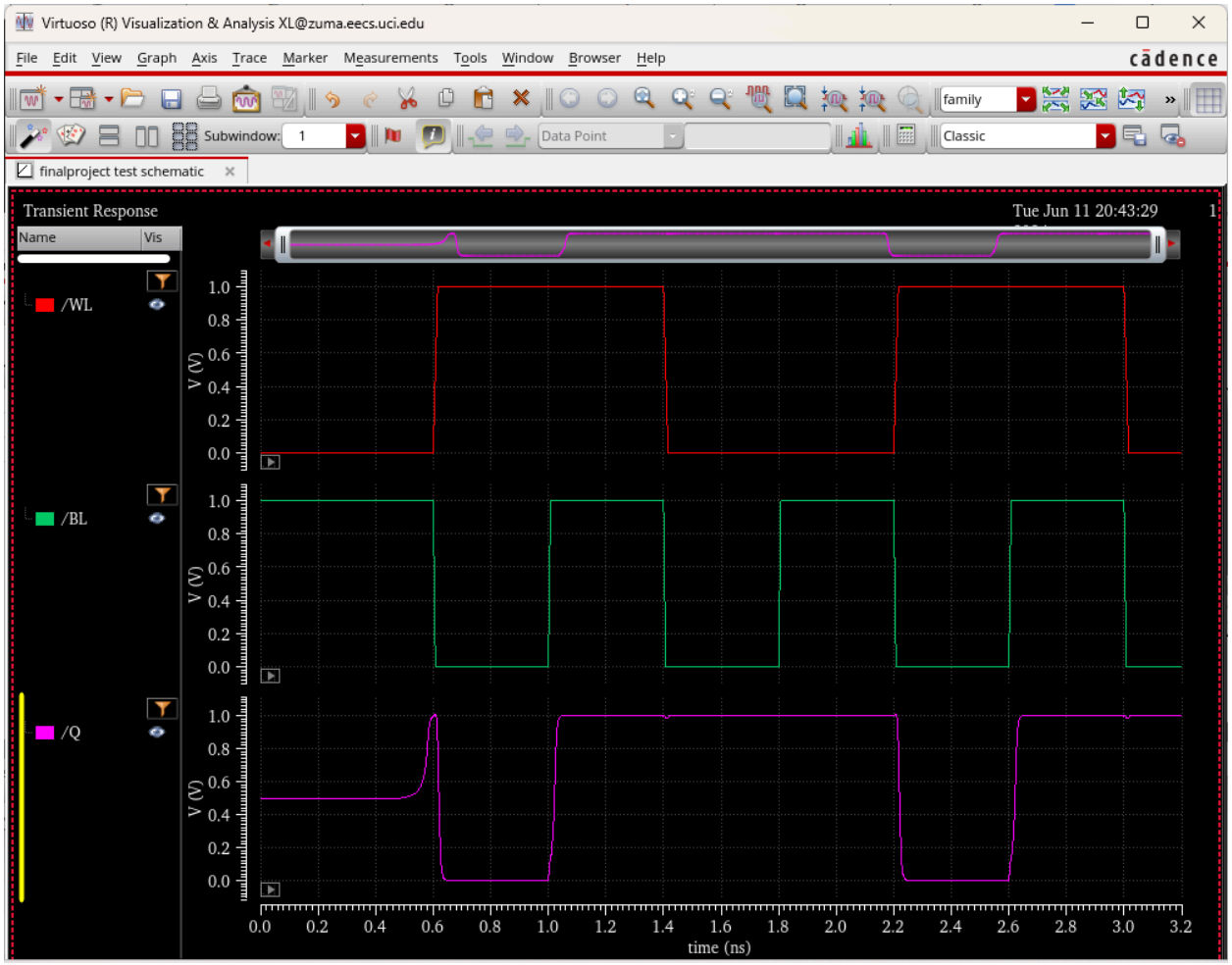
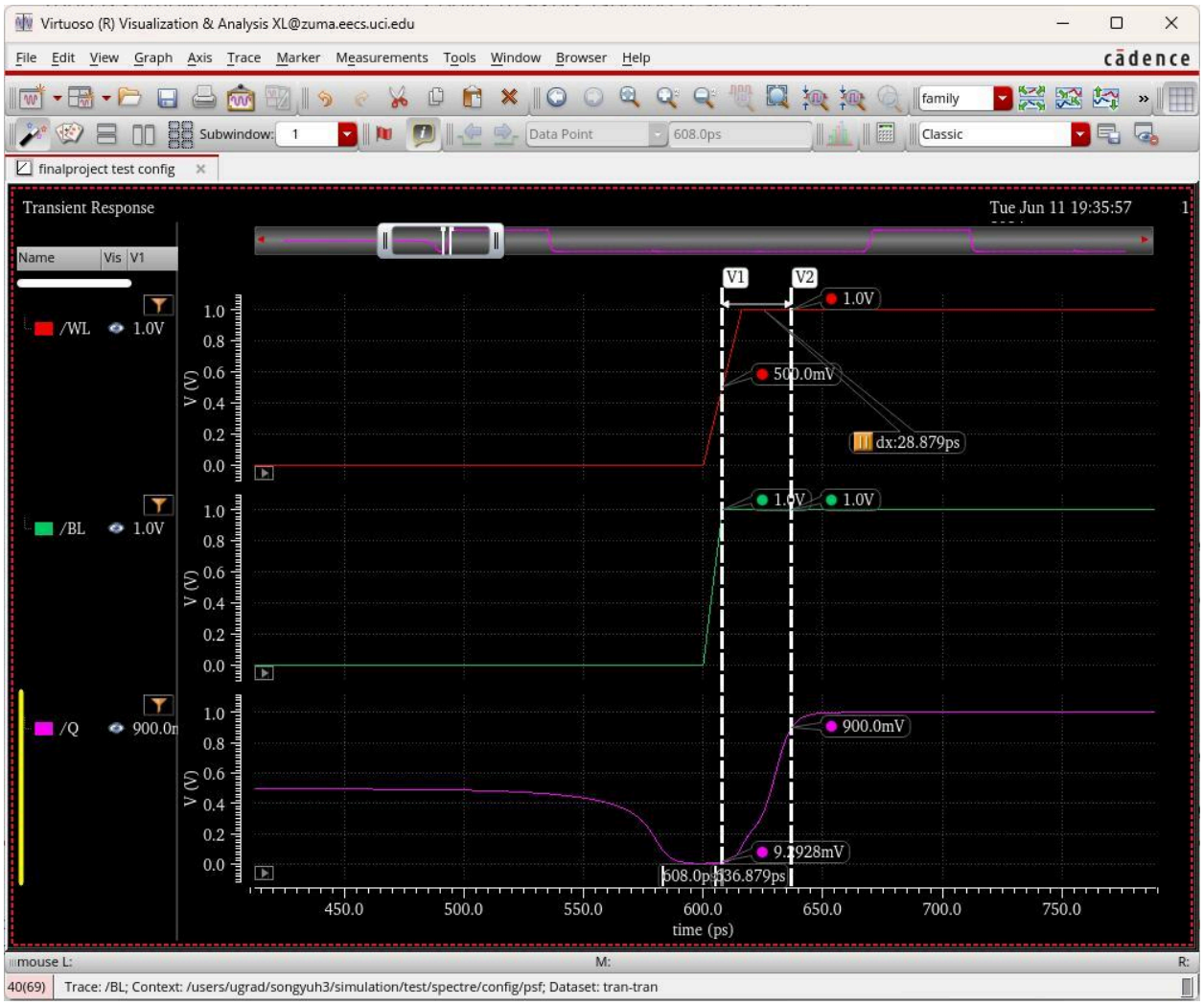


Fig. 29 Working waveform (0->1)

3. Extracted Simulation

a. Extracted simulation result



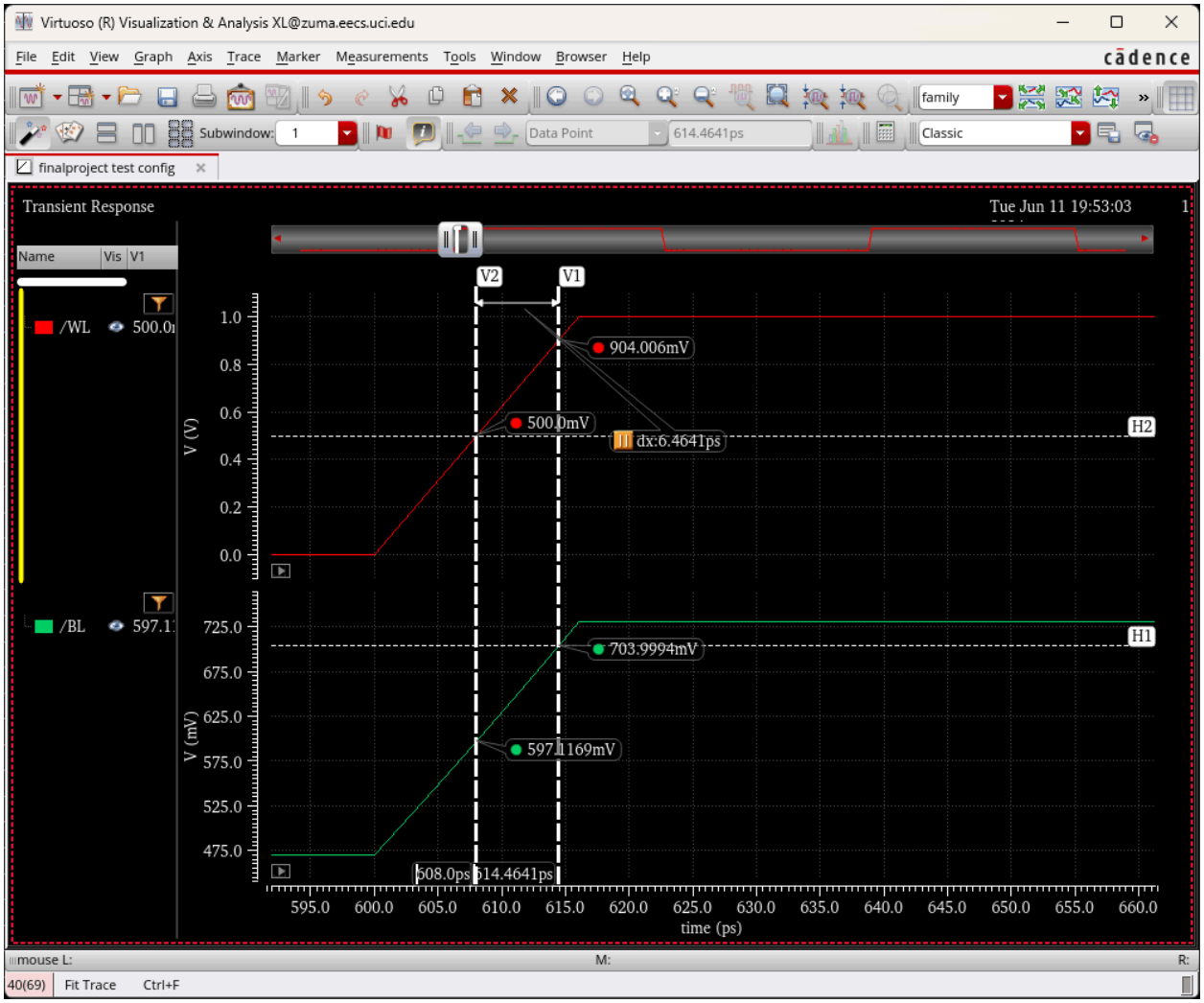


Fig. 30 Extracted Simulation result

4. Design Strategy and Description

a. Goals

Memory Cell Design

- **6-Transistor CMOS SR Flip Flop**: The memory cell design is based on a 6-transistor (6T) CMOS static RAM (SRAM) flip-flop. This configuration provides a good balance of stability, speed, and power consumption.

Memory Organization

- **Array Structure**: The memory cells are organized in a 16x2 bytes (or 16 rows x 16 columns) rectangular array. This structure provides 256 bits of storage.

Address Decoding

- **Row Decoder**: The row decoder addresses the 16 wordlines, each corresponding to a row in the memory array.
- **Column Decoder**: The column decoder addresses the 16 columns, each column being 1 bit wide.

Memory Cell Sizing

- **Performance, Power, Area Optimization**: The memory cell should be optimized for performance, power consumption, and area. It must operate correctly in both read and write modes.

b. Description and Calculations

Read / Write time

The read and write time are measured in **Fig. 30.** The write time is approximately 28.879ps, and the read time is approximately 6.4641ps.

Component Area Size

Components	Length / μm	Width / μm	Area / μm^2
SRAM Cell	4.375	3.695	16.1656
Row Decoder	67.69	11.965	809.9109
Column Decoder	2.555	10.52	26.8786
16x16 Memory Block	79.69	89.79	7155.3651