

VLSI Design

EECS 217

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06/11/2024

# 1. Schematic simulation

## a. Project design requirements

Final Project  
EECS217  
Instructor: Dr. Kavianpour

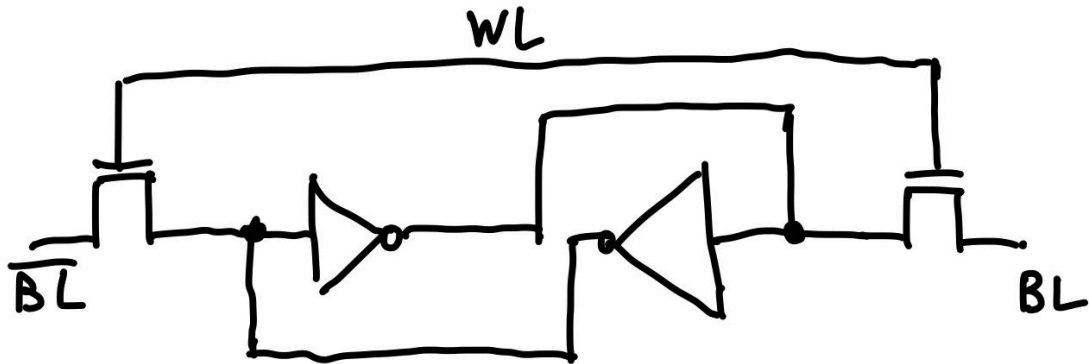
Design 256 bits SRAM with the following characteristics:

- 1- The memory cell is based on the 6-transistor CMOS SR flip flop.
- 2- The memory cells are organized as 16 by two bytes rectangular array.
- 3- Row decoder addresses the 16 wordlines, while column decoder addresses each of the 2 bytes columns. Each row wordline is 16 bits (thus 2 bytes), and each column is 1 byte wide.
- 4- Use NAND design for these decoders.
- 5- Input/output signals swing between Gnd and Vdd and assume to be ideal steps.
- 6- Delays should be measured from the 50% point of the input waveform of the input, to the 50% of the outputs of either of the two decoders (whichever is slower).
- 7- The memory cell should be sized in such a way that the overall memory achieves the goals: performance, power, and area. Your cell design should first be based on proper operation in both *read* and *write* mode.
- 8- You do not need to include the sense amplifier or the tri-state driver in your design
- 9- Assume row word line load is 100fF and the column bit line load is 20pF. 10- Take only the capacitance of the bit- and wordlines into account. IGNORE the resistance. This will give you optimistic results but simplifies the analysis. You should, however, keep the resistance of the bit- and wordlines into account when you layout your cell. Long wires in polysilicon are not the right way to go. Poly-metal contacts also introduce resistance.

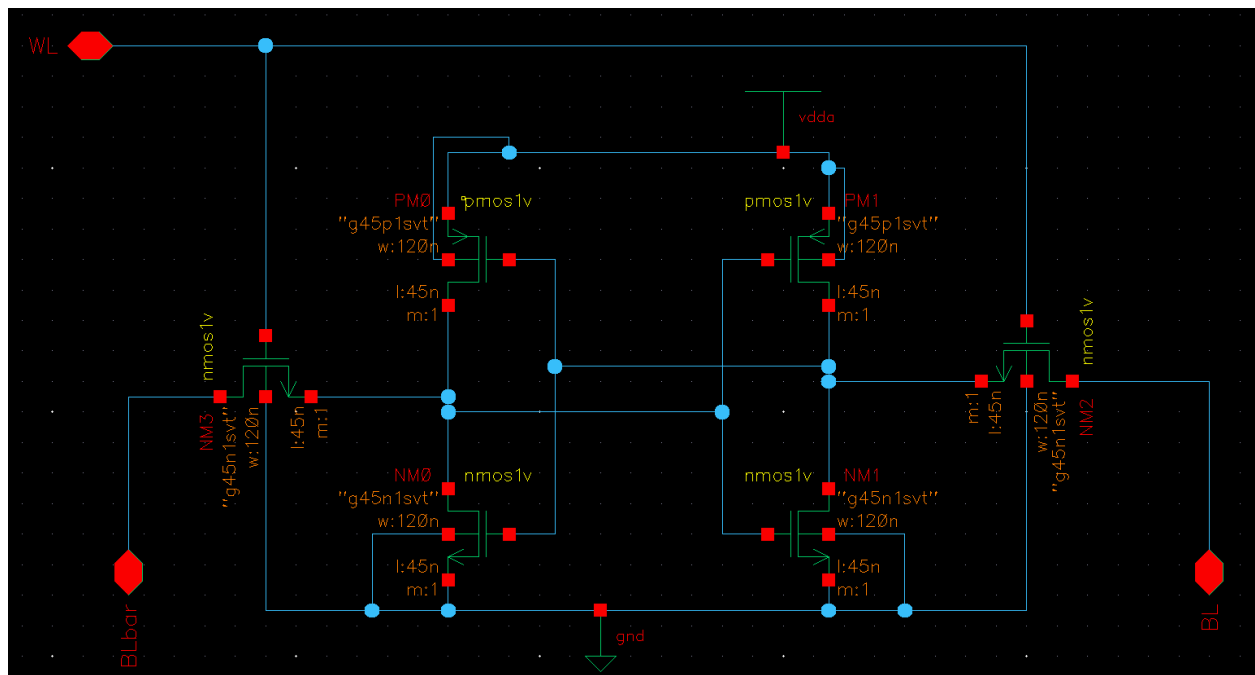
**Fig. 1** Design requirements

## b. Circuit Design

- Memory Cell Circuit

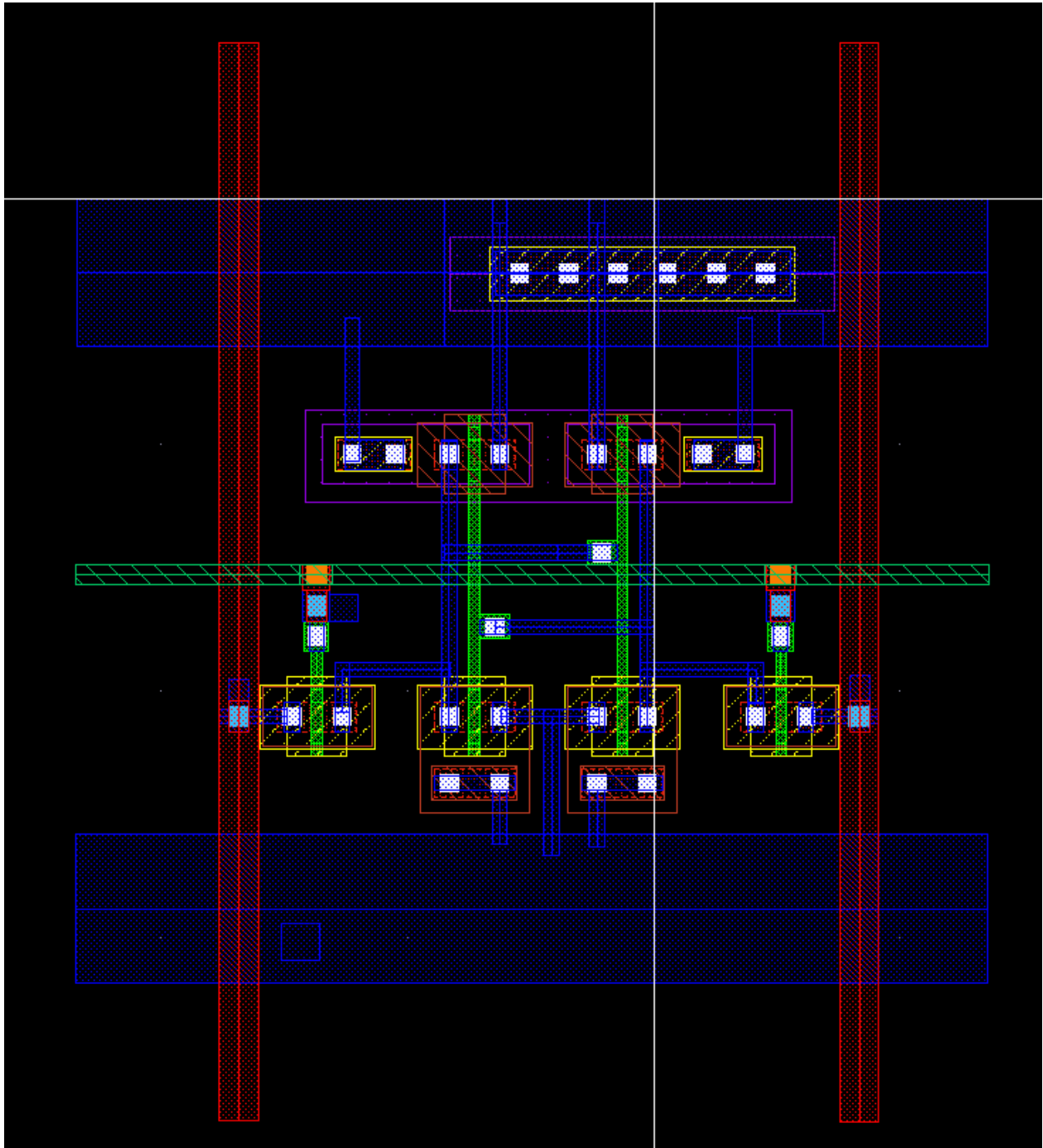


**Fig. 2** Gate level design of Memory Cell



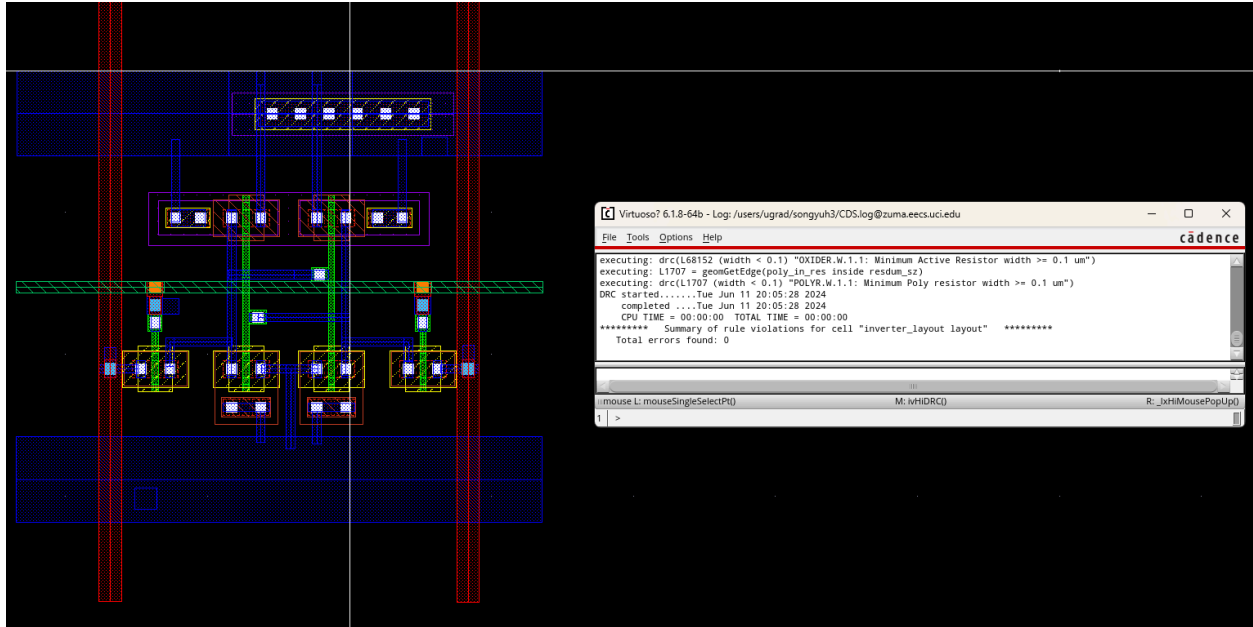
**Fig. 3** Memory Cell Circuit

The circuit is shown in **Fig. 3**, is a single memory cell circuit, whole SRAM include  $16 \times 16 = 256$  memory cell

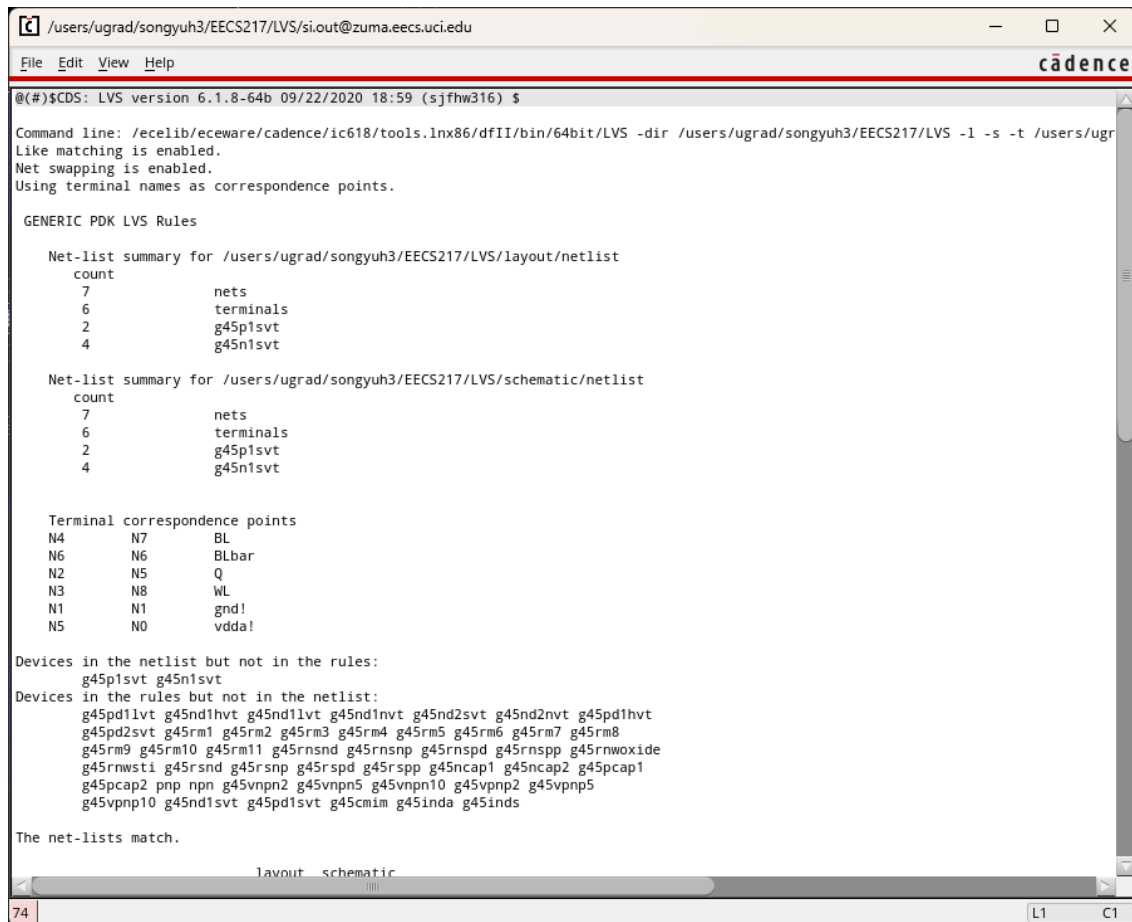


**Fig. 4** Memory Cell Circuit Layout

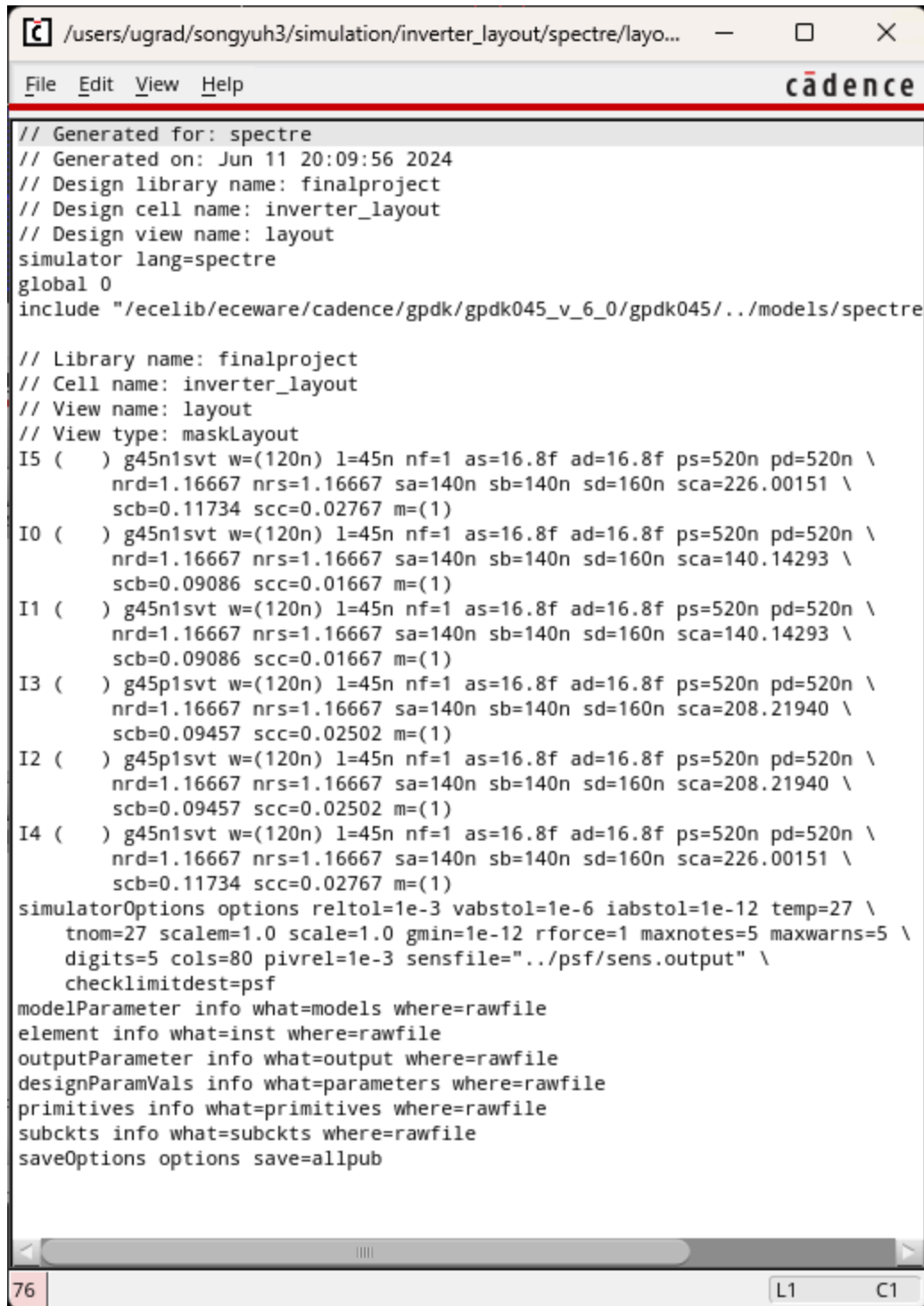
The **Fig. 4** shown the layout of one memory cell.



**Fig. 5** Memory Cell Circuit Layout DRC Check



**Fig. 6** Memory Cell Circuit Layout LVS Check



```
// Generated for: spectre
// Generated on: Jun 11 20:09:56 2024
// Design library name: finalproject
// Design cell name: inverter_layout
// Design view name: layout
simulator lang=spectre
global 0
include "/eclib/eceware/cadence/gpdk/gpdk045_v_6_0/gpdk045/../../models/spectre

// Library name: finalproject
// Cell name: inverter_layout
// View name: layout
// View type: maskLayout
I5 ( ) g45n1svt w=(120n) l=45n nf=1 as=16.8f ad=16.8f ps=520n pd=520n \
    nrd=1.16667 nrs=1.16667 sa=140n sb=140n sd=160n sca=226.00151 \
    scb=0.11734 scc=0.02767 m=(1)
I0 ( ) g45n1svt w=(120n) l=45n nf=1 as=16.8f ad=16.8f ps=520n pd=520n \
    nrd=1.16667 nrs=1.16667 sa=140n sb=140n sd=160n sca=140.14293 \
    scb=0.09086 scc=0.01667 m=(1)
I1 ( ) g45n1svt w=(120n) l=45n nf=1 as=16.8f ad=16.8f ps=520n pd=520n \
    nrd=1.16667 nrs=1.16667 sa=140n sb=140n sd=160n sca=140.14293 \
    scb=0.09086 scc=0.01667 m=(1)
I3 ( ) g45p1svt w=(120n) l=45n nf=1 as=16.8f ad=16.8f ps=520n pd=520n \
    nrd=1.16667 nrs=1.16667 sa=140n sb=140n sd=160n sca=208.21940 \
    scb=0.09457 scc=0.02502 m=(1)
I2 ( ) g45p1svt w=(120n) l=45n nf=1 as=16.8f ad=16.8f ps=520n pd=520n \
    nrd=1.16667 nrs=1.16667 sa=140n sb=140n sd=160n sca=208.21940 \
    scb=0.09457 scc=0.02502 m=(1)
I4 ( ) g45n1svt w=(120n) l=45n nf=1 as=16.8f ad=16.8f ps=520n pd=520n \
    nrd=1.16667 nrs=1.16667 sa=140n sb=140n sd=160n sca=226.00151 \
    scb=0.11734 scc=0.02767 m=(1)
simulatorOptions options reltol=1e-3 vabstol=1e-6 iabstol=1e-12 temp=27 \
    tnom=27 scalem=1.0 scale=1.0 gmin=1e-12 rforce=1 maxnotes=5 maxwarns=5 \
    digits=5 cols=80 pivrel=1e-3 sensfile="../../psf/sens.output" \
    checklimitdest=psf
modelParameter info what=models where=rawfile
element info what=inst where=rawfile
outputParameter info what=output where=rawfile
designParamVals info what=parameters where=rawfile
primitives info what=primitives where=rawfile
subckts info what=subckts where=rawfile
saveOptions options save=allpub
```

76 L1 C1

**Fig. 7** Memory Cell Circuit Layout Netlist

- Column Decoder Circuit

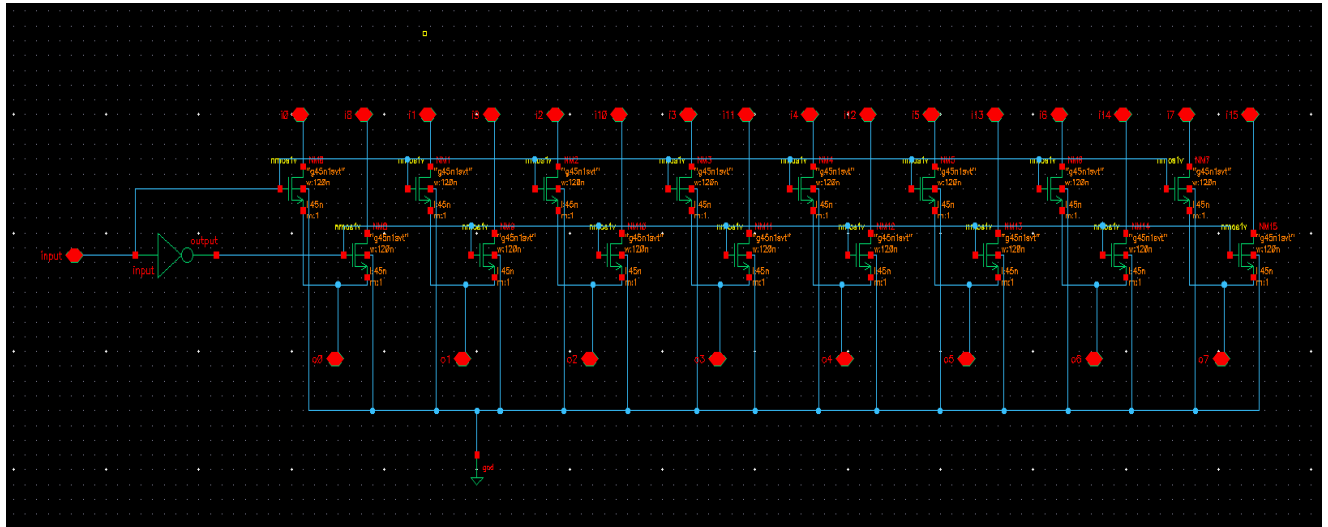


Fig. 8 Column Decoder Circuit

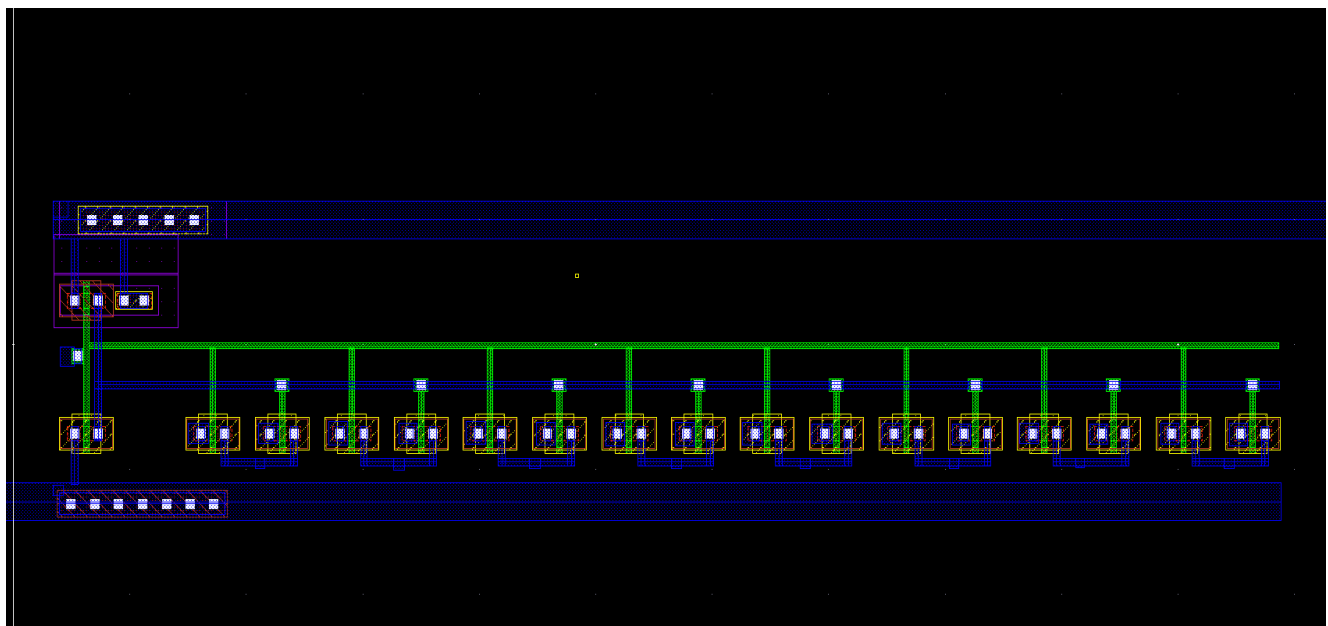
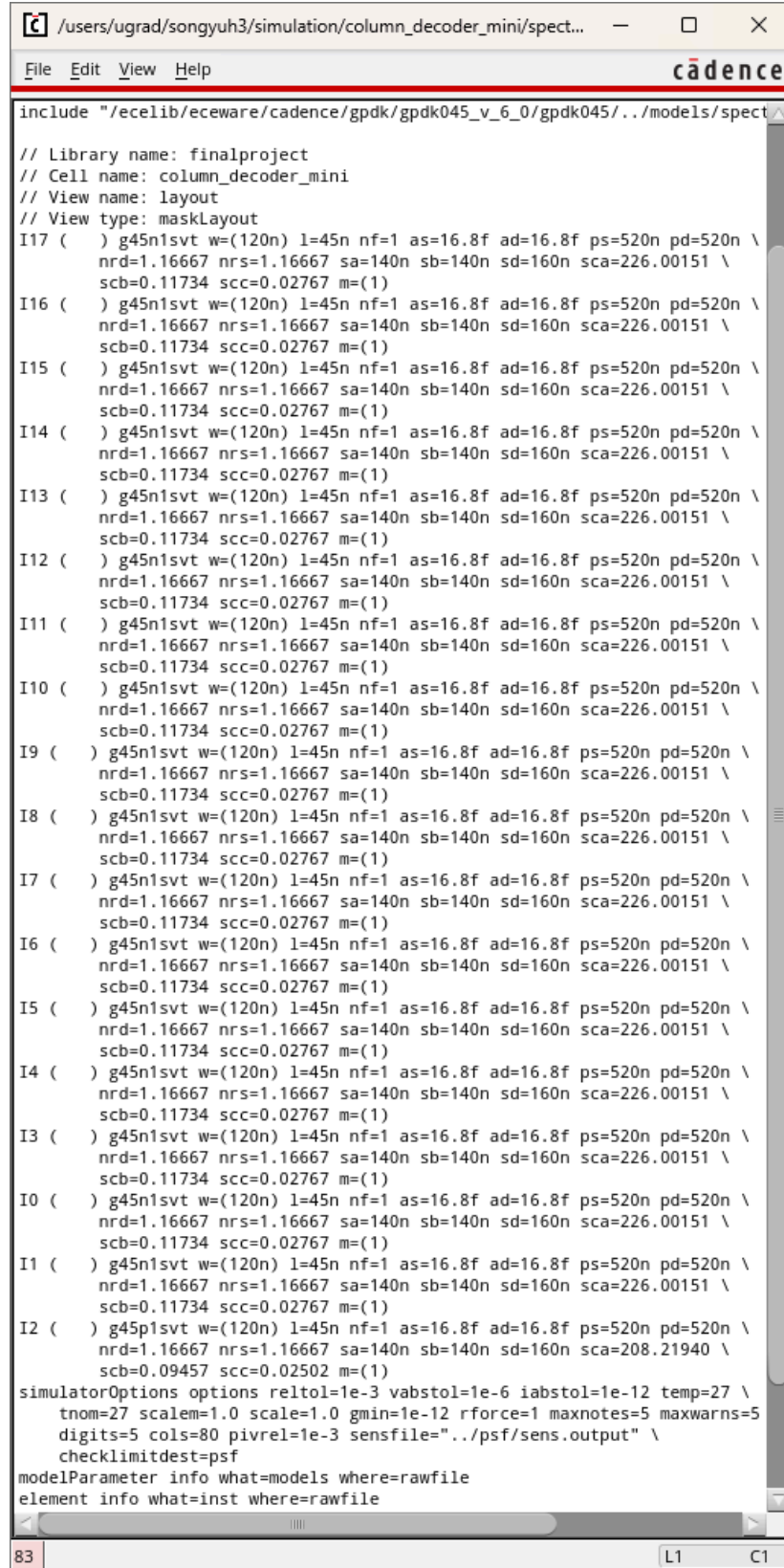


Fig. 9 Column Decoder Circuit Layout







```
include "/eceleb/eceware/cadence/gpdk/gpdk045_v_6_0/gpdk045/./models/spectra"

// Library name: finalproject
// Cell name: column_decoder_mini
// View name: layout
// View type: maskLayout
I17 ( ) g45n1svt w=(120n) l=45n nf=1 as=16.8f ad=16.8f ps=520n pd=520n \
nrd=1.16667 nrs=1.16667 sa=140n sb=140n sd=160n sca=226.00151 \
scb=0.11734 scc=0.02767 m=(1)
I16 ( ) g45n1svt w=(120n) l=45n nf=1 as=16.8f ad=16.8f ps=520n pd=520n \
nrd=1.16667 nrs=1.16667 sa=140n sb=140n sd=160n sca=226.00151 \
scb=0.11734 scc=0.02767 m=(1)
I15 ( ) g45n1svt w=(120n) l=45n nf=1 as=16.8f ad=16.8f ps=520n pd=520n \
nrd=1.16667 nrs=1.16667 sa=140n sb=140n sd=160n sca=226.00151 \
scb=0.11734 scc=0.02767 m=(1)
I14 ( ) g45n1svt w=(120n) l=45n nf=1 as=16.8f ad=16.8f ps=520n pd=520n \
nrd=1.16667 nrs=1.16667 sa=140n sb=140n sd=160n sca=226.00151 \
scb=0.11734 scc=0.02767 m=(1)
I13 ( ) g45n1svt w=(120n) l=45n nf=1 as=16.8f ad=16.8f ps=520n pd=520n \
nrd=1.16667 nrs=1.16667 sa=140n sb=140n sd=160n sca=226.00151 \
scb=0.11734 scc=0.02767 m=(1)
I12 ( ) g45n1svt w=(120n) l=45n nf=1 as=16.8f ad=16.8f ps=520n pd=520n \
nrd=1.16667 nrs=1.16667 sa=140n sb=140n sd=160n sca=226.00151 \
scb=0.11734 scc=0.02767 m=(1)
I11 ( ) g45n1svt w=(120n) l=45n nf=1 as=16.8f ad=16.8f ps=520n pd=520n \
nrd=1.16667 nrs=1.16667 sa=140n sb=140n sd=160n sca=226.00151 \
scb=0.11734 scc=0.02767 m=(1)
I10 ( ) g45n1svt w=(120n) l=45n nf=1 as=16.8f ad=16.8f ps=520n pd=520n \
nrd=1.16667 nrs=1.16667 sa=140n sb=140n sd=160n sca=226.00151 \
scb=0.11734 scc=0.02767 m=(1)
I9 ( ) g45n1svt w=(120n) l=45n nf=1 as=16.8f ad=16.8f ps=520n pd=520n \
nrd=1.16667 nrs=1.16667 sa=140n sb=140n sd=160n sca=226.00151 \
scb=0.11734 scc=0.02767 m=(1)
I8 ( ) g45n1svt w=(120n) l=45n nf=1 as=16.8f ad=16.8f ps=520n pd=520n \
nrd=1.16667 nrs=1.16667 sa=140n sb=140n sd=160n sca=226.00151 \
scb=0.11734 scc=0.02767 m=(1)
I7 ( ) g45n1svt w=(120n) l=45n nf=1 as=16.8f ad=16.8f ps=520n pd=520n \
nrd=1.16667 nrs=1.16667 sa=140n sb=140n sd=160n sca=226.00151 \
scb=0.11734 scc=0.02767 m=(1)
I6 ( ) g45n1svt w=(120n) l=45n nf=1 as=16.8f ad=16.8f ps=520n pd=520n \
nrd=1.16667 nrs=1.16667 sa=140n sb=140n sd=160n sca=226.00151 \
scb=0.11734 scc=0.02767 m=(1)
I5 ( ) g45n1svt w=(120n) l=45n nf=1 as=16.8f ad=16.8f ps=520n pd=520n \
nrd=1.16667 nrs=1.16667 sa=140n sb=140n sd=160n sca=226.00151 \
scb=0.11734 scc=0.02767 m=(1)
I4 ( ) g45n1svt w=(120n) l=45n nf=1 as=16.8f ad=16.8f ps=520n pd=520n \
nrd=1.16667 nrs=1.16667 sa=140n sb=140n sd=160n sca=226.00151 \
scb=0.11734 scc=0.02767 m=(1)
I3 ( ) g45n1svt w=(120n) l=45n nf=1 as=16.8f ad=16.8f ps=520n pd=520n \
nrd=1.16667 nrs=1.16667 sa=140n sb=140n sd=160n sca=226.00151 \
scb=0.11734 scc=0.02767 m=(1)
I0 ( ) g45n1svt w=(120n) l=45n nf=1 as=16.8f ad=16.8f ps=520n pd=520n \
nrd=1.16667 nrs=1.16667 sa=140n sb=140n sd=160n sca=226.00151 \
scb=0.11734 scc=0.02767 m=(1)
I1 ( ) g45n1svt w=(120n) l=45n nf=1 as=16.8f ad=16.8f ps=520n pd=520n \
nrd=1.16667 nrs=1.16667 sa=140n sb=140n sd=160n sca=226.00151 \
scb=0.11734 scc=0.02767 m=(1)
I2 ( ) g45p1svt w=(120n) l=45n nf=1 as=16.8f ad=16.8f ps=520n pd=520n \
nrd=1.16667 nrs=1.16667 sa=140n sb=140n sd=160n sca=208.21940 \
scb=0.09457 scc=0.02502 m=(1)
simulatorOptions options reltol=1e-3 vabstol=1e-6 iabstol=1e-12 temp=27 \
tnom=27 scalem=1.0 scale=1.0 gmin=1e-12 rforce=1 maxnotes=5 maxwarns=5
digits=5 cols=80 pivrel=1e-3 sensfile="/psf/sens.output" \
checklimitdest=psf
modelParameter info what=models where=rawfile
element info what=inst where=rawfile
```

Fig. 12 Column Decoder Circuit Layout Netlist

- Row Decoder Circuit

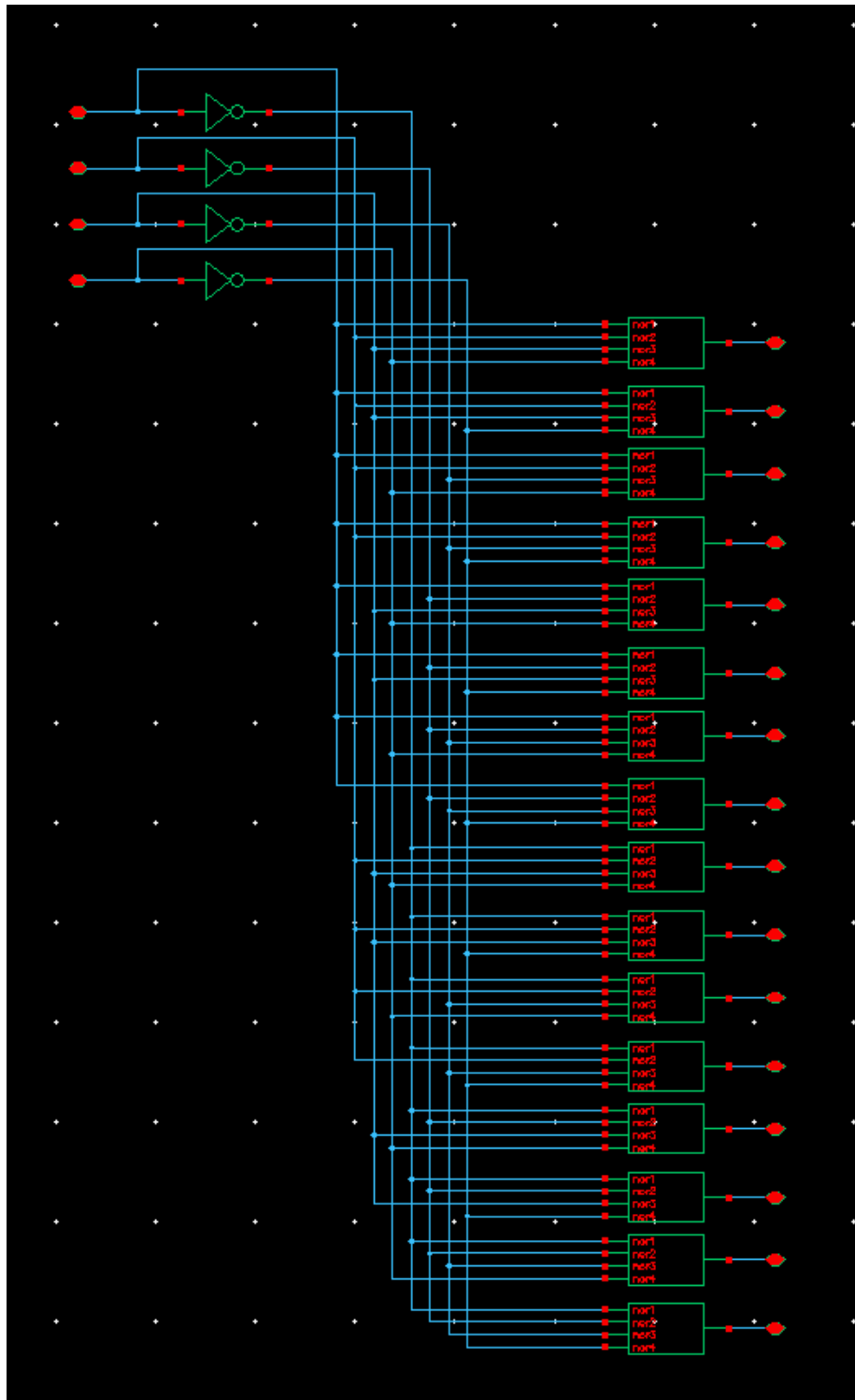
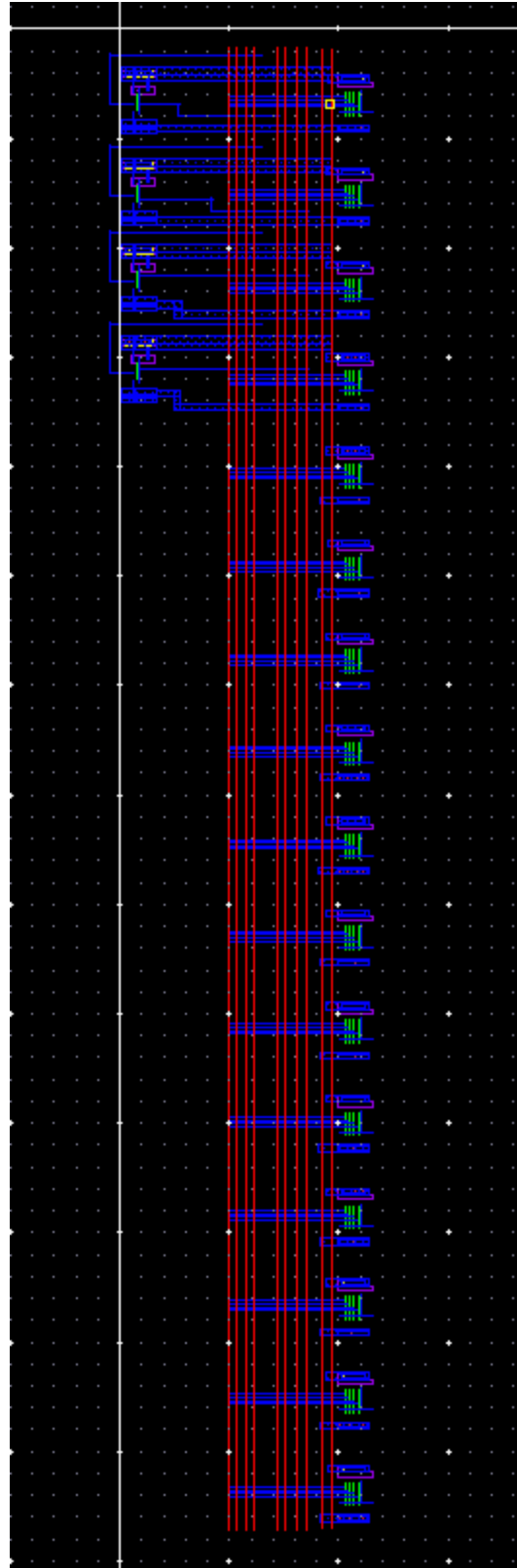
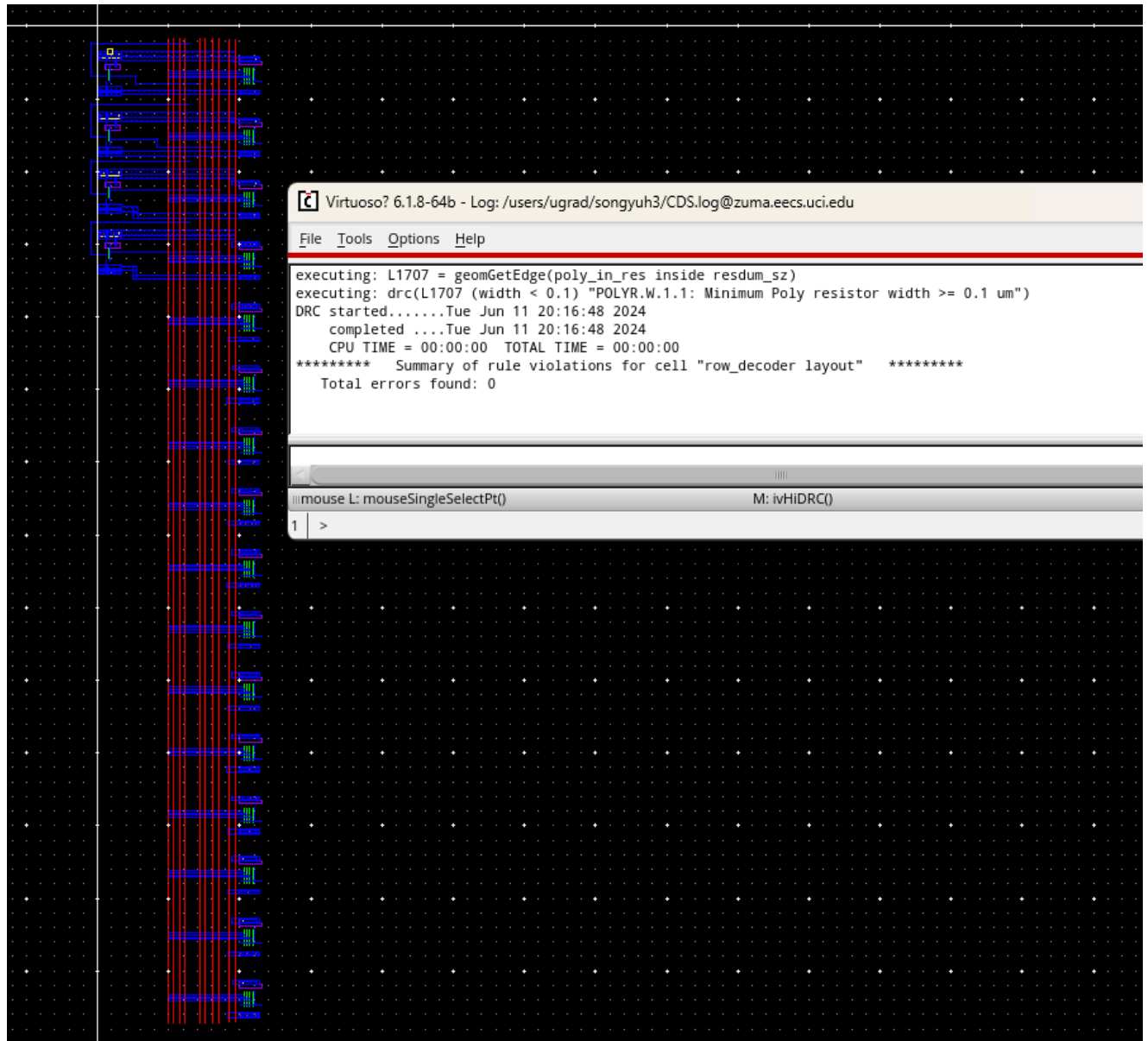


Fig. 13 Row Decoder Circuit



**Fig. 14** Row Decoder Circuit Layout



**Fig. 15** Row Decoder Circuit Layout DRC Check

```

/users/ugrad/songyuh3/EECS217/LVS/si.out@zuma.eecs.uci.edu
File Edit View Help
cadence

@(#)$CDS: LVS version 6.1.8-64b 09/22/2020 18:59 (sjfhw316) $

Command line: /ecelab/ecaware/cadence/ic618/tools.lnx86/dfII/bin/64bit/LVS -dir /users/ugrad/songyuh3/EECS217/LVS -l -s -t /users/ugrad/songyuh3/EECS217/LVS/layout /users/ugrad/songyuh3/EECS217/LVS/schematic
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.

GENERIC PDK LVS Rules

Net-list summary for /users/ugrad/songyuh3/EECS217/LVS/layout/netlist
count
74      nets
22      terminals
68      g45p1svt
68      g45n1svt

Net-list summary for /users/ugrad/songyuh3/EECS217/LVS/schematic/netlist
count
74      nets
22      terminals
68      g45p1svt
68      g45n1svt

Terminal correspondence points
N56      N10      a0
N55      N11      a1
N54      N12      a2
N53      N13      a3
N52      N1      gnd1
N73      N0       vdda!
N66      N5       w0
N65      N8       w1
N72      N20      w10
N71      N21      w11
N70      N22      w12
N69      N23      w13
N68      N24      w14
N67      N25      w15
N64      N3       w2
N63      N2       w3
N62      N14      w4
N61      N15      w5
N60      N16      w6
N59      N17      w7
N58      N18      w8
N57      N19      w9

Devices in the netlist but not in the rules:
g45p1svt g45n1svt
Devices in the rules but not in the netlist:
g45pd1lvt g45nd1hvt g45nd1lvt g45nd1nvt g45nd2svt g45nd2nvt g45pd1hvt
g45pd2svt g45rm1 g45rm2 g45rm3 g45rm4 g45rm5 g45rm6 g45rm7 g45rm8
g45rm9 g45rm10 g45rm11 g45rnsnd g45rnsnp g45rnsdp g45rnspp g45rnwoxide
g45rnwsti g45rsnd g45rsnp g45rspd g45rspp g45ncap1 g45ncap2 g45pcap1
g45pcap2 pnp npn g45vnpn2 g45vnpn5 g45vnpn10 g45vnpn2 g45vnpn5
g45vnpn10 g45nd1svt g45pd1svt g45cmim g45inda g45inds

The net-lists match.

          layout schematic
          instances
un-matched      0      0
rewired         0      0
size errors     0      0
pruned          0      0

```

**Fig. 16** Row Decoder Circuit Layout LVS Check

```

/users/ugrad/songyuh3/simulation/row_decoder/spectre/schematic/netlist...
File Edit View Help cadence

// View name: schematic
subckt _sub1 nor1 nor2 nor3 nor4 out
NM3 (out nor3 0 0) g45n1svt w=(120n) l=45n nf=1 as=16.8f ad=16.8f \
ps=520n pd=520n nrd=1.16667 nrs=1.16667 sa=140n sb=140n sd=160n \
sca=226.00151 scb=0.11734 scc=0.02767 m=(1)
NM2 (out nor4 0 0) g45n1svt w=(120n) l=45n nf=1 as=16.8f ad=16.8f \
ps=520n pd=520n nrd=1.16667 nrs=1.16667 sa=140n sb=140n sd=160n \
sca=226.00151 scb=0.11734 scc=0.02767 m=(1)
NM1 (out nor2 0 0) g45n1svt w=(120n) l=45n nf=1 as=16.8f ad=16.8f \
ps=520n pd=520n nrd=1.16667 nrs=1.16667 sa=140n sb=140n sd=160n \
sca=226.00151 scb=0.11734 scc=0.02767 m=(1)
NM0 (out nor1 0 0) g45n1svt w=(120n) l=45n nf=1 as=16.8f ad=16.8f \
ps=520n pd=520n nrd=1.16667 nrs=1.16667 sa=140n sb=140n sd=160n \
sca=226.00151 scb=0.11734 scc=0.02767 m=(1)
PM3 (net2 nor1 vdda! vdda!) g45p1svt w=(120n) l=45n nf=1 as=16.8f \
ad=16.8f ps=520n pd=520n nrd=1.16667 nrs=1.16667 sa=140n sb=140n \
sd=160n sca=226.00151 scb=0.11734 scc=0.02767 m=(1)
PM2 (net3 nor2 net2 vdda!) g45p1svt w=(120n) l=45n nf=1 as=16.8f \
ad=16.8f ps=520n pd=520n nrd=1.16667 nrs=1.16667 sa=140n sb=140n \
sd=160n sca=226.00151 scb=0.11734 scc=0.02767 m=(1)
PM1 (net4 nor3 net3 vdda!) g45p1svt w=(120n) l=45n nf=1 as=16.8f \
ad=16.8f ps=520n pd=520n nrd=1.16667 nrs=1.16667 sa=140n sb=140n \
sd=160n sca=226.00151 scb=0.11734 scc=0.02767 m=(1)
PM0 (out nor4 net4 vdda!) g45p1svt w=(120n) l=45n nf=1 as=16.8f \
ad=16.8f ps=520n pd=520n nrd=1.16667 nrs=1.16667 sa=140n sb=140n \
sd=160n sca=226.00151 scb=0.11734 scc=0.02767 m=(1)
ends _sub1
// End of subcircuit definition.

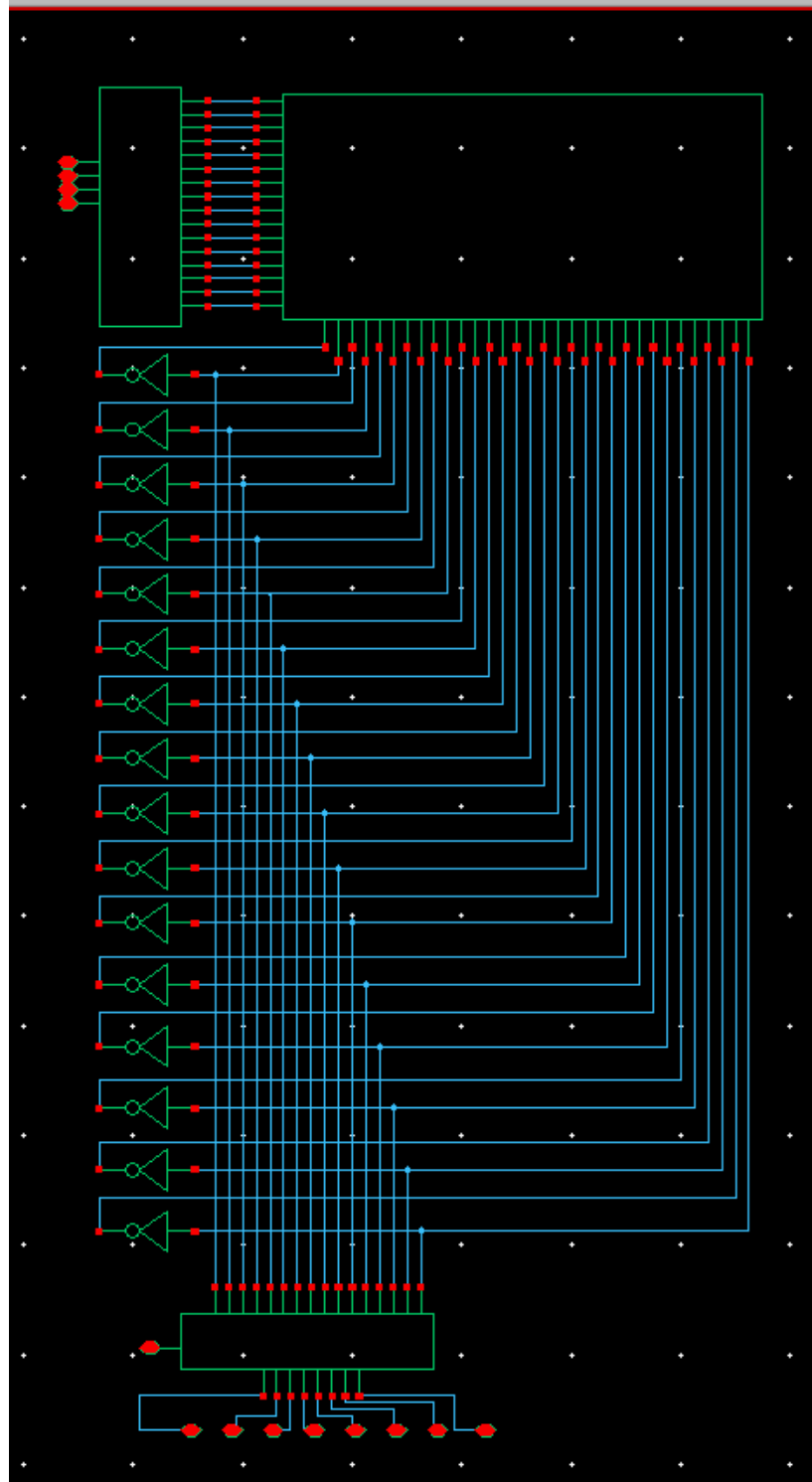
// Library name: finalproject
// Cell name: inverter
// View name: schematic
subckt inverter _net1 _net0
M1 (_net0 _net1 0 0) g45n1svt w=(120n) l=45n nf=1 as=16.8f ad=16.8f \
ps=520n pd=520n nrd=1.16667 nrs=1.16667 sa=140n sb=140n sd=160n \
sca=226.00151 scb=0.11734 scc=0.02767 m=(1)
PM0 (_net0 _net1 vdda! vdda!) g45p1svt w=(120n) l=45n nf=1 as=16.8f \
ad=16.8f ps=520n pd=520n nrd=1.16667 nrs=1.16667 sa=140n sb=140n \
sd=160n sca=226.00151 scb=0.11734 scc=0.02767 m=(1)
ends inverter
// End of subcircuit definition.

// Library name: finalproject
// Cell name: row_decoder
// View name: schematic
I15 (net8 net6 net3 net5 w15) _sub1
I14 (net8 net6 net3 a3 w14) _sub1
I13 (net8 net6 a2 net5 w13) _sub1
I12 (net8 net6 a2 a3 w12) _sub1
I11 (net8 a1 net3 net5 w11) _sub1
I10 (net8 a1 net3 a3 w10) _sub1
I9 (net8 a1 a2 net5 w9) _sub1
I8 (net8 a1 a2 a3 w8) _sub1
I7 (a0 net6 net3 net5 w7) _sub1
I6 (a0 net6 net3 a3 w6) _sub1
I5 (a0 net6 a2 net5 w5) _sub1
I4 (a0 net6 a2 a3 w4) _sub1
I3 (a0 a1 net3 net5 w3) _sub1
I2 (a0 a1 net3 a3 w2) _sub1
I1 (a0 a1 a2 net5 w1) _sub1
I0 (a0 a1 a2 a3 w0) _sub1
I19 (a3 net5) inverter
I18 (a2 net3) inverter
I17 (a1 net6) inverter
I16 (a0 net8) inverter
simulatorOptions options reltol=1e-3 vabstol=1e-6 iabstol=1e-12 temp=27 \

```

Fig. 17 Row Decoder Circuit Layout Netlist

c. **Finished Circuit**



**Fig. 18** Finished circuit

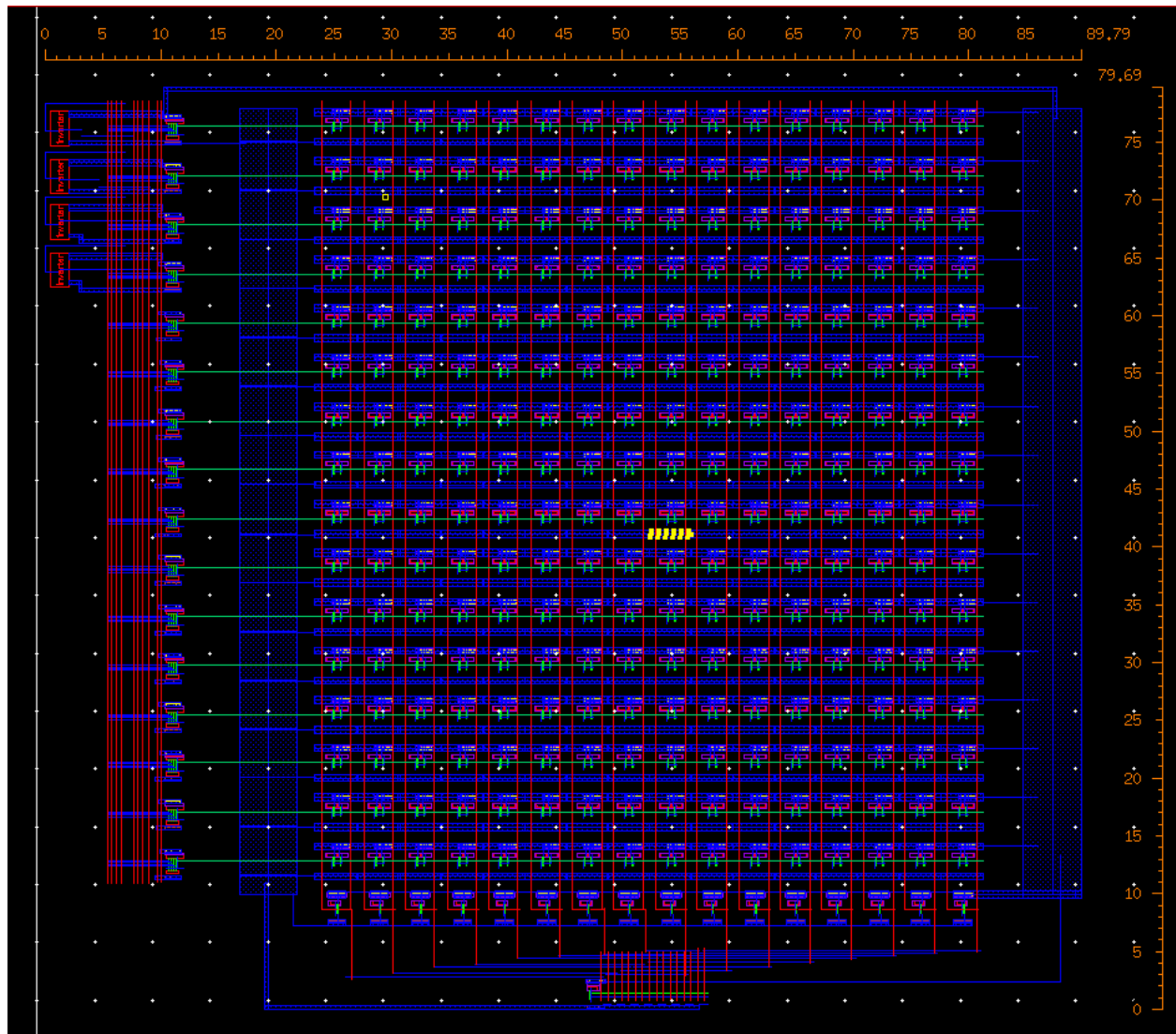
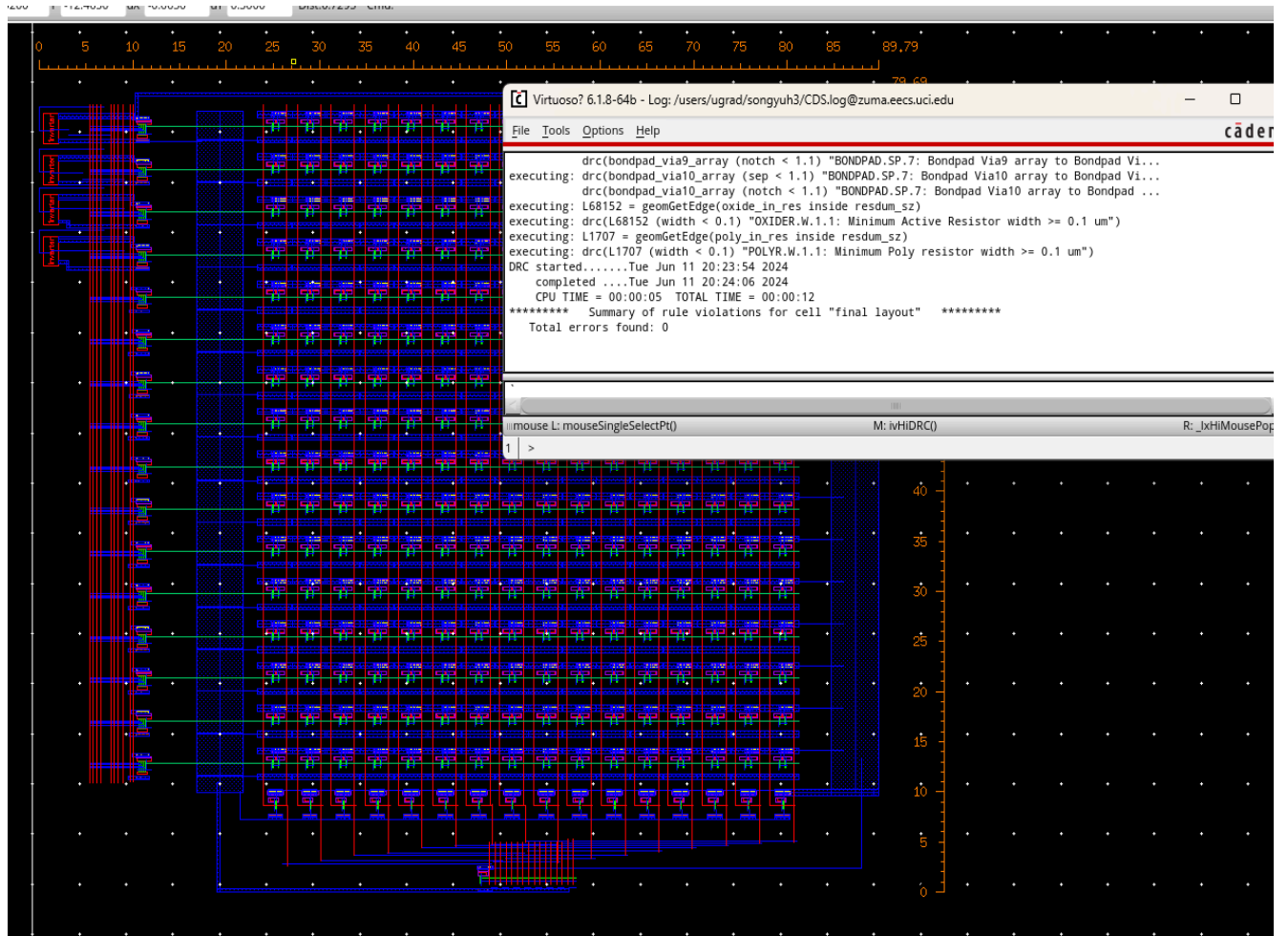


Fig. 19 Finished circuit Layout





**Fig. 20** Finished circuit Layout DRC Check

```

/users/ugrad/songyuh3/EECS217/LVS/si.out@zuma.eecs.uci.edu
File Edit View Help
cadence

Command line: /ecelab/ceaware/cadence/ic618/tools.lnx86/dftI/bin/64bit/LVS -dir /users/ugrad/songyuh3/EECS217/LVS -l -s -t /users/ugrad/songyuh3/EECS217/LVS/layout /users/ugrad/songyuh3/EECS217/LVS/schematic
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.

GENERIC PDK LVS Rules

Net-list summary for /users/ugrad/songyuh3/EECS217/LVS/layout/netlist
count
628      nets
15       terminals
597      g45plsvt
1125     g45nlsvt

Net-list summary for /users/ugrad/songyuh3/EECS217/LVS/schematic/netlist
count
628      nets
15       terminals
597      g45plsvt
1125     g45nlsvt

Terminal correspondence points
N618    N45    a0
N617    N39    a1
N616    N38    a2
N615    N37    a3
N613    N1     gnd!
N614    N41    input
N626    N36    o0
N625    N35    o1
N624    N34    o2
N623    N33    o3
N622    N40    o4
N621    N42    o5
N620    N43    o6
N619    N44    o7
N627    N0     vdda!

Devices in the netlist but not in the rules:
g45plsvt g45nlsvt
Devices in the rules but not in the netlist:
g45pd1lvt g45nd1hvt g45nd1lvt g45nd1nvt g45nd2svt g45nd2nvt g45pd1hvt
g45pd2svt g45rm1 g45rm2 g45rm3 g45rm4 g45rm5 g45rm6 g45rm7 g45rm8
g45rm9 g45rm10 g45rm11 g45rnsnd g45rnsnp g45rnsdp g45rnspp g45rnwoxide
g45rnwsti g45rsnd g45rsnp g45rspd g45rspp g45ncap1 g45ncap2 g45pcap1
g45pcap2 pnp npn g45vnpn2 g45vnpn5 g45vnpn10 g45vnpn2 g45vnpn5
g45vnpn10 g45nd1svt g45pd1svt g45cmim g45inda g45inds

The net-lists match.

          layout schematic
          instances
un-matched      0      0
rewired          0      0
size errors     0      0
pruned          0      0
active          1722   1722
total           1722   1722

          nets
un-matched      0      0
merged          0      0
pruned          0      0
active          628   628
total           628   628

```

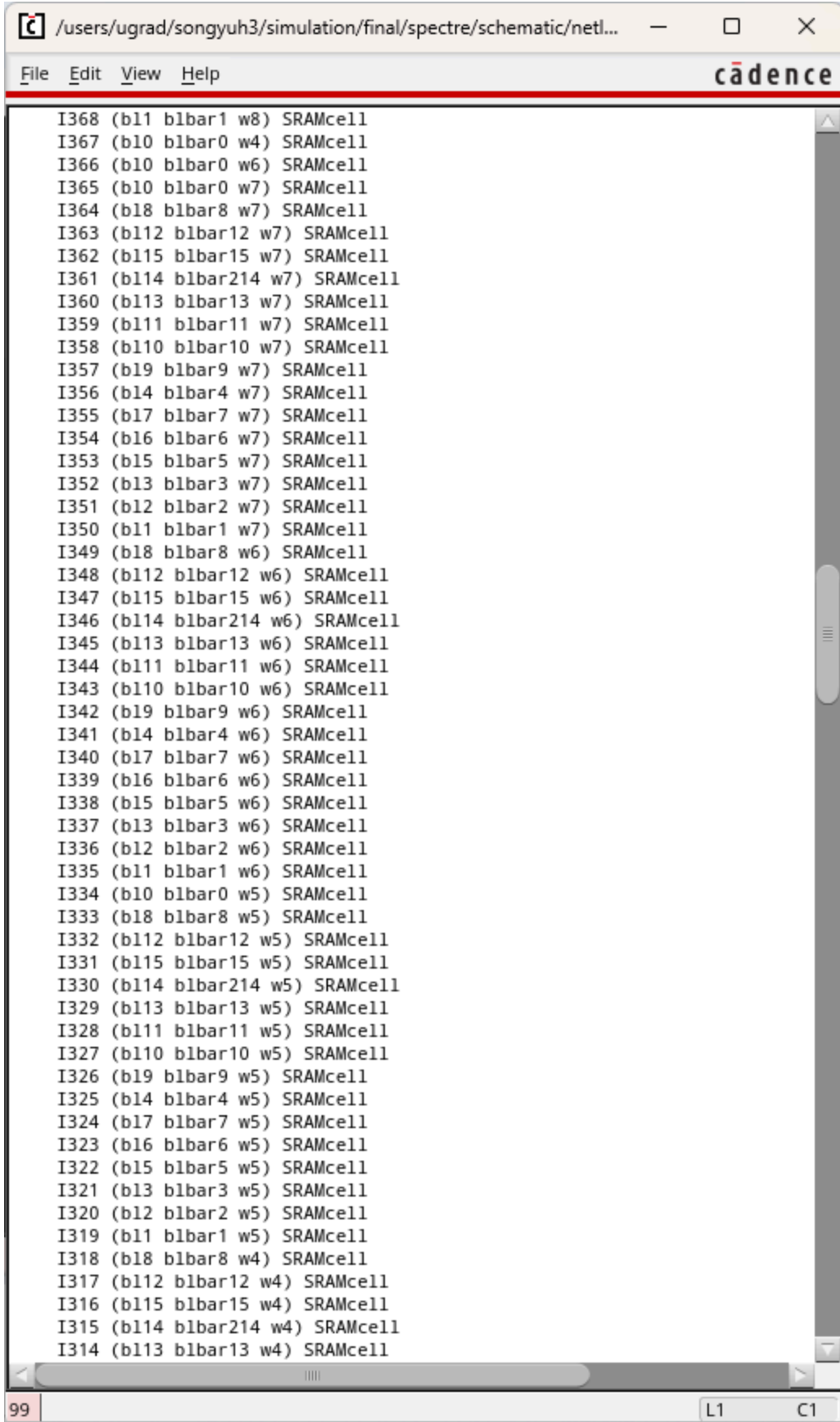
Fig. 21 Finished circuit Layout LVS Check

```
/users/ugrad/songyuh3/simulation/final/spectre/schematic/netl...
File Edit View Help cadence

// Design view name: schematic
simulator lang=spectre
global 0 vdda!
include "/ecelib/eceware/cadence/gpdk/gpdk045_v_6_0/gpdk045/./models/spectre

// Library name: finalproject
// Cell name: SRAMcell
// View name: schematic
subckt SRAMcell BL BLbar WL
  NM3 (BLbar WL net2 0) g45n1svt w=(120n) l=45n nf=1 as=16.8f ad=16.8f \
    ps=520n pd=520n nrd=1.16667 nrs=1.16667 sa=140n sb=140n sd=160n \
    sca=226.00151 scb=0.11734 scc=0.02767 m=(1)
  NM2 (BL WL net1 0) g45n1svt w=(120n) l=45n nf=1 as=16.8f ad=16.8f \
    ps=520n pd=520n nrd=1.16667 nrs=1.16667 sa=140n sb=140n sd=160n \
    sca=226.00151 scb=0.11734 scc=0.02767 m=(1)
  NM1 (net1 net2 0 0) g45n1svt w=(120n) l=45n nf=1 as=16.8f ad=16.8f \
    ps=520n pd=520n nrd=1.16667 nrs=1.16667 sa=140n sb=140n sd=160n \
    sca=226.00151 scb=0.11734 scc=0.02767 m=(1)
  NM0 (net2 net1 0 0) g45n1svt w=(120n) l=45n nf=1 as=16.8f ad=16.8f \
    ps=520n pd=520n nrd=1.16667 nrs=1.16667 sa=140n sb=140n sd=160n \
    sca=226.00151 scb=0.11734 scc=0.02767 m=(1)
  PM1 (net1 net2 vdda! vdda!) g45p1svt w=(120n) l=45n nf=1 as=16.8f \
    ad=16.8f ps=520n pd=520n nrd=1.16667 nrs=1.16667 sa=140n sb=140n \
    sd=160n sca=226.00151 scb=0.11734 scc=0.02767 m=(1)
  PM0 (net2 net1 vdda! vdda!) g45p1svt w=(120n) l=45n nf=1 as=16.8f \
    ad=16.8f ps=520n pd=520n nrd=1.16667 nrs=1.16667 sa=140n sb=140n \
    sd=160n sca=226.00151 scb=0.11734 scc=0.02767 m=(1)
ends SRAMcell
// End of subcircuit definition.

// Library name: finalproject
// Cell name: 16x16
// View name: schematic
subckt finalproject_16x16_schematic b10 b11 b110 b111 b112 b113 b114 b115 \
  b12 b13 b14 b15 b16 b17 b18 b19 blbar0 blbar1 blbar10 blbar11 \
  blbar12 blbar13 blbar15 blbar2 blbar214 blbar3 blbar4 blbar5 \
  blbar6 blbar7 blbar8 blbar9 w0 w1 w10 w11 w12 w13 w14 w15 w2 w3 w4
  w5 w6 w7 w8 w9
  I495 (b10 blbar0 w8) SRAMcell
  I494 (b10 blbar0 w12) SRAMcell
  I493 (b10 blbar0 w14) SRAMcell
  I492 (b10 blbar0 w15) SRAMcell
  I491 (b18 blbar8 w15) SRAMcell
  I490 (b112 blbar12 w15) SRAMcell
  I489 (b115 blbar15 w15) SRAMcell
  I488 (b114 blbar214 w15) SRAMcell
  I487 (b113 blbar13 w15) SRAMcell
  I486 (b111 blbar11 w15) SRAMcell
  I485 (b110 blbar10 w15) SRAMcell
  I484 (b19 blbar9 w15) SRAMcell
  I483 (b14 blbar4 w15) SRAMcell
  I482 (b17 blbar7 w15) SRAMcell
  I481 (b16 blbar6 w15) SRAMcell
  I480 (b15 blbar5 w15) SRAMcell
  I479 (b13 blbar3 w15) SRAMcell
```



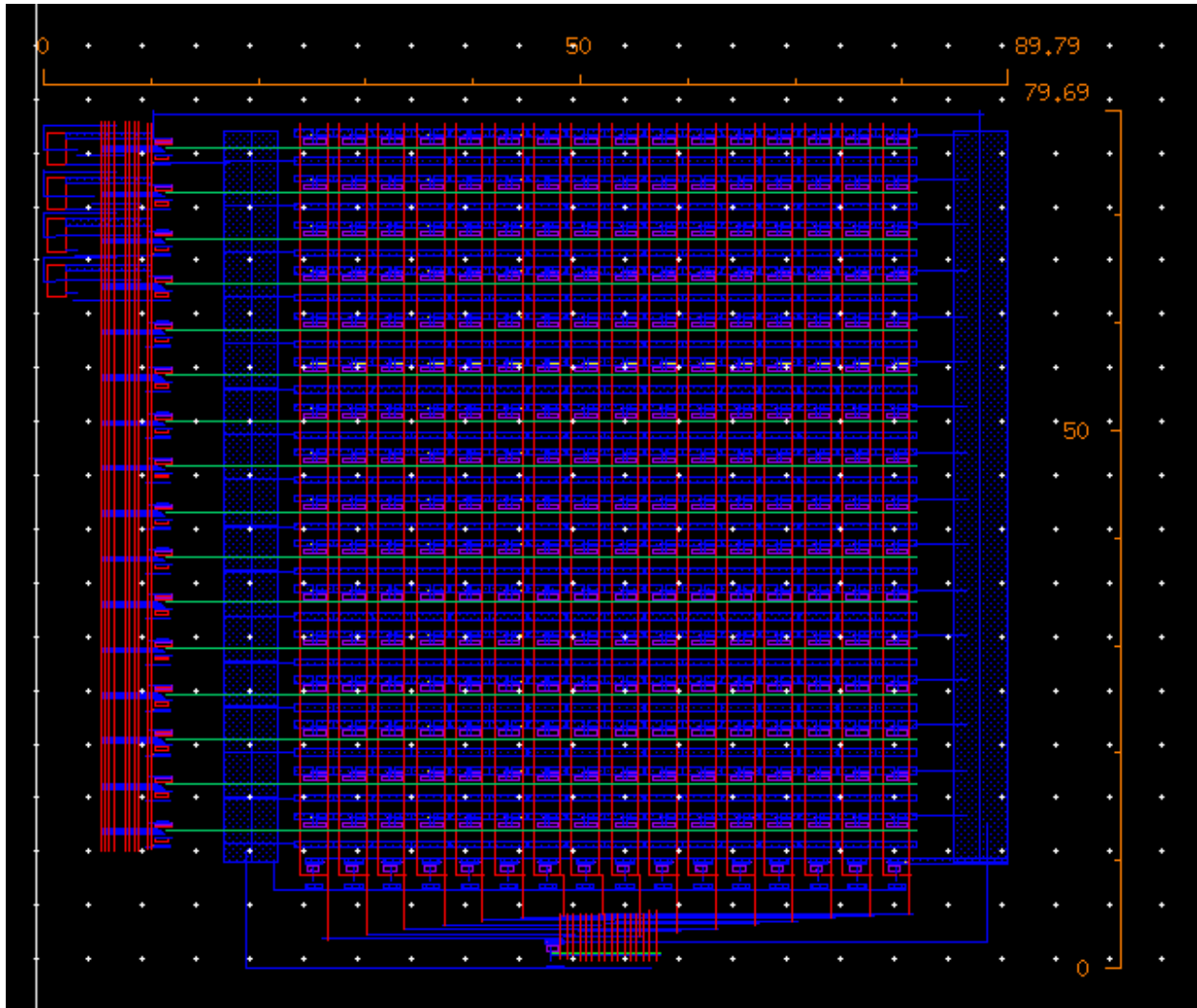
```
sca=226.00151 scb=0.11734 scc=0.02767 m=(1)
NM14 (i14 net6 o6 0) g45n1svt w=(120n) l=45n nf=1 as=16.8f ad=16.8f \
ps=520n pd=520n nrd=1.16667 nrs=1.16667 sa=140n sb=140n sd=160n \
sca=226.00151 scb=0.11734 scc=0.02767 m=(1)
NM13 (i13 net6 o5 0) g45n1svt w=(120n) l=45n nf=1 as=16.8f ad=16.8f \
ps=520n pd=520n nrd=1.16667 nrs=1.16667 sa=140n sb=140n sd=160n \
sca=226.00151 scb=0.11734 scc=0.02767 m=(1)
NM12 (i12 net6 o4 0) g45n1svt w=(120n) l=45n nf=1 as=16.8f ad=16.8f \
ps=520n pd=520n nrd=1.16667 nrs=1.16667 sa=140n sb=140n sd=160n \
sca=226.00151 scb=0.11734 scc=0.02767 m=(1)
NM11 (i11 net6 o3 0) g45n1svt w=(120n) l=45n nf=1 as=16.8f ad=16.8f \
ps=520n pd=520n nrd=1.16667 nrs=1.16667 sa=140n sb=140n sd=160n \
sca=226.00151 scb=0.11734 scc=0.02767 m=(1)
NM10 (i10 net6 o2 0) g45n1svt w=(120n) l=45n nf=1 as=16.8f ad=16.8f \
ps=520n pd=520n nrd=1.16667 nrs=1.16667 sa=140n sb=140n sd=160n \
sca=226.00151 scb=0.11734 scc=0.02767 m=(1)
NM9 (i9 net6 o1 0) g45n1svt w=(120n) l=45n nf=1 as=16.8f ad=16.8f \
ps=520n pd=520n nrd=1.16667 nrs=1.16667 sa=140n sb=140n sd=160n \
sca=226.00151 scb=0.11734 scc=0.02767 m=(1)
NM7 (i7 _net2 o7 0) g45n1svt w=(120n) l=45n nf=1 as=16.8f ad=16.8f \
ps=520n pd=520n nrd=1.16667 nrs=1.16667 sa=140n sb=140n sd=160n \
sca=226.00151 scb=0.11734 scc=0.02767 m=(1)
NM6 (i6 _net2 o6 0) g45n1svt w=(120n) l=45n nf=1 as=16.8f ad=16.8f \
ps=520n pd=520n nrd=1.16667 nrs=1.16667 sa=140n sb=140n sd=160n \
sca=226.00151 scb=0.11734 scc=0.02767 m=(1)
NM5 (i5 _net2 o5 0) g45n1svt w=(120n) l=45n nf=1 as=16.8f ad=16.8f \
ps=520n pd=520n nrd=1.16667 nrs=1.16667 sa=140n sb=140n sd=160n \
sca=226.00151 scb=0.11734 scc=0.02767 m=(1)
NM4 (i4 _net2 o4 0) g45n1svt w=(120n) l=45n nf=1 as=16.8f ad=16.8f \
ps=520n pd=520n nrd=1.16667 nrs=1.16667 sa=140n sb=140n sd=160n \
sca=226.00151 scb=0.11734 scc=0.02767 m=(1)
NM3 (i3 _net2 o3 0) g45n1svt w=(120n) l=45n nf=1 as=16.8f ad=16.8f \
ps=520n pd=520n nrd=1.16667 nrs=1.16667 sa=140n sb=140n sd=160n \
sca=226.00151 scb=0.11734 scc=0.02767 m=(1)
NM2 (i2 _net2 o2 0) g45n1svt w=(120n) l=45n nf=1 as=16.8f ad=16.8f \
ps=520n pd=520n nrd=1.16667 nrs=1.16667 sa=140n sb=140n sd=160n \
sca=226.00151 scb=0.11734 scc=0.02767 m=(1)
NM1 (i1 _net2 o1 0) g45n1svt w=(120n) l=45n nf=1 as=16.8f ad=16.8f \
ps=520n pd=520n nrd=1.16667 nrs=1.16667 sa=140n sb=140n sd=160n \
sca=226.00151 scb=0.11734 scc=0.02767 m=(1)
NM8 (i8 net6 o0 0) g45n1svt w=(120n) l=45n nf=1 as=16.8f ad=16.8f \
ps=520n pd=520n nrd=1.16667 nrs=1.16667 sa=140n sb=140n sd=160n \
sca=226.00151 scb=0.11734 scc=0.02767 m=(1)
NM0 (i0 _net2 o0 0) g45n1svt w=(120n) l=45n nf=1 as=16.8f ad=16.8f \
ps=520n pd=520n nrd=1.16667 nrs=1.16667 sa=140n sb=140n sd=160n \
sca=226.00151 scb=0.11734 scc=0.02767 m=(1)
I2 (_net2 net6) inverter
ends column_decoder_mini
// End of subcircuit definition.

// Library name: finalproject
// Cell name: 4-nor
// View name: schematic
subckt _sub2 nor1 nor2 nor3 nor4 out
NM3 (out nor3 0 0) g45n1svt w=(120n) l=45n nf=1 as=16.8f ad=16.8f \
```

Fig. 22 Finished circuit Layout Netlist

**d. Floor Plan of SRAM and dimension of each block**

- SRAM dimension



**Fig. 23** Finished Circuit Layout Dimension

- 

**Fig. 24** Each memory cell dimension

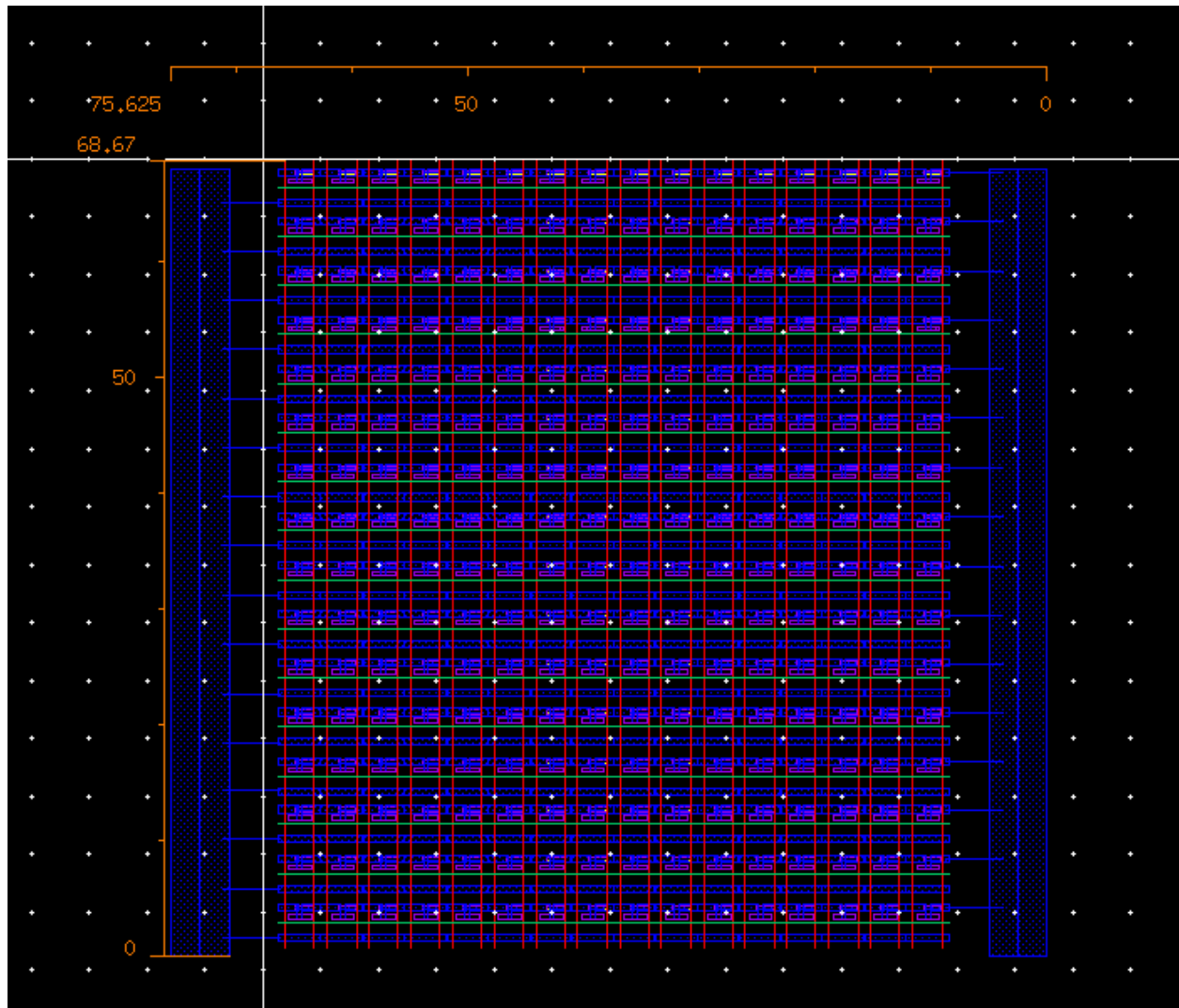


Fig. 25 16\*16 memory cell block dimension



- Row decoder block dimension

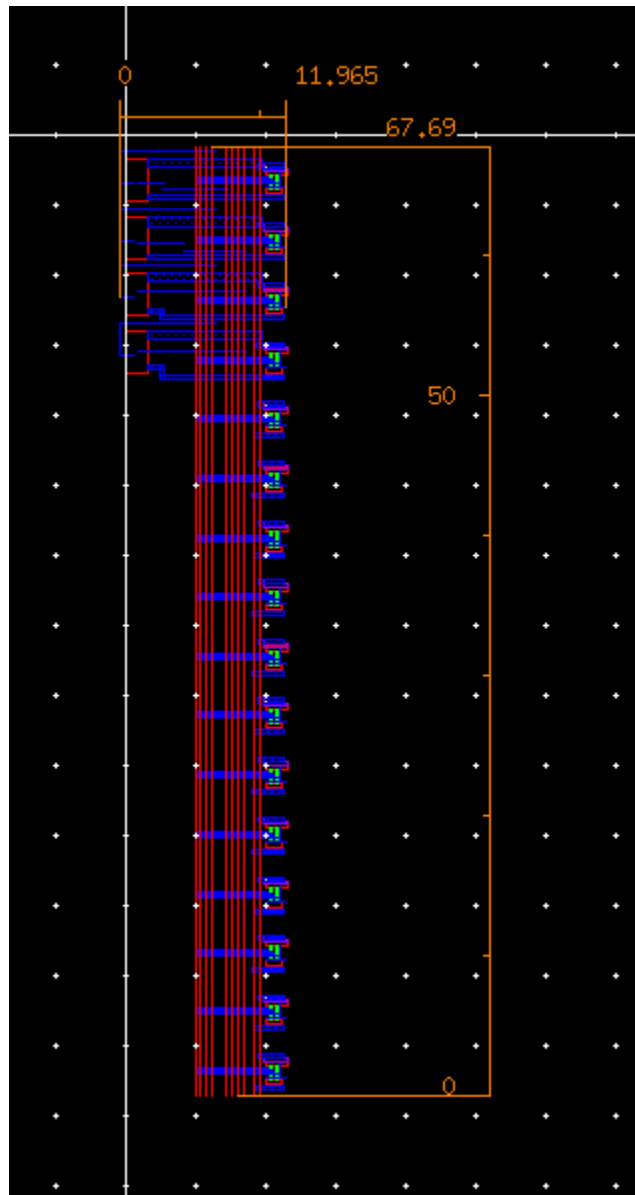


Fig. 26 Row decoder block dimension

- Column decoder block dimension

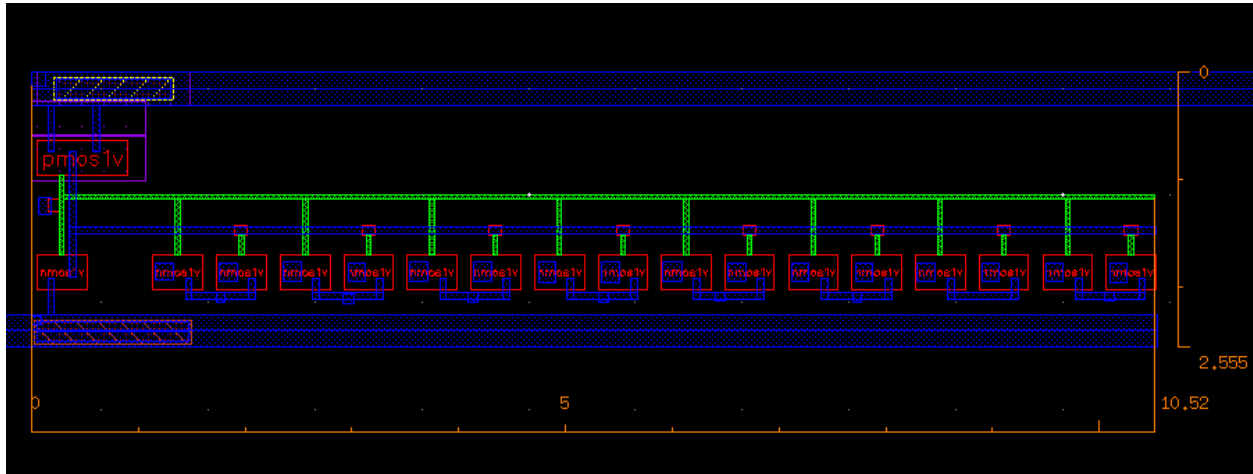


Fig. 27 Column decoder block dimension

## 2. Simulation result

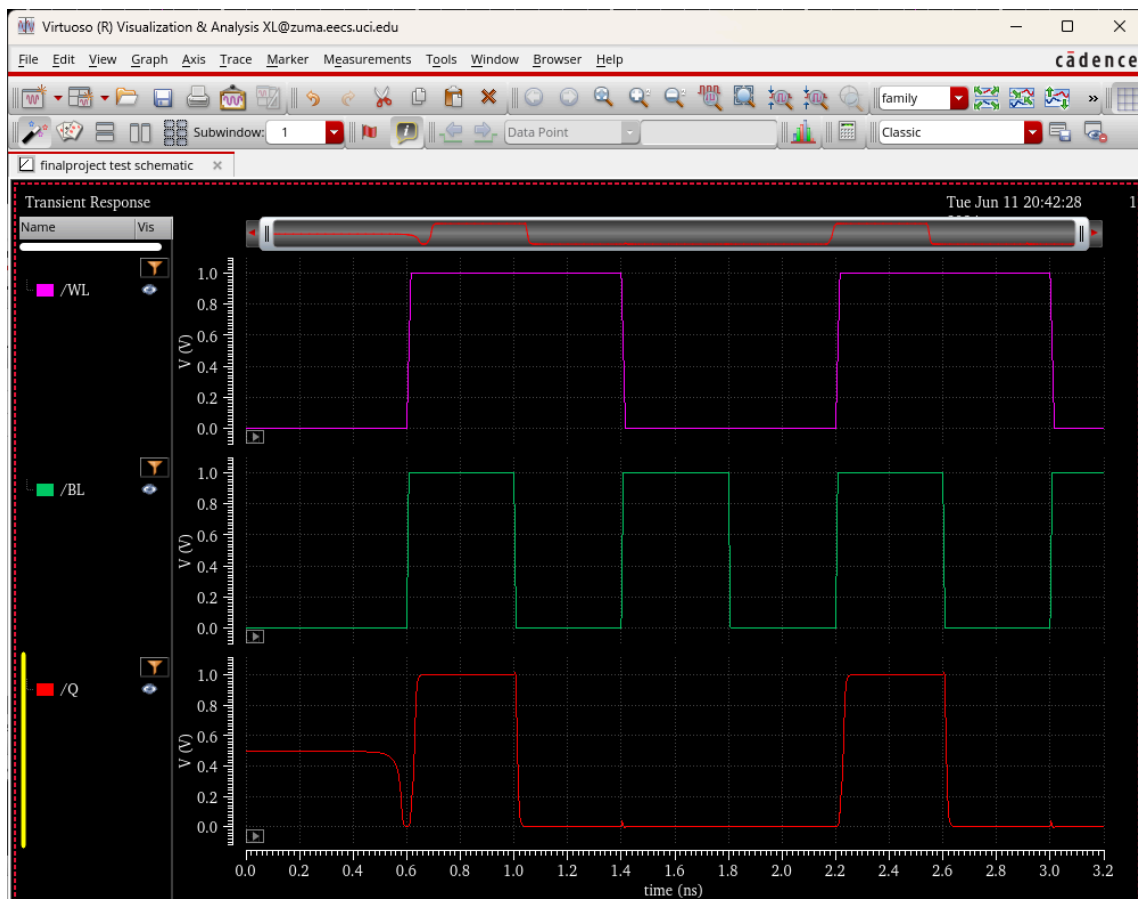


Fig. 28 Working waveform (1->0)

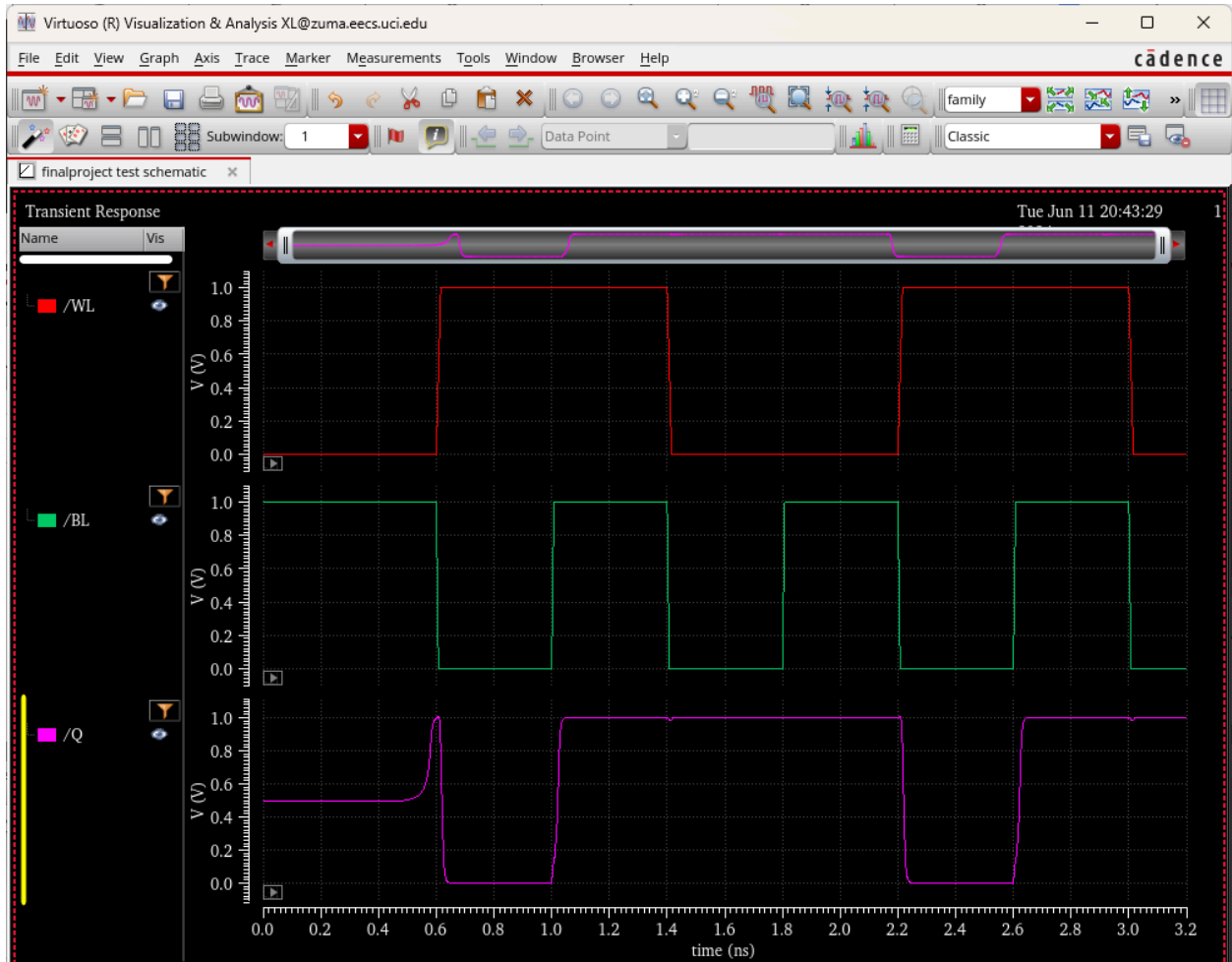
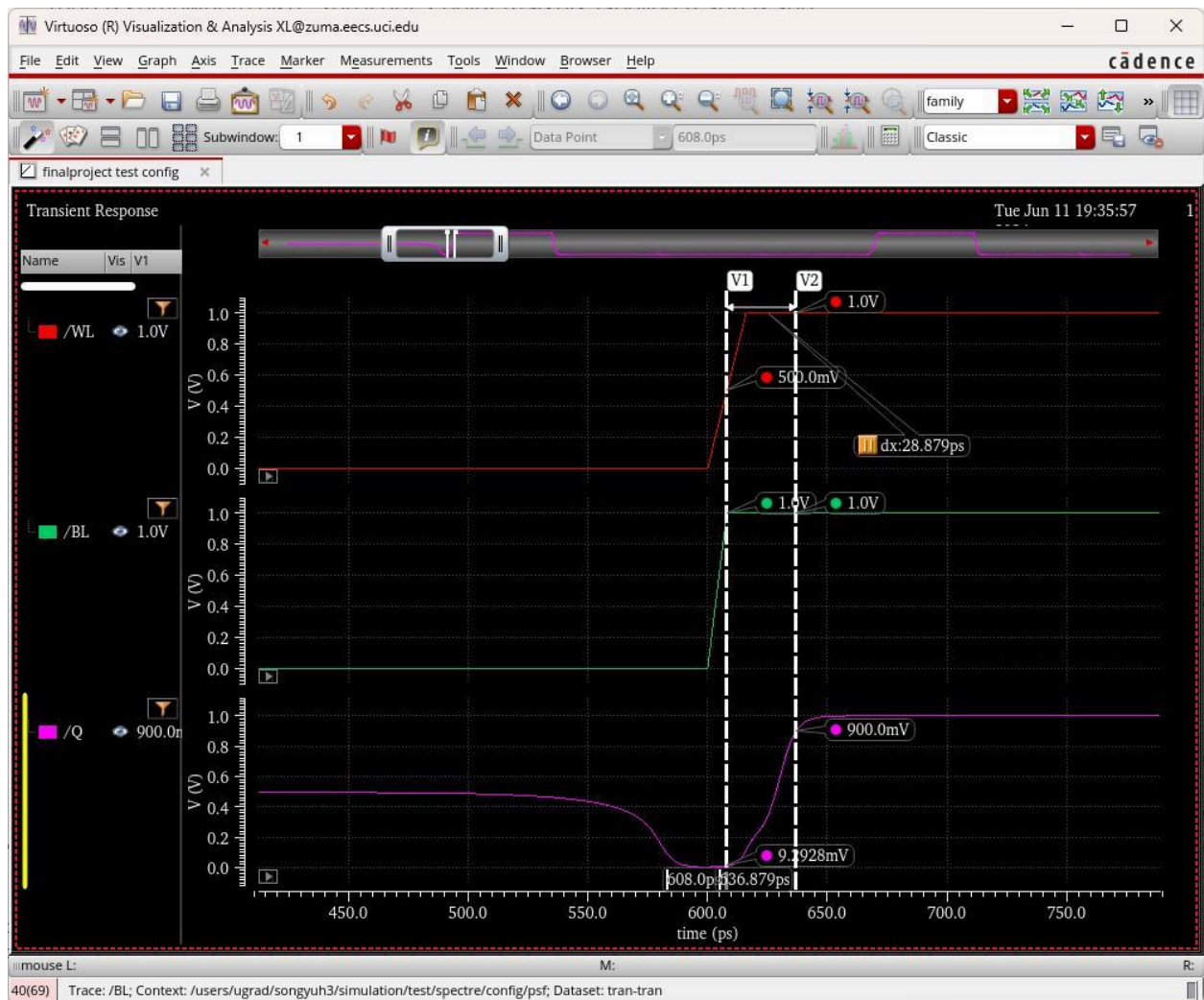


Fig. 29 Working waveform (0->1)



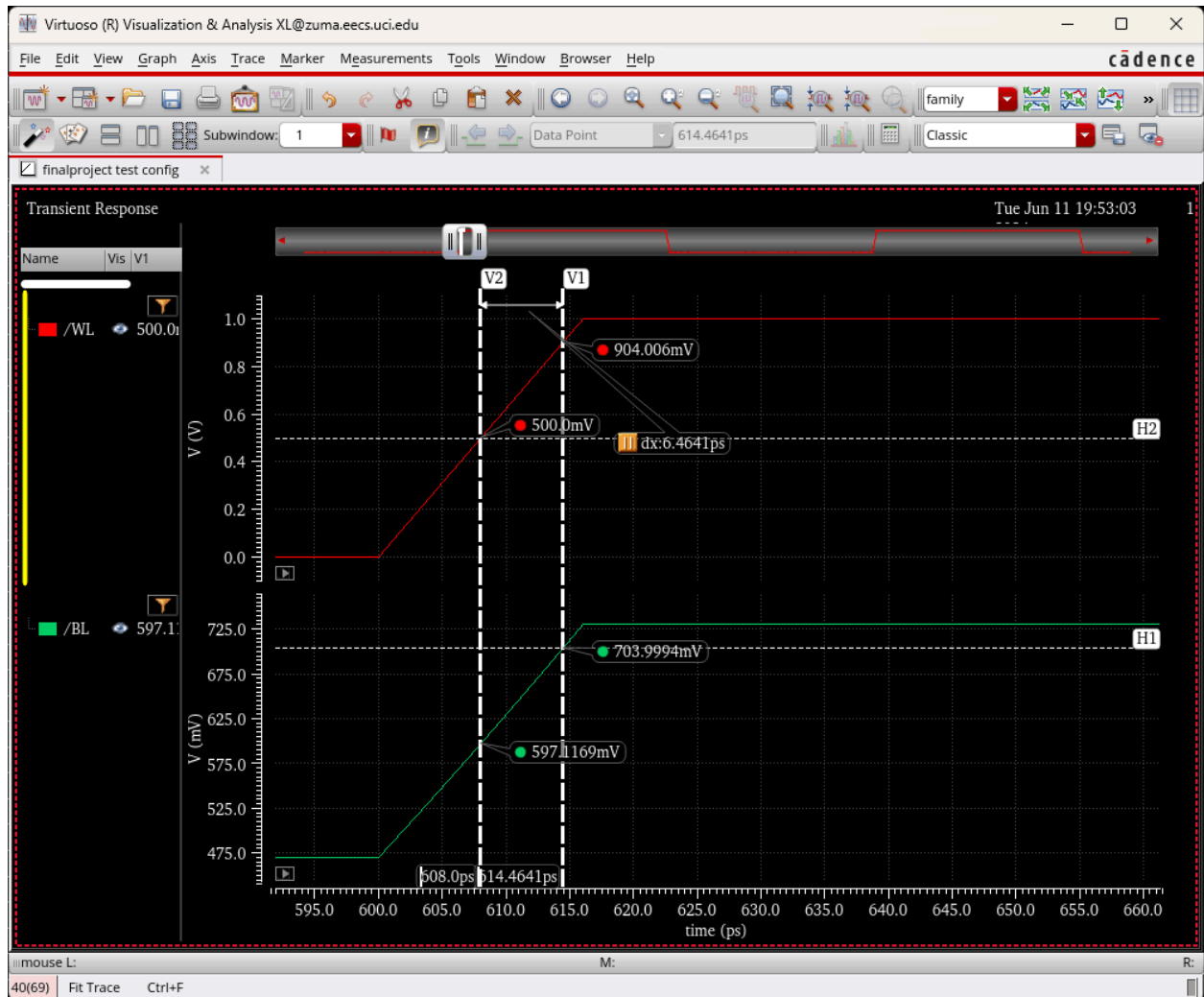


Fig. 30 Extracted Simulation result

#### 4. Design Strategy and Description

##### a. Goals

##### Memory Cell Design

- **6-Transistor CMOS SR Flip Flop:** The memory cell design is based on a 6-transistor (6T) CMOS static RAM (SRAM) flip-flop. This configuration provides a good balance of stability, speed, and power consumption.

### Memory Organization

- **Array Structure:** The memory cells are organized in a 16x2 bytes (or 16 rows x 16 columns) rectangular array. This structure provides 256 bits of storage.

### Address Decoding

- **Row Decoder:** The row decoder addresses the 16 wordlines, each corresponding to a row in the memory array.
- **Column Decoder:** The column decoder addresses the 16 columns, each column being 1 bit wide.

### Memory Cell Sizing

- **Performance, Power, Area Optimization:** The memory cell should be optimized for performance, power consumption, and area. It must operate correctly in both read and write modes.

## b. Description and Calculations

### Read / Write time

The read and write time are measured in **Fig. 30**. The write time is approximately 28.879ps, and the read time is approximately 6.4641ps.

### Component Area Size

Components	Length / $\mu\text{m}$	Width / $\mu\text{m}$	Area / $\mu\text{m}^2$
SRAM Cell	4.375	3.695	16.1656
Row Decoder	67.69	11.965	809.9109
Column Decoder	2.555	10.52	26.8786
16x16 Memory Block	79.69	89.79	7155.3651