Hardware information to be used in driver.

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1. Device Address Mapping

A. (Debug) Direct Access to BRAM memory

0x40000000 - 0x40000FFF : BRAM 1

0x40001000 - 0x40001FFF : BRAM 2

0x40002000 - 0x40002FFF : BRAM 3

0x40003000 - 0x40003FFF : BRAM 4

B. Write Packet Register to switch Port

0x80000014 : Write Packet to Port 1

0x80001014 : Write Packet to Port 2

0x80002014 : Write Packet to Port 3

0x80003014 : Write Packet to Port 4

C. Read Response Register (after read request) from switch Port

0x8000001C : Read from Port 1

0x8000101C : Read from Port 2

0x8000201C : Read from Port 3

0x8000301C : Read from Port 4

D. Read the total packets passed from port

0x80000024 : Read from Port 1

0x80001024 : Read from Port 2

0x80002024 : Read from Port 3

0x80003024 : Read from Port 4

E. Read the dropped packets (due to Fifo full error) from port

0x8000002C : Read from Port 1

0x8000102C : Read from Port 2

0x8000202C : Read from Port 3

0x8000302C : Read from Port 4

F. Read the dropped packets (due firewall rule) from port

0x80000034 : Read from Port 1

0x80001034 : Read from Port 2

0x80002034 : Read from Port 3

0x80003034 : Read from Port 4

G. Firewall Setup address Mapping for switch ports

0x50000014 : Setup Firewall Lower Address Range Register for port 1

0x5000001C : Setup Firewall Lower Address Range Register for port 2

0x50000024 : Setup Firewall Lower Address Range Register for port 3

0x5000002C : Setup Firewall Lower Address Range Register for Port 4

0x50000034 : Setup Firewall Upper Address Range Register for port 1

0x5000003C : Setup Firewall Upper Address Range Register for port 2

0x50000044 : Setup Firewall Upper Address Range Register for port 3

0x5000004C : Setup Firewall Upper Address Range Register for Port 4

0x50000054 : Setup Firewall Rule Register for port 1

0x5000005C : Setup Firewall Rule Register for port 2

0x50000064 : Setup Firewall Rule Register for port 3

0x5000006C : Setup Firewall Rule Register for Port 4

H. Debug Firewall Interface (will be removed in production)

0x50001014 : Firewall Upper Address Range Register for port 1

0x5000101C : Firewall Upper Address Range Register for port 2

0x50001024 : Firewall Upper Address Range Register for port 3

0x5000102C : Firewall Upper Address Range Register for Port 4

0x50001034 : Firewall Lower Address Range Register for port 1

0x5000103C : Firewall Lower Address Range Register for port 2

0x50001044 : Firewall Lower Address Range Register for port 3

0x5000104C : Firewall Lower Address Range Register for Port 4

0x50001054 : Firewall Rule Register for port 1

0x5000105C : Firewall Rule Register for port 2

0x50001064 : Firewall Rule Register for port 3

0x5000106C : Firewall Rule Register for Port 4

2. Registers Structure

A. Firewall Registers when Firewall operating in simple mode

- Input port

- Upper Address Register

[31:0] : Upper physical Address for the Firewall Rule

- Lower Address Register

[31:0] : Lower physical Address for the Firewall Rule

- Rule Register

[31:8] : Unused

[7] : Value set to 1 to enable the Rule

[6] : Value set to 0 to operate in compatibility mode

[5] : Value set to 1 to enable rule for Write operations

[4] : Value set to 1 to enable rule for Read operations

[3:0] : Unused

B. Firewall Registers when Firewall operating in NoC mode

-input port

- Upper Address Register

[31:10] : must be set to 0x0 value

[9:0] : Upper Address offeset for the Firewall Rule

- Lower Address Register

[31:10] : must be set to 0x0 value

[9:0] : Lower Address offeset for the Firewall Rule

- Rule Register

[31:8] : Unused

[7] : Value set to 1 to enable the Rule

[6] : Value set to 1 to operate in NoC mode

[5] : Value set to 1 to enable rule for Write operations

[4] : Value set to 1 to enable rule for Read operations

[3] : Value set to 1 to enable rule for output port 4 (BRAM 4)

[2] : Value set to 1 to enable rule for output port 3 (BRAM 3)

[1] : Value set to 1 to enable rule for output port 2 (BRAM 2)

[0] : Value set to 1 to enable rule for output Port 1 (BRAM 1)

C. Switch Input Port Packet Structure (Write Packet Register)

[31:22] : Address Offset

[21:20] : Operation Code:

0x0 for write operation

0x1 for read operation

[19:18] : Unused (internal is used for the Source Port id)

[17:16] : Destination Port address:

0x0 for output port 1

0x1 for output port 2

0x2 for output port 3

0x3 for output Port 4

[15:0] : Packet payload (small int) →command value 16 bit

D. Switch Responce Port Packet Structure (Responce Register)

[31] : Pending Read flag. Is set to 1 while fetching result and 0

when result is ready or packet was firewalled

[30:16] : Unused

[15:0] : Packet payload (small int)