Protecting Low Voltage ADC from High Voltage Amp

TI Precision Labs – ADCs

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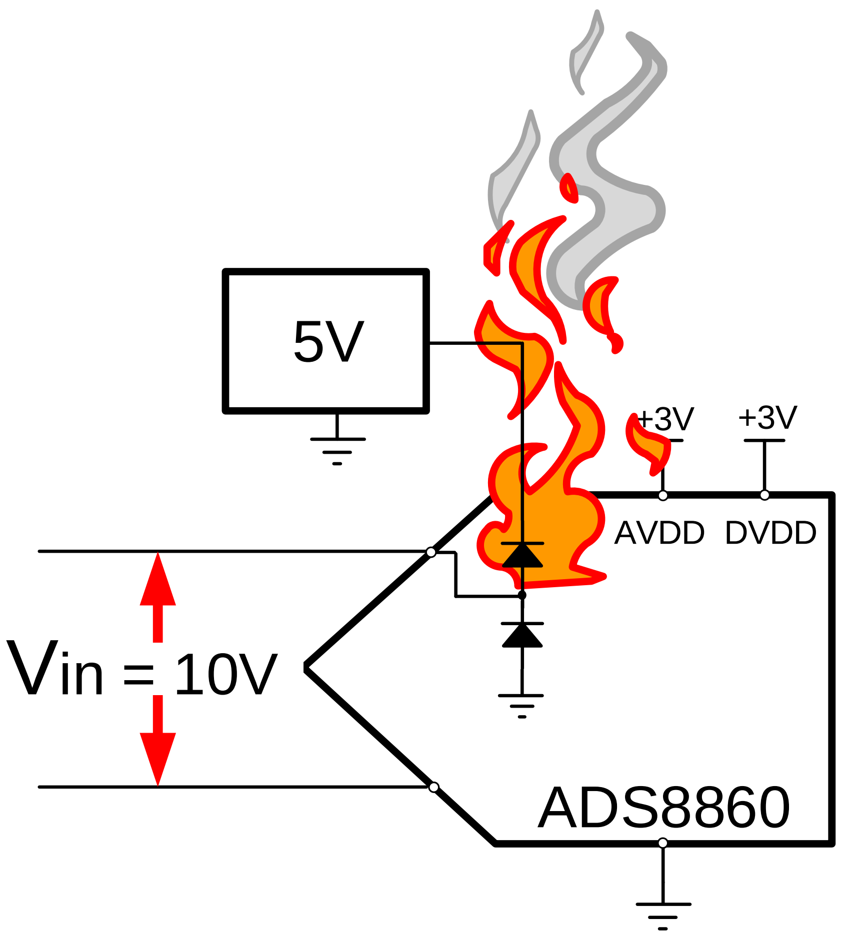
Prepared by Dale Li

Absolute Maximum Ratings – Data Converters

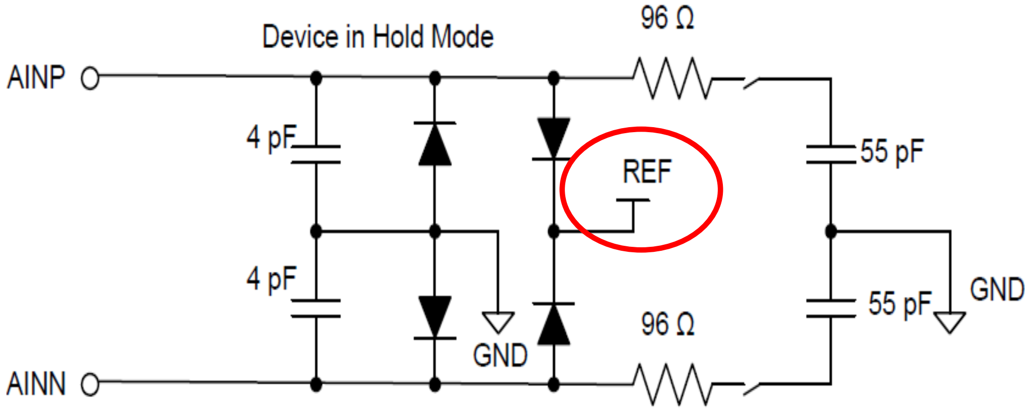
- Absolute Maximum (Abs Max) Ratings represent the voltage/current ratings. Exceeding these ratings may damage the device
- Exceeding Abs Max ratings can also degrade device reliability and cause permanent degradation in performance
- Abs Max Ratings are at or beyond linear operating conditions
- Input protection schemes should ensure that the device is not exposed to conditions that exceed the Abs Max Ratings



Abs Max Ratings - Input Voltage

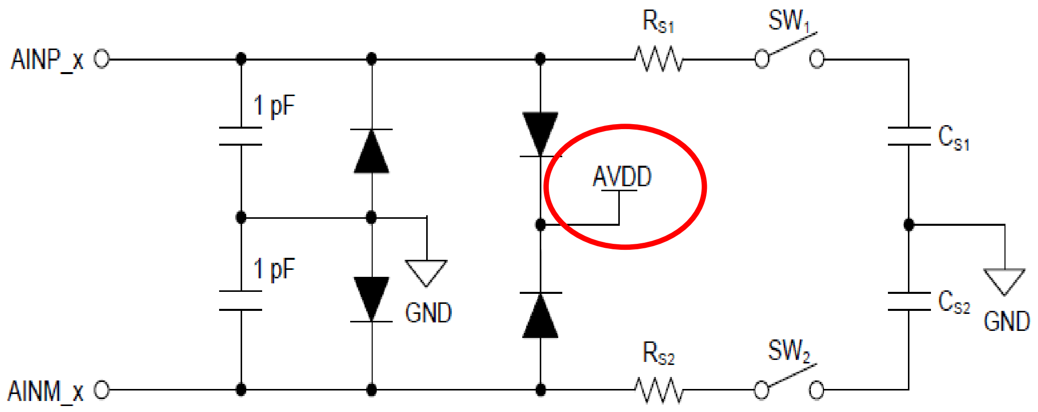
ADS8860:

Absolute Maximum Ratings	MIN	MAX	UNIT
AINP to GND or AINN to GND	-0.3	REF+0.3	V
AVDD to GND or DVDD to GND	-0.3	4	V
REF to GND	-0.3	5.7	V
Digital Input Voltage to GND	-0.3	DVDD+0.3	V
Digital Output to GND	-0.3	DVDD+0.3	V



ADS9224R:

Absolute Maximum Ratings	MIN	MAX	UNIT
AINP to GND or AINM to GND	-0.3	AVDD+0.3	V
AVDD to GND	-0.3	6	V
DVDD to GND	-0.3	6	V
Digital Input Voltage	-0.3	DVDD+0.3	V
Input or Output Current	-10	+10	mA



(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *electrical characteristics* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Abs Max Ratings - Current Limit

ADS8588S:

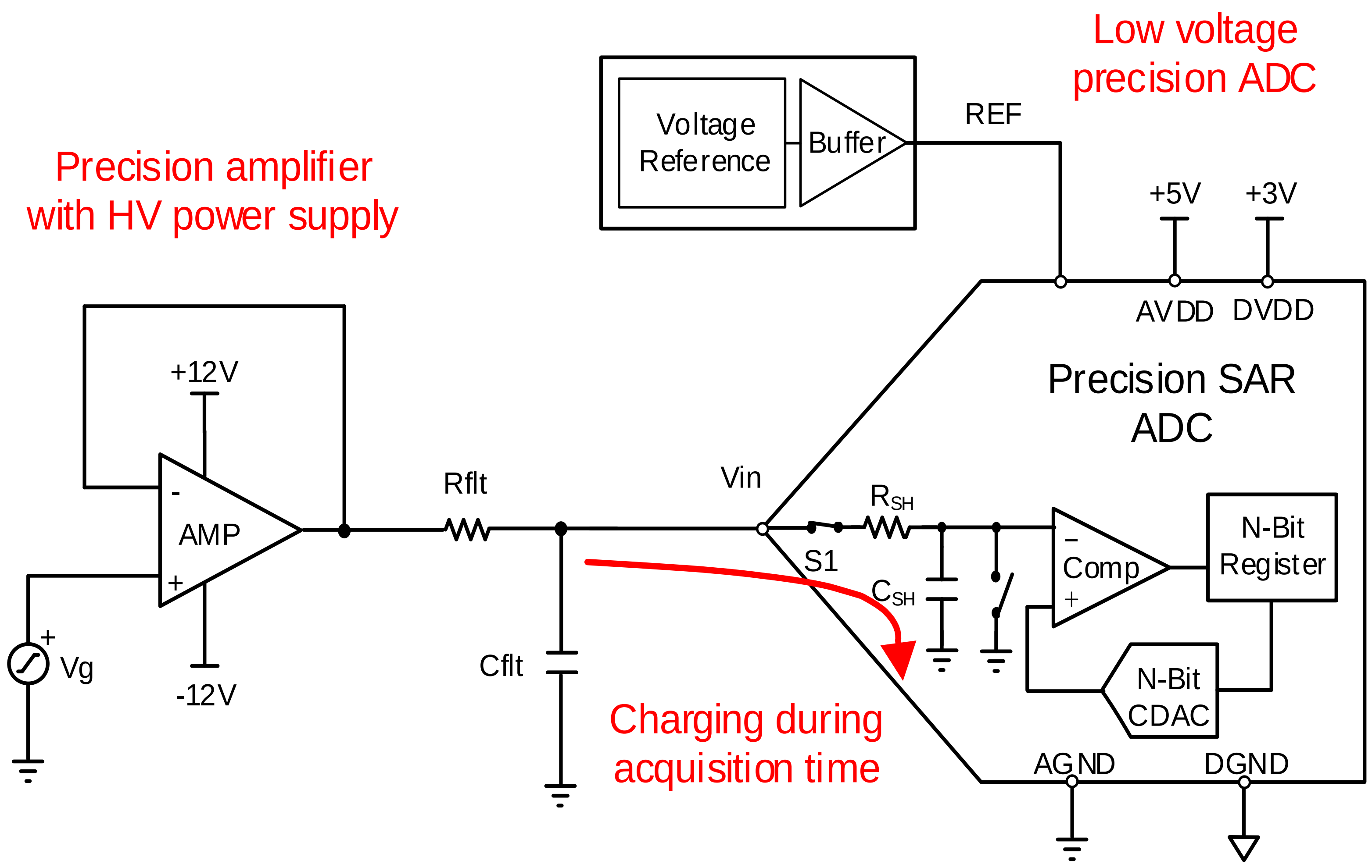
Absolute Maximum Ratings	MIN	MAX	UNIT
Analog Input Voltage to AGND	-15	+15	V
AVDD(DVDD) to AGND(DGND)	-0.3	7	V
REFIN to AGND	-0.3	AVDD+0.3	V
Digital Input to DGND	-0.3	DVDD+0.3	V
Input or Output Current	**-10**	**+10**	**mA**

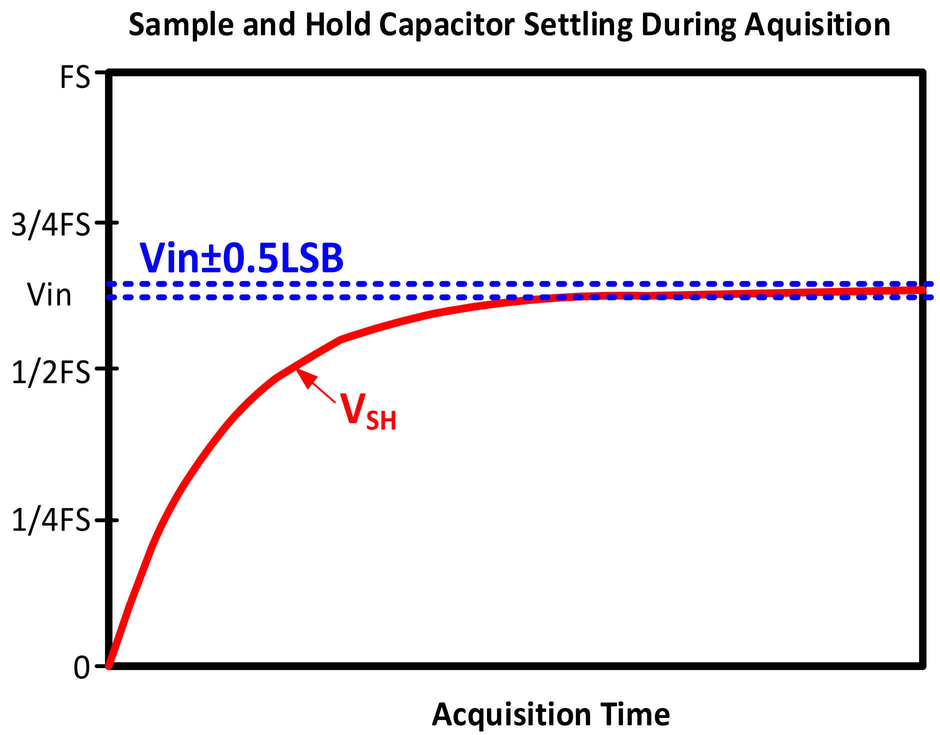
ADS9224R:

Absolute Maximum Ratings	MIN	MAX	UNIT
AINP to GND or AINM to GND	-0.3	AVDD+0.3	V
AVDD to GND	-0.3	6	V
DVDD to GND	-0.3	6	V
Digital Input Voltage	-0.3	DVDD+0.3	V
Input or Output Current	**-10**	**+10**	**mA**

- Limiting input current to be less than 10mA with a margin is recommended
- Resistance(R) in series with the inputs can limit the input current and protect the ADC
- Larger value R can make device safer and reduce the chance of a Latch-up event, and help to clamp overvoltage input signal with external protection diodes
- Larger value R may affect signal settling on C_{SH} for Switched-capacitor Input ADCs

Common Data Acquisition System in industrial application



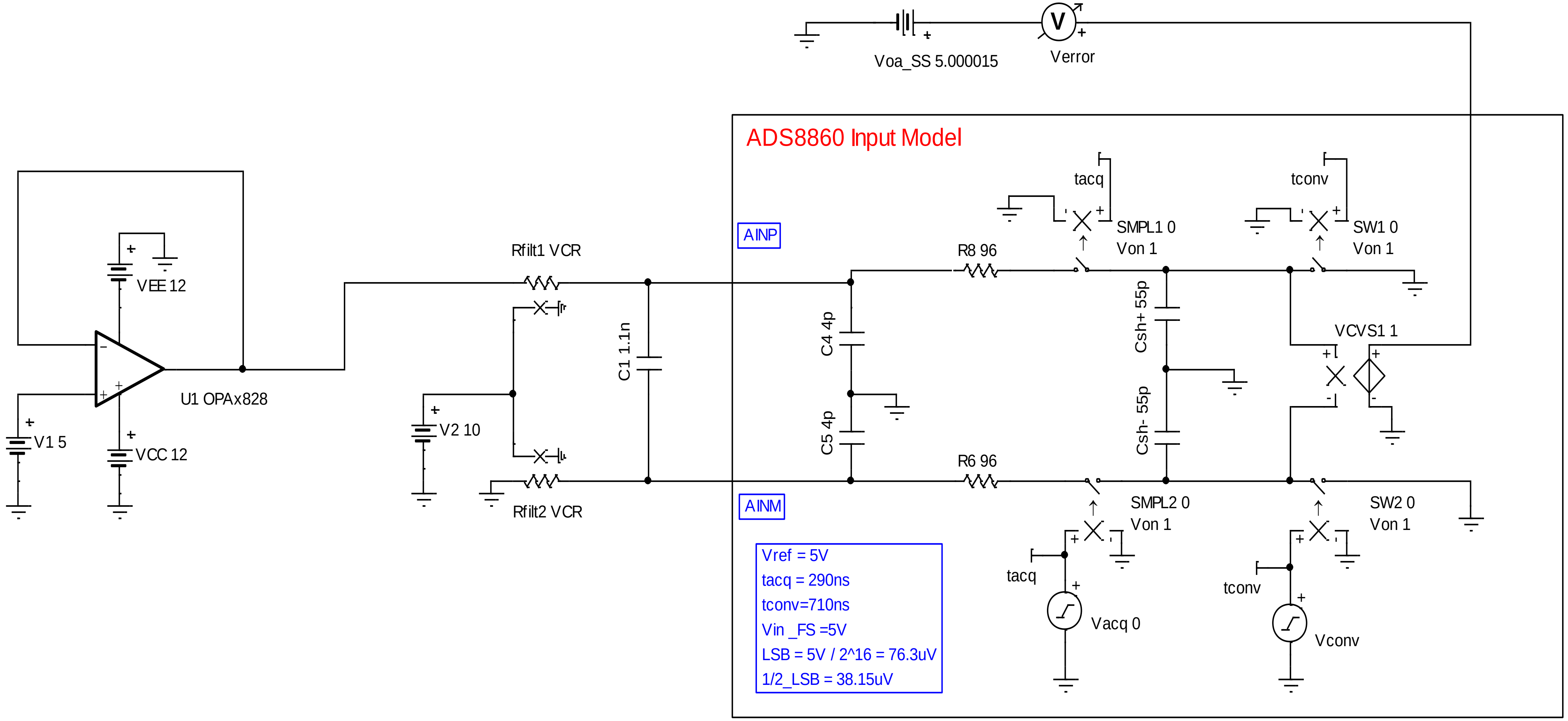


Driving Circuit:

- Proper R_{filt} and C_{filt} in charge bucket filter will optimize signal settling.
- Achieve final settling of 0.5LSB or better at end of tacq (acquisition time).

Driving Circuit without External diode - Simulation

Based on Precision labs training, build SAR Model and find proper RC with amp to drive:



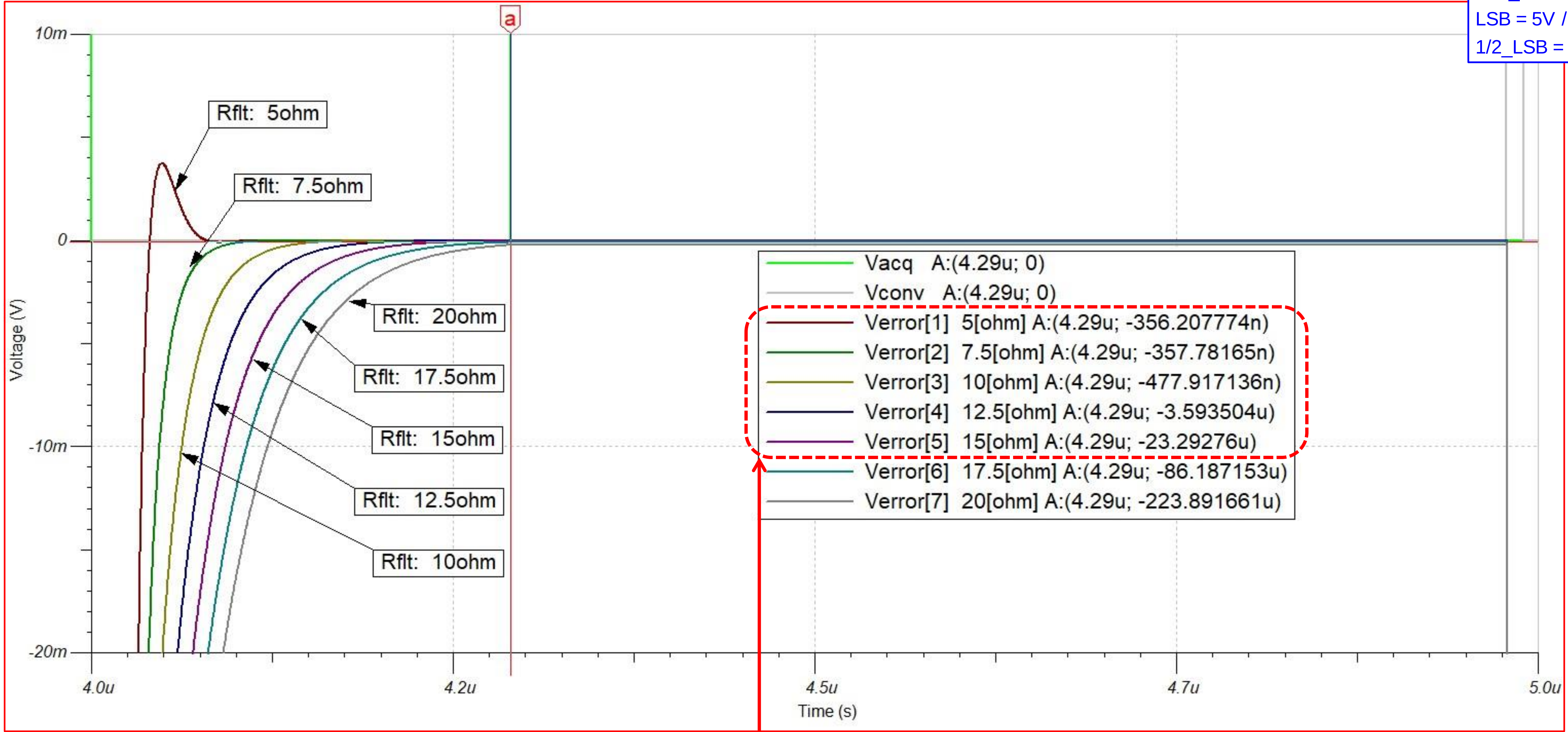
No diode_Step 1 and 2.TSC

No diode_Step 3.TSC

- High Bandwidth OPA828 is selected to drive ADS8860.
- Rflt ≤ **15.8**Ω to achieve settling error less than 0.5LSB.

Settling Error Check (Rflt=15ohm,Cflt=1.1nF)

Vref = 5V
tacq = 290ns
tconv=710ns
Vin _FS =5V
LSB = 5V / 2^16 = 76.3uV
1/2_LSB = 38.15uV

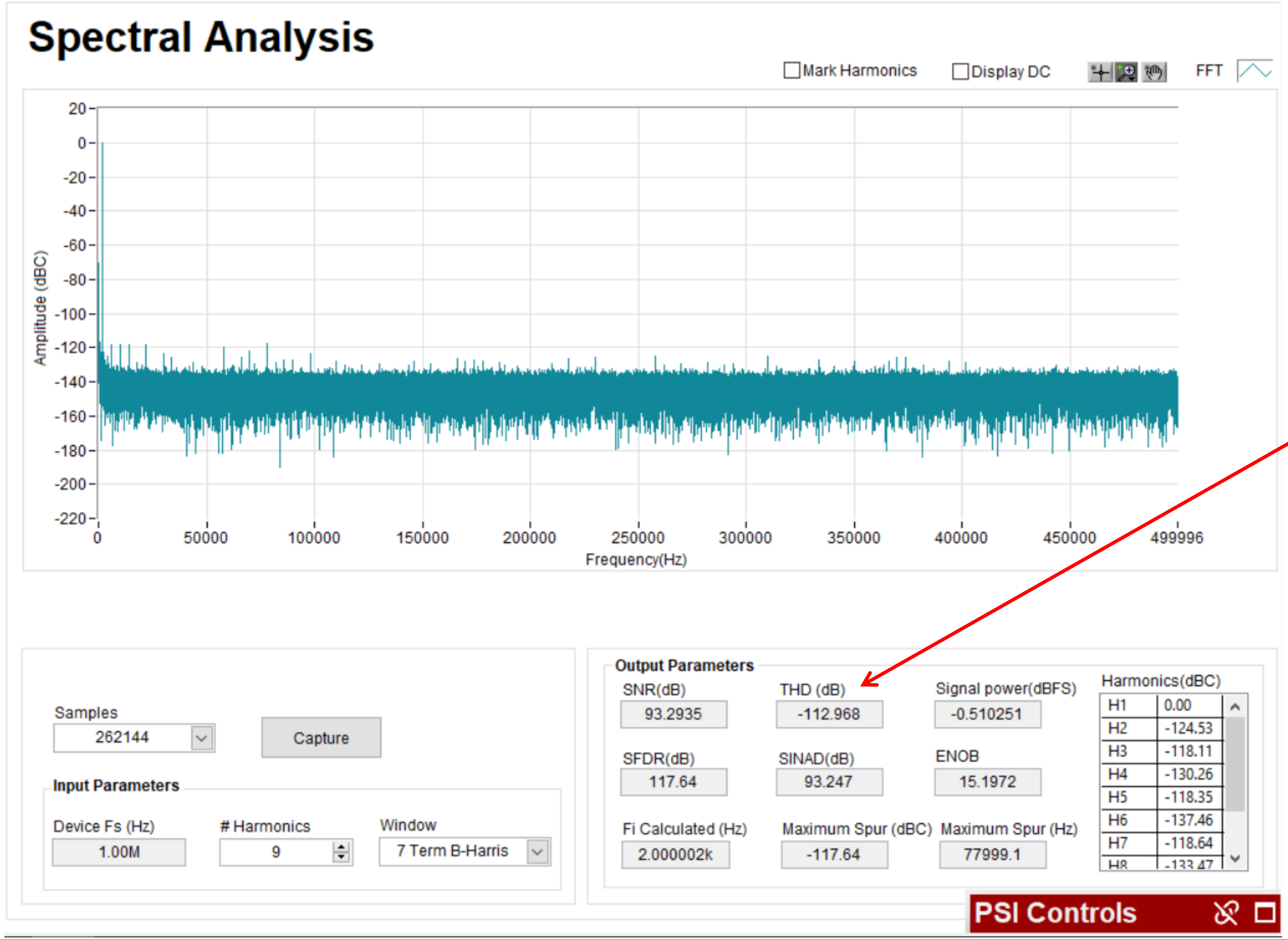


At end of Vacq, Verror = - 23.3uV -> 0.305 LSB (Rflt=15Ω) !!

Note: <1/2 LSB is expected.

Hardware Performance Check

(Rflt=15Ω, Cflt=1.1nF, OPA828+ADS8860 at 1Msps sampling rate)



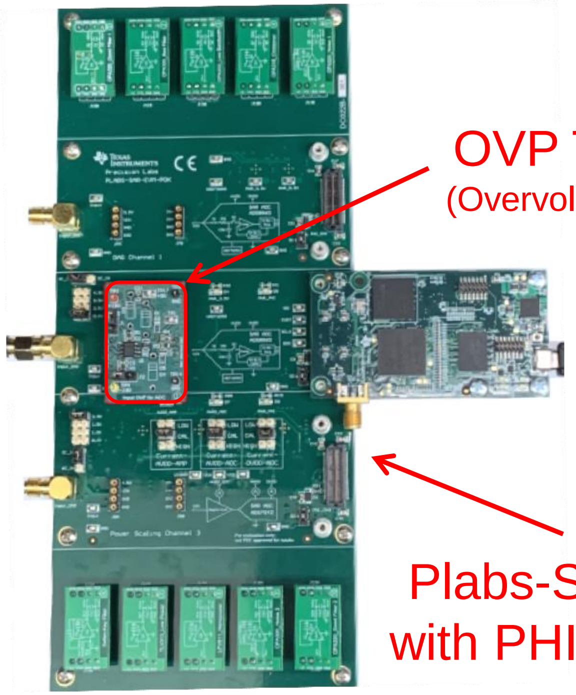
ADS8860 Data Sheet (1Msps)

Parameter	Min	Typ	Max	Unit
SNR	92	93		dB
THD		-108		dB

Measured:

SNR = 93.29dB

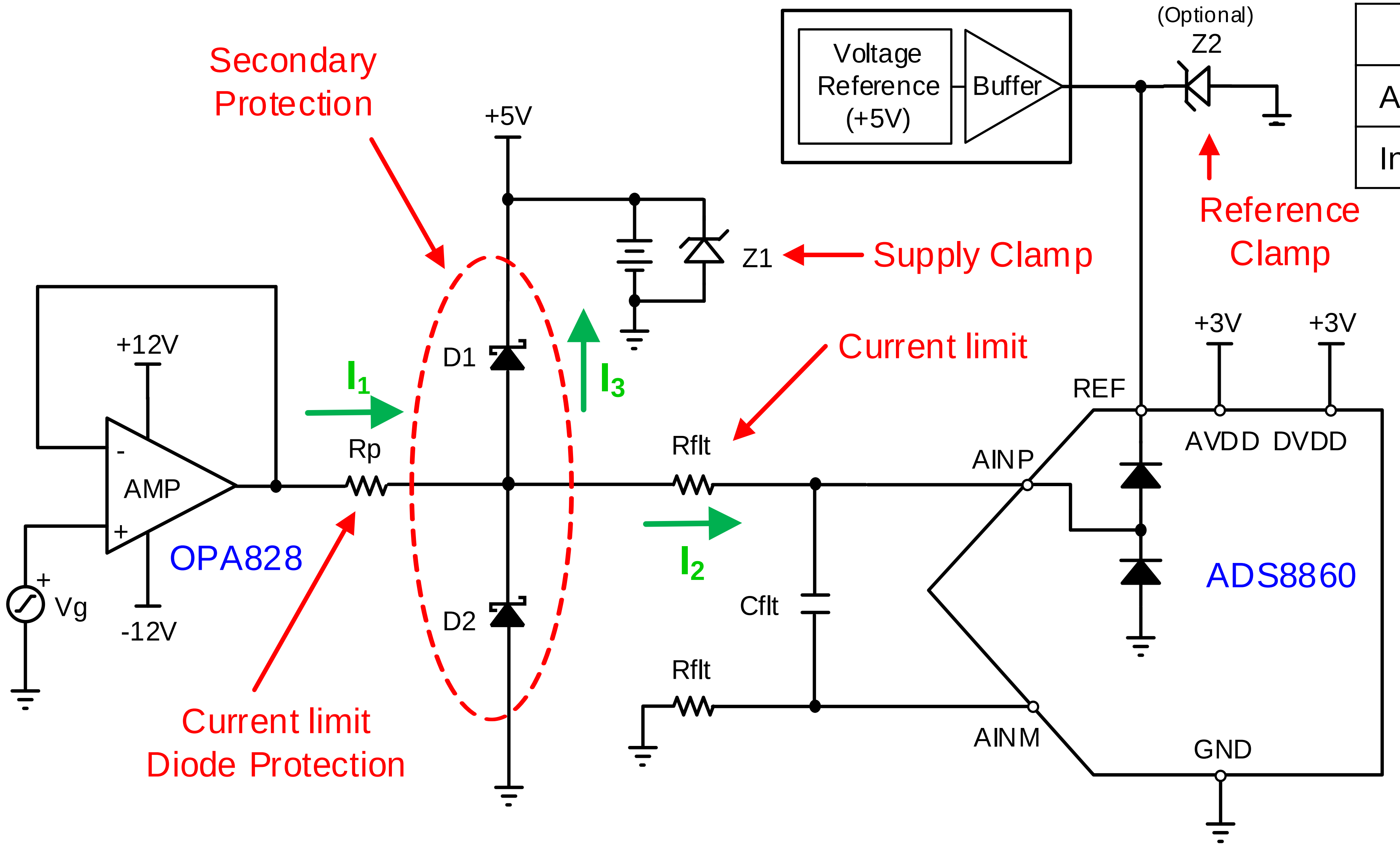
THD = - 112.9dB



OVP Test Board
(Overvoltage Protection)

Plabs-SAR-EVM
with PHI controller

Input Protection– External Diode



ADS8860 Absolute Maximum Ratings:

	Min	Max	Unit
AINP to GND or AINN to GND	-0.3	REF+0.3	V
Input Current	-10	10	mA

Note:

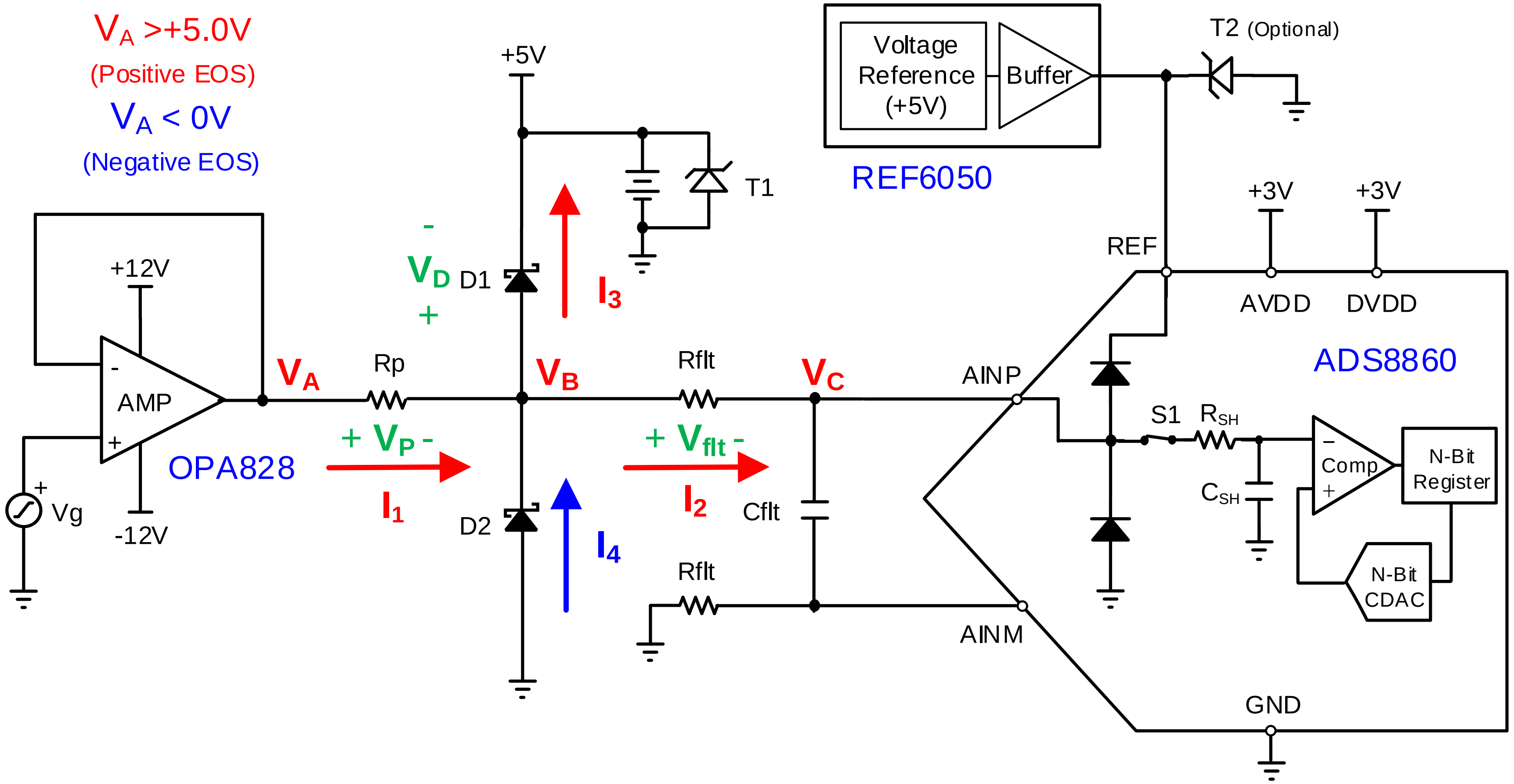
R_{flt} forces $I_2 << I_3$,

which ensures that the majority of the surge Energy is diverted by external Diodes rather than by the IC's internal protection diodes.

Understanding the protection scheme

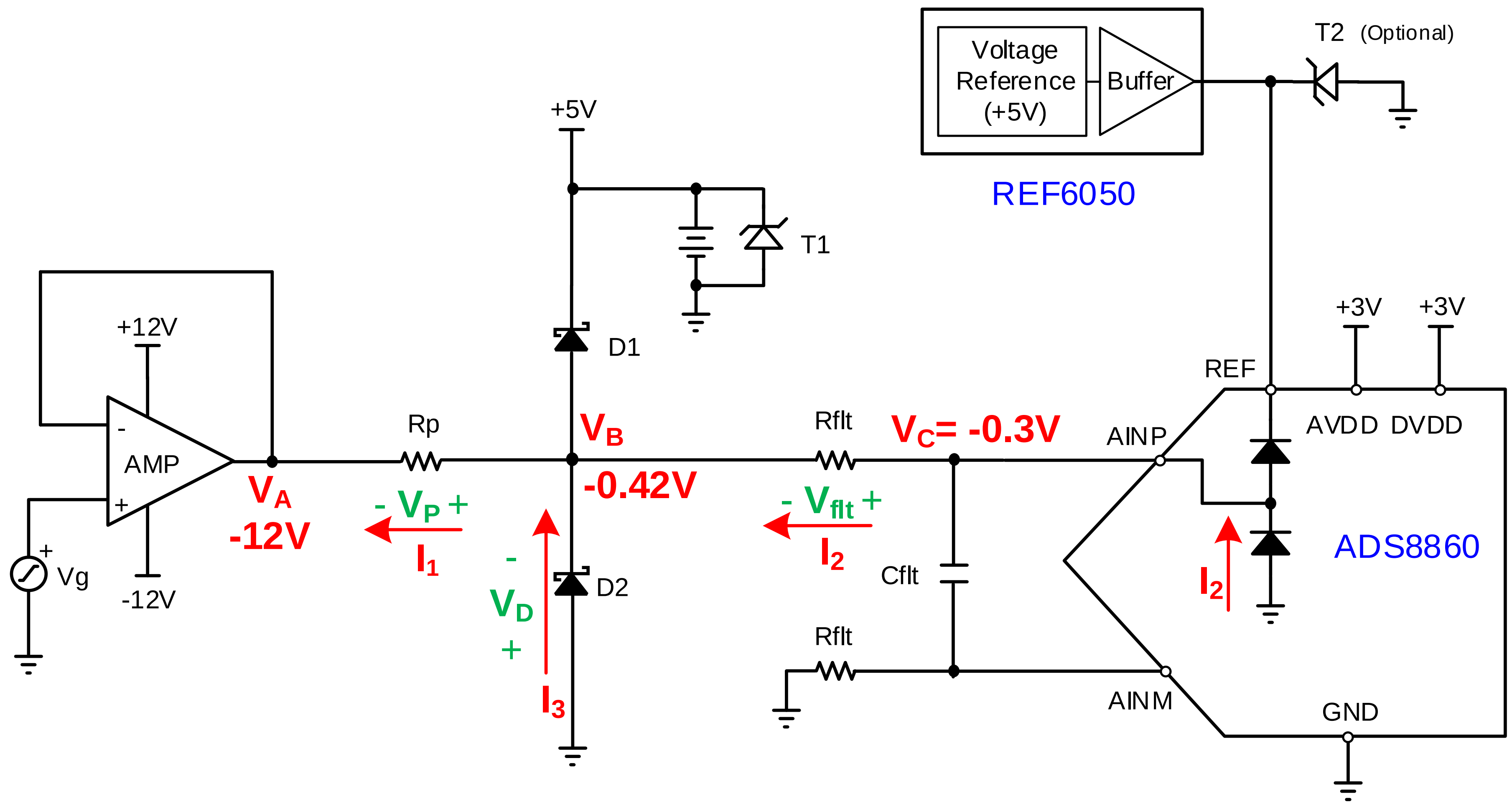
OPA828 Max Output Voltage:	
EOS Voltage range (Vo)	$-12V \leq V_O < 0V$ $5V < V_O \leq 12V$
OPA828 Max Output Current:	
Short-circuit current (I_{SC})	±50mA

ADS8860 Absolute Maximum Ratings:			
	Min	Max	Unit
AINP or AINN to GND	-0.3	+5.3	V
Input Current	-10	+10	mA



- **Normal Operation:**
  - ➢ D_1 and D_1 are Reverse-Biased.
- **Positive EOS: V_A> 5V**
  - ➢ Forward-Biased on D_1 for positive EOS.
  - ➢ Reverse-Biased state on D_2.
- **Negative EOS: V_A< 0V**
  - ➢ Forward-Biased on D_2 for negative EOS.
  - ➢ Reverse-Biased state on D_1.
- **R_P considerations**
  - ➢ Limiting total current I_1.
  - ➢ Lower I_1 keeps V_D lower
  - ➢ Watch the power in R_P and the Amp
- **V_D is smaller to keep:**
  - ➢ Lower V_B.
  - ➢ Lower V_C (Better ≤ +5.3V).
- **I_2 should be less than 10mA.**
- **Impact to settle signal on ADC's C_{SH}:**
  - ➢ Larger R_P and Rfil degrade settling
  - ➢ Diode's capacitance.
  - ➢ Diode's leakage current.

Select R_P and R_{flt}



Parameters known:		
1	I_1 (OPA828)	$\pm 50mA$ (Short current, I_{SC})
2	V_A (OPA828)	$\pm 12V$ (Maximum, V_O)
3	I_2 (ADC Input)	$\pm 10mA$ (Maximum, $I_{ADC\_in\_Abs}$)
4	V_C (ADC Input)	$+5.3V$ (Maximum, $V_{ADC\_in\_max}$) $-0.3V$ (Minimum, $V_{ADC\_in\_min}$)
Select R_P and R_{flt} (for negative EOS):		
1	I_3	$I_{3(min)} = I_1 - I_2 = 40mA$ $I_{3(max)} = I_1 - 0 = 50mA$
2	V_D (BAT54)	$V_D = 0.42V$ **(Selected V_F)**
3	V_B	$V_B = -0.42V$
4	R_P	$R_P > \frac{(12-0.42)V}{50mA} > 232\Omega$
5	R_{flt}	$R_{flt} \geq \frac{(0.42-0.3)V}{10mA} \geq 12\Omega$
6	**Select R_{flt} =15Ω, R_P =249Ω**	

Diode Comparison Chart - Schottky

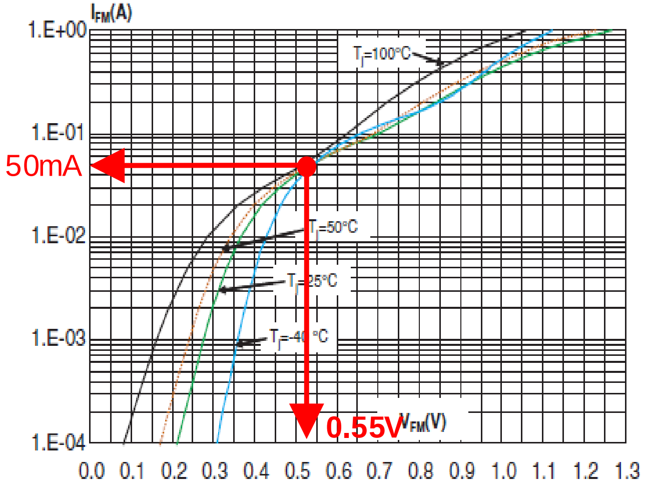
Electrical Characteristics:

Part Numbers	Manufacturer	Reverse Breakdown Voltage(V_{BR})V	Forward voltage (V_F) mV	Leakage current (I_R) uA	Total Capacitance (C_T) pF	Forward continuous current (I_F)mA	Repetitive peak forward current (I_{FSM}) A	Power Dissipation (P_D) mW
1N5712	Avago	20	580@10mA	0.15	1.2	35		250
BAT54	Diodes	30	400mV@10mA	2.0	10	200	0.3	200
BAT60	Infineon	10	150mV@10mA	1000	35	3000	5	1350
BAS70	Infineon	70	750mV@10mA	0.1	2	70	0.1	250
1PS70SB82	NXP	15	340mV@1mA	0.2	1@typ	30		
DB2S20500L	Panasonic	20	390mV@200mA	50	30	200	1	
VS-10BQ015-M3/5BT	Vishay	15	330 @1A	500	390	1000	140	

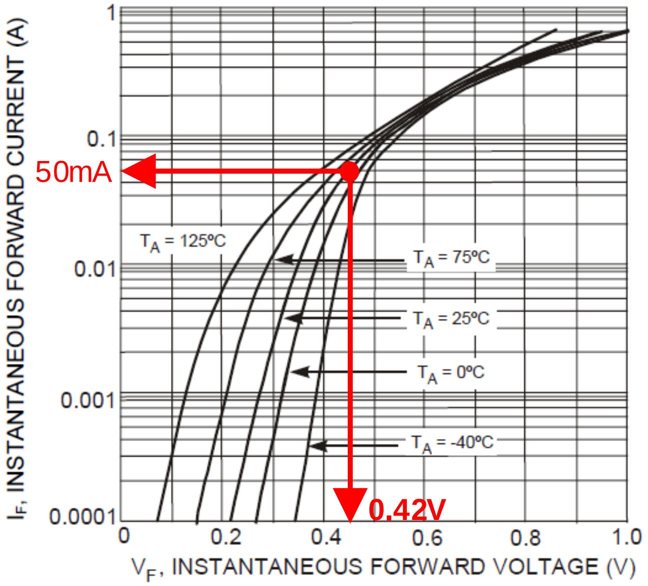
BAT54 has the best trade off for forward voltage, leakage, and capacitance.

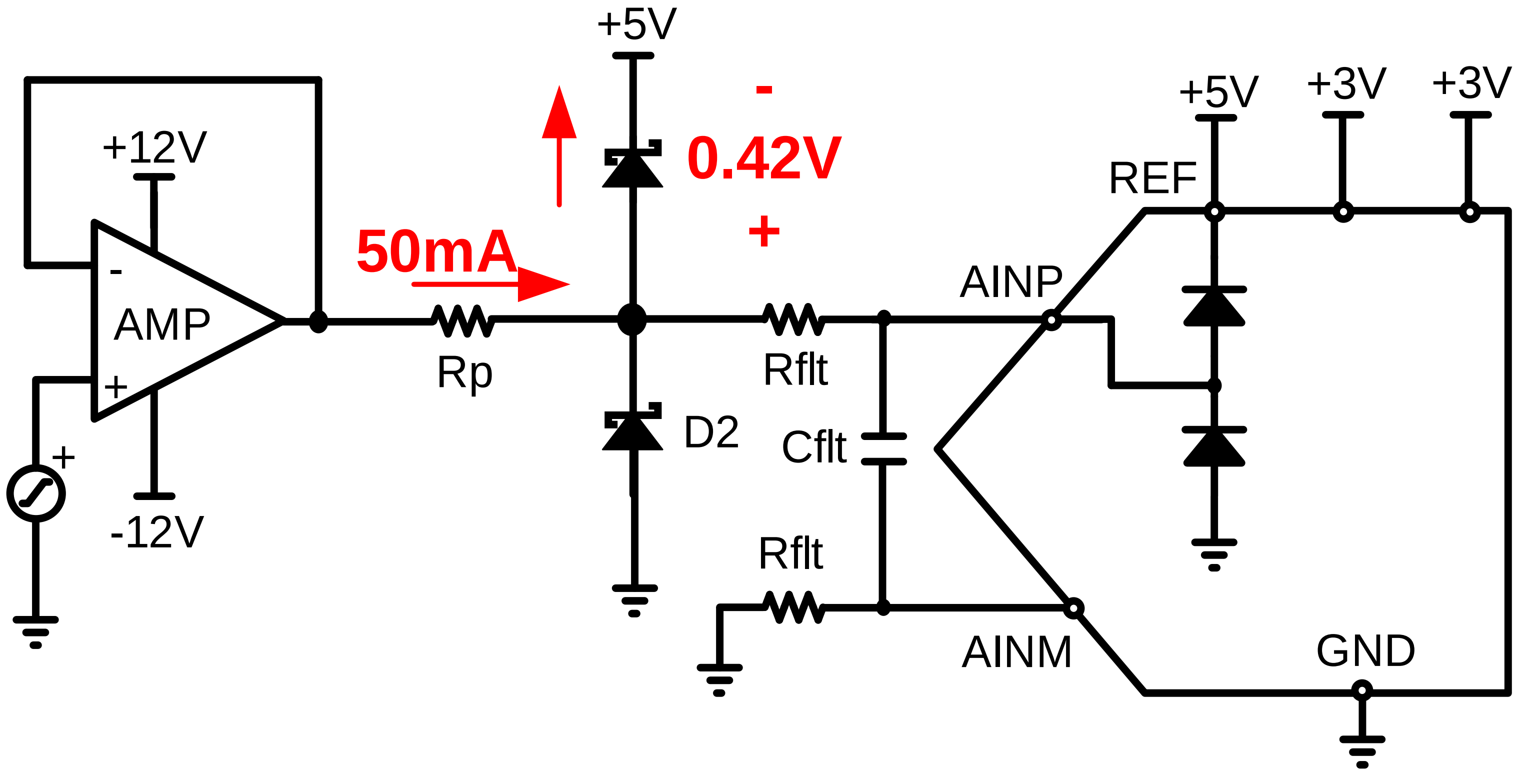
Using Diode V-I Curves

ST – BAT54



Diodes Inc. – BAT54

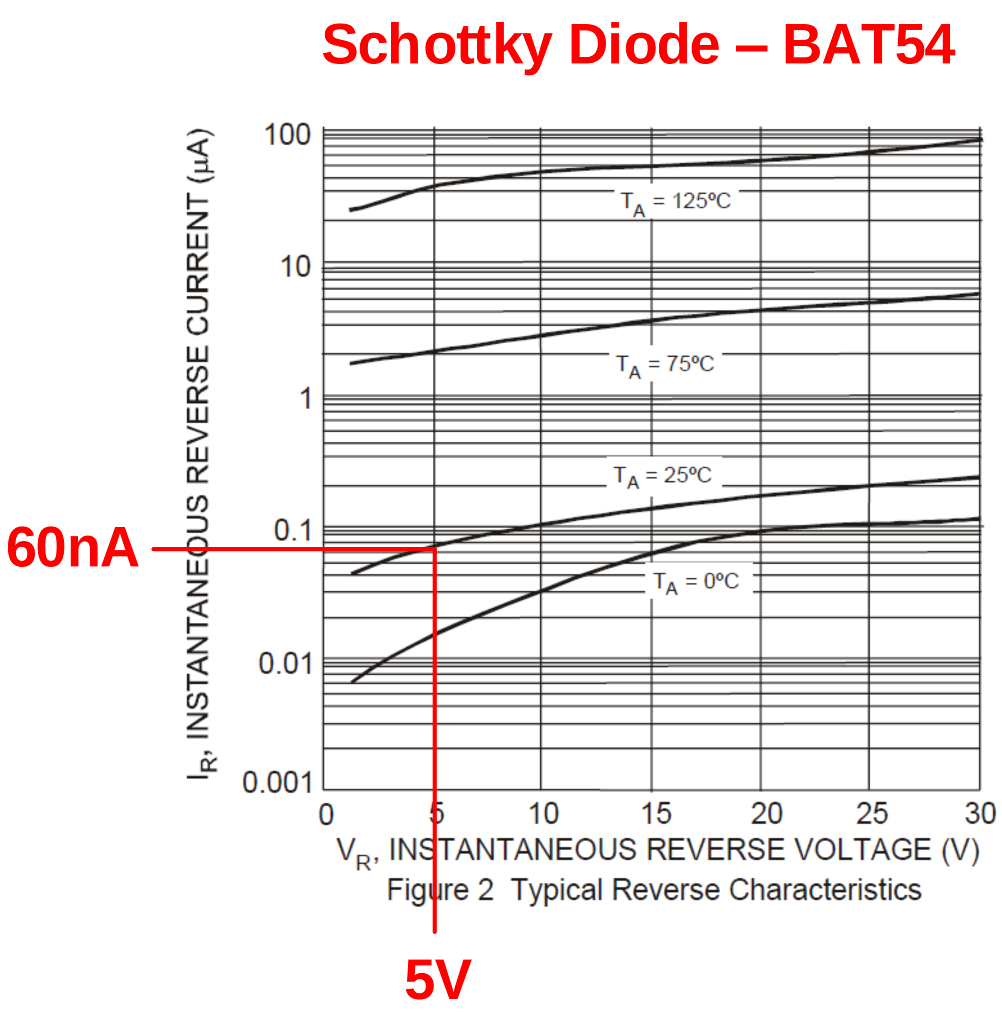


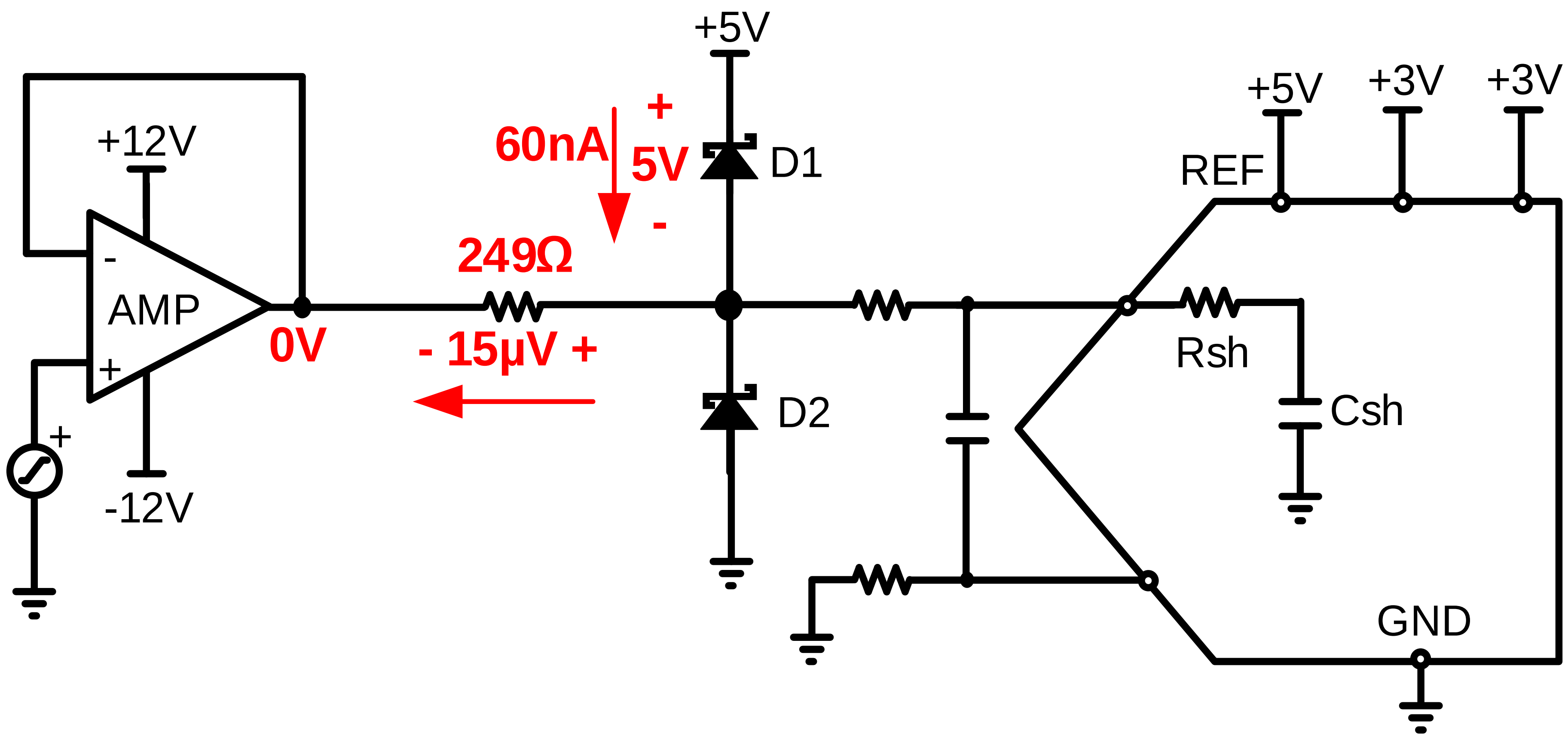


- BAT54 from “Diodes Inc.” manufacturer has better forward voltage (V = 0.42V)
- Same current (I_F = 50mA)
- Same temperature (+25°C).

Reverse leakage current on Diode – Not issue for this example

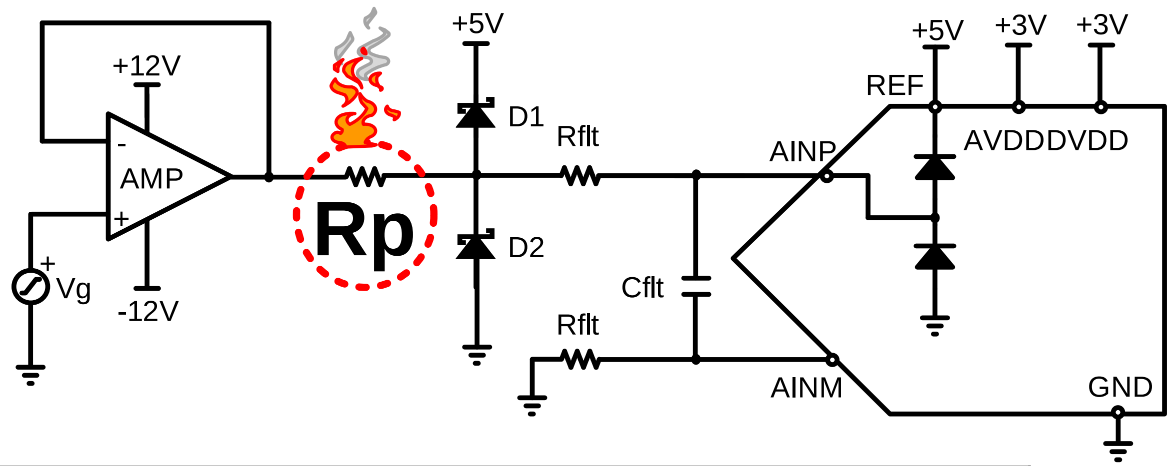
- Leakage current is not constant with reserve voltage(<1uA for BAT54 at room temp).
- Leakage current is changing with temperature.





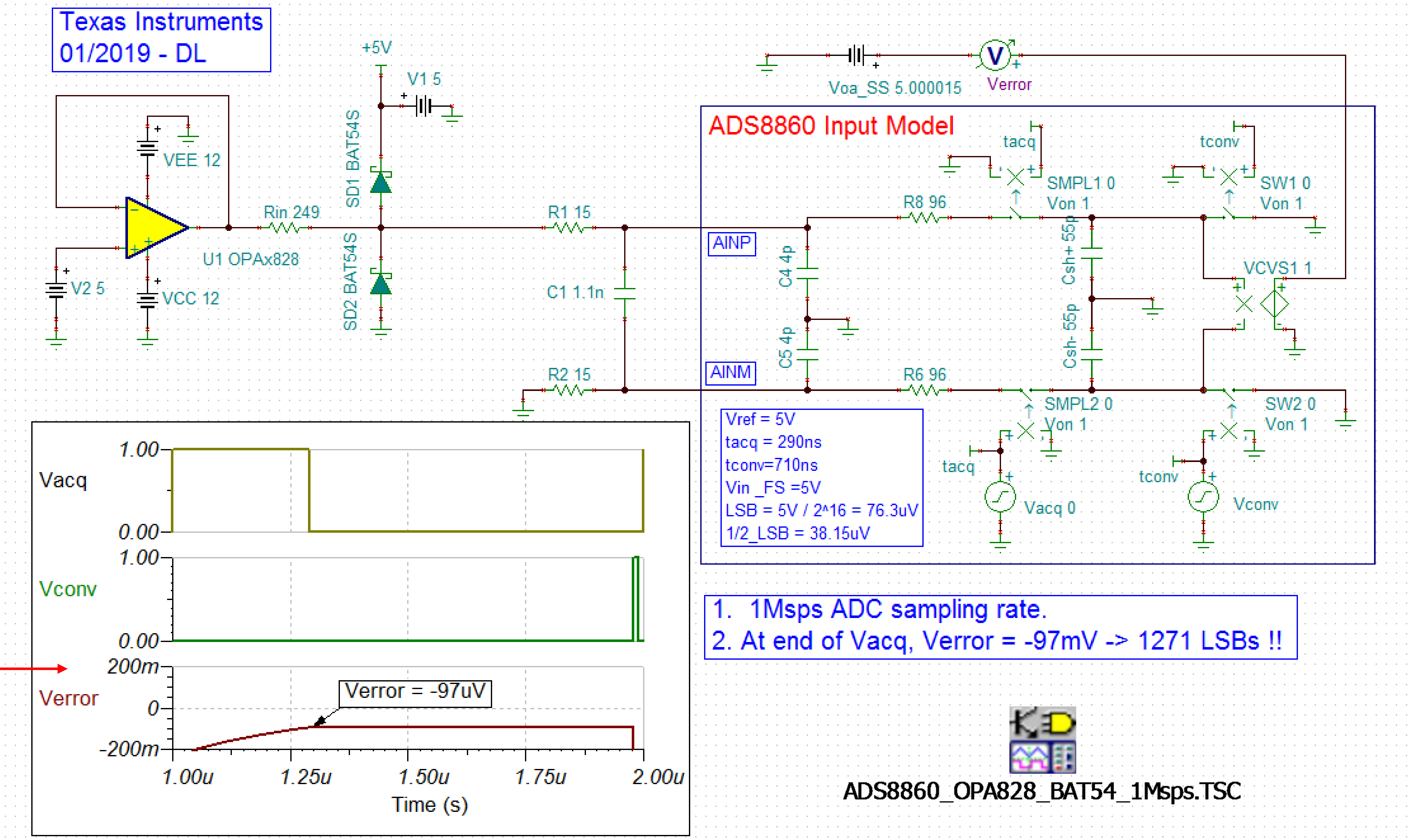
Power Dissipation on R_P

- Voltage drop across Rp may not be acceptable.
- Power Dissipation on Rp may be a challenge:



1	V_O (OPA828)	$\pm 12V$ (Choose -12V for worst case across Rp)
2	V_B	$V_B = -0.42V$
3	V_P (Volts on R_P)	$V_P = V_O - V_B = -12V - (-0.42V) = -11.58V$
4	I_1 (Current through R_P)	$I_1 = \frac{V_P}{R_P} = \frac{-11.58V}{249\Omega} = -38.6mA$
5	P_p (Power Dissipation on Rp)	$P_P = I_1^2 * R_P = (38.6mA)^2 * 249\Omega = 371mW$
Note:	1. Actual resistor should have at least double power dissipation ability which requires larger package size. 2. Higher V_O or power supply to amplifier will require higher power dissipation on Rp.	

Driving circuit with Schottky diode - Simulation



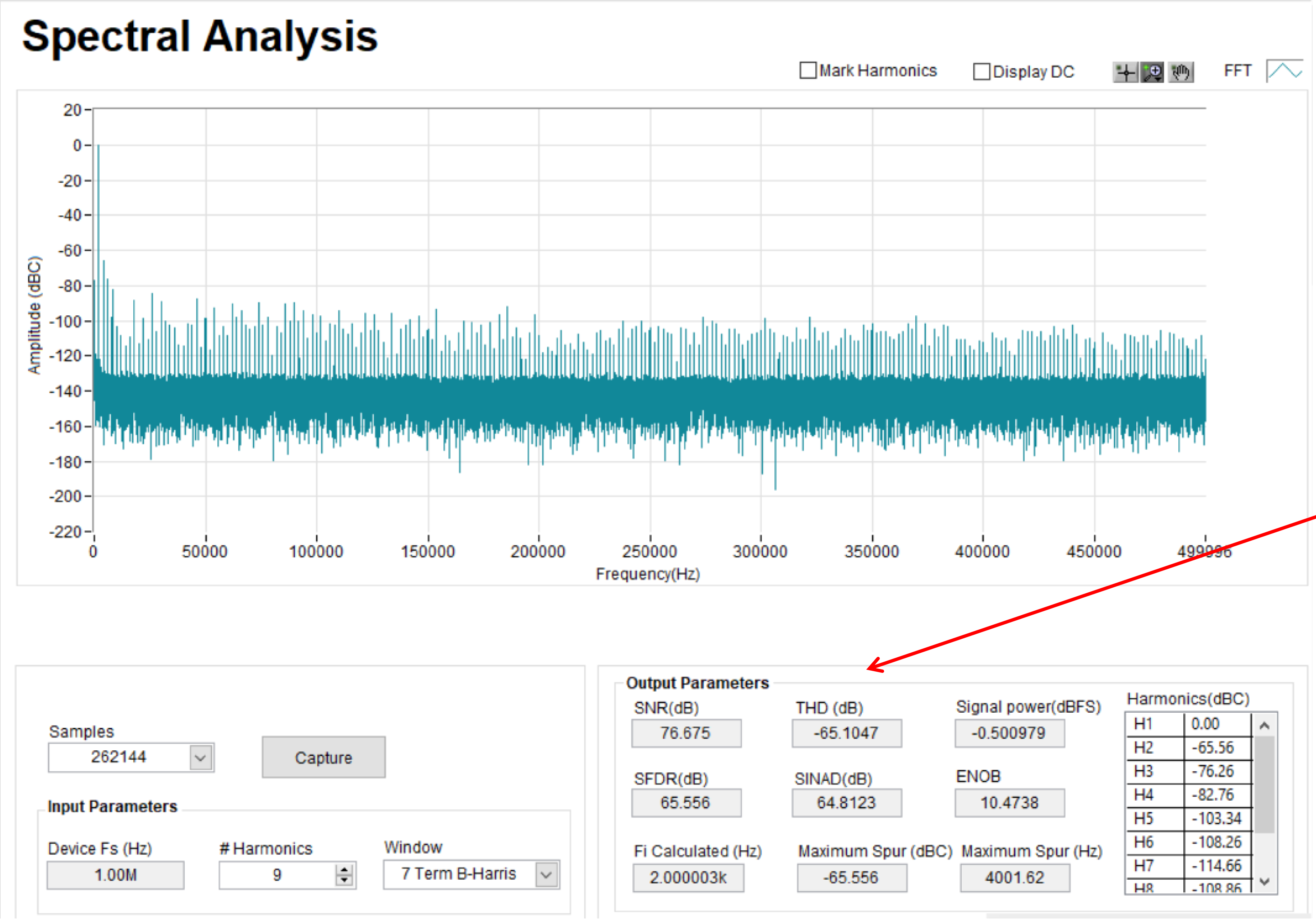
The settling error target is less than 38µV, so 97mV is a large error and poor THD and SNR is expected.

1. 1Msps ADC sampling rate.
2. At end of Vacq, Verror = -97mV -> 1271 LSBs !!

ADS8860_OPA828_BAT54_1Msps.TSC

Hardware Performance Check

(BAT54 Schottky diode, Rp=249Ω, Rflt=15Ω, Cflt=1.1nF, OPA828+ADS8860 at 1Msps sampling rate)



ADS8860 Data Sheet (1Msps)

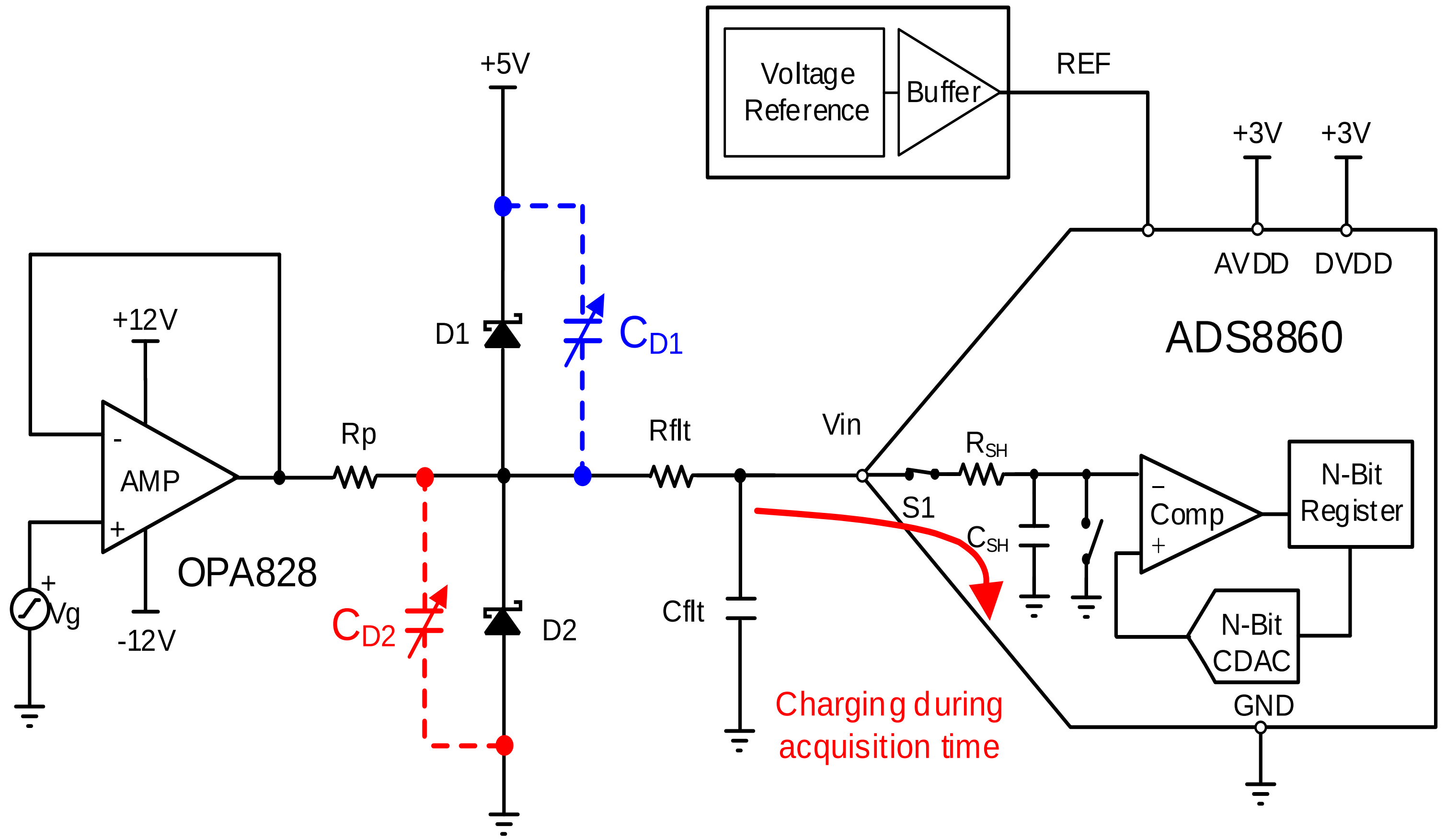
Parameter	Min	Typ	Max	Unit
SNR	92	93		dB
THD		-108		dB

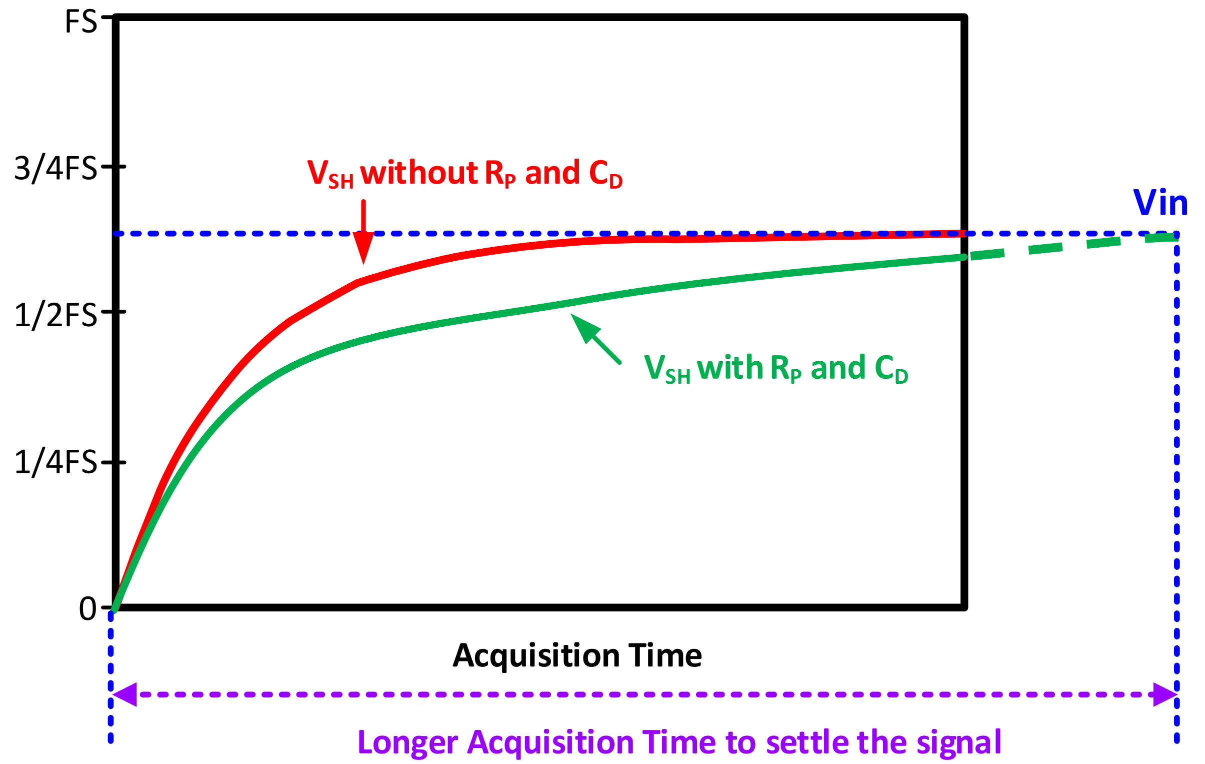
Measured with BAT54:

SNR = 76.6dB

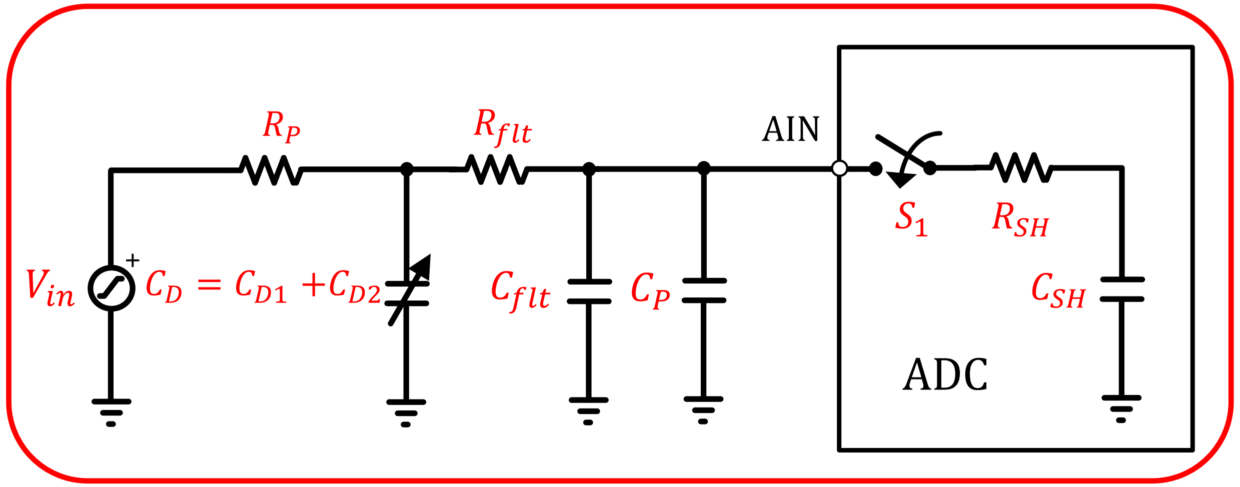
THD = - 65.1dB

Large series resistance impacts settling





Equivalent Circuit

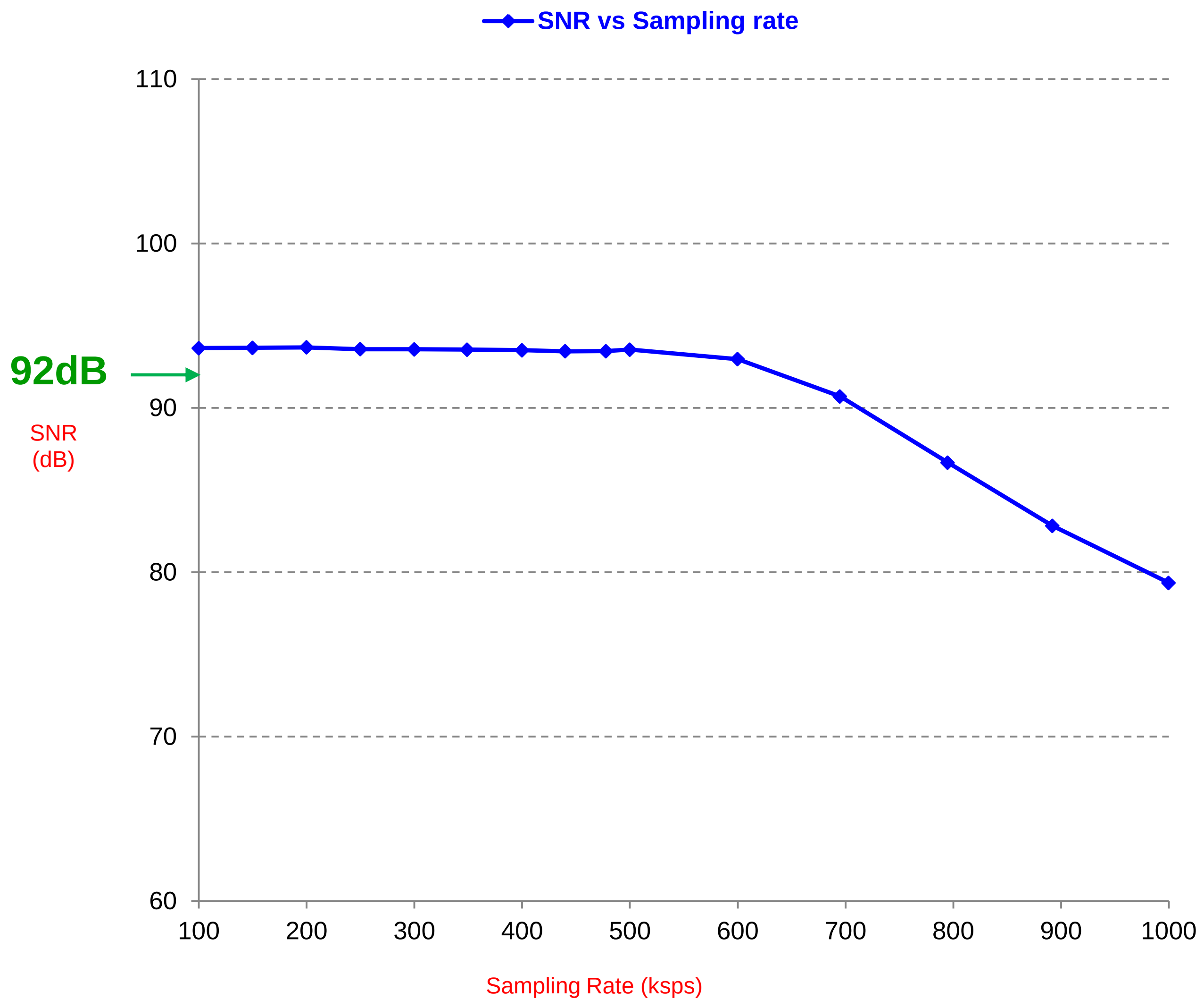


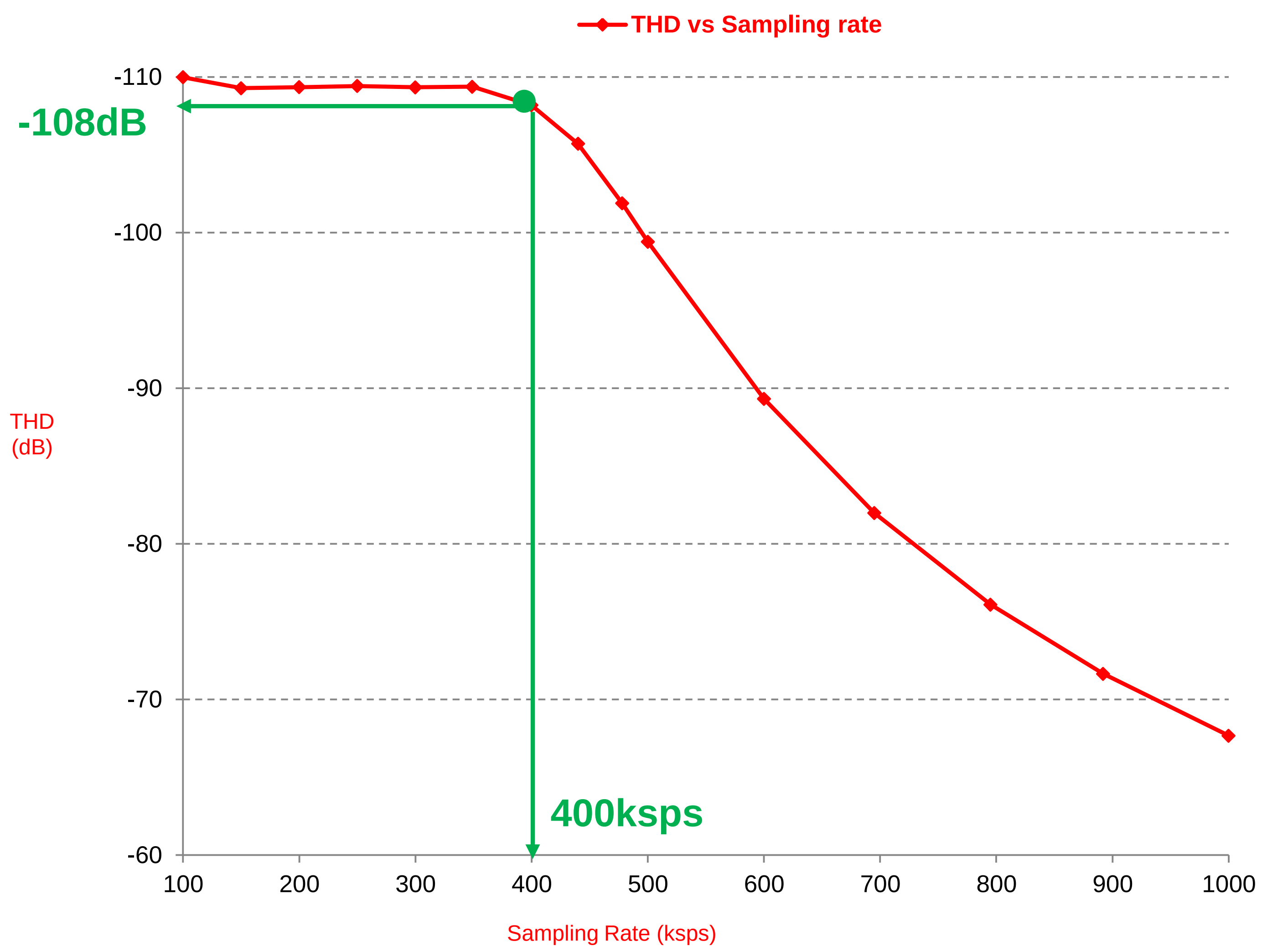
- Need longer time to settle the signal with R_P and Rfilt
- Reducing F_S can **extend the ADC's acquisition time** to meet the requirement.

* C_P is parasitic capacitance.

Limitation on Protection Solution – Hardware Check

Sampling rate ≤ 400ksps can achieve the performance specified in ADS8860 datasheet.



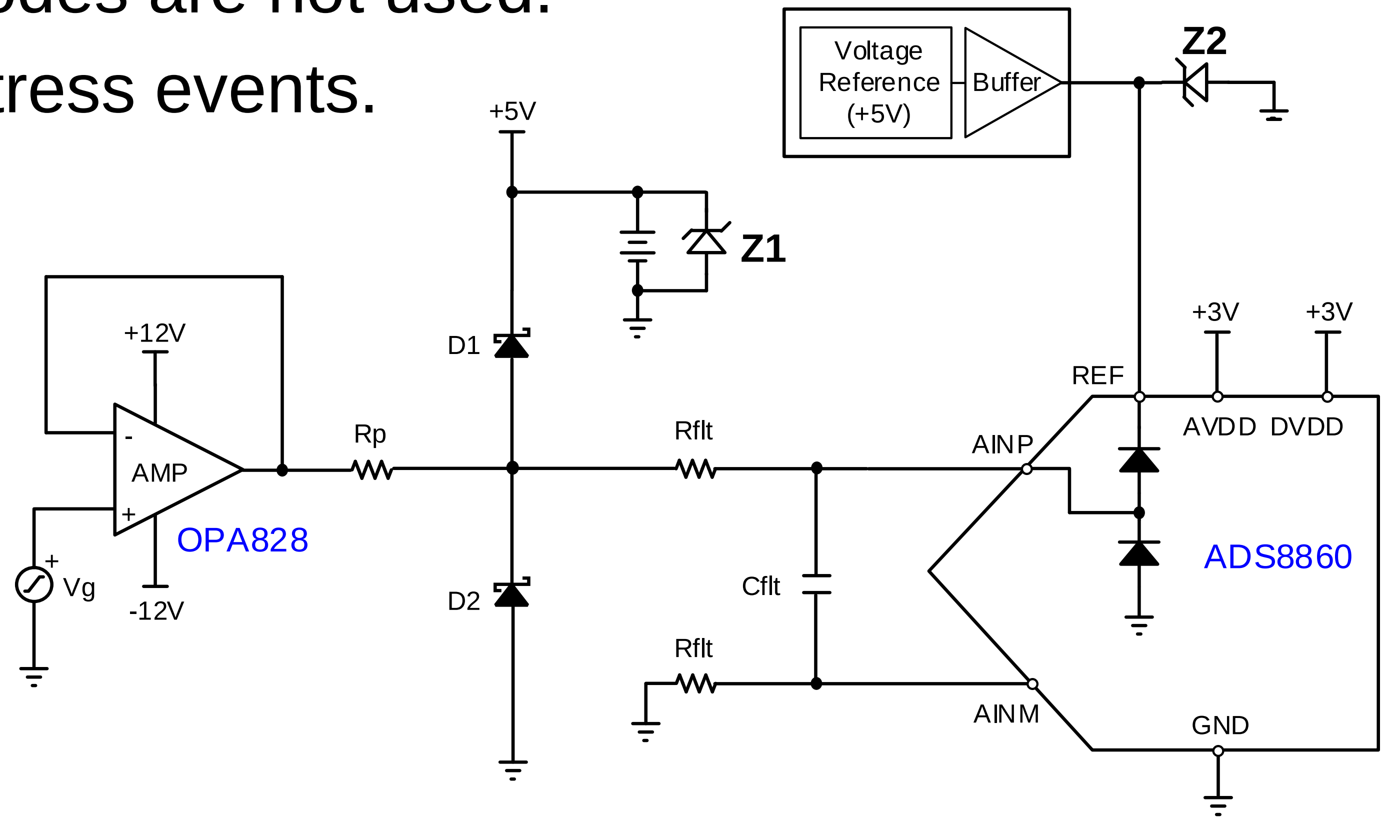


Note: Real test results with 2kHz sinewave and R_P =200Ω, R_{flt} =15Ω, R_{flt} =1.1nF on OVP card and Plabs-SAR-EVM hardware.

Thanks for your time!
Please try the quiz.

Questions: Protecting Low Voltage ADC

1. For the circuit below, what is the purpose of the TVS diode (Z1) on the 5V supply for the Schottky diodes?
   a. The 5V supply may not be able to sink current; the TVS will turn on an limit the voltage for large positive transients.
   b. The TVS is only required if the Schottky diodes are not used.
   c. The TVS minimizes RF noise during overstress events.
   d. The TVS regulates the 5V supply.



Questions: Protecting Low Voltage ADC

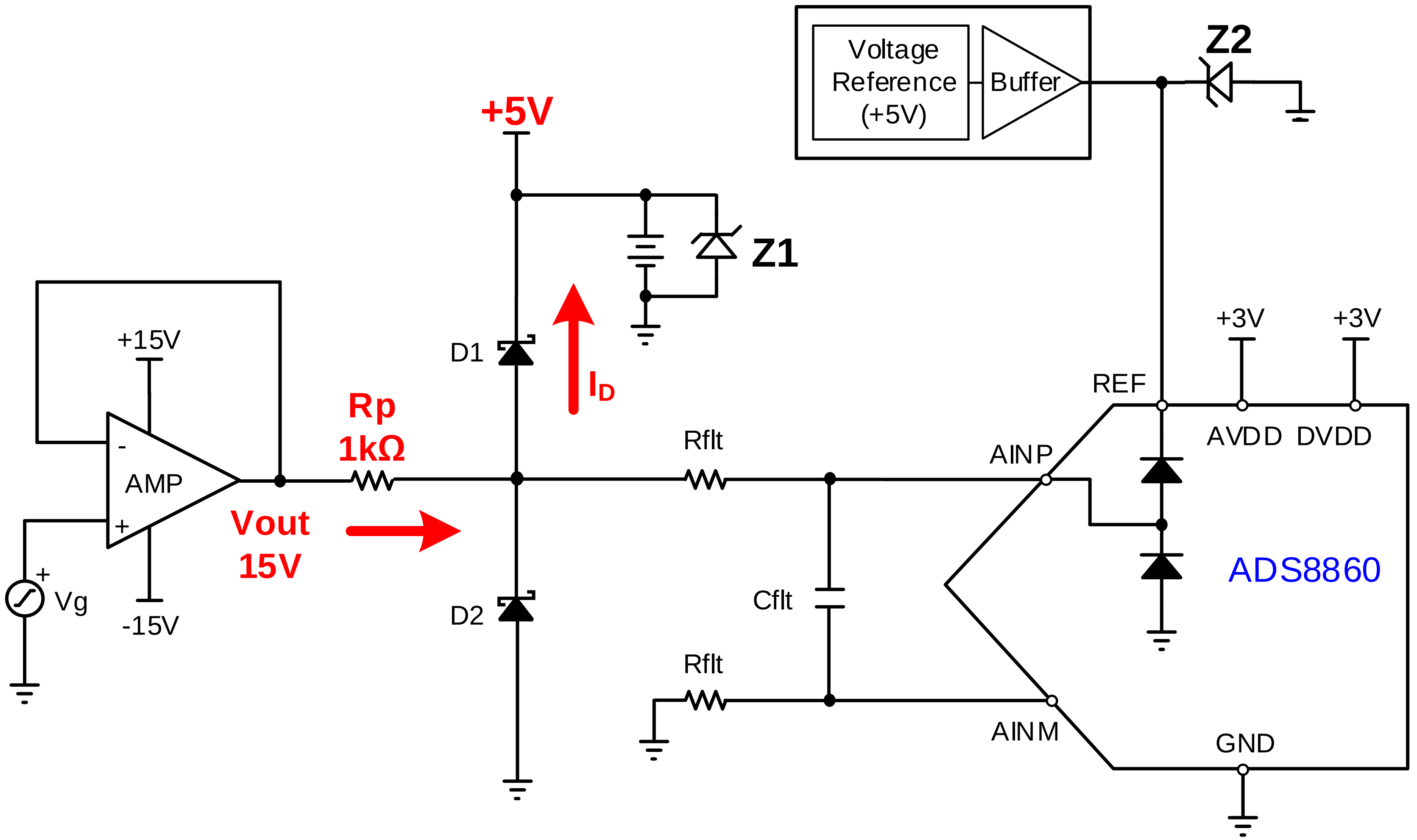
2. (T/F) The internal ESD diodes can be connected to either the analog supply, or digital supply?
   a. True.
   b. False.

3. (T/F) Schottky diodes have better leakage current than a PN signal diode.
   a. True.
   b. False.

4. (T/F) Schottky diodes have lower forward voltage than a PN signal diode.
   a. True.
   b. False.

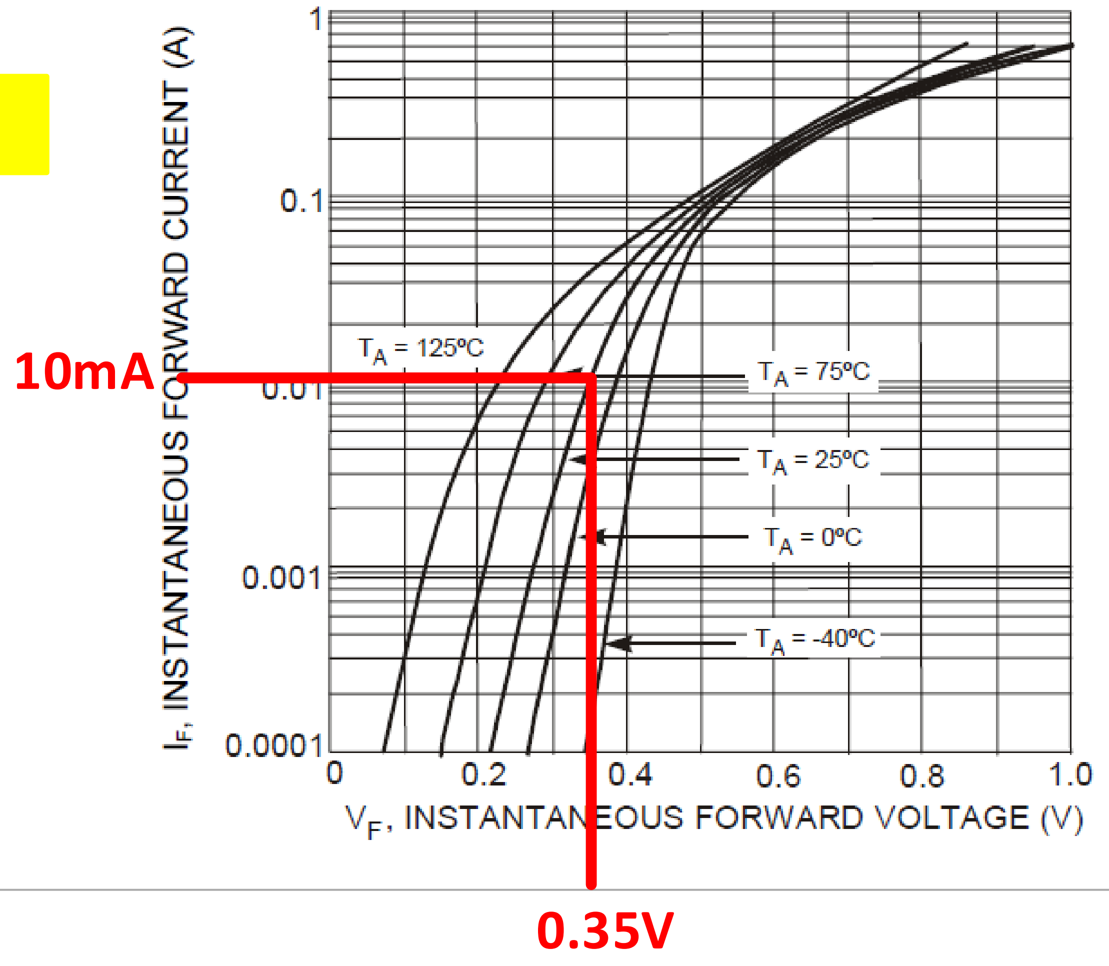
Questions: Protecting Low Voltage ADC

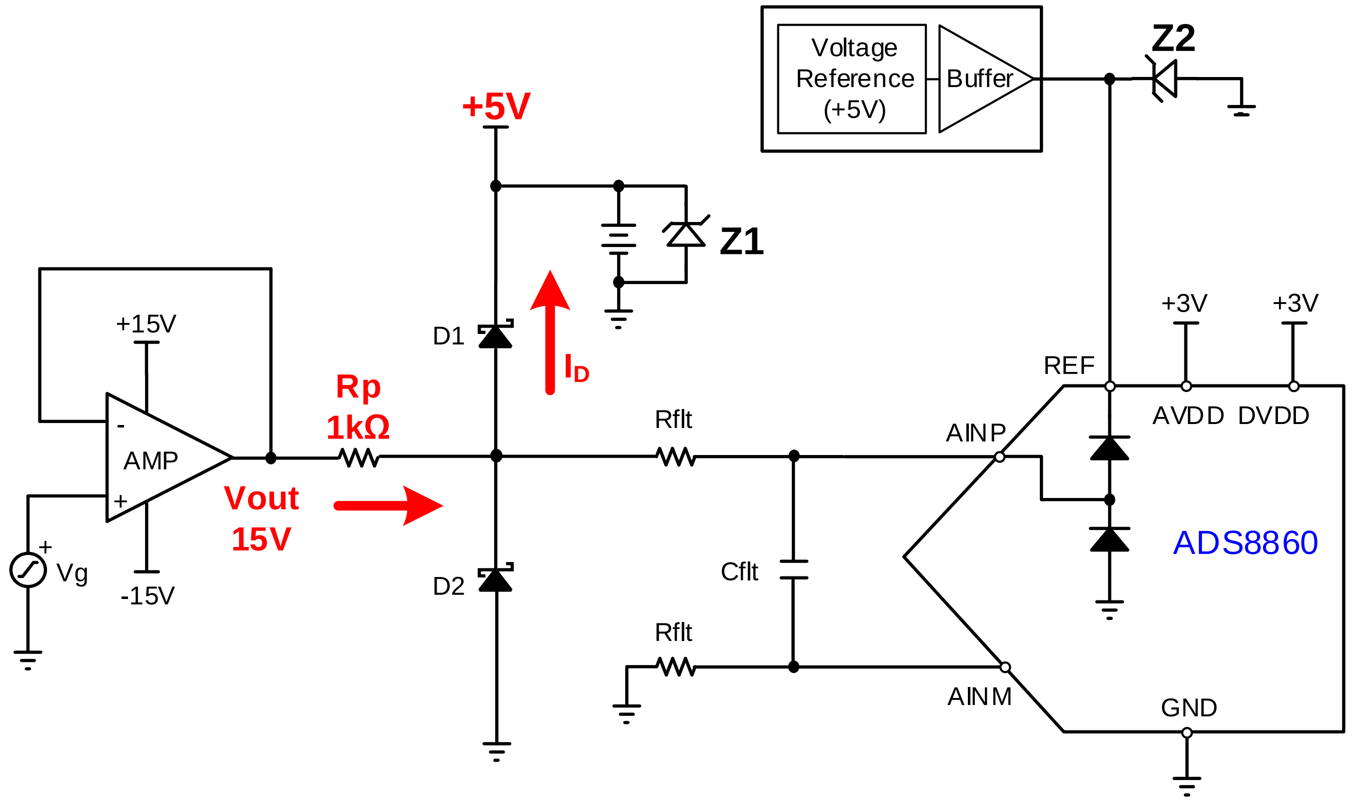
5. For the circuit below, what is the approximate current in the diode (I_D)?
   a. 1mA.
   b. 1.5mA.
   c. 10mA.
   d. 15mA.
   e. 50mA



Questions: Protecting Low Voltage ADC

6. Continuing with the circuit from the previous slide, what is the forward voltage drop across D1 at 25C?
   a. 0.2V.
   b. 0.25V.
   c. 0.3V.
   d. 0.35V.
   e. 0.4V





Questions: Protecting Low Voltage ADC

7. Assuming the protection circuit is causing distortion. How can the distortion be reduced?
    a. Increase the series resistance
    b. Increase the sampling rate.
    c. Decrease the sampling rate
    d. Increase the power rating of the TVS diode

Questions: Protecting Low Voltage ADC

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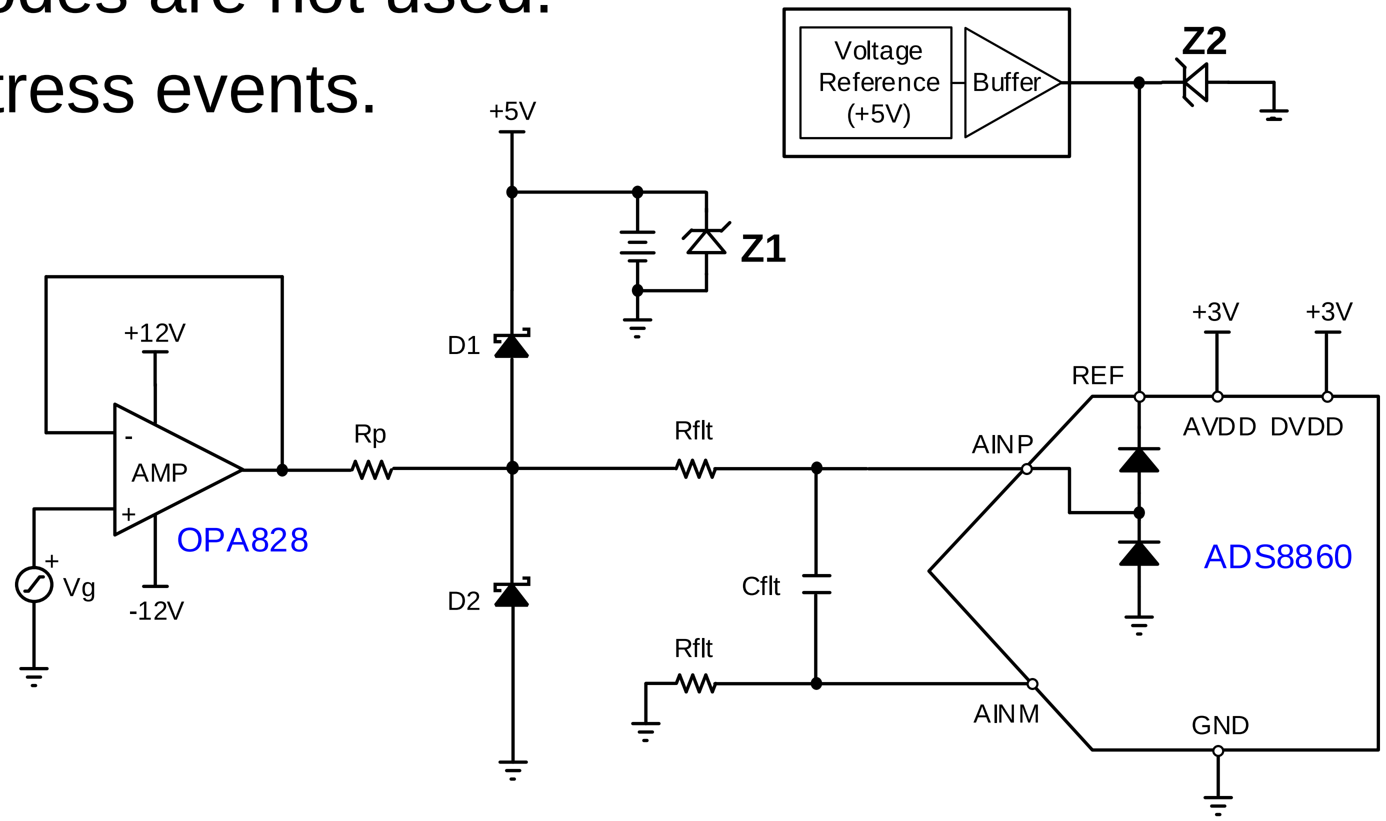
   d. The TVS regulates the 5V supply.



Questions: Protecting Low Voltage ADC

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Questions: Protecting Low Voltage ADC

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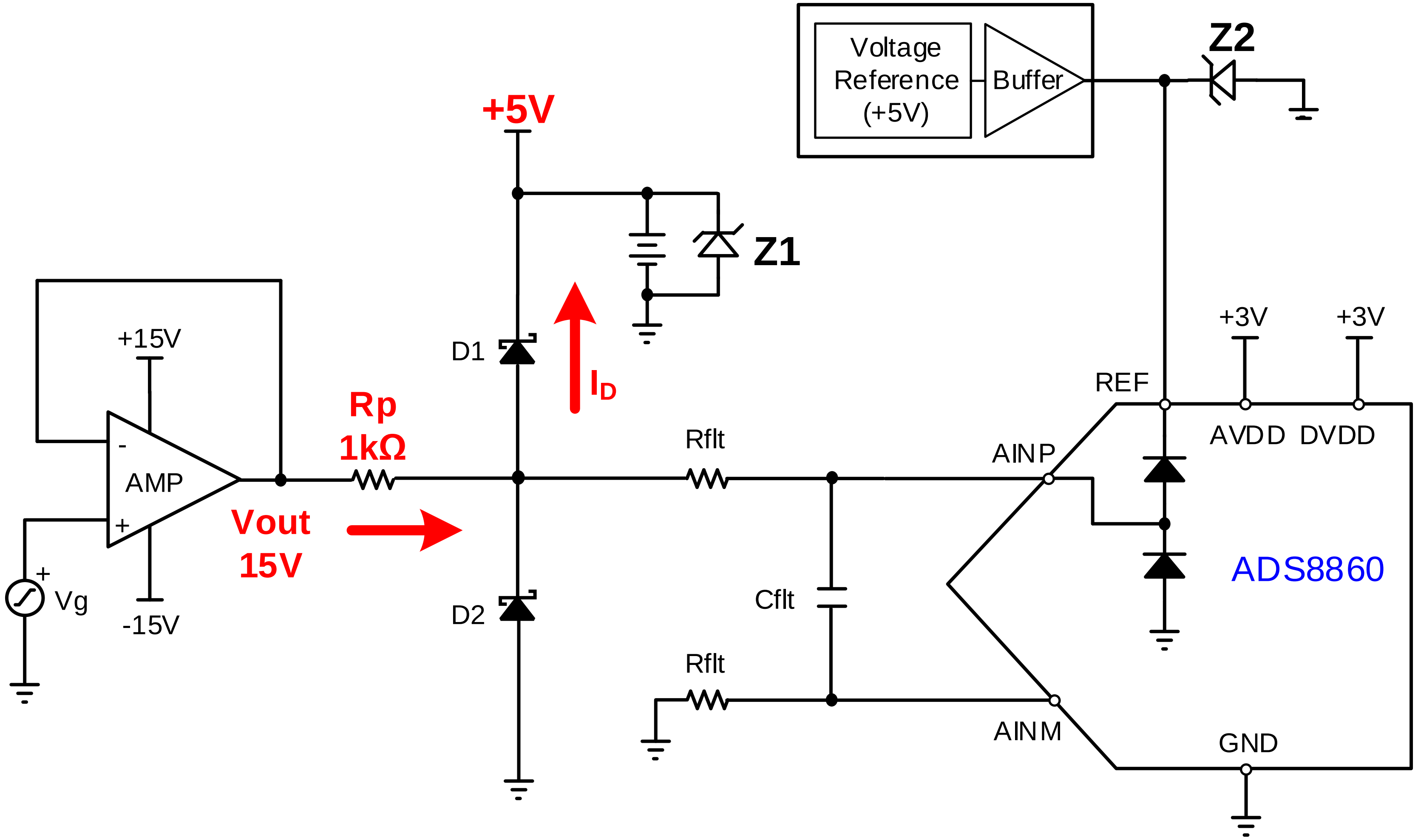

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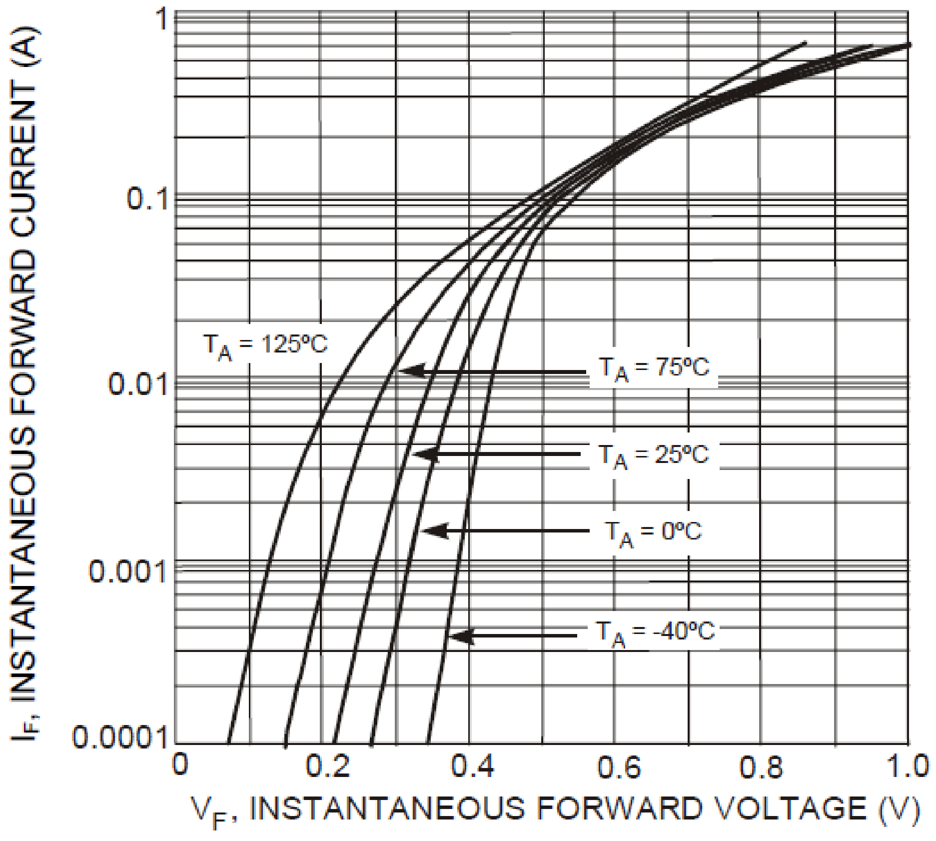

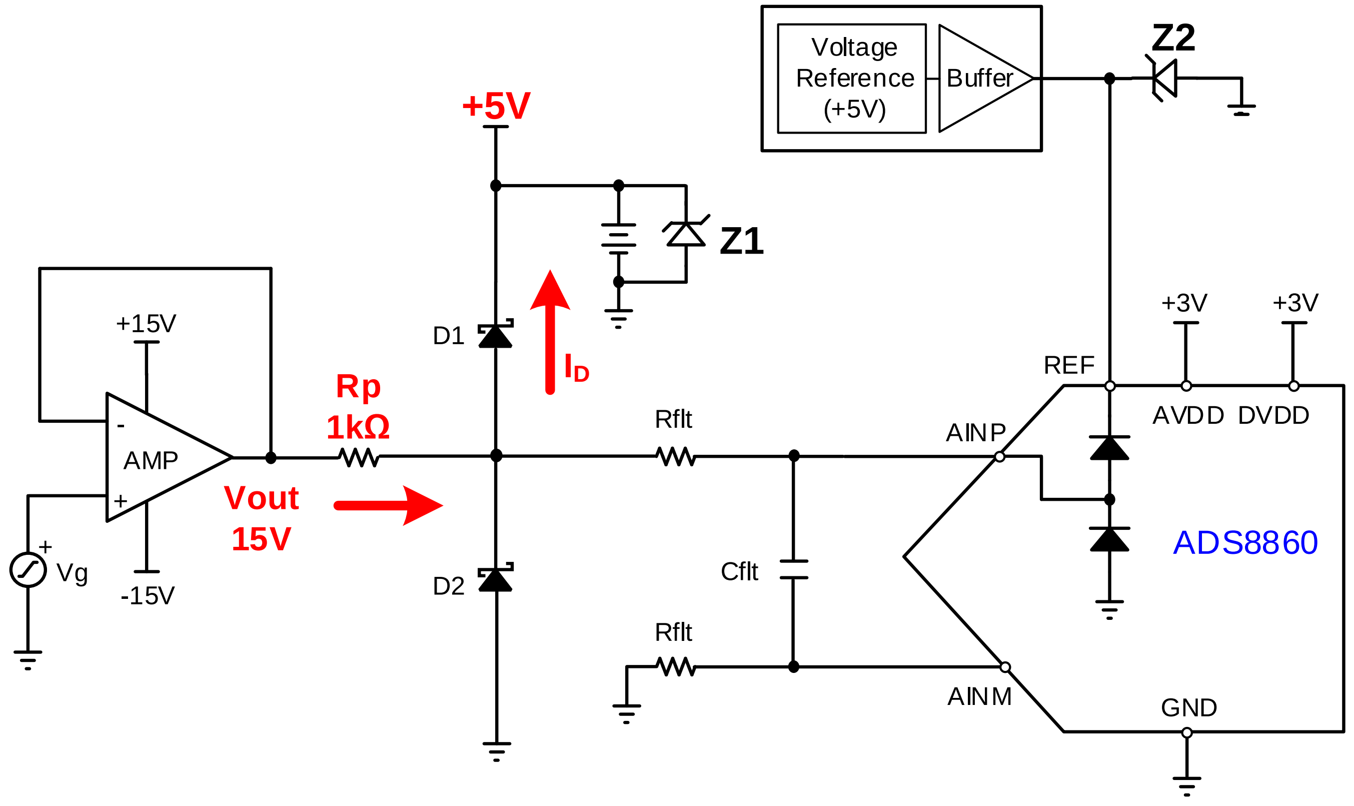

Questions: Protecting ADC with TVS Diode - Improved

7. Assuming the protection circuit is causing distortion. How can the distortion be reduced?
    a. Increase the series resistance
    b. Increase the sampling rate.
    c. Decrease the sampling rate
    d. Increase the power rating of the TVS diode