Network Synchronizer: Key Parameters and Specifications

TI Precision Labs – Clocks and Timing

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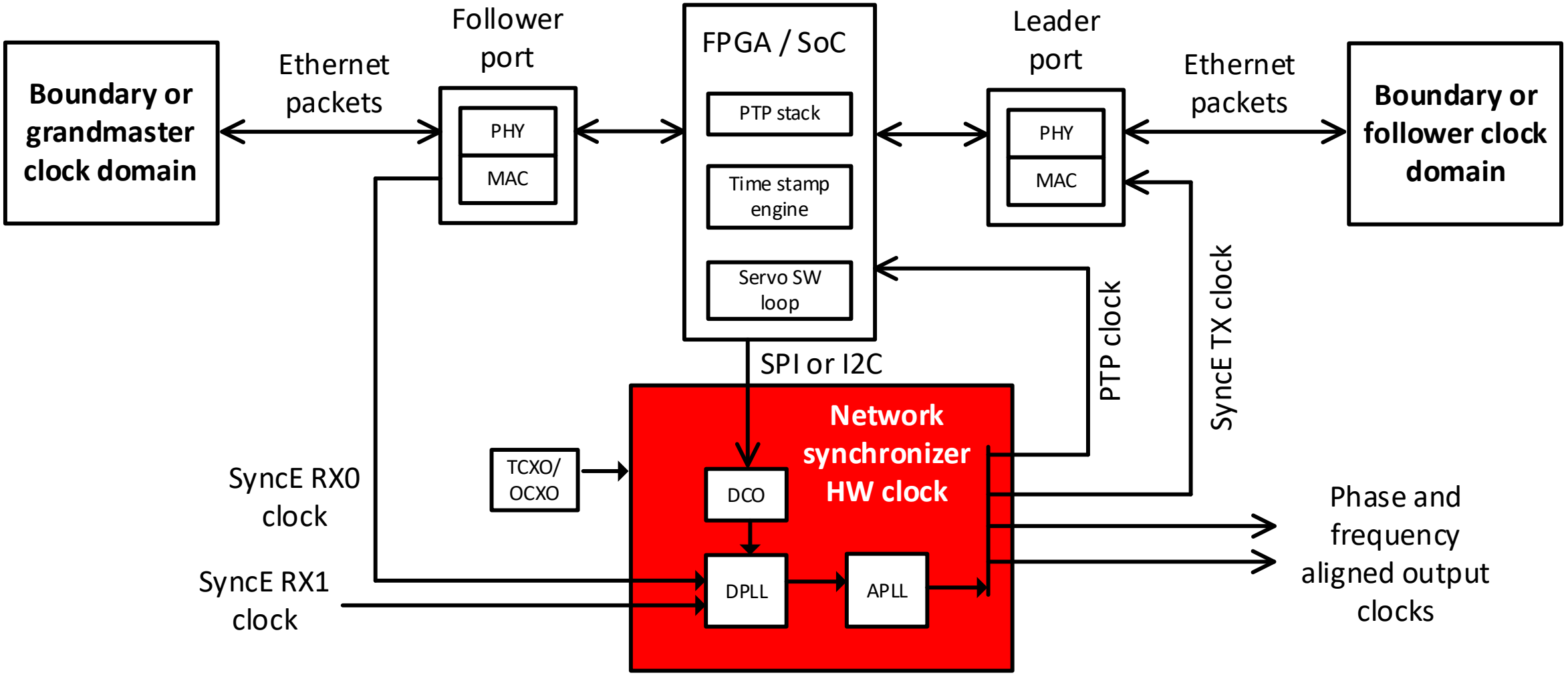
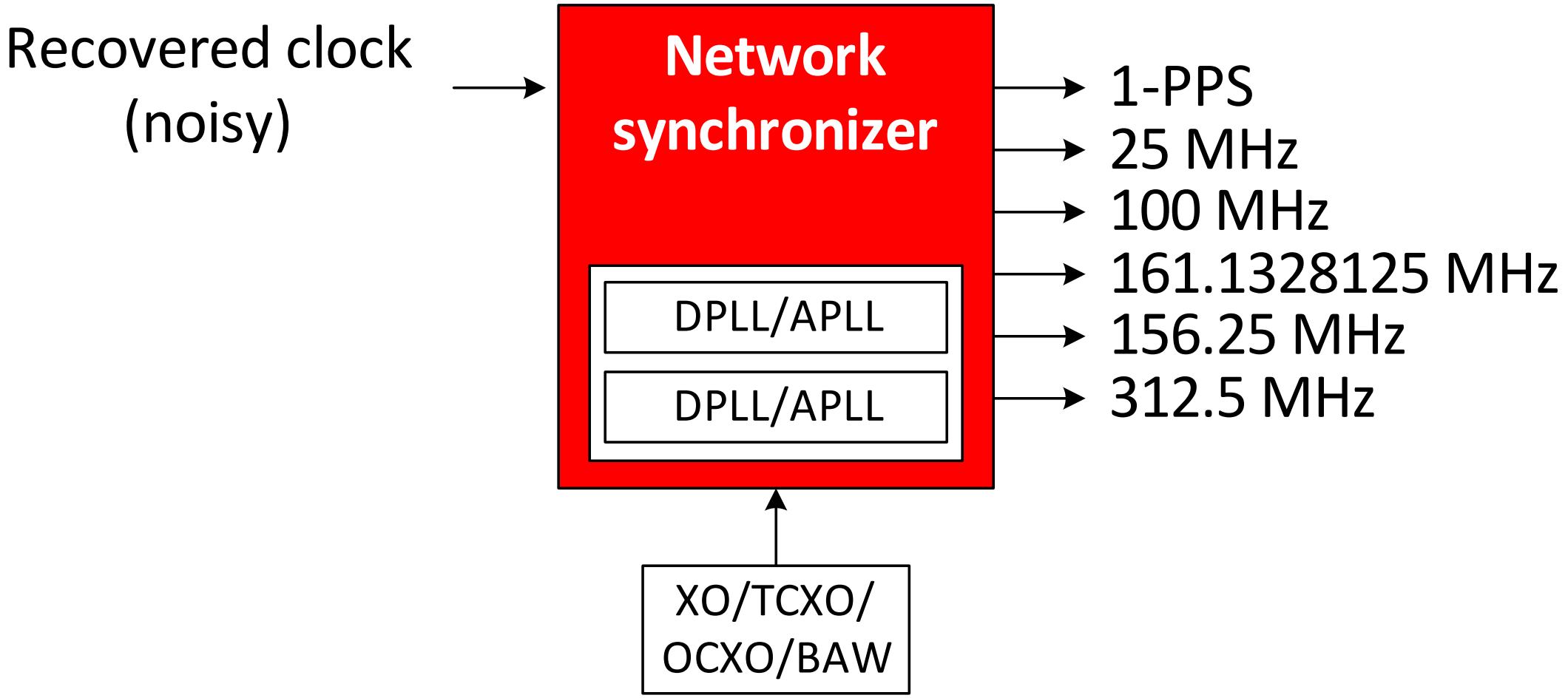
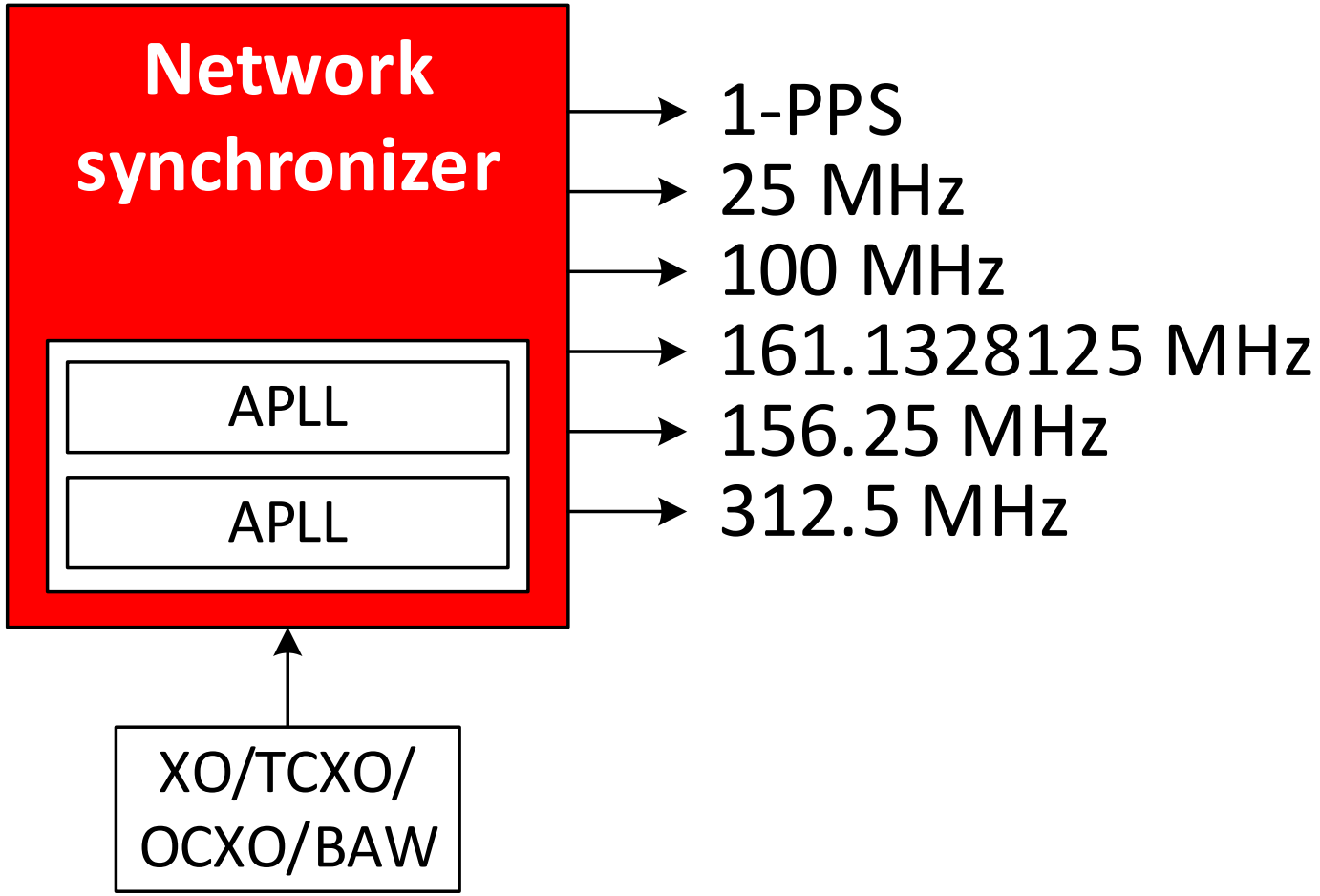
Boundary clock system example



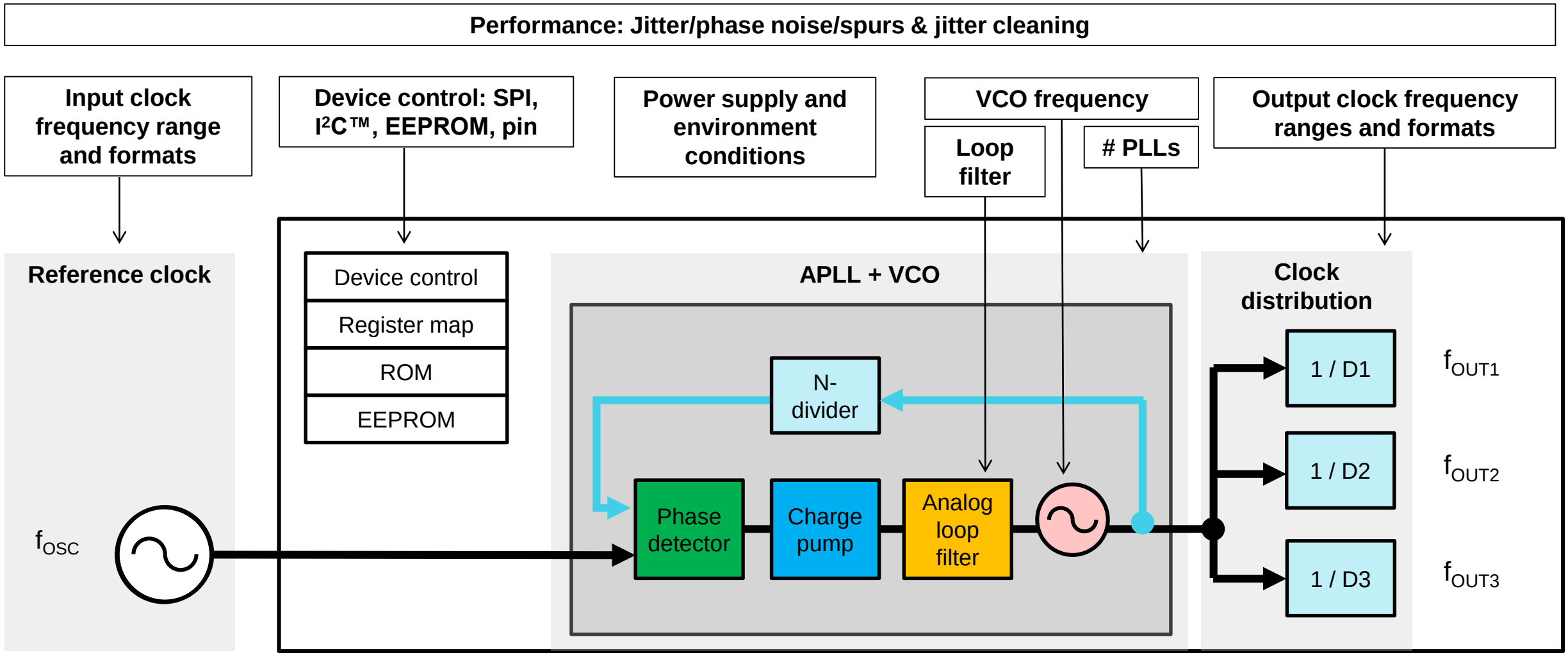
Network synchronizer as a jitter cleaner



Network synchronizer as a clock generator

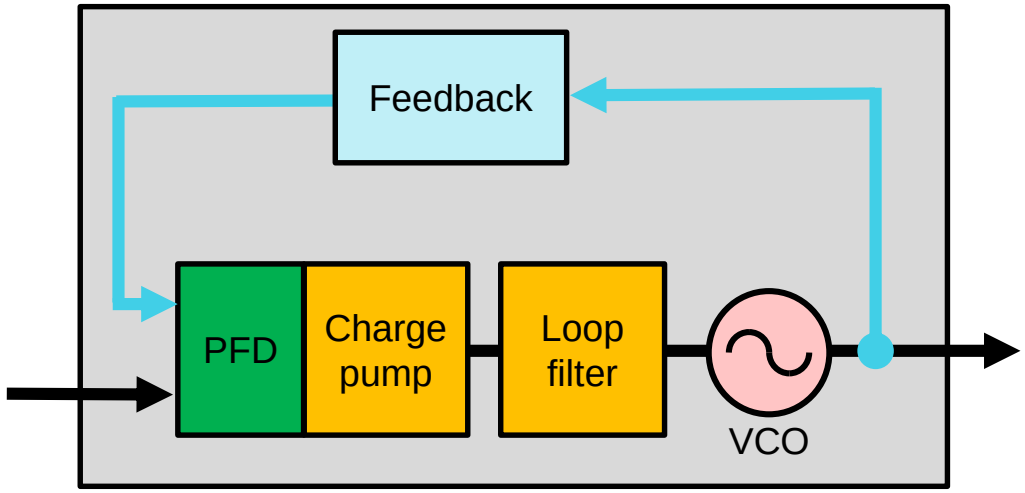


Key parameters and specs for clocking devices



APLL vs DPLL

Analog PLL (APLL)

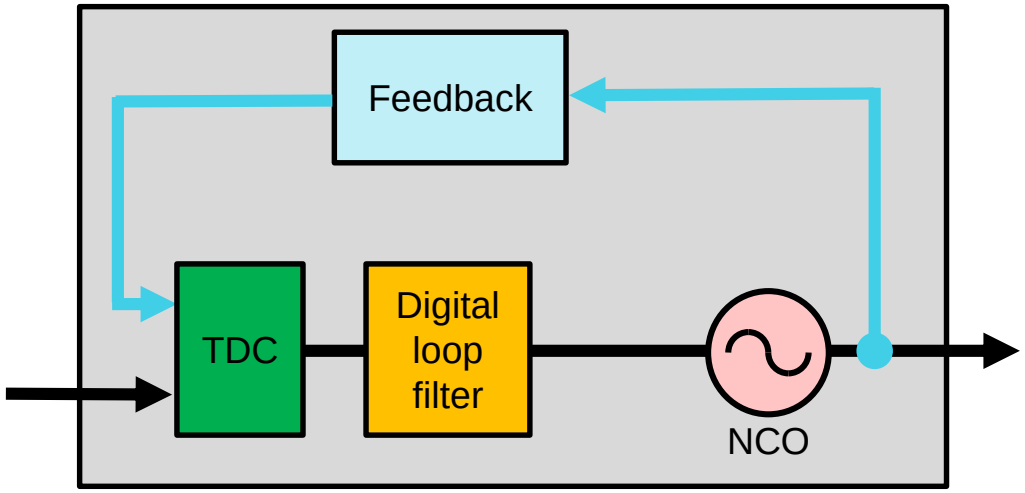


PFD (Phase frequency detector)

Charge pump and loop filter

VCO (Voltage controlled oscillator)

Digital (DPLL)



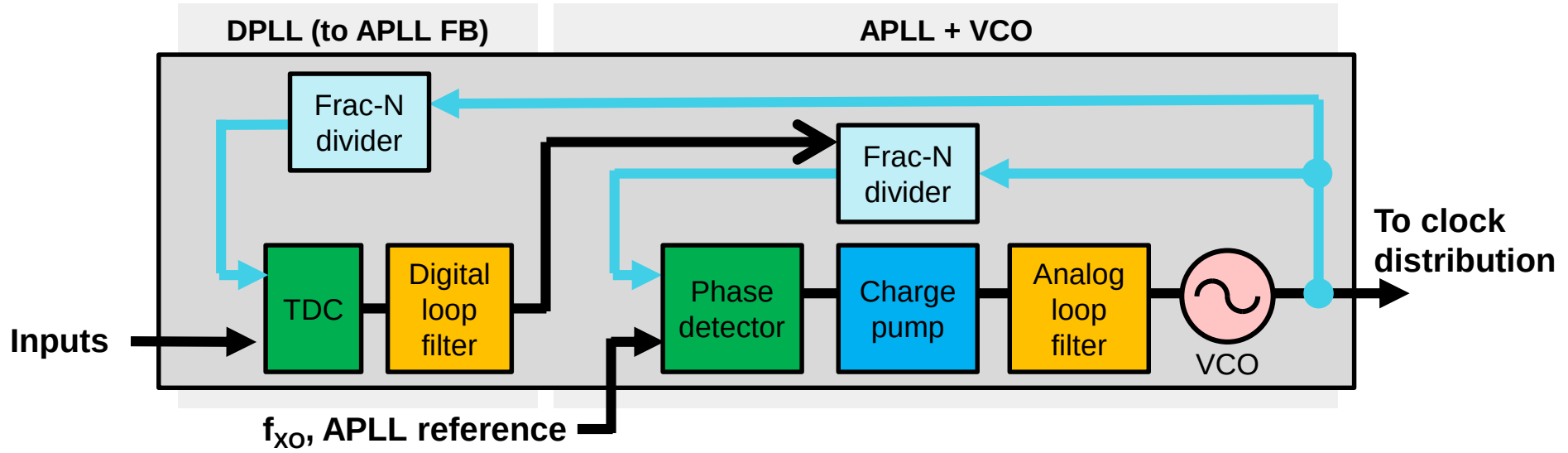
TDC (Time to digital converter)

Digital loop filter

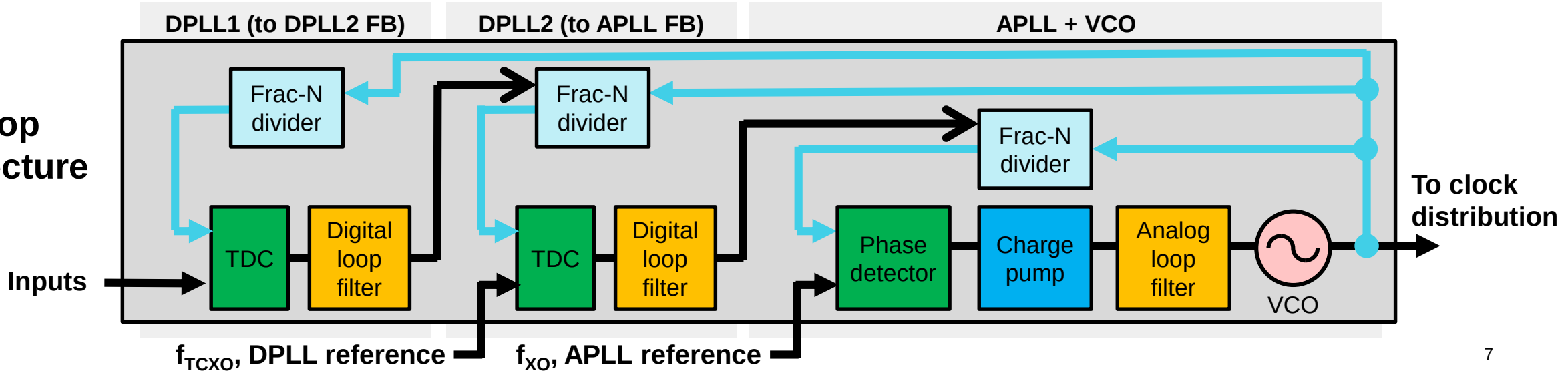
NCO (Numeric controlled oscillator)

DPLL architecture

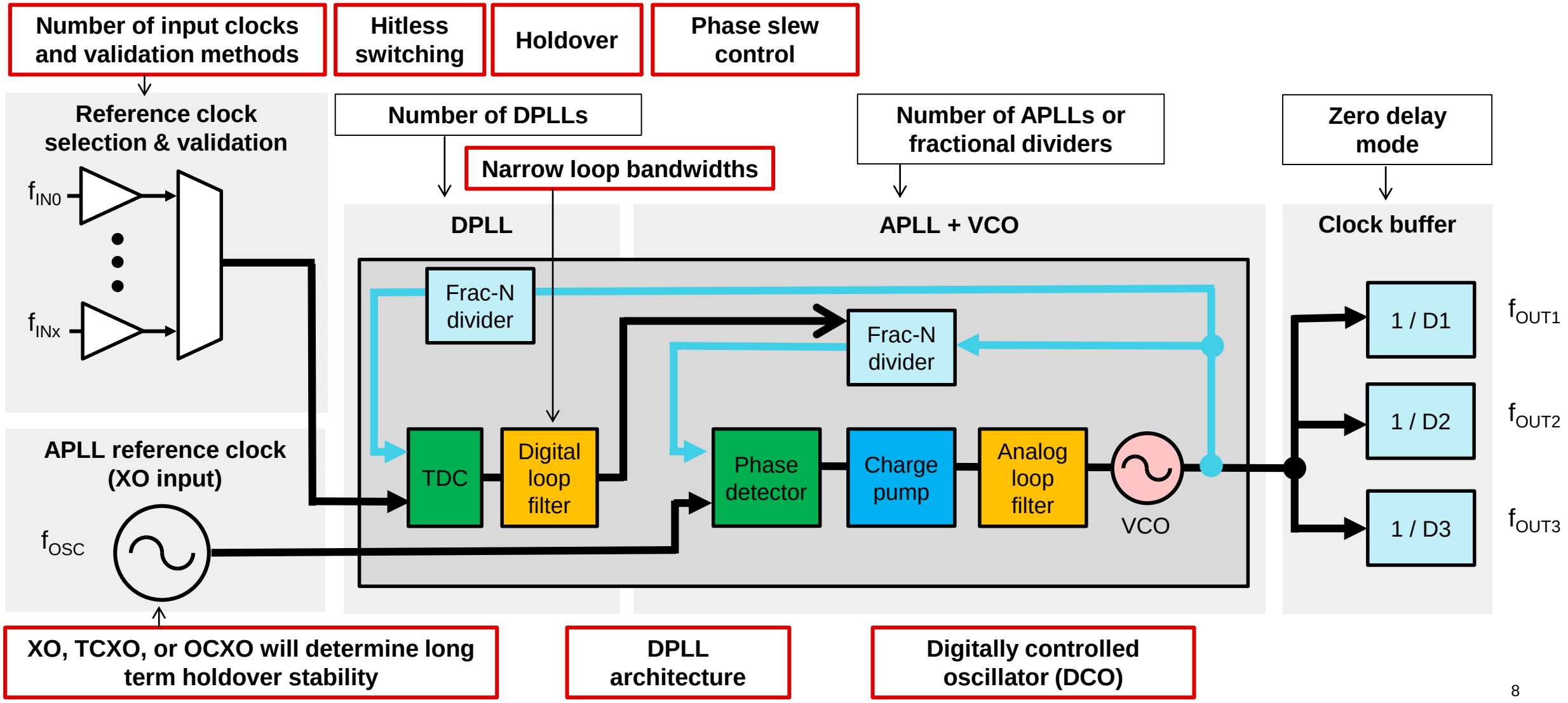
2-loop architecture



3-loop architecture

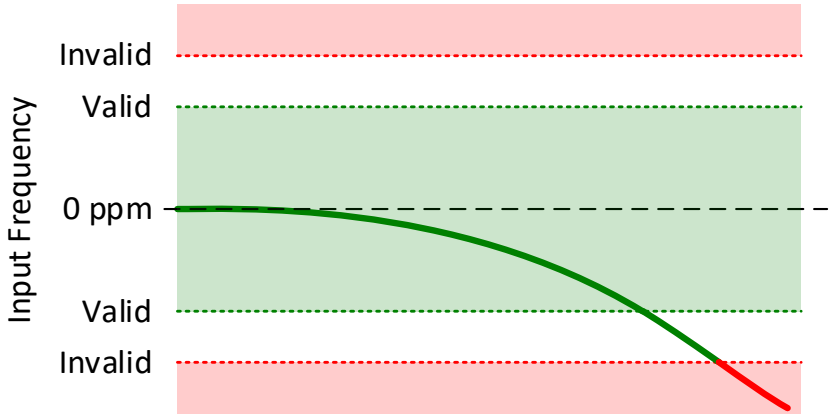


Key parameters and specs for network synchronizers

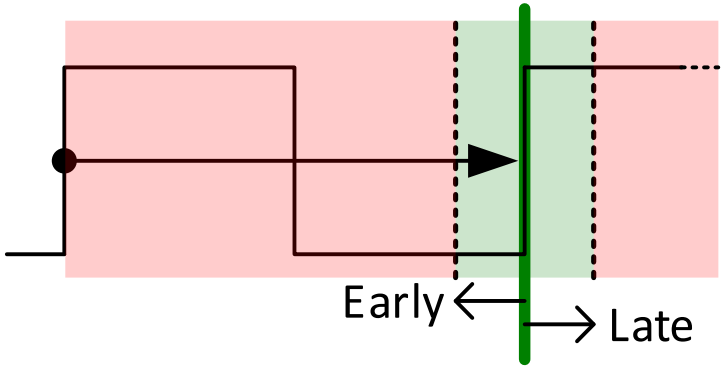


Input validation

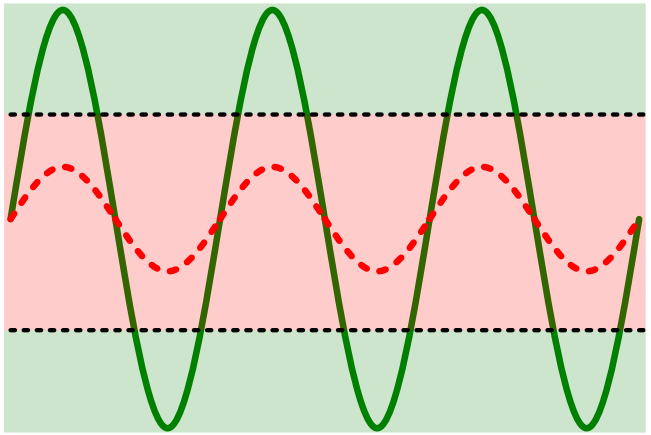
Frequency detect



Early/late clock detect

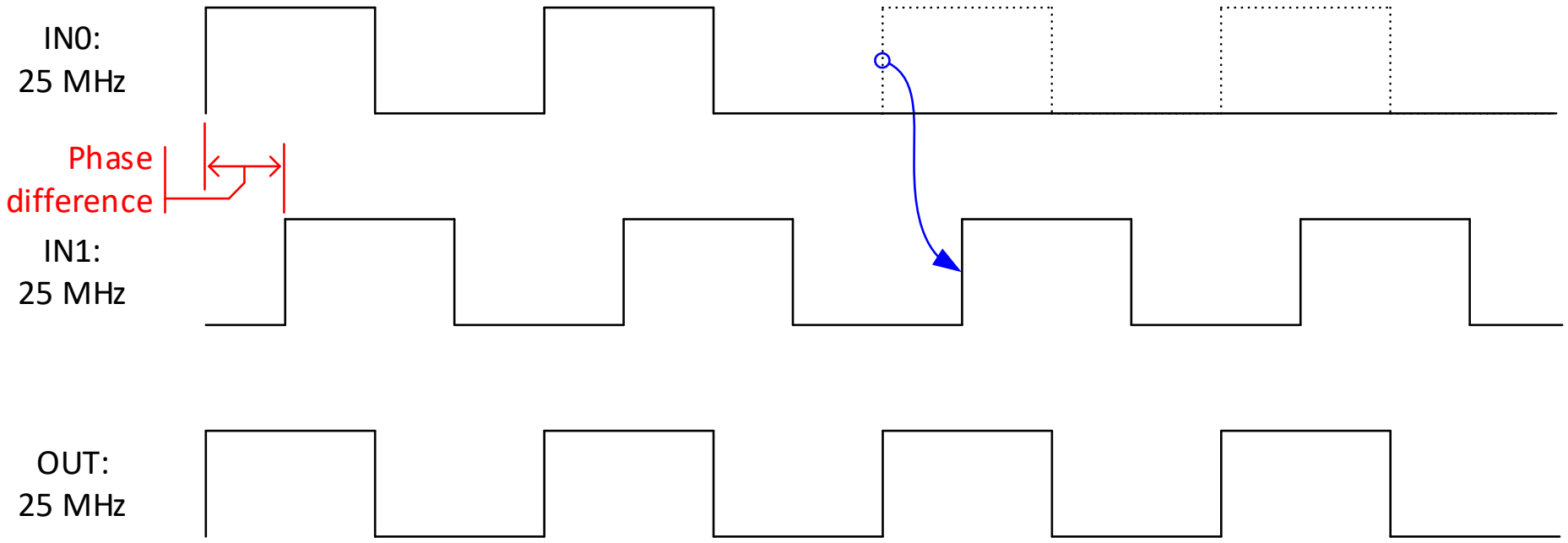


Amplitude detect



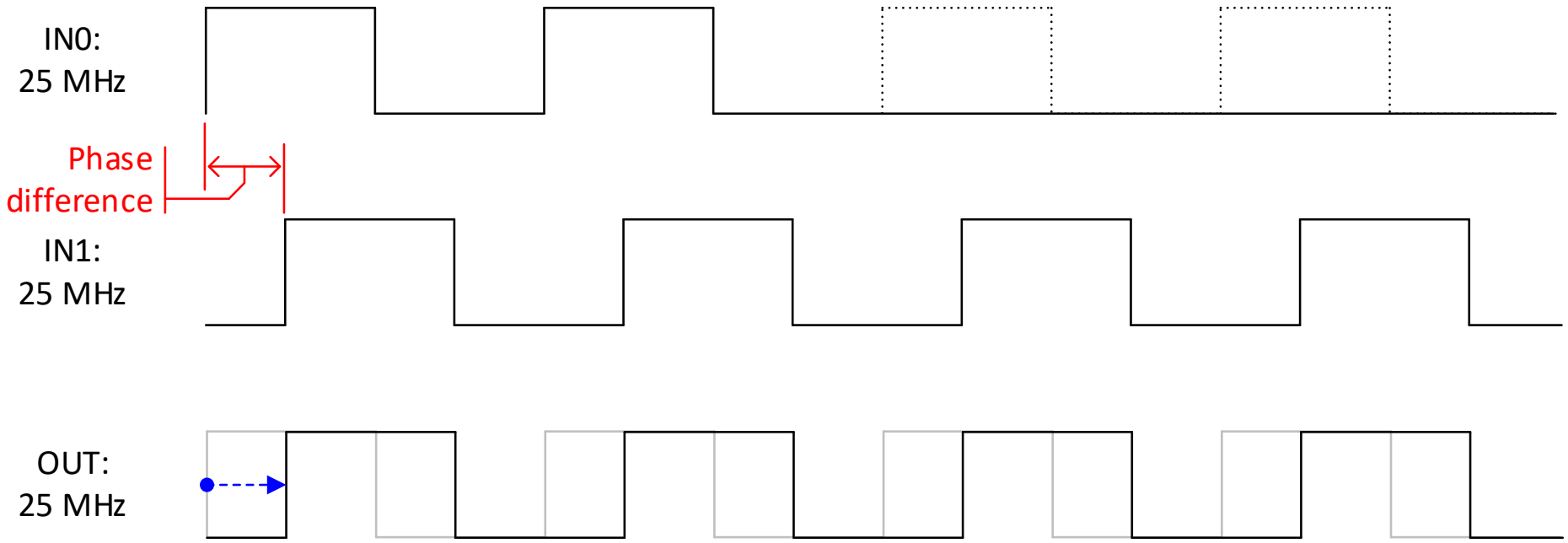
Hitless switching: phase build-out

What is the allowed phase and frequency variation during a clock switch event?



Hitless switching: phase slew control

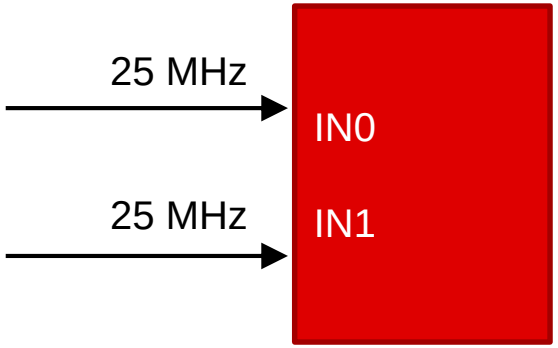
Does system require output clock phase to align with input clock phase?



Relationship of frequency error and phase slew rate of change:
1 ppm = 1 µs/s 1 ppb = 1 ns/s 1 ppt = 1 ps/s

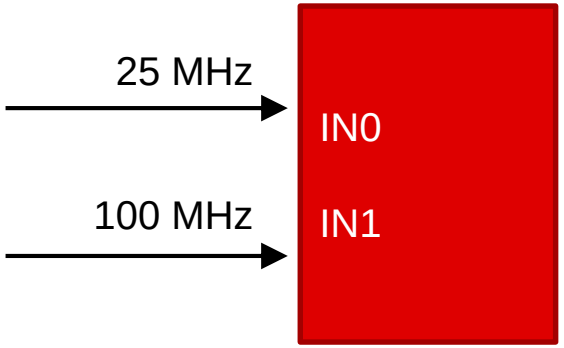
Hitless switching: input frequency flexibility

Same frequency



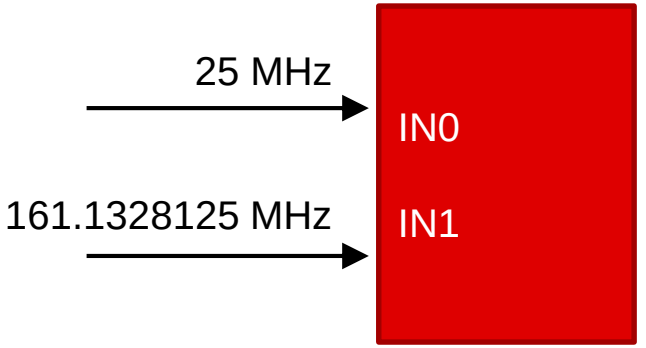
GCD of IN0 and IN1 is 25 MHz

Different frequencies, simple integer relationship



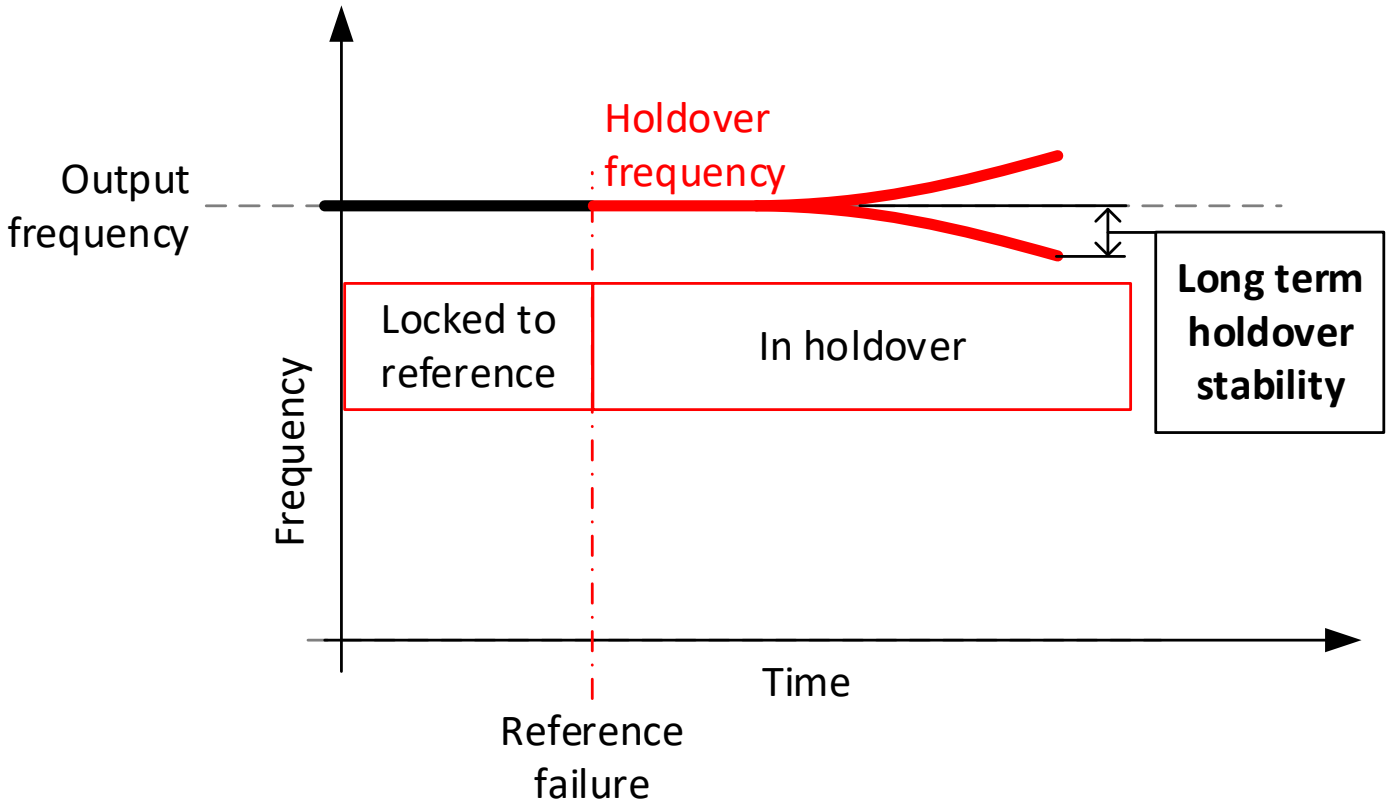
GCD of IN0 and IN1 is 25 MHz

Different frequency, poorly related frequencies



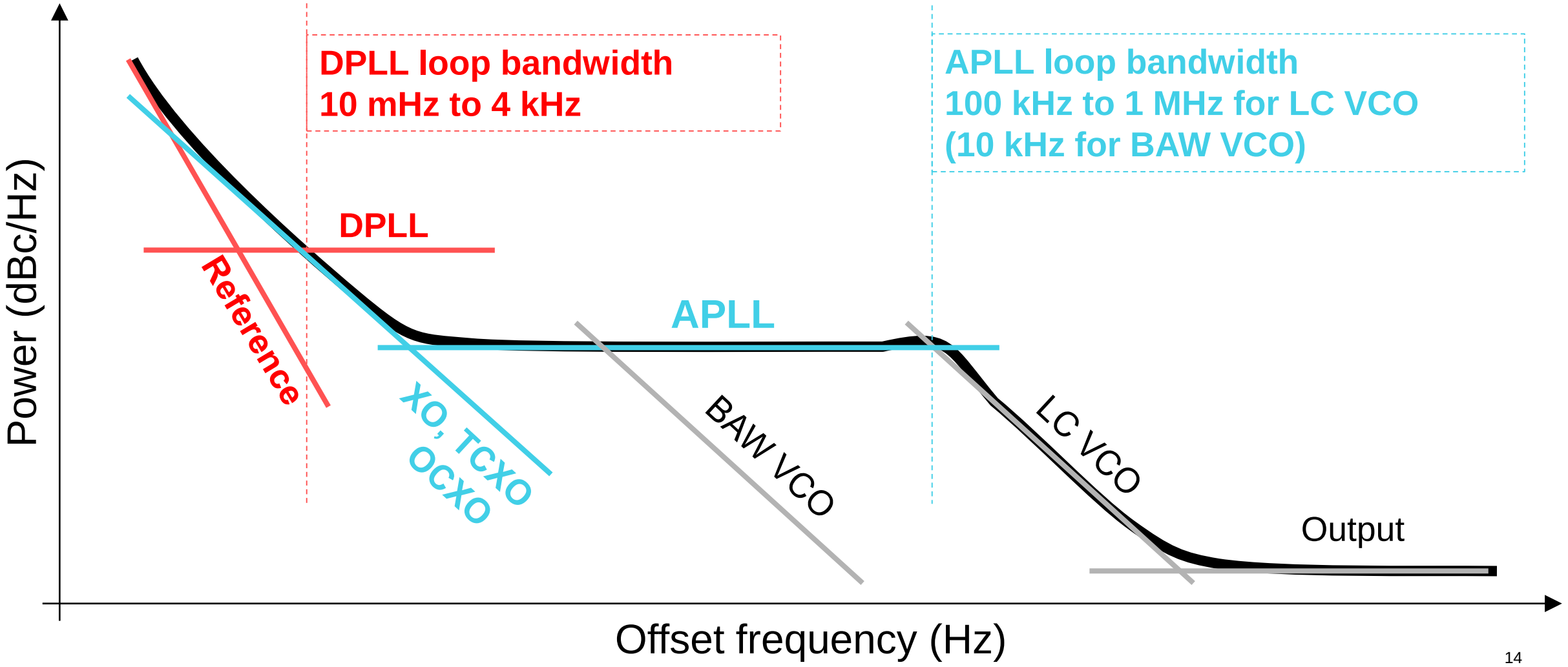
GCD of IN0 and IN1 is 195.3125 kHz

Long term holdover stability



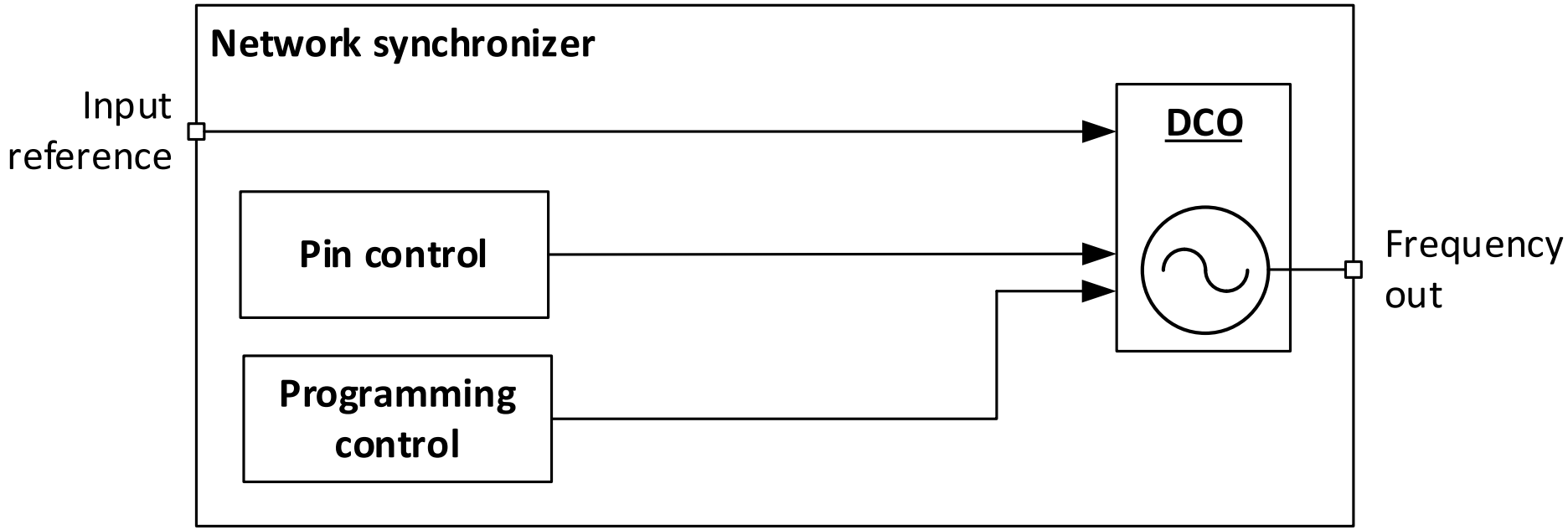
2-loop
architecture

Network synchronizer performance



Digitally controlled oscillator (DCO)

The digitally controlled oscillator feature allows the user to control the output frequency by making manual updates to the network synchronizer.



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Quiz

1. True or false: A network synchronizer can be used as a jitter cleaner or clock generator.
2. True or false: How the network synchronizer handles clock inputs is a significant feature of a network synchronizer.
3. True or false: Phase build-out prevents changing phase on network synchronizer reference input from propagating to output.
4. True or false: The long term holdover stability specification may depend on system components other than the network synchronizer itself.
5. True or false: DCO feature can be used to lock clock outputs to a time standard not provided to the reference input of the network synchronizer directly.

Quiz

1. True or false: A network synchronizer can be used as a jitter cleaner or clock generator.
   - True, the network synchronizer behaves as a jitter cleaner when the narrow loop bandwidth of the network synchronizer attenuates reference noise and “replaces it” with noise on the XO input. When operation without a reference, the network synchronizer behaves as a clock generator.
2. True or false: How the network synchronizer handles clock inputs is a significant feature of a network synchronizer.
   - True, hitless switching is a key feature of a network synchronizer.
3. True or false: Phase build-out prevents changing phase on network synchronizer reference input from propagating to output.
   - True, this phase change could come from a phase disruption from an upstream clock source or because of a switch between references provided to the network synchronizer directly.
4. True or false: The long term holdover stability specification may depend on system components other than the network synchronizer itself.
   - True, if the XO input is from an external device such as XO, TCXO, or OCXO then those specifications must be taken into consideration. However a network may also integrate this reference in which case long term holdover stability is fully a function of the network synchronizer.
5. True or false: DCO feature can be used to lock clock outputs to a time standard not provided to the reference input of the network synchronizer directly.
   - True, a logic device could perform serial communication writes to the network synchronizer or toggle pin states to cause the network synchronizer to lock to reference not provided to the network synchronizer inputs.