SAR REF Input: The Capacitive DAC (CDAC)

TIPL 4503
TI Precision Labs – ADCs

Created by Luis Chioye
Presented by Cynthia Sosa



Agenda

Reference Performance Specifications:

Initial Accuracy, Drift, Long Term Drift, and Noise

Overview of SAR REF Drive Topologies:

Reference standalone VS Buffered Reference

SAR ADCs with Internal Reference Buffer

SAR REF Input Overview: The Capacitive DAC (CDAC)

Build TINA REF Input Model for a SAR:

Discrete Charge Model

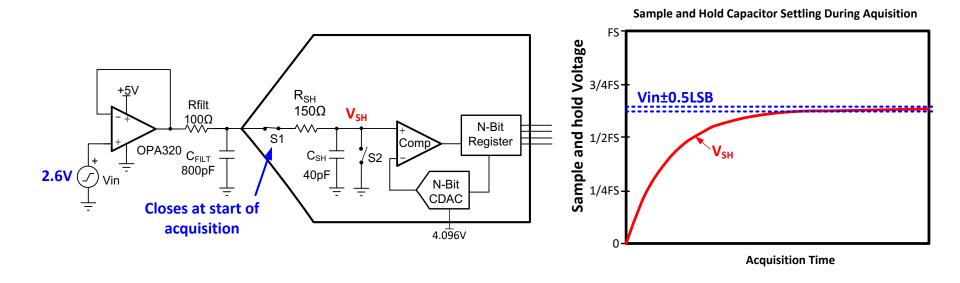
TI Device Specific Model

SAR REF Drive Circuit Design:

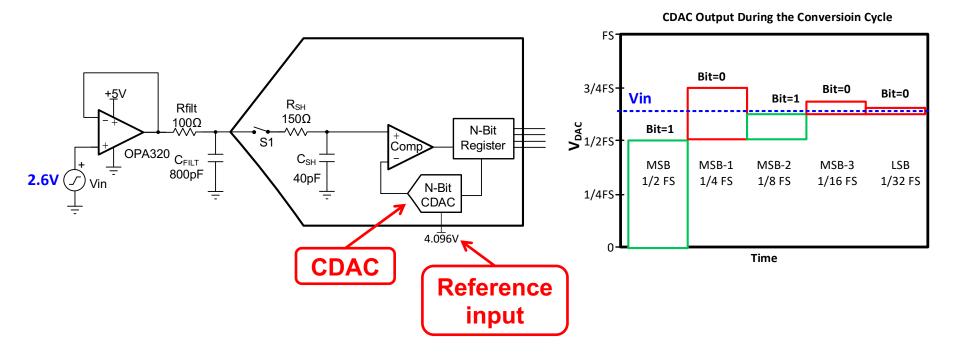
Reference Bypass Capacitor

Reference Buffer Stability and Compensation

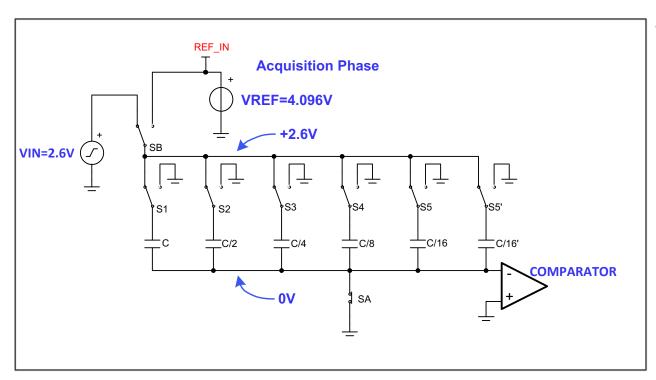
Acquisition phase

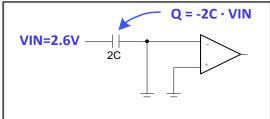


Conversion Phase

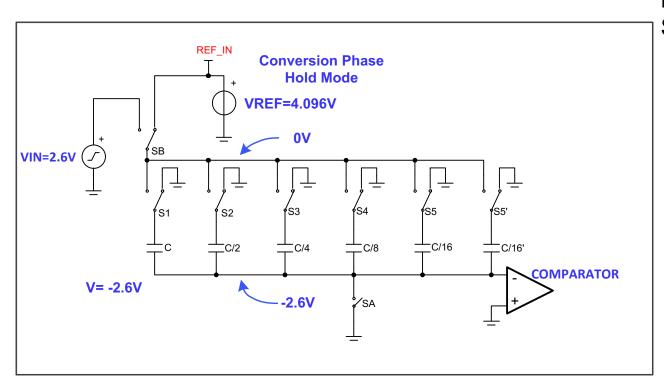


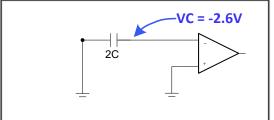
SAR ADC Architecture: The Capacitive DAC (1)



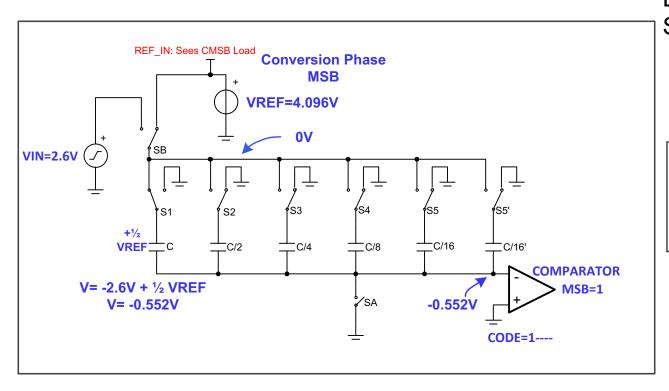


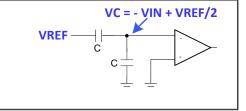
SAR ADC Architecture: The Capacitive DAC (2)



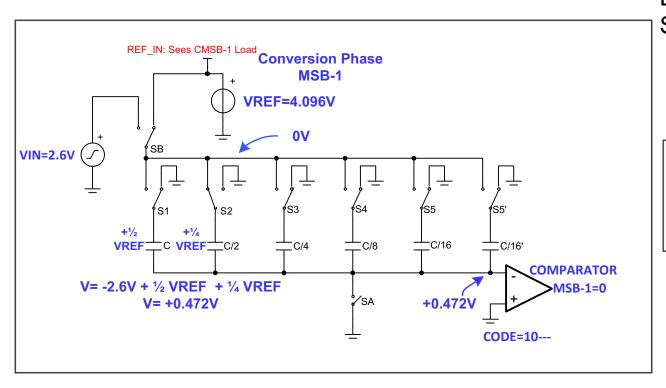


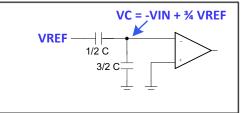
SAR ADC Architecture: The Capacitive DAC (3)



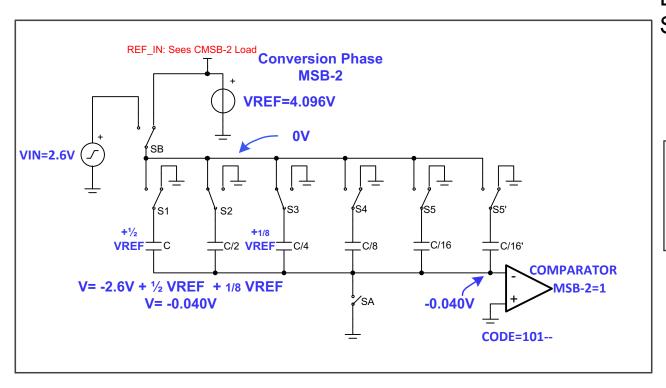


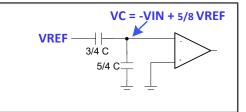
SAR ADC Architecture: The Capacitive DAC (4)



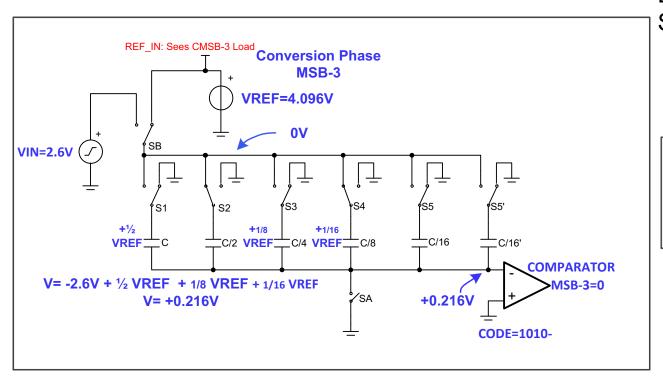


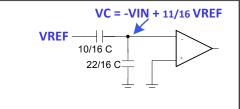
SAR ADC Architecture: The Capacitive DAC (5)



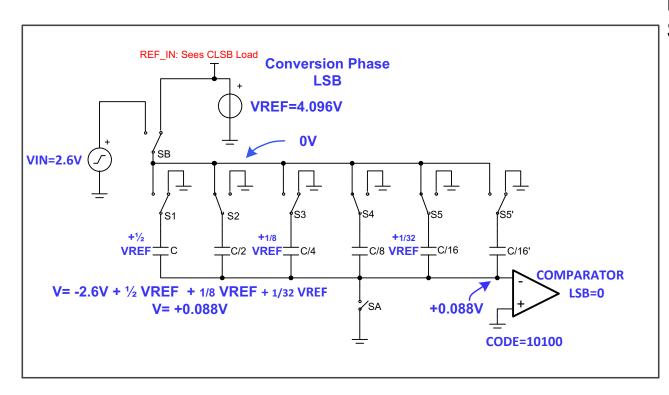


SAR ADC Architecture: The Capacitive DAC (6)

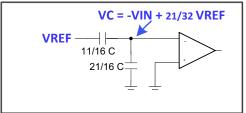




SAR ADC Architecture: The Capacitive DAC (7)



Based on TLV- Series SAR ADCs



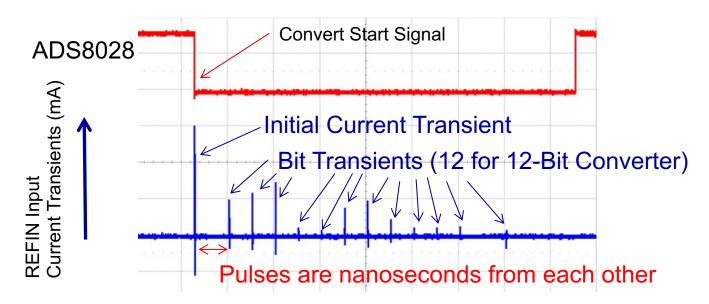
Thomas Kulgelstad:

The operation of the SAR-ADC based on charge redistribution,

Analog Applications Journal (slyt176), Texas Instruments, February 2000.

SAR ADC Architecture

- The Reference is sampled several times during each conversion
- High-current transients (~10's mA range) are present in this REF input where the ADC's internal capacitor array is switched and charged as the bit decisions are made.
- Current transient pulses occur only a few nanoseconds away of each other during conversion.



Thanks for your time! Please try the quiz.



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