

$\Delta\Sigma$ Digital Filters and Latency

TIPL 4011

TI Precision Labs – ADCs

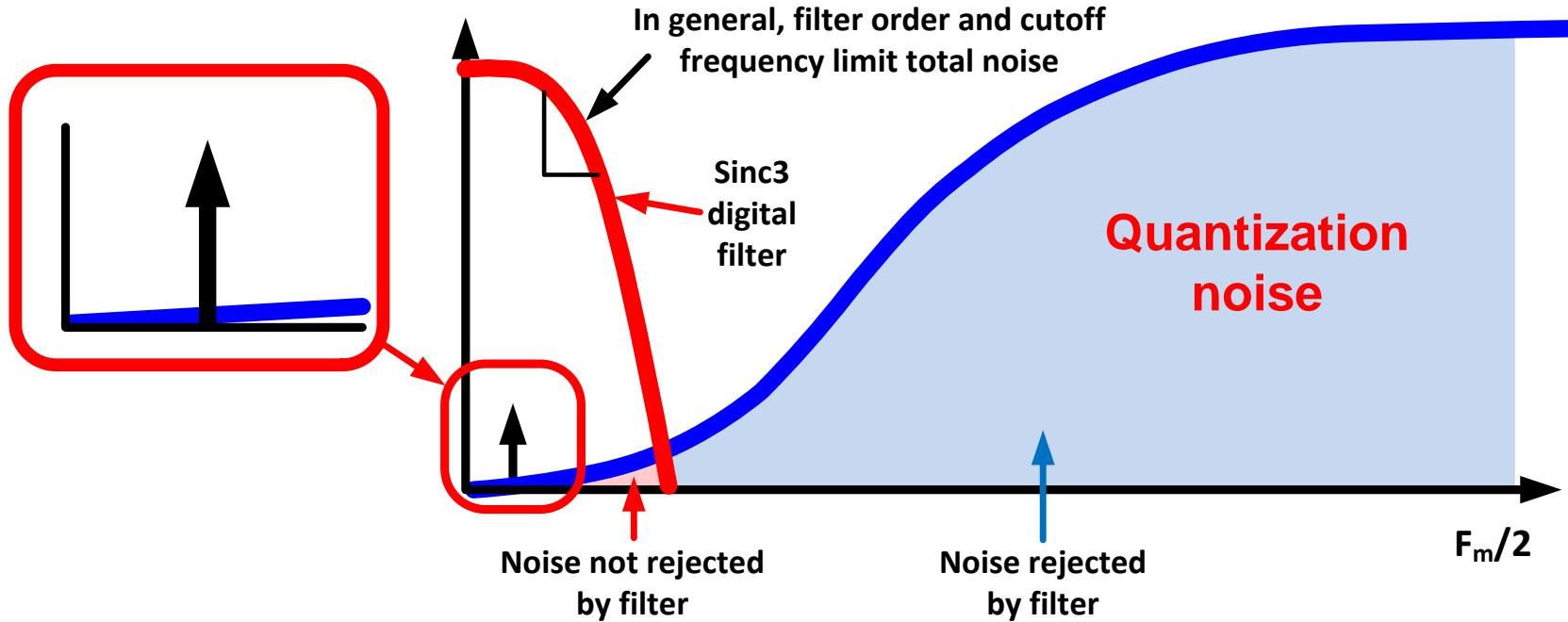
Created by Art Kay and Ryan Andrews

Presented by Ryan Andrews



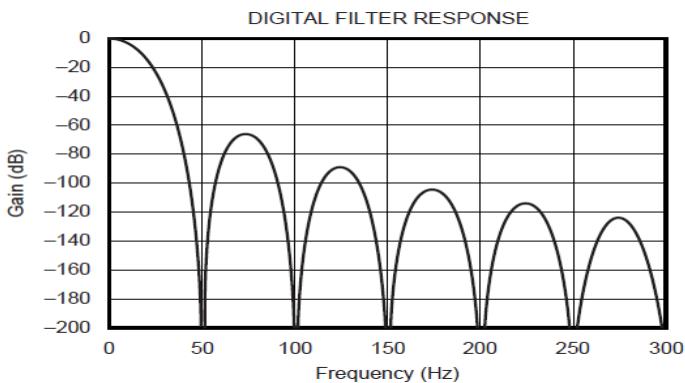
Texas Instruments

Digital Filter in $\Delta\Sigma$ to Minimize Quantization Noise

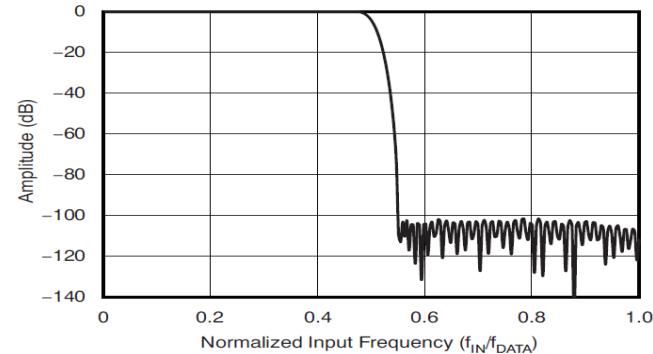


Digital Filter

- Latency is the delay between when the input signal is applied and the ADC is settled
- “Sinc” is a common low latency filter type
- “Flat Passband” is a typical high latency type filter.



Sinc Filter (Low Latency)



Flat Passband Filter (High Latency)

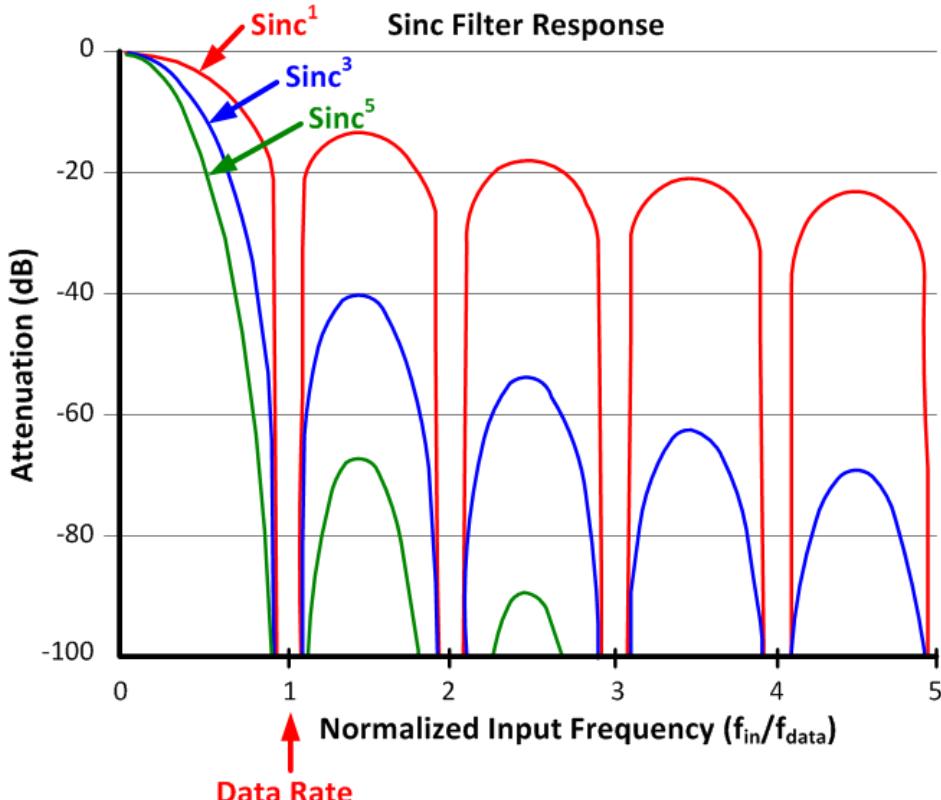
Low Latency Sinc Digital Filter

Advantages

- Low latency gives low “settling time”
- Less silicon area, easy to implement
 - Low cost, Low power
- Order refers to slope of roll-off
 - Number Cycles = Sinc order
 - Notches at multiples of data rate
- Filter notches can target specific frequencies (ex. 50/60 Hz)
- Good for dc measurements

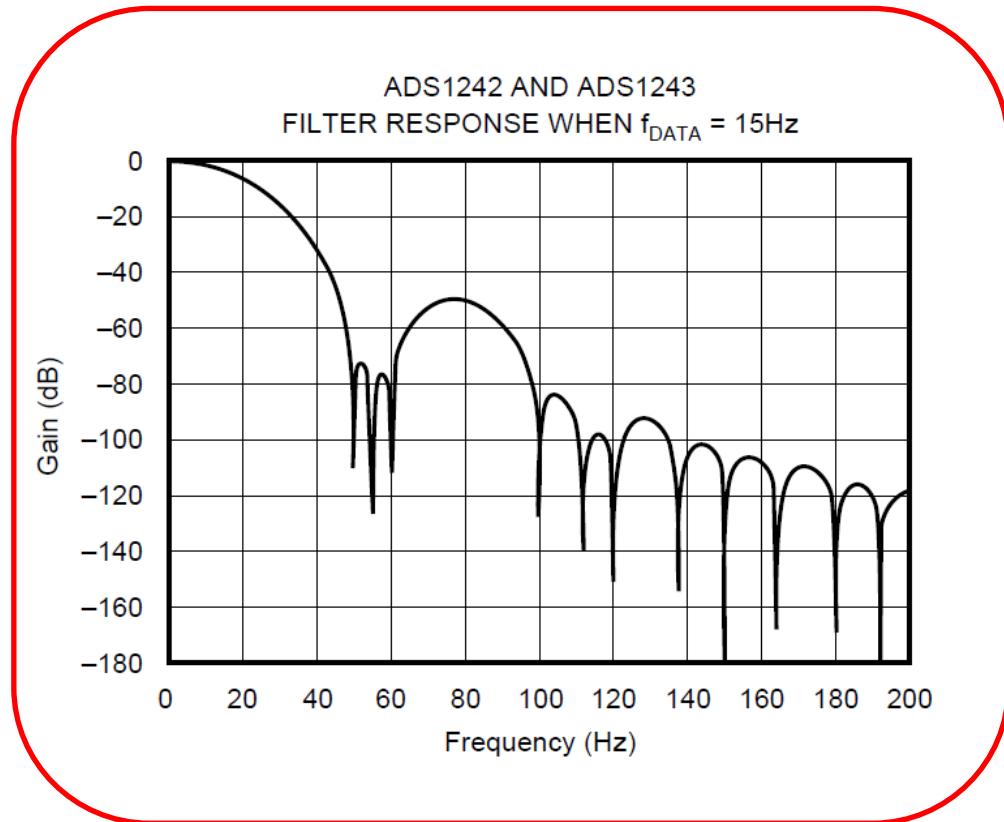
Disadvantages

- Pass band droop-limit to low frequency
- Weak Stop band attenuation



Low Latency FIR Digital Filter

- FIR = Finite Impulse Response
- Technically Sinc is an FIR filter
- This response is different than a typical Sinc
- This type of FIR filter has at double notch that keeps the attenuation good at both 50 and 50Hz.
- Sinc filter has notches that repeat at multiples of data rate



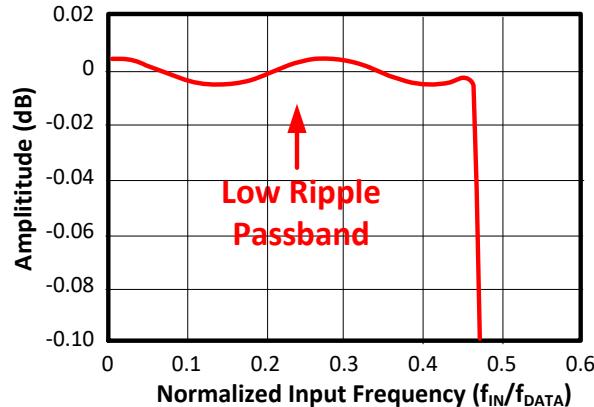
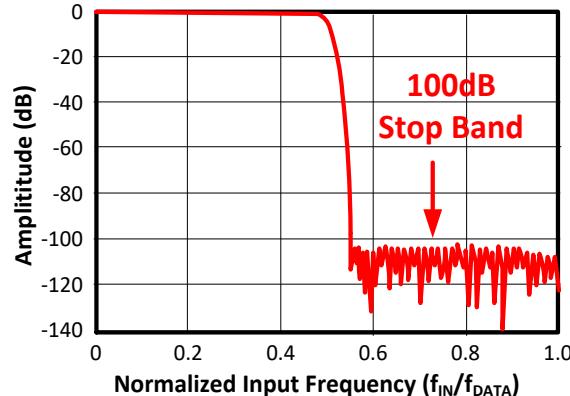
High Latency: Flat Pass Band Filter

Advantages

- Frequency Response
 - Very low ripple pass band
 - Sharp Nyquist transition band
 - Large stopband attenuation: lower than -100dB (simplify aliasing requirement)
- Frequency response scalable with data rate

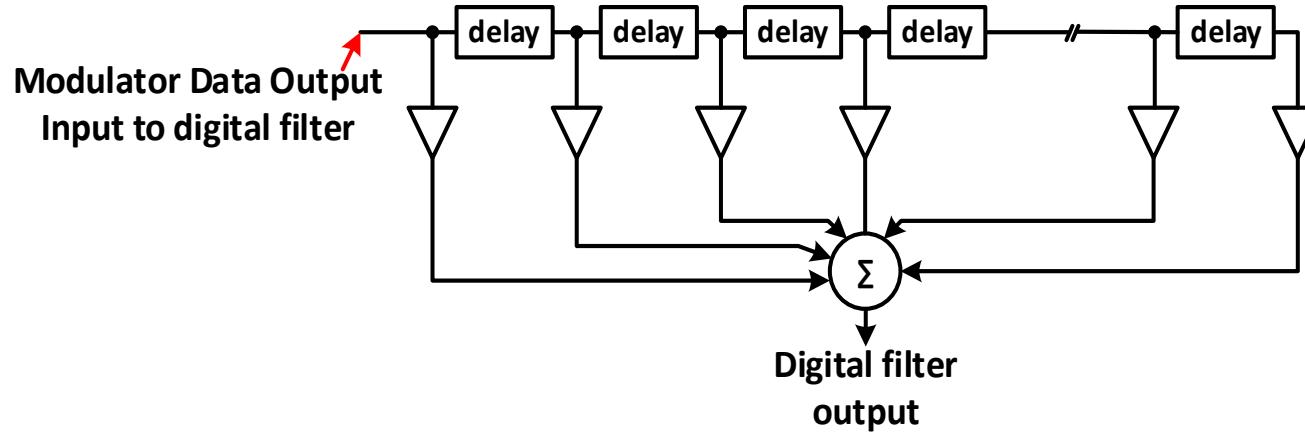
Disadvantages

- Multi-order / high tap filter – Large latency (e.g. 55 cycles)
- Large area – Costly

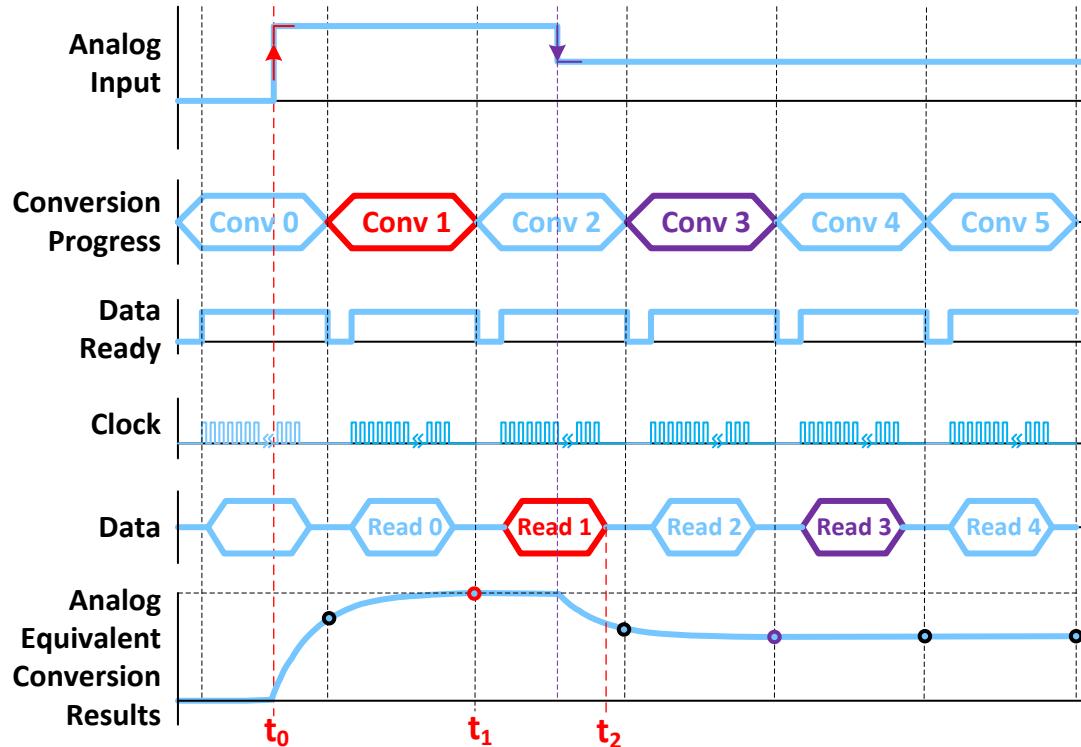


Filter topology – What causes latency?

- The latency of the filter depends on the number of delay blocks used
- Sinc filters are very efficient → minimum number of delay blocks
- Flat Passband filters require a lot delay blocks to maintain desired AC response
 - Example: ADS1672 requires 55 cycles to settle



Sinc 1: Latency Communications Example



Settling for Sinc 1 $\Delta\Sigma$

t_0 – analog input transitions and settles to constant

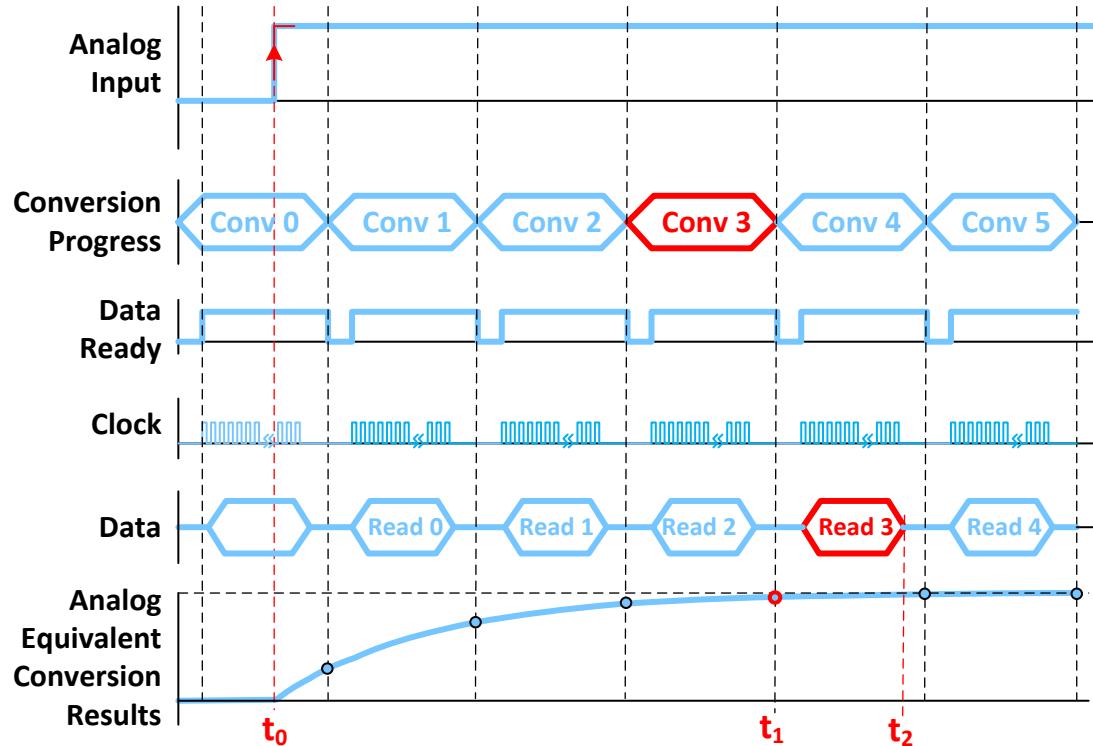
t_1 – Internal conversion fully settled after 1 cycle (Sinc1)

t_2 – Read of internal conversion 1 complete

Note: the same process can be applied to the second (purple) input transition



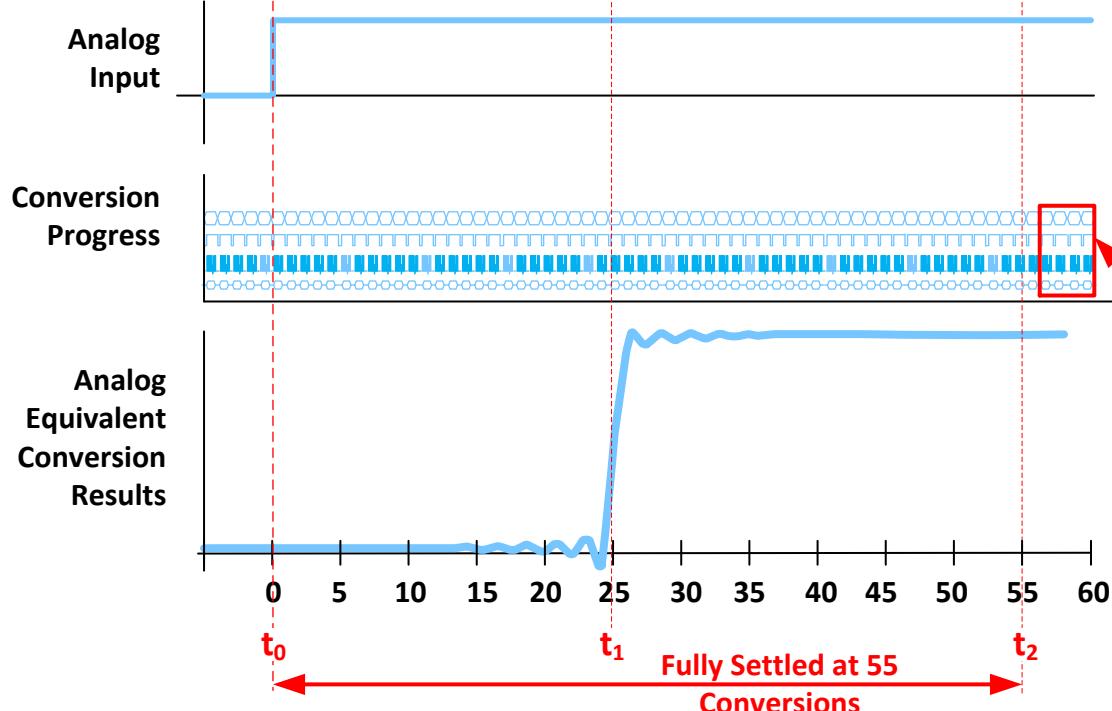
Sinc 3: Latency Communications Example



Settling for Sinc3 $\Delta\Sigma$

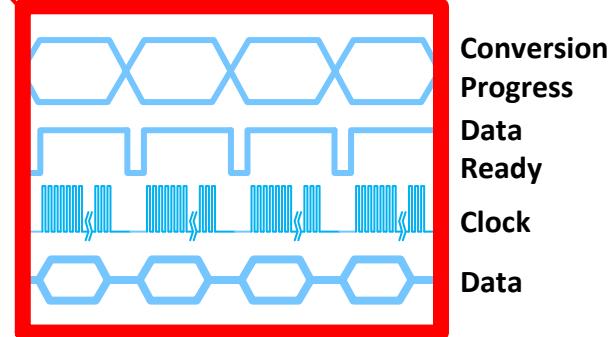
- t_0 – analog input transitions and settles to constant
- t_1 – Internal conversion fully settled after 3 cycles (Sinc3)
- t_2 – Read of internal conversion 3 complete

Flat Passband: Latency Communications Example



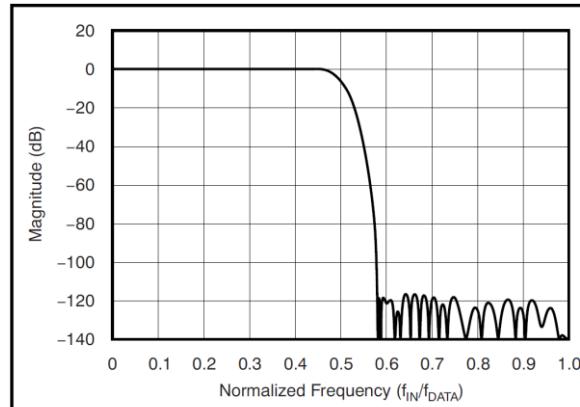
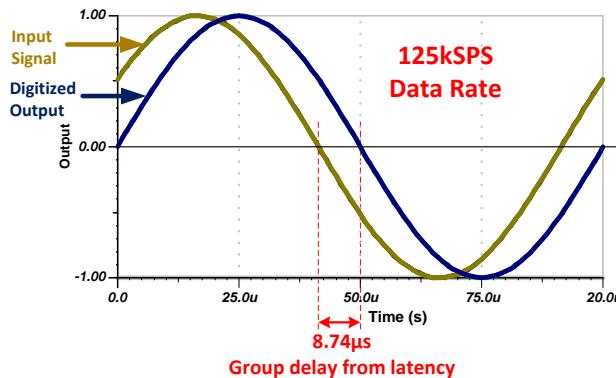
Settling for Flat Passband $\Delta\Sigma$

- t_0 – analog input transitions and settles to constant
- t_1 – Internal conversion propagates through by about 28 cycles
- t_2 – Internal conversion fully settled after 55 cycles



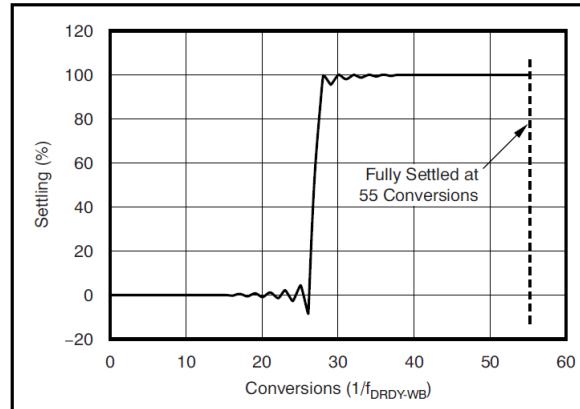
Flat Passband: Data Sheet Excerpt ADS1675

Data Rate (kSPS)	-3dB BW (kHz)	Settling Time		Group Delay	
		(μ s)	Cycles	(μ s)	Cycles
125	59.375	17.48	55	8.74	28
250	118.75	9.38	55	4.69	28
500	237.5	5.48	55	2.74	28
1000	475	3.63	55	1.82	28
2000	950	2.76	55	1.38	28
4000	1900	2.39	55	1.20	28

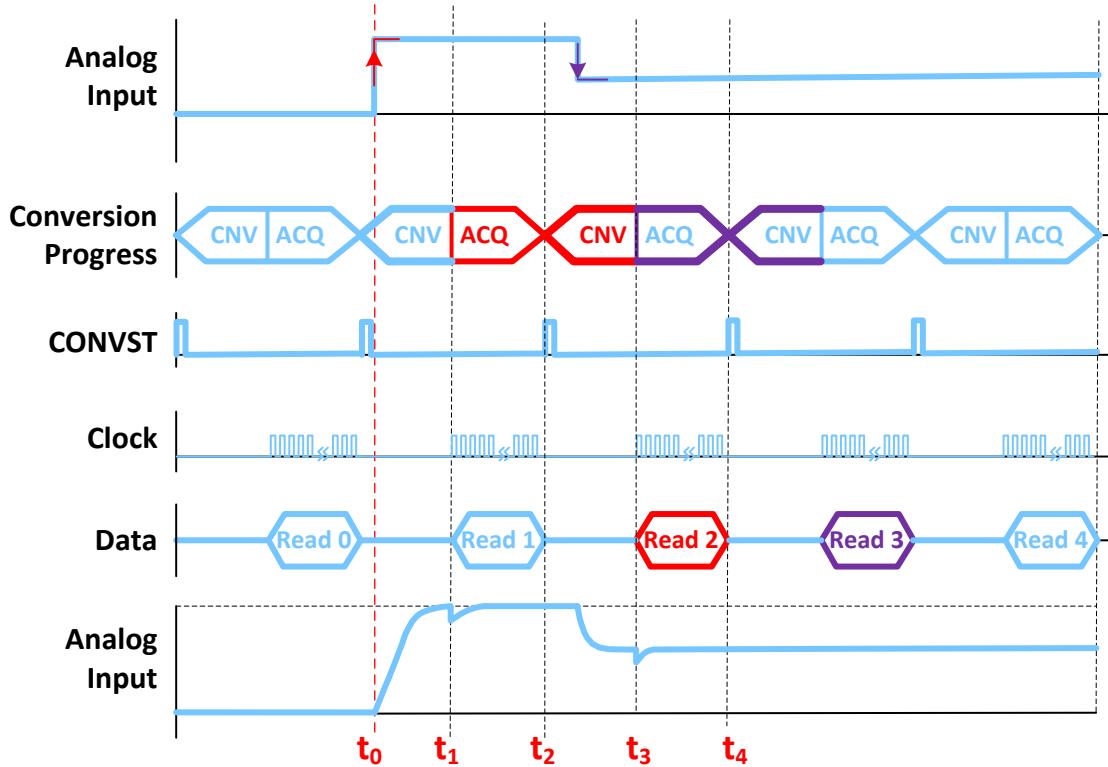


Flat Passband $\Delta\Sigma$

- Sine wave has a group delay
- Step input has delay and settling
- Full settling can take many conversion cycles



SAR latency



Settling for SAR

- t_0 – analog input transitions
- t_1 – start of acquisition cycle
- t_2 – End of acquisition. Analog sample and hold settled. Start of conversion cycle.
- t_3 – End of conversion cycle. Voltage from t_0 conversion complete. Start to clock out conversion results
- t_4 – Conversion results from t_0 fully clocked out (Read 2).

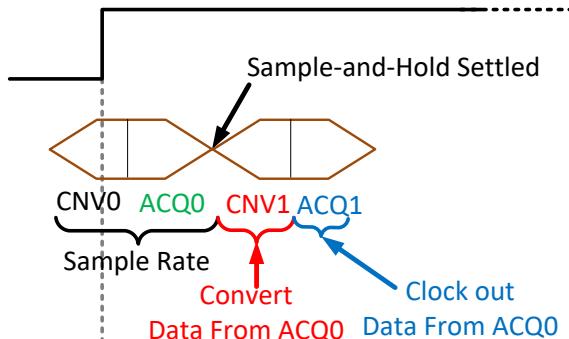


Latency Comparison: SAR vs Delta-Sigma

SAR

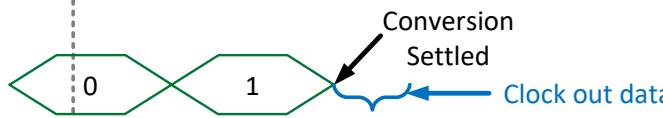
Input step change

Number of cycles settling = 1
“Zero cycle latency”

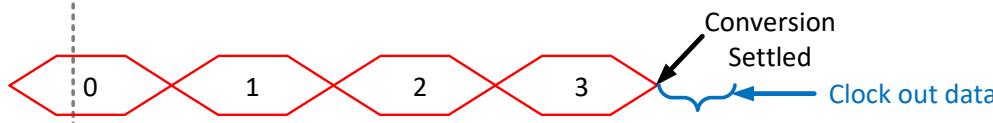


Delta-Sigma

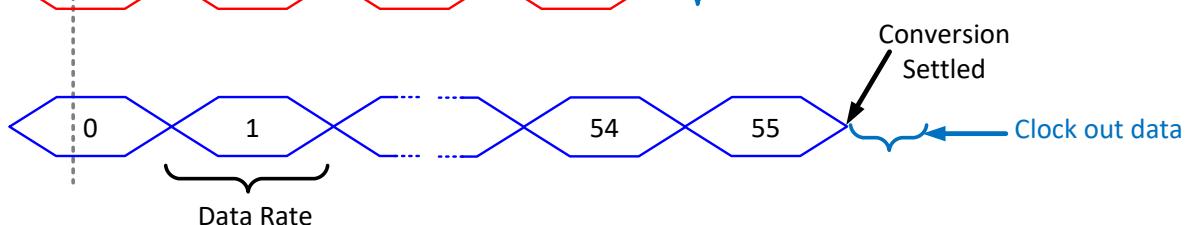
Sinc¹ Digital filter
Number of cycles settling = 1



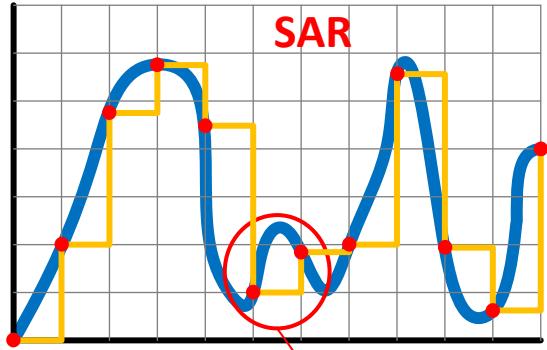
Sinc³ Digital filter
Number of cycles settling = 3
Settling time = data_rate x 3



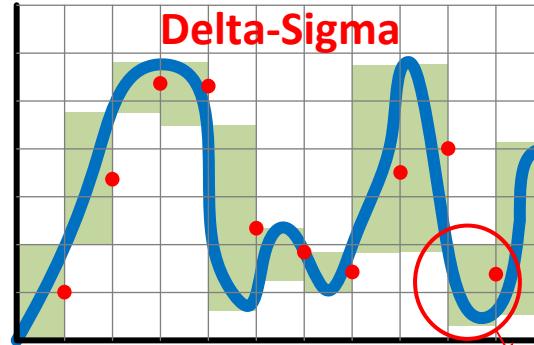
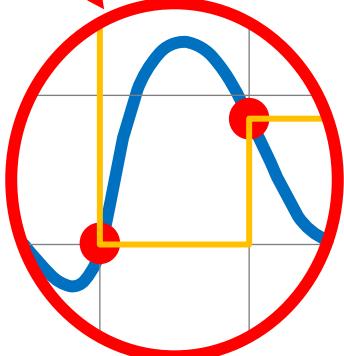
Flat Passband Digital filter
Number of cycles settling = 55
Settling time = data_rate x 55



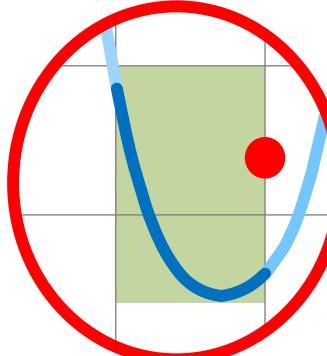
SAR vs Delta-Sigma Sampling transient signal



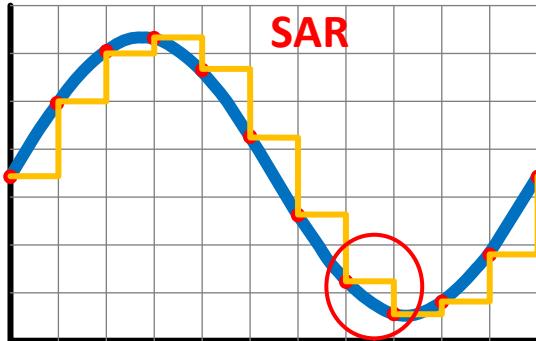
SAR:
Red dot indicates
the “snap-shot”
captured



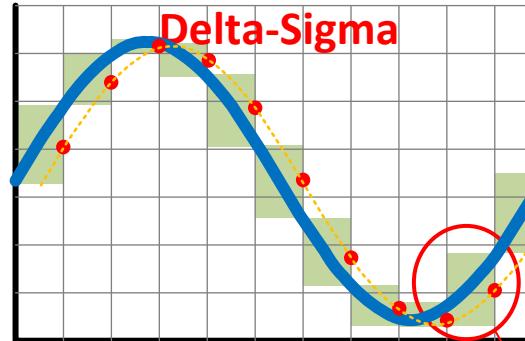
Delta-Sigma:
Red dot indicates
the average of the
signal in the green
sampling interval



SAR vs Delta-Sigma Sampling periodic signal

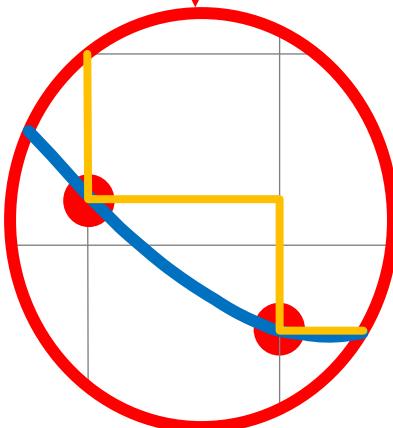


SAR

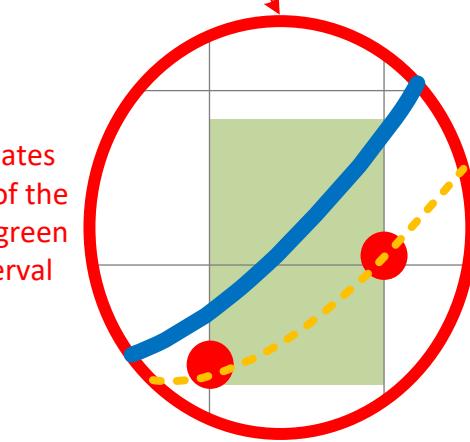


Delta-Sigma

SAR:
Red dot indicates
the “snap-shot”
captured



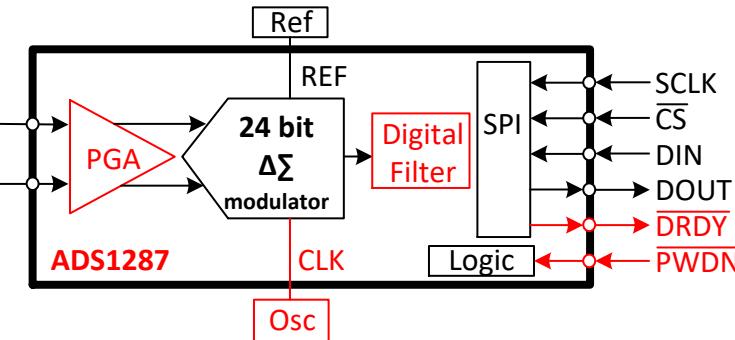
Delta-Sigma:
Red dot indicates
the average of the
signal in the green
sampling interval



Summary of differences between SAR & $\Delta\Sigma$

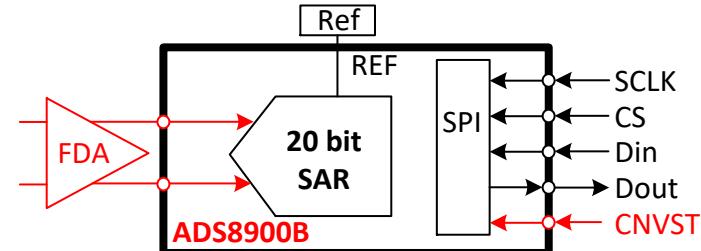
$\Delta\Sigma$ Block diagram

- Master clock for modulator
- Data-ready (/DRDY) tells controller when conversion is done
- Data rate lower than modulator rate
- Power-down (/PWDN) control
- Integrated PGA common
- Integrated digital filter



SAR Block diagram

- No master clock
- Controller uses Convert Start (CNVST) to sets timing
- Data rate = input sample rate
- Typically in “power down” state automatically when idle
- Amplifier typically external



**Thanks for your time!
Please try the quiz.**



TEXAS INSTRUMENTS

Questions: Digital Filters and Latency

1. Which filter has the longest latency?

- a. Sinc1
- b. Sinc3
- c. Flat Passband (FIR)

2. (T/F) The flat passband (FIR) filter can have a notch to eliminate 60Hz noise.

- a. True
- b. False

Questions: Digital Filters and Latency

3. Which of the following is not an advantage of the flat passband filter?
 - a. Large stopband attenuation (Attenuation > 100dB)
 - b. Less silicon area, easy to implement (lower cost)
 - c. Very low ripple (Ripple < 0.1dB)
 - d. Sharp Nyquist transition (i.e. high order filter)
4. (T/F) The group delay is approximately equal to half the settling time for a flat passband filter?
 - a. True
 - b. False

Questions: Digital Filters and Latency

5. Which type of converter uses the data-ready pin to indicate that the conversion is complete?
 - a. Delta-Sigma
 - b. SAR
 - c. Both Delta-Sigma and SAR use a data-ready pin

6. (T/F) The Sinc filter is typically **not** used for wide bandwidth Delta-Sigma
 - a. True
 - b. False





©Copyright 2017 Texas Instruments Incorporated. All rights reserved.

This material is provided strictly “as-is,” for informational purposes only, and without any warranty.
Use of this material is subject to TI’s **Terms of Use**, viewable at TI.com

$\Delta\Sigma$ Digital Filters and Latency

TIPL 4011

TI Precision Labs – ADCs

Created by Art Kay and Ryan Andrews

Presented by Ryan Andrews

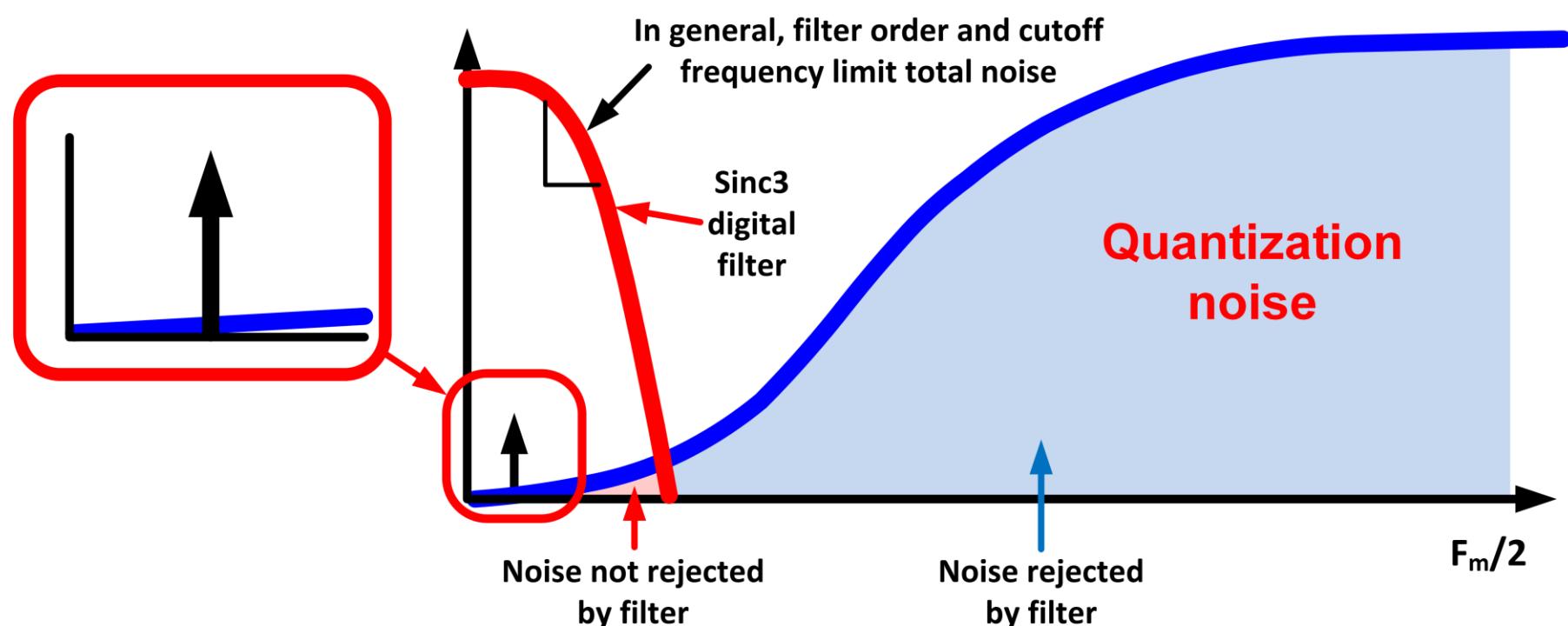


Hello, and welcome to the TI Precision Lab series covering digital filters and latency for delta-sigma converters. Previously, we introduced both SAR and delta-sigma converters, and presented an overview of their general operation.

In this video, we'll do a deep dive on the digital filters used inside delta-sigma converters. Specifically, we will focus on how digital filters introduce latency as this is a significant difference between SAR and delta-sigma ADCs. The goal here is to provide enough background on the differences between SAR and delta-sigma to effectively contrast the two topologies.

Let's start by reviewing the delta-sigma modulator output and the need for a digital filter. Then we will compare and contrast different types of digital filters used with delta-sigma converters.

Digital Filter in $\Delta\Sigma$ to Minimize Quantization Noise

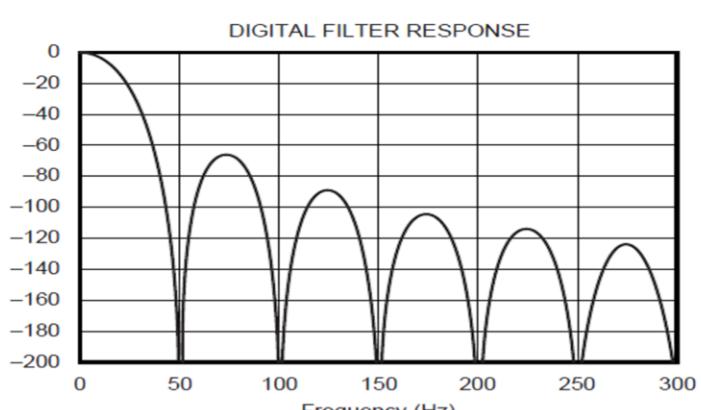


 TEXAS INSTRUMENTS

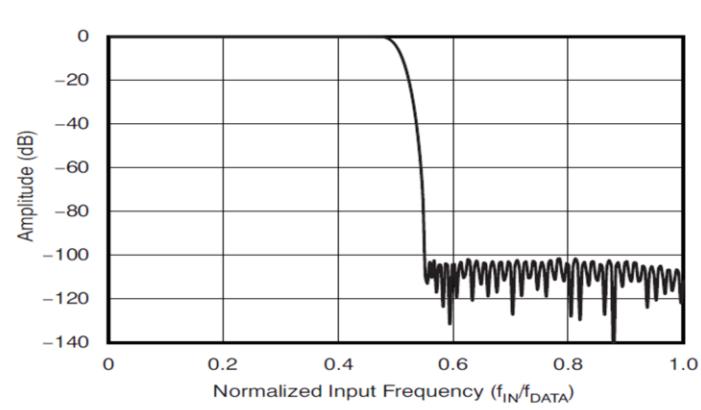
In the last presentation, we learned that the delta-sigma modulator shapes quantization noise. That is - it minimizes the noise near the signals of interest. To eliminate the large noise at higher frequencies, a low-pass digital filter is required. The cutoff frequency and order of the filter will impact the amount of noise rejected by the filter. A low cutoff frequency or a high-order filter with a sharp roll-off can be used to minimize the total noise. There are two general categories of filters used for this purpose: low latency and high latency.

Digital Filter

- Latency is the delay between when the input signal is applied and the ADC is settled
- “Sinc” is a common low latency filter type
- “Flat Passband” is a typical high latency type filter.



Sinc Filter (Low Latency)



Flat Passband Filter (High Latency)



Here we compare and contrast the low and high latency filters. Latency is defined as the delay between when the input signal is applied and when the ADC output is settled.

A Sinc filter type is a typical low latency filter. This kind of filter is often used for low frequency input signals from 10's of hertz to a few kilohertz. In this video series we refer to ADCs that use the low latency filter as DC optimized.

A “flat passband” filter is a high latency type filter. This kind of filter is used for wide bandwidth delta-sigma systems. These wide bandwidth delta-sigma ADC can achieve sampling rates in the 10's of megahertz. Let's take a closer look at the low latency filter.

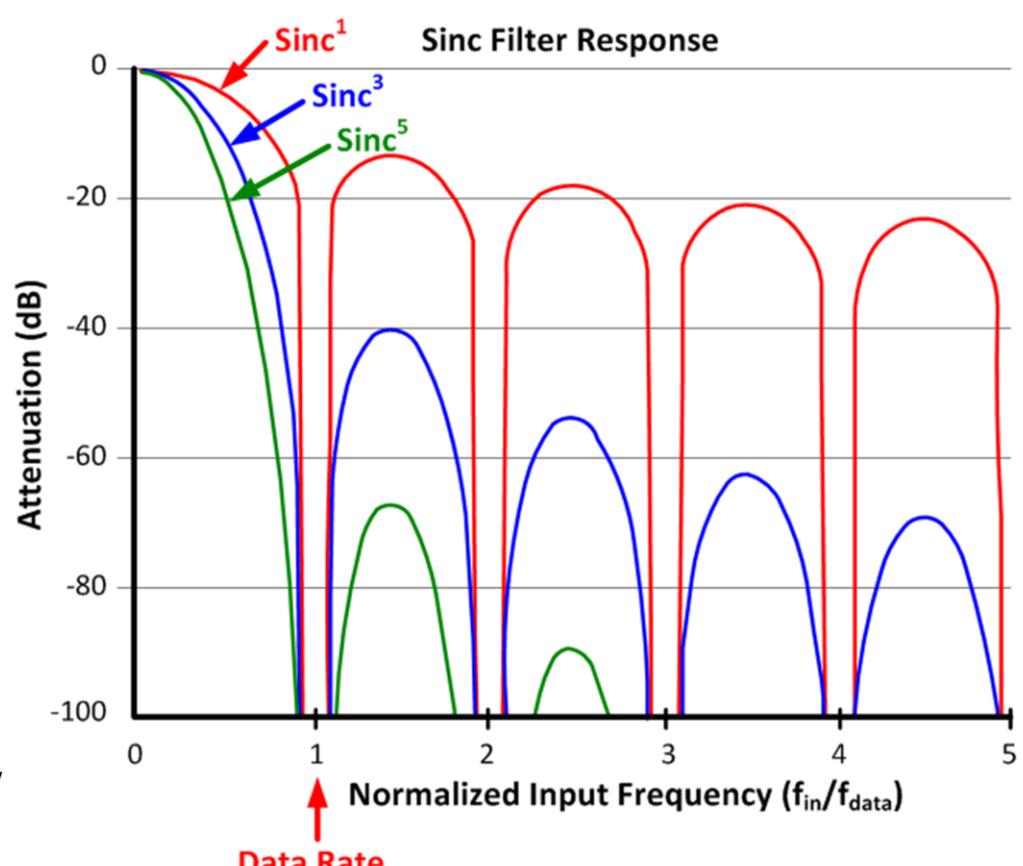
Low Latency Sinc Digital Filter

Advantages

- Low latency gives low “settling time”
- Less silicon area, easy to implement
 - Low cost, Low power
- Order refers to slope of roll-off
 - Number Cycles = Sinc order
 - Notches at multiples of data rate
- Filter notches can target specific frequencies (ex. 50/60 Hz)
- Good for dc measurements

Disadvantages

- Pass band droop-limit to low frequency
- Weak Stop band attenuation



 TEXAS INSTRUMENTS

The low latency filter is a very simple filter that is implemented using some basic math functions, like averaging. A common type of low latency filter is the Sinc filter. One of the main advantages of the low latency filter is that the delay due to latency or digital “settling time” is short compared to a higher latency filter.

Another advantage is that this type of filter is simple and easier to implement than more complex high-latency filters. This means that it will be less silicon area and thus will be lower cost. Furthermore the simple implementation tends to consume less power as well..

Filter order refers to how steep the roll-off of the curve is for the filter. You can see this by examining the Sinc-1, Sinc-3, and Sinc-5 filters in this example. The 5th order filter rolls-off faster than the first order filter. For this kind of filter, the order will also refer to the latency. So a Sinc-1 has one conversion cycle of latency and the Sinc-3 has three conversion cycles of latency. Also, notice that the Sinc filter has notches that occur at multiples of the data rate. In this example you can see the notch occurring at multiples of the data rate up to five times the data rate. By adjusting the data rate frequency, these notches can be tuned to reject certain frequencies, such as 50 or 60Hz power line frequencies. In the next slide we will look at a different low latency filter that can notch out both 50 and 60Hz simultaneously.

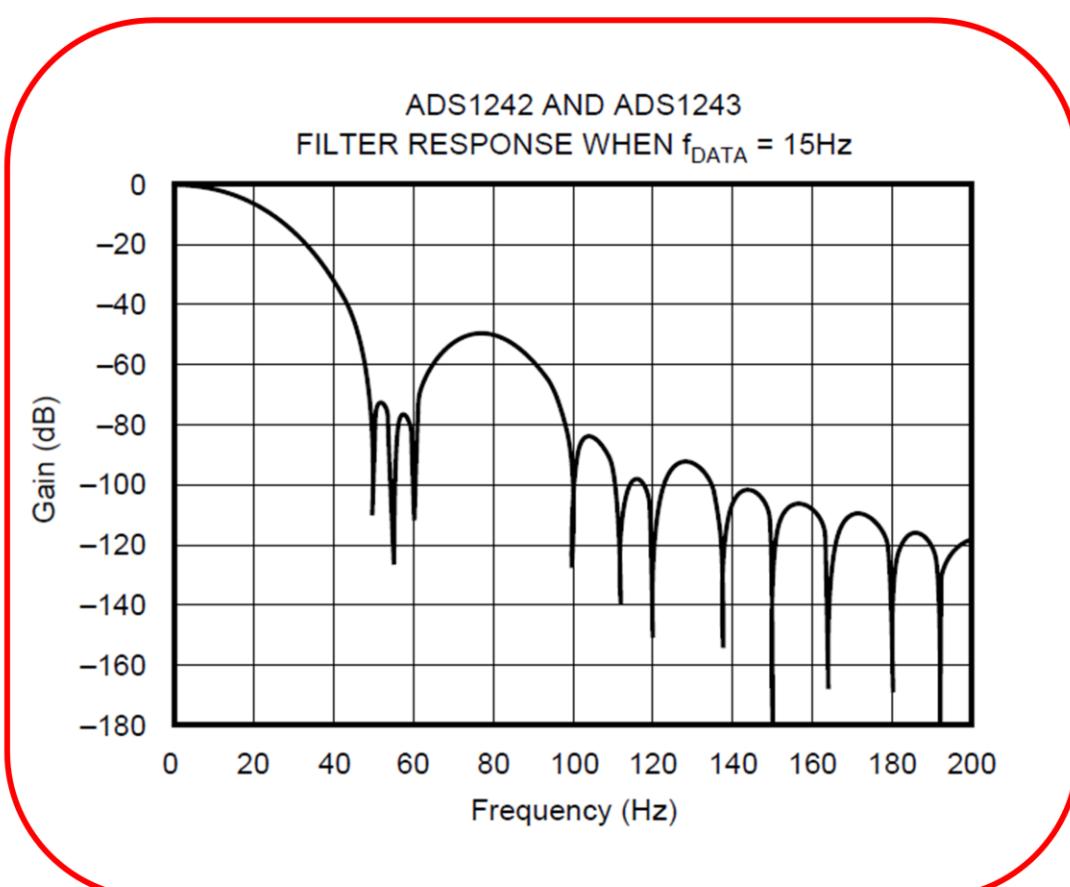
One final advantage of this kind of filter is that they are very good for DC signals as they often have very limited bandwidth and reject noise at higher frequencies. Thus, some DC optimized delta-sigma converters have excellent noise performance.

The disadvantages of this kind of filter mainly relate to the fact that the pass band begins to droop at very low frequencies. Looking at this example, you can see that the pass band attenuation is 0dB at 0Hz, but for higher frequencies the filter immediately begins to attenuate the signal. Normally, for any AC signal, the ideal filter has minimal attenuation and a flat response in the pass-band, but this filter's response clearly is not flat. Thus this type of filter is limited to DC and low frequency signals. Typical conversion rates for this kind of filter can be in the low hertz up to a few kilohertz.

Another disadvantage can be seen by looking in the stop band. For lower order Sinc filters the stop band attenuation is not very good. In this example you can see for the Sinc-1 filter the stopband attenuation is about 20dB between 1 and 2 times the data rate. Ideally we would like much higher stop band attenuations. Fortunately, the stop-band attenuation is much better for higher order sinc filters. You can see for the Sinc-5 filter that the attenuation 50dB better than the Sinc-1 filter over the same frequency range.

Low Latency FIR Digital Filter

- FIR = Finite Impulse Response
- Technically Sinc is an FIR filter
- This response is different than a typical Sinc
- This type of FIR filter has at double notch that keeps the attenuation good at both 50 and 50Hz.
- Sinc filter has notches that repeat at multiples of data rate



 TEXAS INSTRUMENTS

Some low latency filters are somewhat different than the Sinc filter. These filter types are frequently referred to as "FIR" filters. The acronym FIR stands for Finite-Impulse-Response. The category FIR actually encompasses many different filters and in fact, Sinc filters are a type of FIR filter. Nevertheless, the style of filter shown in the graph here is normally referred to as an FIR filter in literature to differentiate it from the Sinc filter.

From a response perspective, the difference between this type of filter and the Sinc filter is the fact that it has a notch at both 50Hz and 60Hz simultaneously. For a Sinc filter, the notch can only be placed at either 50Hz or 60Hz. This is a nice feature as the hardware will not need to be adjusted according to the regional power line frequency. As a side product of this design, you will notice that the notches do not occur at regular intervals as they do with a simple Sinc filter.

Now that we have covered the low latency filters let's take a look at the high latency filters.

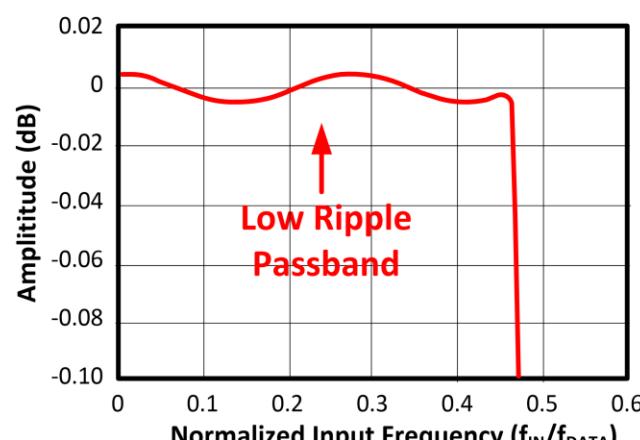
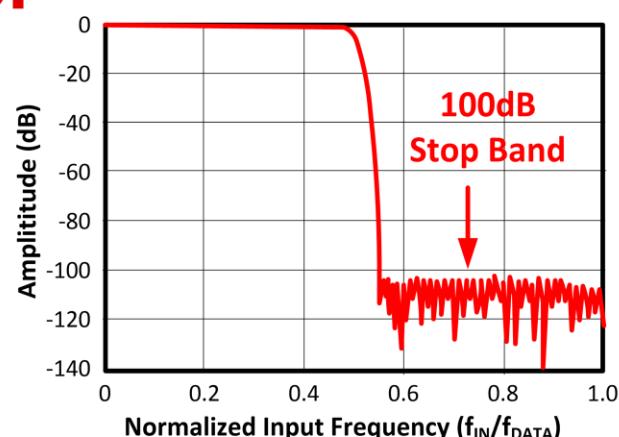
High Latency: Flat Pass Band Filter

Advantages

- Frequency Response
 - Very low ripple pass band
 - Sharp Nyquist transition band
 - Large stopband attenuation: lower than -100dB (simplify aliasing requirement)
- Frequency response scalable with data rate

Disadvantages

- Multi-order / high tap filter – Large latency (e.g. 55 cycles)
- Large area – Costly



 TEXAS INSTRUMENTS

Here you can see an example of a typical high latency filter, often referred to as a “flat-passband” filter. Unlike the Sinc filter, the Flat Passband filter is much more like an ideal ‘brick wall’ filter. It provides nearly a flat pass-band response followed by a rapid transition to a high-attenuation stop band. This type of filter is used in the wide bandwidth category of delta-sigma converters. Typical conversion rates can be as fast as 10’s of Megaherts. For example the ADS1610 has a 10-MHz output data rate.

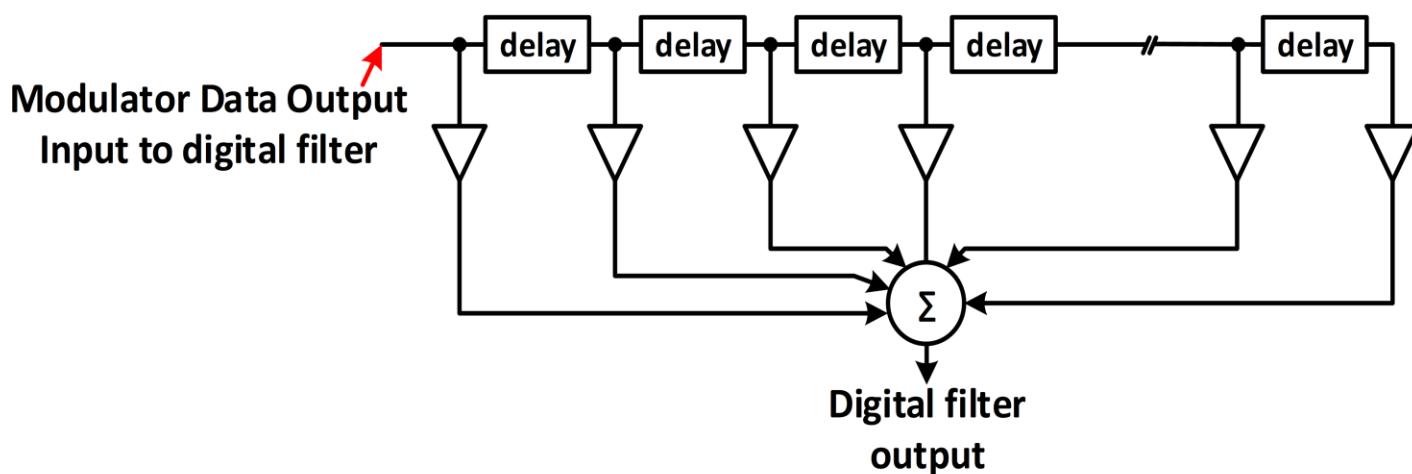
Notice when looking at the flat passband filter that the passband has very little ripple. In fact, the plot at the bottom zooms into the passband and you can see the ripple in the passband is less than 0.01dB. Also notice that the filter transition is very sharp, and the stopband attenuation is very low. One final point to mention on this filter is that the cut-off frequency scales with the data rate. In this example, you can see that the filter cutoff is set at about 0.5 times the data rate. This is helpful as this filter acts as an antialiasing filter and limits input signals to the Nyquist frequency. In the next video we will cover this in more detail.

The main disadvantage of this filter is that it has high latency. A typical latency for this kind of filter could be as high as 55 conversion cycles. In other words, if a step input is applied to an ADC with this kind of filter, the output would not be settled for the next 55 conversions. For an AC sinusoidal input, this latency amounts to a group delay effect. This group delay and settling is similar to what happens with a discrete RLC

network. Later we will also look at this in detail.

Filter topology – What causes latency?

- The latency of the filter depends on the number of delay blocks used
- Sinc filters are very efficient → minimum number of delay blocks
- Flat Passband filters require a lot delay blocks to maintain desired AC response
 - Example: ADS1672 requires 55 cycles to settle

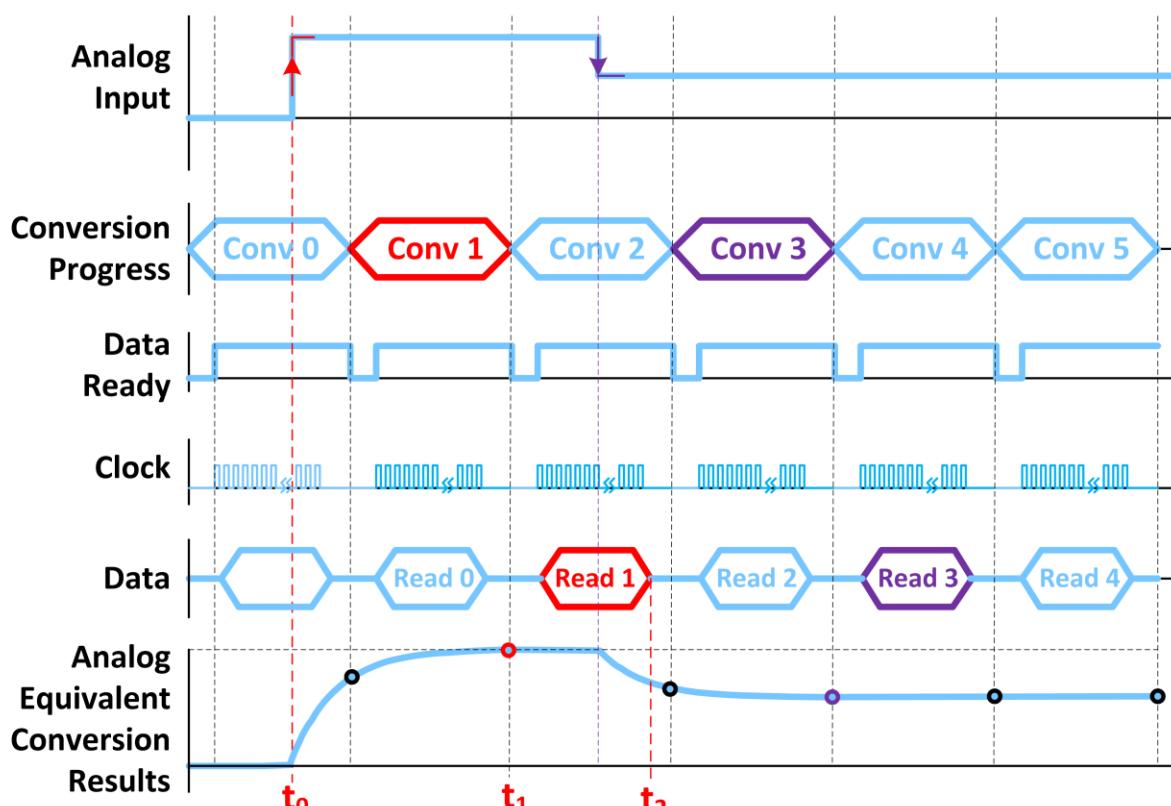


So what causes filter latency? This diagram shows a typical implementation for an FIR filter. All of the filters discussed today are generally implemented using this topology. The objective here is not to become digital filter experts, but rather to provide some insight into what causes delay in a filter.

The digital filter consists of three elements: delay elements, multiplier blocks, and summing blocks. The overall filter latency is related to the delay elements. The data propagates through the delay elements one conversion cycle at a time, so a conversion applied to the input does not propagate to the output until it has gone through all the delay elements. Thus, if a flat passband filter has 55 delay elements, the latency of the filter will be 55 conversion cycles. In the case of a Sinc filter, on the other hand, the number of delay elements is equal to the order of the Sinc filter. That is, a third order Sinc filter will have three conversion cycles of latency.

Now that we have a basic understanding of latency, let's compare and contrast a timing example using a SAR ADC, a delta-sigma ADC with low latency, and a delta-sigma ADC with high latency.

Sinc 1: Latency Communications Example



Settling for Sinc 1 $\Delta\Sigma$

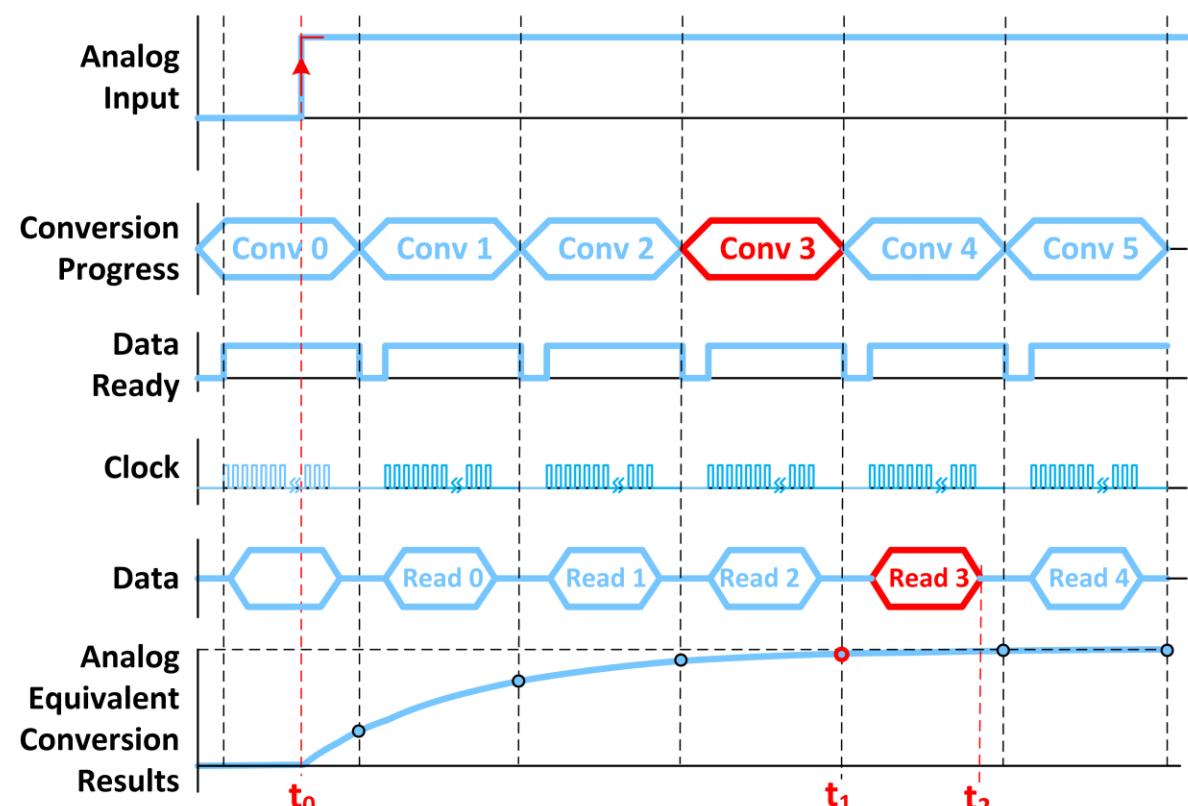
t_0 – analog input transitions and settles to constant
 t_1 – Internal conversion fully settled after 1 cycle (Sinc1)
 t_2 – Read of internal conversion 1 complete

Note: the same process can be applied to the second (purple) input transition



Here is a Sinc-1 low latency filter timing example. In this example, a step input is applied to the ADC input at time t_0 . Notice that this step occurs in the middle of conversion cycle 0. For the Sinc-1 filter, it takes one full conversion cycle to settle to a step input. Since the step happened in the middle of a conversion cycle, the ADC will need another full cycle to settle. At the bottom of the diagram you can see the internal analog equivalent conversion results. Note that at the end of conversion cycle 1, which is time t_1 , the internal ADC is fully settled. Now that the conversion result is fully settled, the data can be read by the microcontroller. This data transfer is shown as "Read 1" in the diagram, and the read is done at time t_2 . The same method can be used to show how the purple input voltage step settles. Note that for delta-sigma converters, the data ready is used to indicate when the conversion is complete. This is the general way that a Sinc 1 low latency filter will operate from a timing perspective. Next let's look at a Sinc 3.

Sinc 3: Latency Communications Example



Settling for Sinc3 $\Delta\Sigma$

- t_0 – analog input transitions and settles to constant
- t_1 – Internal conversion fully settled after 3 cycles (Sinc3)
- t_2 – Read of internal conversion 3 complete

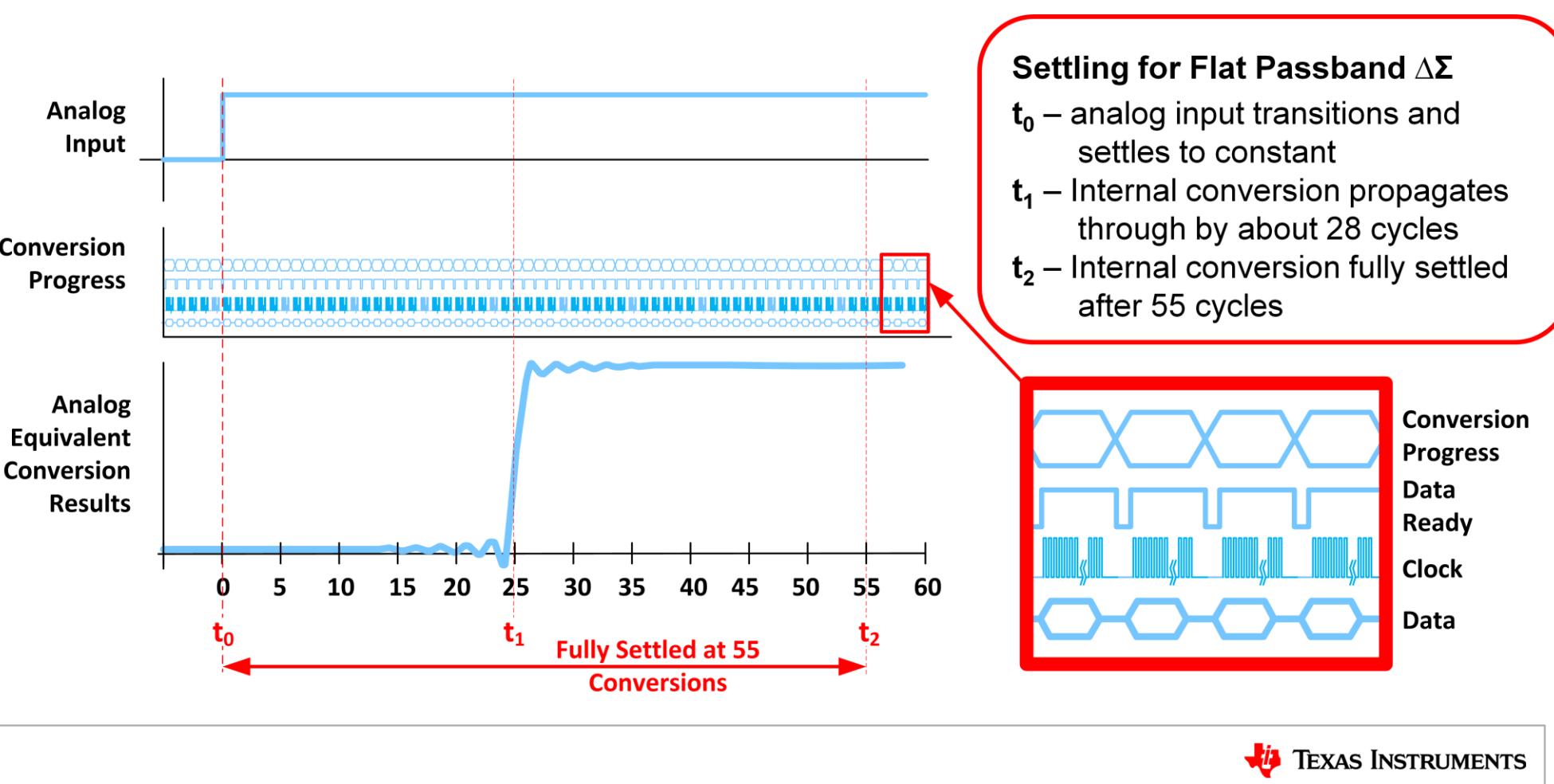


Here is a Sinc-3 low latency filter timing diagram. This example is very similar to the last one except that the latency is three conversion cycles instead of one. In this case the step is applied during conversion cycle 0. It takes three full conversion cycles to settle, so the internal ADC is settled at the end of conversion 3. Once settled, the data for the conversion needs to be read by the microcontroller.

One point to mention here is that the timing is not necessarily to scale. For example, a conversion cycle may take 16ms, but the data communications may be only a few microseconds long. The main point here is to illustrate how latency is an internal settling of a digital filter and that the data cannot be retrieved from the device until after the latency delay.

Next we'll repeat the example for a high latency filter.

Flat Passband: Latency Communications Example

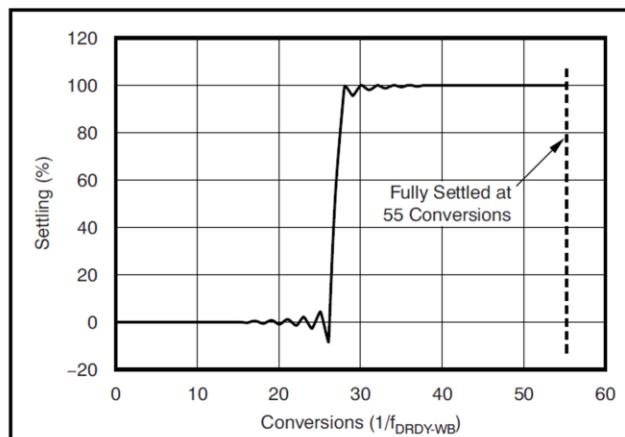
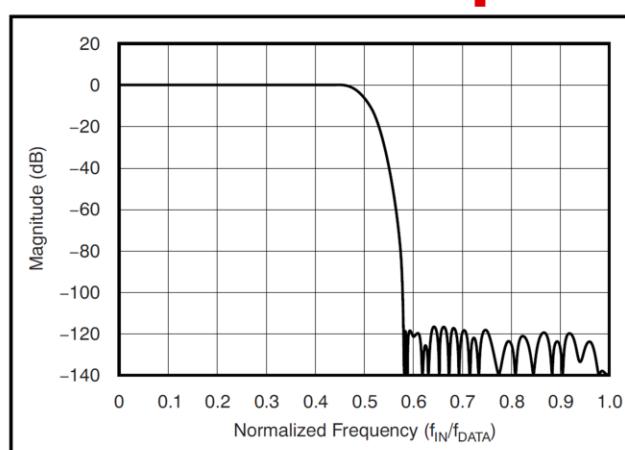


This timing diagram shows how settling occurs in delta-sigma converter with a high latency filter. In this example the latency is 55 cycles so you have to zoom in on a small segment of the conversion progress signals to see the data ready, clock, and data.

Notice that after the step is applied, the output shows almost no response until approximately 28 cycles. This is about half of the total latency and is equal to the group delay for the device. Once the output responds, however, there is another 27 cycles before the output fully settles. In other words the output will be fully settled after 55 conversion cycles. This kind of response is somewhat analogous to applying a step input to an RLC circuit. There is a delay, rise time, and settling associated with the response. This delay and settling may seem excessive, but keep in mind that this type of converter normally will not be used to capture multiplexer outputs or DC transients. Rather, this converter will be used to capture AC sinusoidal signals. In this case the converter will simply introduce a group delay, but the impact of this delay may not be significant. Let's look at a data sheet excerpt for a delta-sigma converter using a high latency filter.

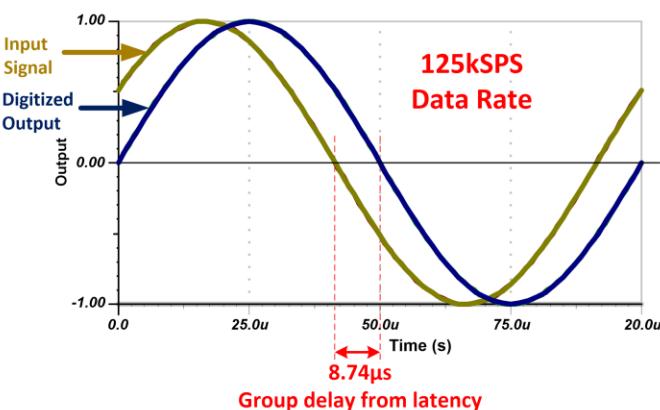
Flat Passband: Data Sheet Excerpt ADS1675

Data Rate (kSPS)	-3dB BW (kHz)	Settling Time		Group Delay	
		(μs)	Cycles	(μs)	Cycles
125	59.375	17.48	55	8.74	28
250	118.75	9.38	55	4.69	28
500	237.5	5.48	55	2.74	28
1000	475	3.63	55	1.82	28
2000	950	2.76	55	1.38	28
4000	1900	2.39	55	1.20	28



Flat Passband $\Delta\Sigma$

- Sine wave has a group delay
- Step input has delay and settling
- Full settling can take many conversion cycles



This slide shows the specifications for an example device that has an internal flat passband filter with high latency. The frequency response curve shows a very sharp transition from the pass band to the stopband at approximately one-half the data rate. Also, notice that the attenuation in the stopband is quite good; below 120dB in this case. The table shows the -3dB bandwidth, settling time, and group delay for this device. Again, notice that the -3dB point is about one-half the data rate. The cutoff was selected to minimize aliases, which will cover more in the next video.

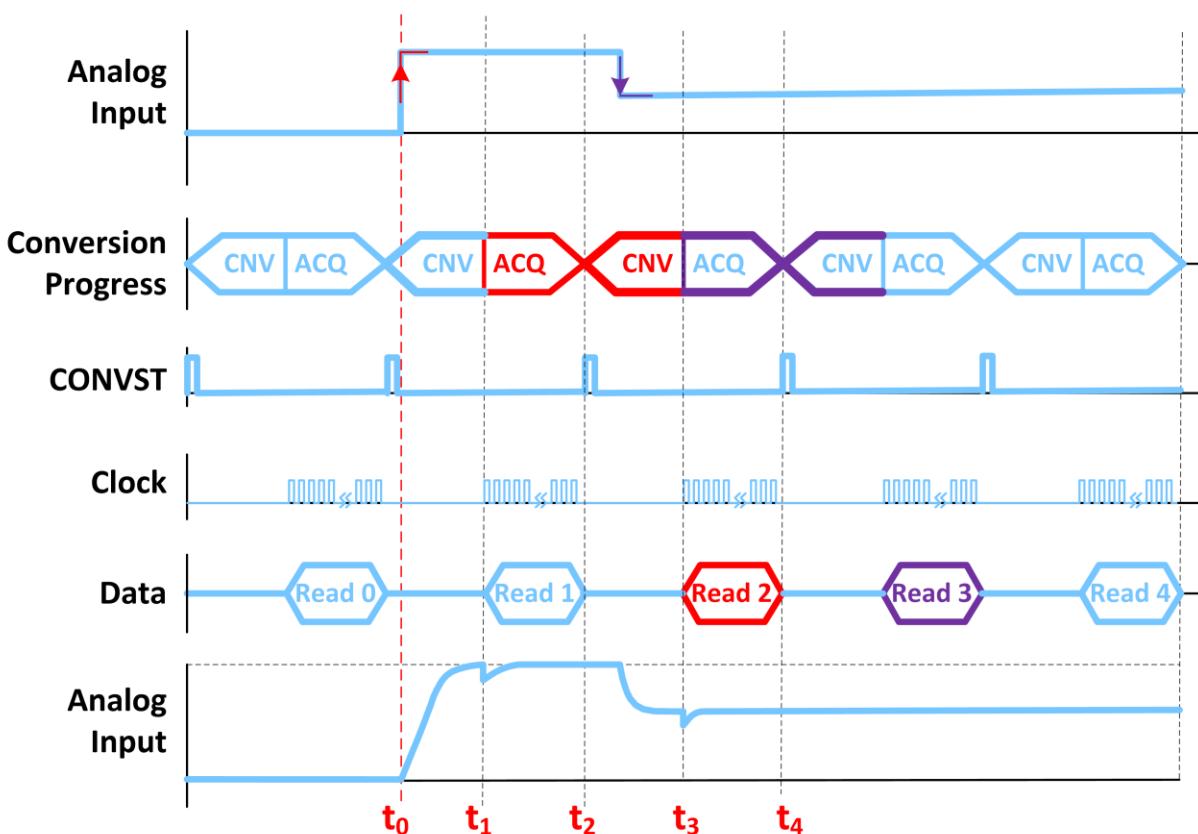
The settling time is related to the filter design, and the number may be different for other converters. The step response shows that it takes 55 cycles to fully settle. Notice from the step response that you don't see any output until about 28 conversion cycles, then it takes the remaining 27 cycles to fully settle.

Finally the group delay is roughly half the settling time. Group delay is the time shift between the applied sinusoidal input and the equivalent digitized output. The group delay effect is illustrated in the sinusoidal graph at the bottom of the page. Since group delay and settling time are a fixed number of conversion cycles, the actual time will scale with data rate. Thus, the group delay and settling time will be lower for high sampling rates.

Now that we have looked at the settling time example using a delta-sigma converter with both low and high-latency filters, let's take a look at how they compare to the SAR converter.



SAR latency



Settling for SAR

t_0 – analog input transitions
 t_1 – start of acquisition cycle
 t_2 – End of acquisition. Analog sample and hold settled. Start of conversion cycle.
 t_3 – End of conversion cycle. Voltage from t_0 conversion complete. Start to clock out conversion results
 t_4 – Conversion results from t_0 fully clocked out (Read 2).



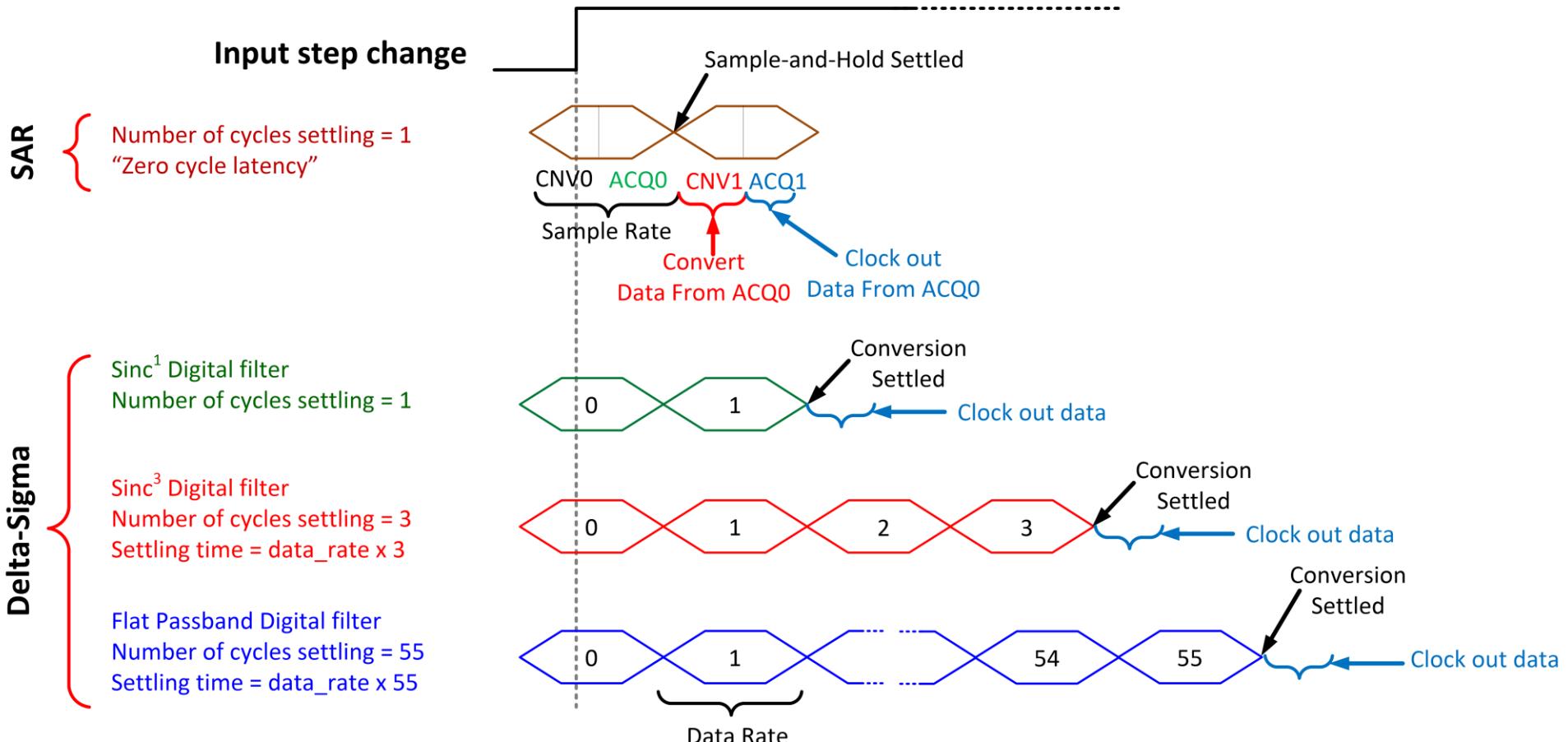
One key difference between the SAR and delta-sigma converters is that the SAR has an acquisition phase and a conversion phase, but the delta-sigma converts continuously.

With this in mind, the analog input signal can transition during the conversion phase of a SAR ADC without impacting the settling during the acquisition phase. This is what happens at time t_0 in this example. At time t_0 , the analog input makes a step change. This step occurs during the conversion phase so the analog input can complete the transition before the ADC starts acquiring the input signal.

At the beginning of the acquisition phase, or time t_1 , the analog input will see a brief transient as the sample and hold capacitor is charged. At time t_2 the acquisition period ends and the analog input is captured on the sample and hold. Now the conversion cycle begins and the sampled voltage is converted to a digital equivalent. At time t_3 the conversion is complete and the data can now be read by a microcontroller. At t_4 the data read is complete. Looking at the digital communications signals for the SAR converter, you will notice that the conversion is initiated with a convert start signal. For the SAR the microcontroller will initiate the start of the conversion, whereas for the delta-sigma, the ADC is continuously converting and it will tell the microcontroller when the conversion is complete.

Sometimes SAR converters are called zero-latency converters as they have a minimal delay between when the data is captured and when the conversion is available. Keep in mind, however, all converters will have some conversion delay and also some time is required to read the conversion result from the converter.

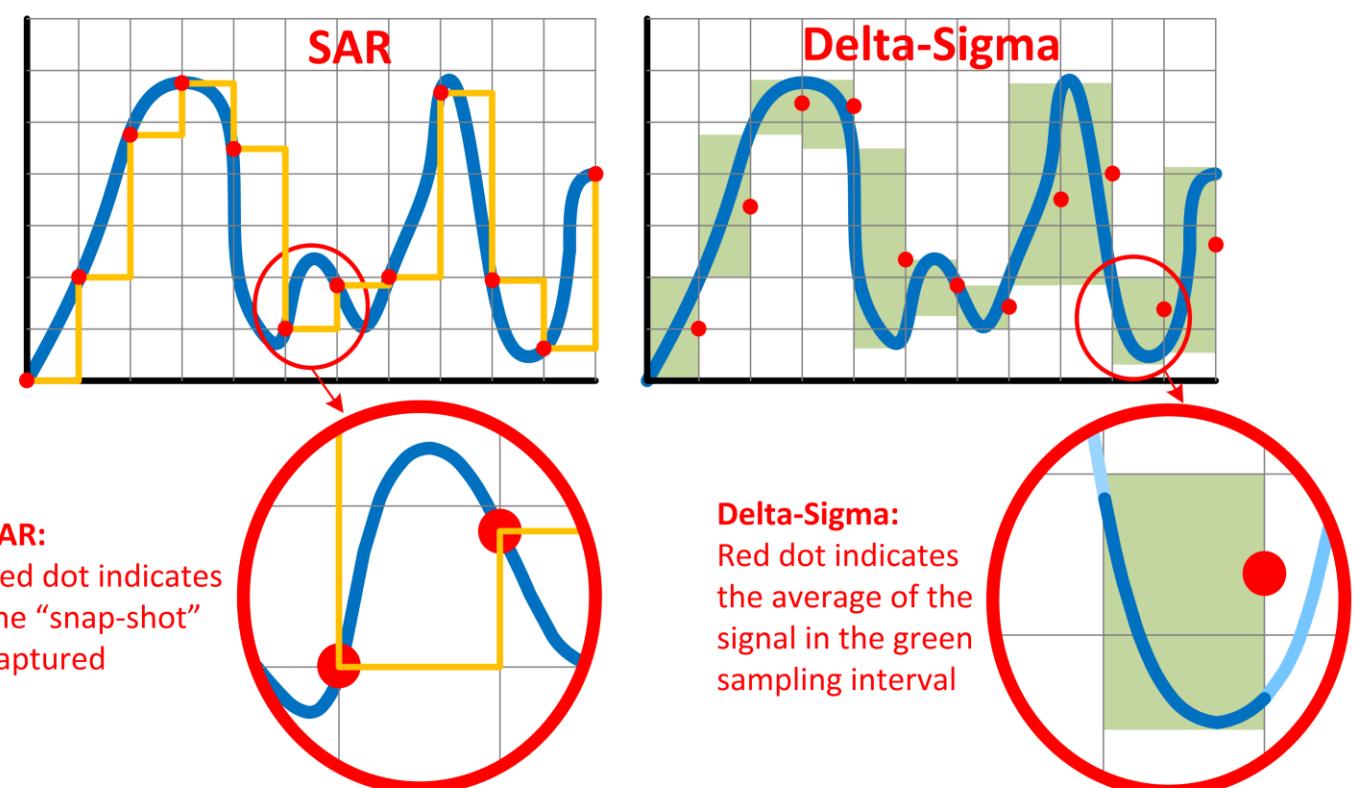
Latency Comparison: SAR vs Delta-Sigma



TEXAS INSTRUMENTS

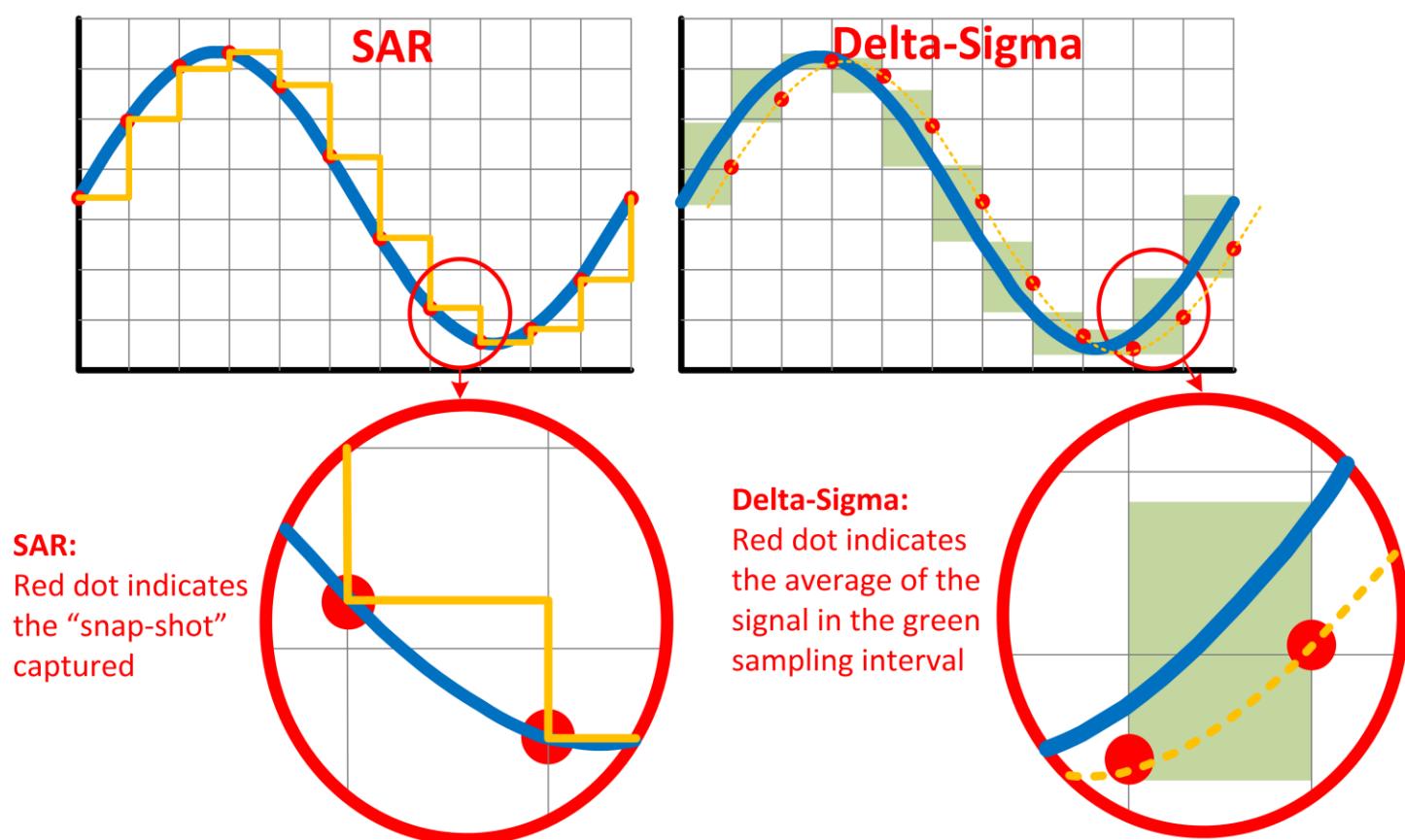
This slide summarizes the four different cases that we considered in this video. Notice that the shortest latency is the SAR converter followed closely by the delta-sigma with a Sinc-1 filter. The delta-sigma with a flat pass band filter has the highest latency at 55 conversion cycles. It is important to remember that latency is not always a key consideration. For example, in an audio system an ADC can be used to record sound. In this case, a short delay between when the sound is detected by the microphone and when the conversion is stored in memory is not an issue. On the other hand, in a safety system, the ADC may be monitoring a sensor where a near instantaneous response is required. In that case latency may be critical. You will have to determine whether or not latency is important for your application.

SAR vs Delta-Sigma Sampling transient signal



This slide reviews how a SAR and delta-sigma ADC capture a non-periodic transient signal. The key difference here is to understand that the SAR takes a snapshot in time, whereas the delta-sigma averages across a time interval. In this example we are not looking at the effect of latency but rather are focusing on how data is captured. A SAR ADC may capture some of the transient voltage spikes, whereas the delta-sigma would average some of them out

SAR vs Delta-Sigma Sampling periodic signal



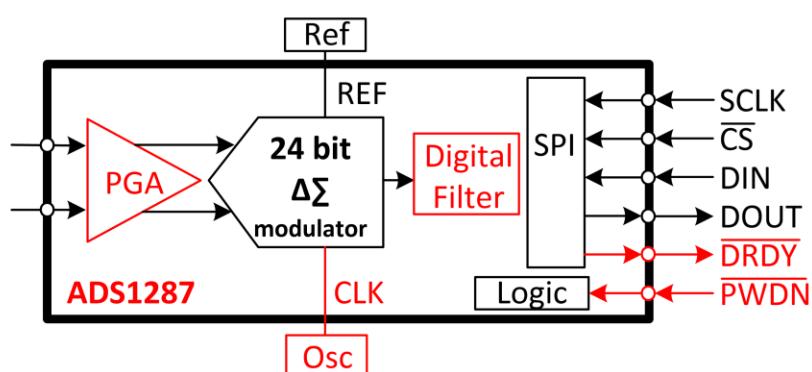
 TEXAS INSTRUMENTS

In the case of period sinusoidal waveform, both the SAR and delta-sigma can properly track the signal. The difference here between the two converters is that the delta-sigma may have a significant latency delay.

Summary of differences between SAR & $\Delta\Sigma$

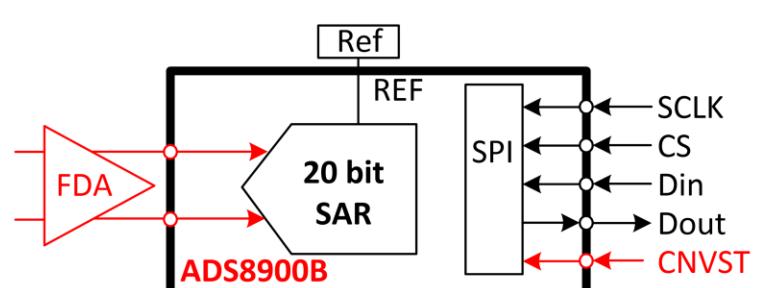
$\Delta\Sigma$ Block diagram

- Master clock for modulator
- Data-ready (/DRDY) tells controller when conversion is done
- Data rate lower than modulator rate
- Power-down (/PWDN) control
- Integrated PGA common
- Integrated digital filter



SAR Block diagram

- No master clock
- Controller uses Convert Start (CNVST) to sets timing
- Data rate = input sample rate
- Typically in “power down” state automatically when idle
- Amplifier typically external



TEXAS INSTRUMENTS

To conclude this video, let's look at various features that differ between the delta-sigma and SAR block diagrams.

First, notice that the delta-sigma can have an internal PGA and the SAR usually has an external differential amplifier. This isn't necessarily always the case, but it is much more common to see a PGA integrated into a delta-sigma converter than a SAR.

Next, notice that the delta-sigma has a master clock input. This clock is used to run the modulator. In many cases, an internal clock divider will be used on the master clock signal. For some delta-sigma converters this clock source is internal. Meanwhile, the SAR does not have a master clock input. Some SAR converters will have an integrated oscillator that is used for timing during the conversion cycle, but the SAR generally does not require an external oscillator.

All delta-sigma converters will have an integrated digital filter, but SAR converters seldom offer this feature.

A SAR ADC typically consumes very little power when they are not converting, so they generally do not need a power down control. On the other hand, the delta-sigma converter typically converts continuously, so a power down control is often used to put the device into an idle state to minimize power consumption when conversions are not needed.

Lastly, the delta-sigma ADC has a data-ready interrupt pin to tell the microcontroller when a conversion is complete. Typically the microcontroller will use an interrupt or polling method to know when data can be read. The SAR converter, on the other hand, is explicitly controlled by the microcontroller using the convert start pin.

**Thanks for your time!
Please try the quiz.**



That concludes the theory part of this video. Thank you for your time! The next video will focus on noise differences between the SAR and delta sigma converter. Keep watching to try the quiz and check your understanding of this video's content.

Questions: Digital Filters and Latency

1. Which filter has the longest latency?
 - a. Sinc1
 - b. Sinc3
 - c. Flat Passband (FIR)

2. (T/F) The flat passband (FIR) filter can have a notch to eliminate 60Hz noise.
 - a. True
 - b. False



Question 1: Which filter has the longest latency?

- a) Sinc1
- b) Sinc3
- c) Flat Passband – also known as an FIR filter

The answer is C. – the flat passband filter has the longest latency.

Question 2: True or False – the flat passband FIR filter can have a notch to eliminate 60 Hz noise.

The answer is false – only a sinc filter can have notches at 50 or 60 Hz.

Questions: Digital Filters and Latency

3. Which of the following is not an advantage of the flat passband filter?
 - a. Large stopband attenuation (Attenuation > 100dB)
 - b. Less silicon area, easy to implement (lower cost)
 - c. Very low ripple (Ripple < 0.1dB)
 - d. Sharp Nyquist transition (i.e. high order filter)

4. (T/F) The group delay is approximately equal to half the settling time for a flat passband filter?
 - a. True
 - b. False



Question 3: Which of the following is not an advantage of the flat passband filter?

- a) Large stopband attenuation (Attenuation > 100dB)
- b) Less silicon area, easy to implement (which translates to lower cost)
- c) Very low ripple (less than 0.1dB)
- d) Sharp Nyquist transition (i.e. high order filter)

The answer is b.). A flat passband filter offers great performance, but at the cost of a more complex design.

Question 4: True or False – The group delay is approximately equal to half of the settling time for a flat passband filter?

The answer is true. The total settling time is about twice group delay.

Questions: Digital Filters and Latency

5. Which type of converter uses the data-ready pin to indicate that the conversion is complete?
 - a. Delta-Sigma
 - b. SAR
 - c. Both Delta-Sigma and SAR use a data-ready pin

6. (T/F) The Sinc filter is typically **not** used for wide bandwidth Delta-Sigma
 - a. True
 - b. False



Question 5: Which type of converter uses the data-ready pin to indicate that the conversion is complete?

- a) Delta-Sigma
- b) SAR
- c) Both Delta-Sigma and SAR use the data-ready pin.

The answer is a.) only a delta-sigma ADC uses a data-ready pin to indicate when conversions are complete.

Question 6: True or false: The sinc filter is typically NOT used for wide bandwidth delta-sigma ADC applications?

The answer is true. The passband of the sinc filter is not sufficient for wide bandwidth applications.



©Copyright 2017 Texas Instruments Incorporated. All rights reserved.

This material is provided strictly “as-is,” for informational purposes only, and without any warranty.
Use of this material is subject to TI’s **Terms of Use**, viewable at TI.com

This slide should be leveraged for external recordings. Leave on screen for 5 seconds.