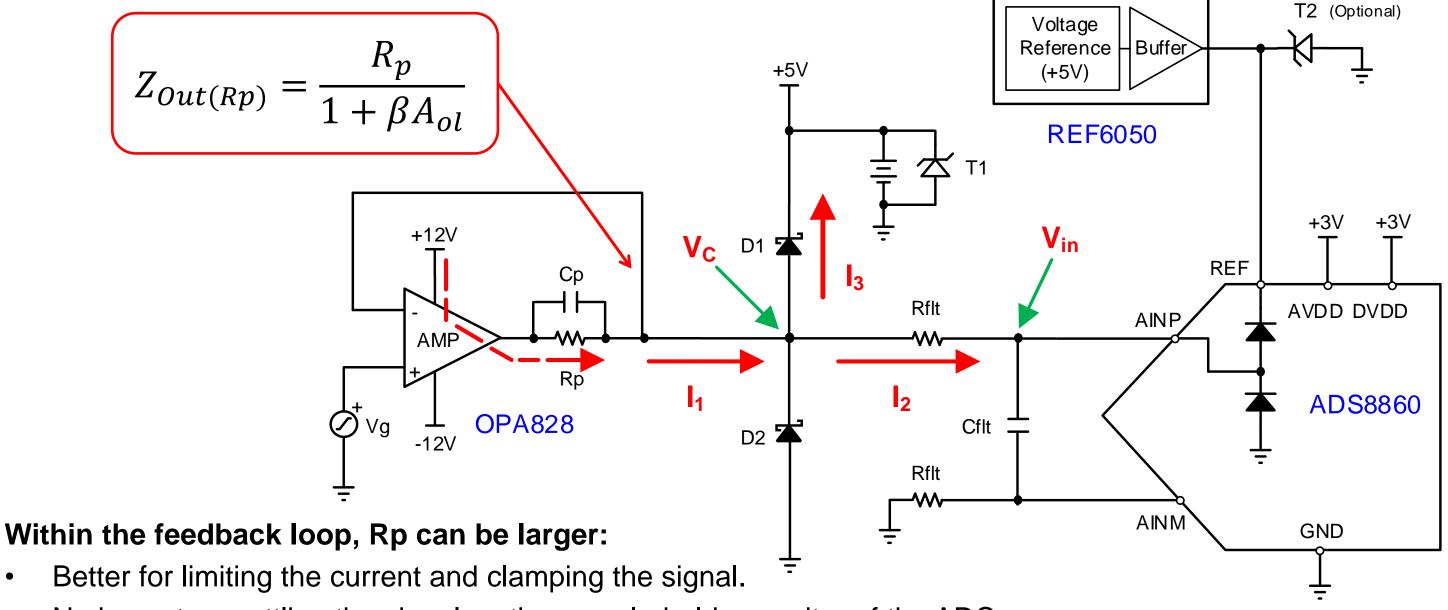
Protecting Low Voltage ADC - Improved Solution TI Precision Labs - ADCs

Presented by Alex Smith Prepared by Dale Li

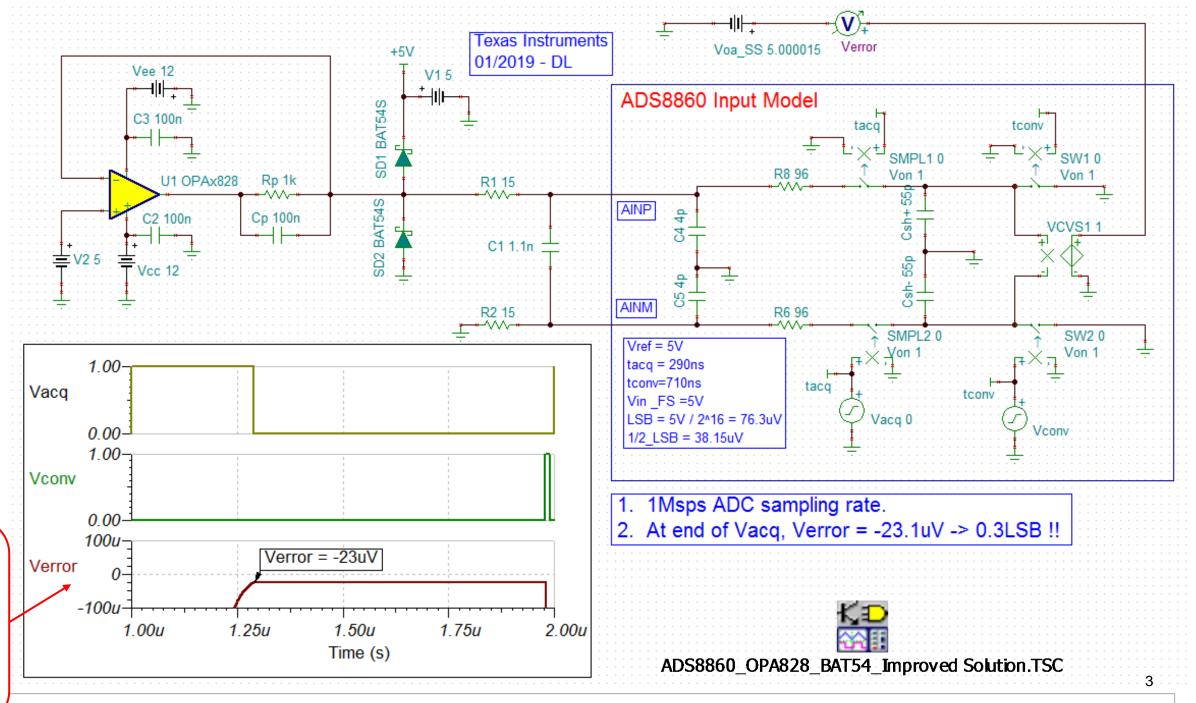


Solution to Improve Settling



- No impact on settling the signal on the sample-hold capacitor of the ADC.
- A small size and low power dissipation resistor can be used.

TINA Simulation for Improved Solution



The settling error target is 38µV, so -23µV meets the requirement.

Hardware Performance Check for Improved Solution

(BAT54, Riso=1k Ω , C_comp=100nF, RfIt=15 Ω , CfIt=1.1nF, OPA828+ADS8860 at 1Msps sampling rate)



ADS8860 Data Sheet (1Msps)

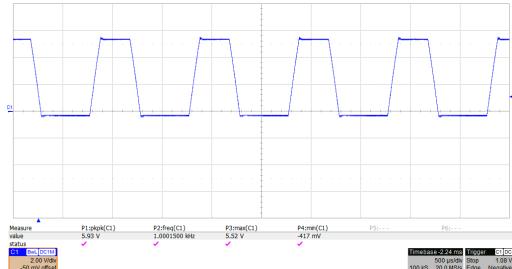
Parameter	Min	Тур	Max	Unit
SNR	92	93		dB
THD		-108		dB

Measured Performance:

SNR = 93.3dB

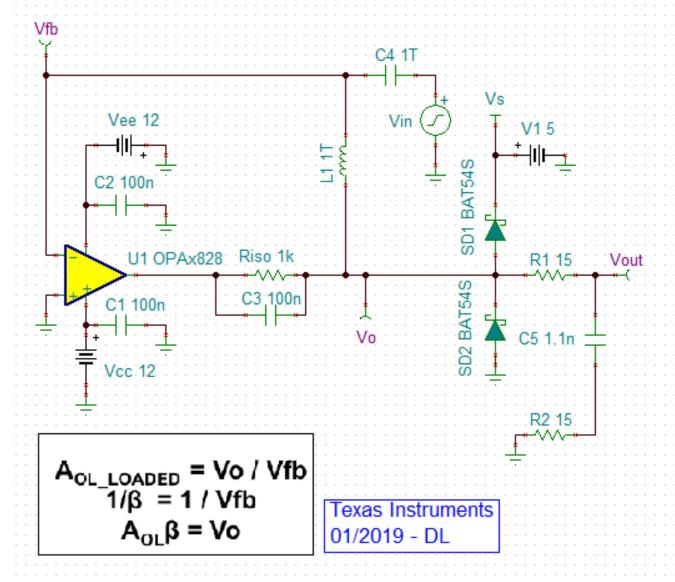
THD = -113.7dB

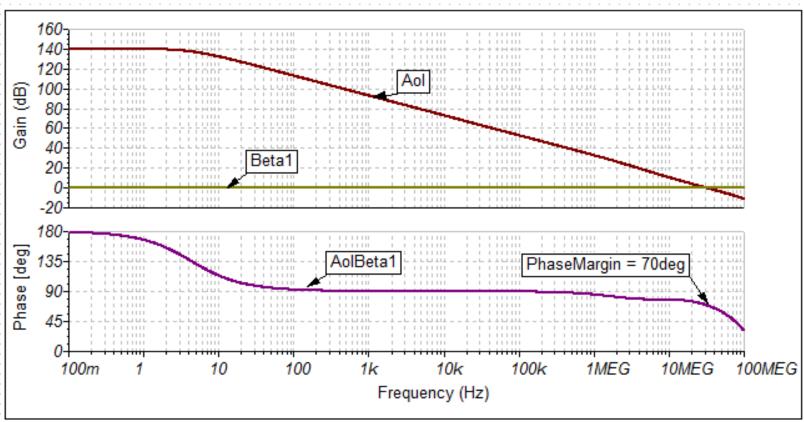
HV Sinewave Input Signal Clamped:





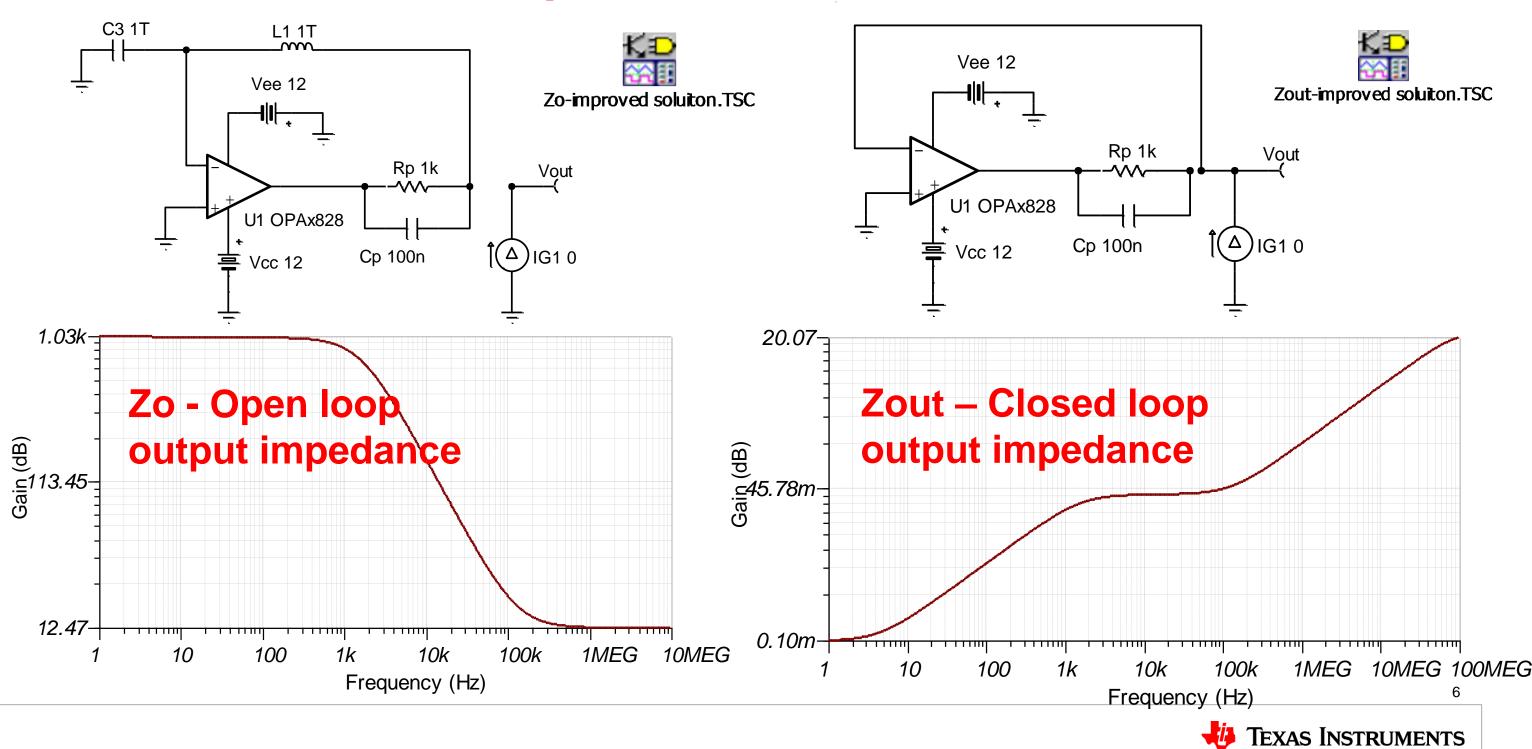
OPA828 Stability Check - Improved Solution







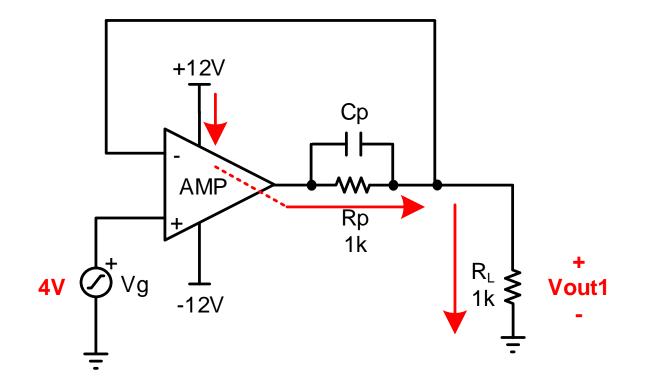
Zo and Zout with Improved Solution

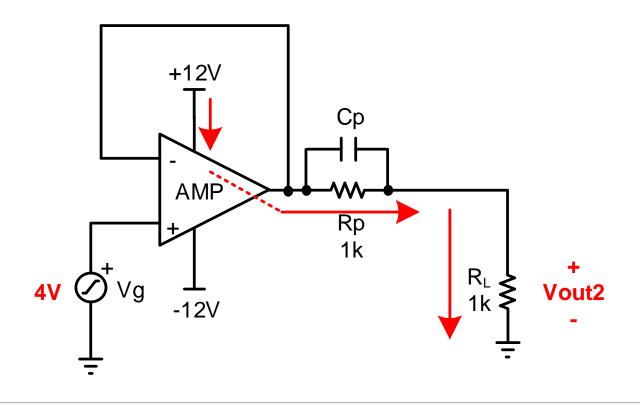


Thanks for your time! Please try the quiz.

Questions: Protecting Low Voltage ADC

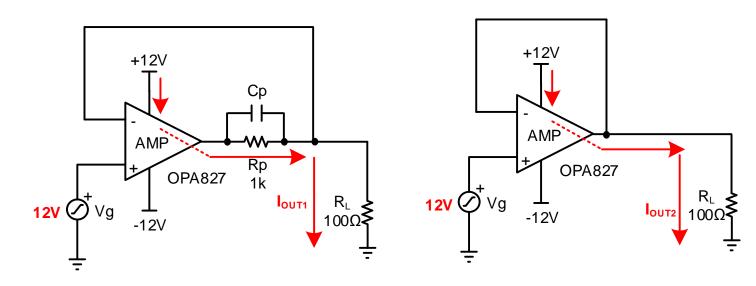
- 1. For the circuits below, what is the voltage delivered to the load?
 - a. Vout1 = 4V, Vout2 = 4V.
 - b. Vout1 = 2V, Vout2 = 4V.
 - c. Vout1 = 4V, Vout2 = 2V.
 - d. Vout1 = 2V, Vout2 = 2V.

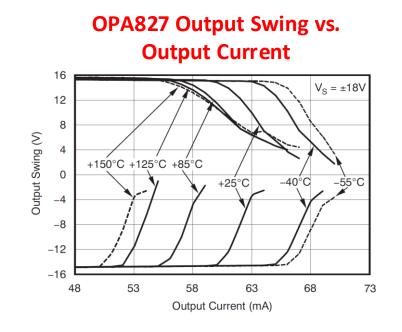




Questions: Protecting Low Voltage ADC

- 2. For the circuits below, what is the current delivered to the load?
 - a. lout1 = 12mA, lout2 = 120mA.
 - b. lout1 = 120mA, lout2 = 120mA.
 - c. lout1 = 12mA, lout2 = 60mA.
 - d. lout1 = 120mA, lout2 = 60mA.





Thanks for your time!



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