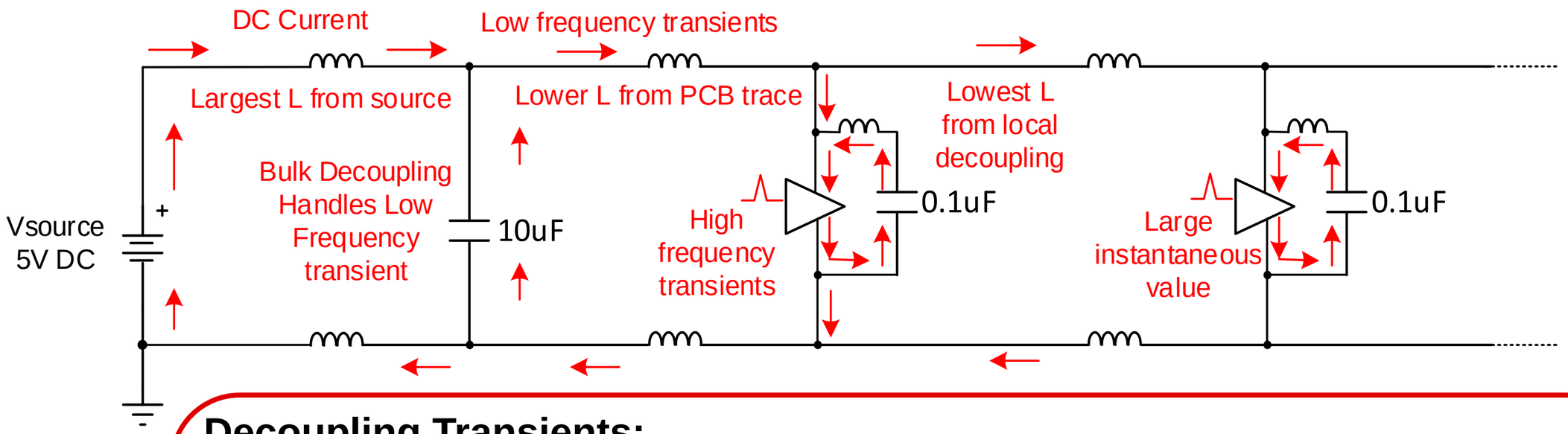
Decoupling capacitors

TI Precision Labs – ADCs

Created and Presented by Art Kay

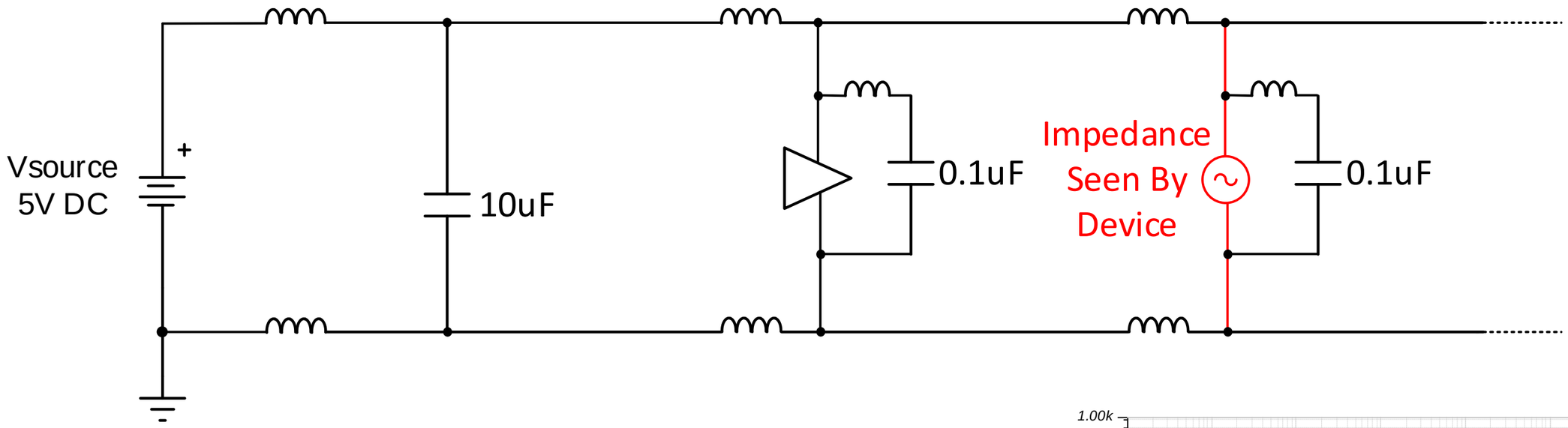
Decoupling from a Transient Perspective



Decoupling Transients:

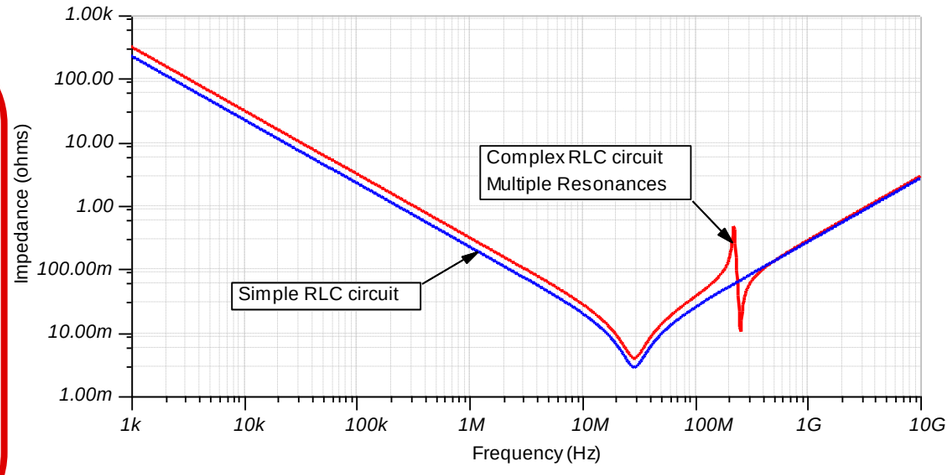
- Local decoupling provides high frequency transient current
- Instantaneous transient current from device can be high
- Bulk decoupling provides low frequency current
- The source has highest inductance, PCB power traces have lower inductance, and local decoupling has lowest inductance
- Decoupling minimizes noise local to device and minimizes the impact on other devices sharing the power bus

Decoupling from an AC Impedance Perspective

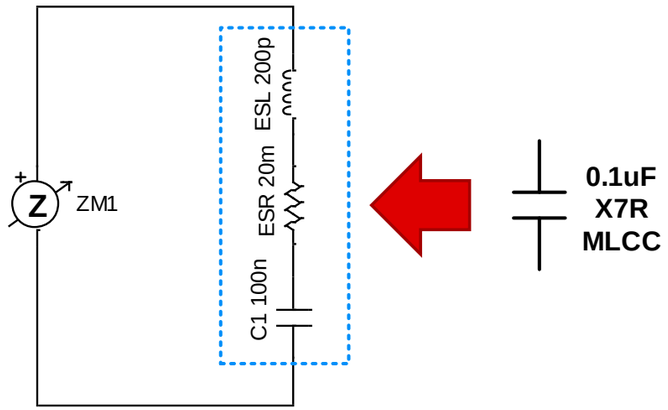


Impedance Seen by Device:

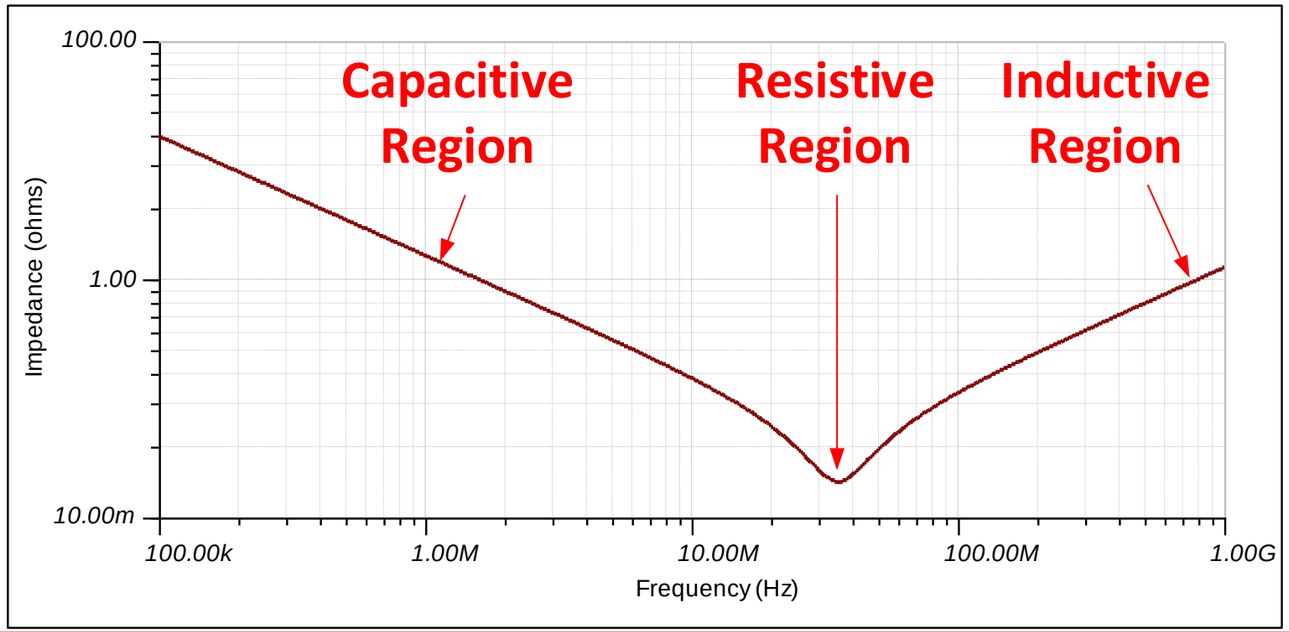
- High impedance at DC
- *Ideally* would have zero impedance at high frequency to short out high frequency transients
- Practical decoupling will be low at high frequency but will begin to increase from parasitic inductance.
- Practical decoupling may have multiple resonant peaks



Model of a practical capacitor



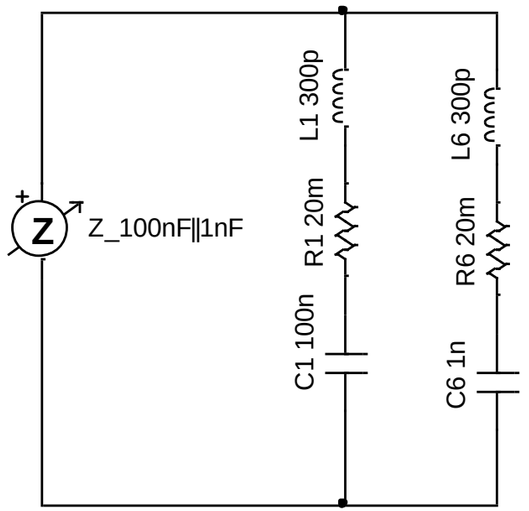
0.1uF
X7R
MLCC

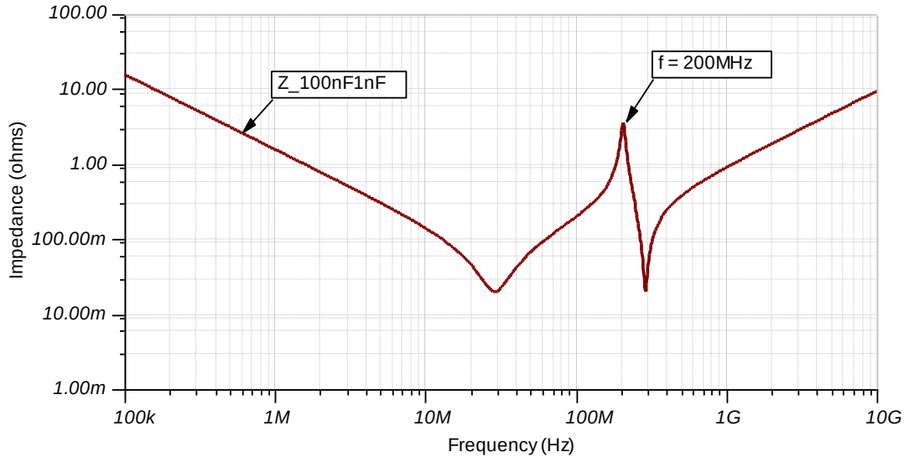


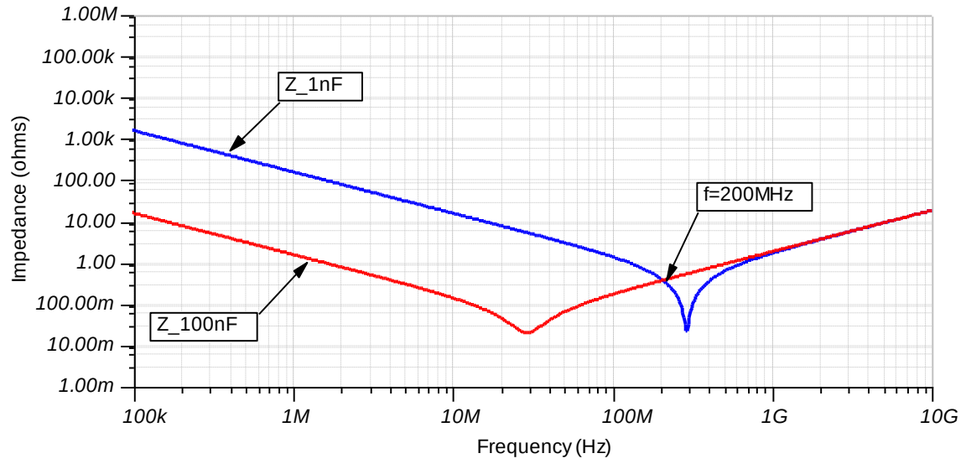
Practical impedance of Capacitor:

- ESR – parasitic resistance of capacitor
- ESL – parasitic inductance of capacitor
- Practical capacitor acts like capacitor at low frequency and like an inductor at high frequency
- Values shown in this example are typical for a X7R decoupling capacitor
- More accurate models provided by capacitor manufacture.

Resonance from Different Decoupling Capacitors



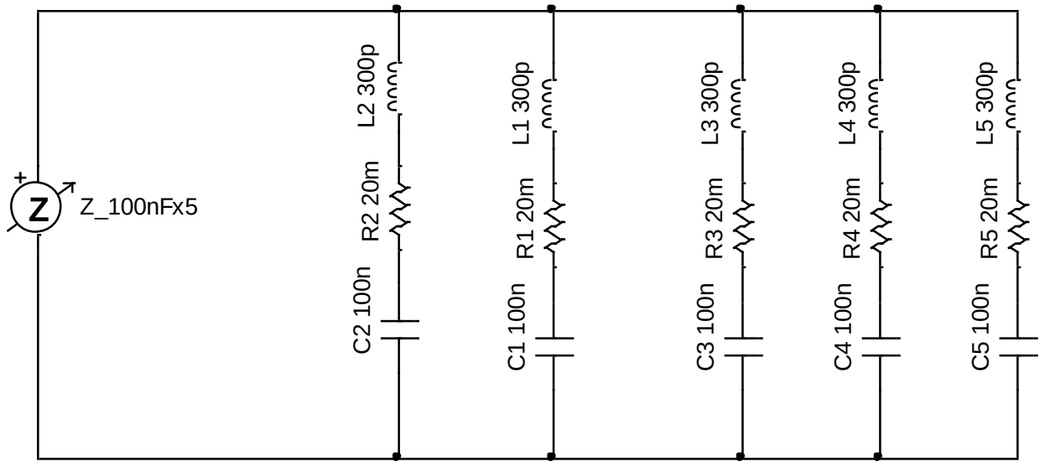


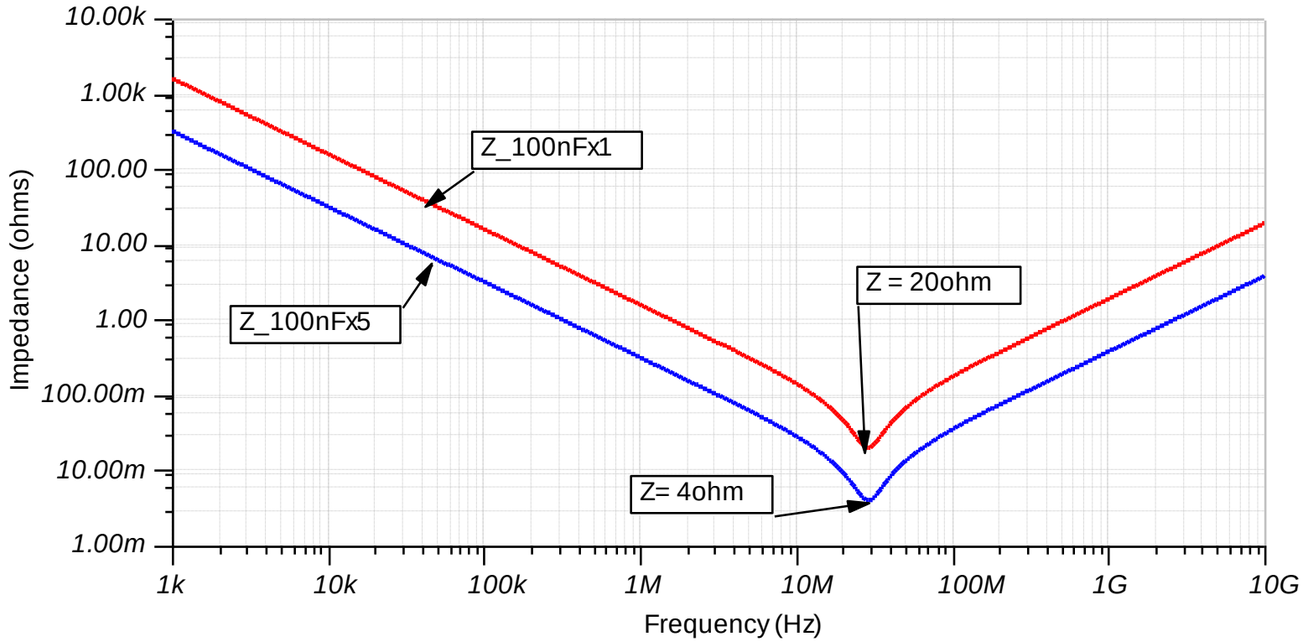


Don’t use two different capacitor values for “better” high frequency bypass

- The practice of using two different parallel capacitors was developed 1970’s for through-hole capacitors. It doesn’t apply to modern surface mount ceramic
- ESL is relatively independent of capacitance value
  - e.g. ESL for a 100pF, 1000pF, and 10,000pF (25V, 0603, X7R) is approximately the same (ESL ≈ 200pH GRM033R71E103ME14, GRM033R71E102ME14, GRM033R71E101ME14)
- Using two different parallel capacitors can create a resonance

Multiple Same Value Decoupling





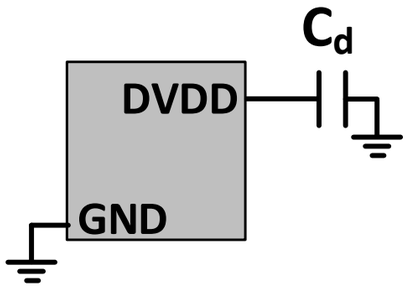
Using Multiple Same Type / Value Decoupling Capacitors

- Total impedance is divided by the number of capacitors
  - The example shows five capacitors in parallel ($Z_{total} = Z_c/5$)
- No resonance in impedance -- all capacitors are the same

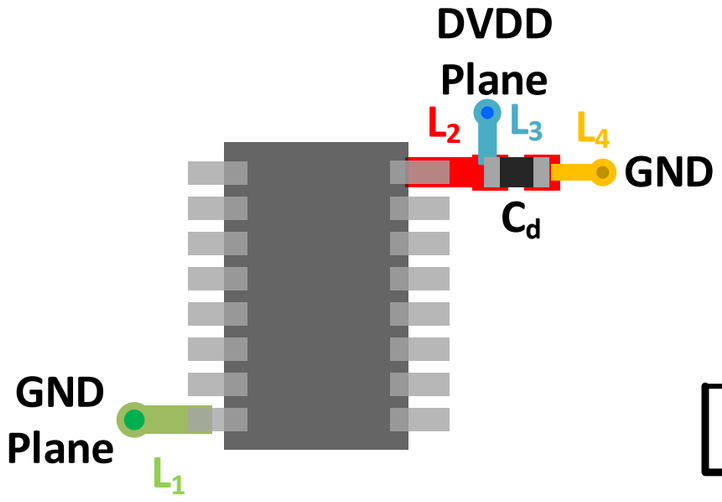
PCB Design for good decoupling

- **Main objective:** reduce the parasitic inductances from traces and vias.
- Use short wide traces or polygons
- Use multiple vias (or larger via) for plane connections if possible
- Thin dielectric spacing between top layer and plane reduce via inductance
- Use low ESL capacitor

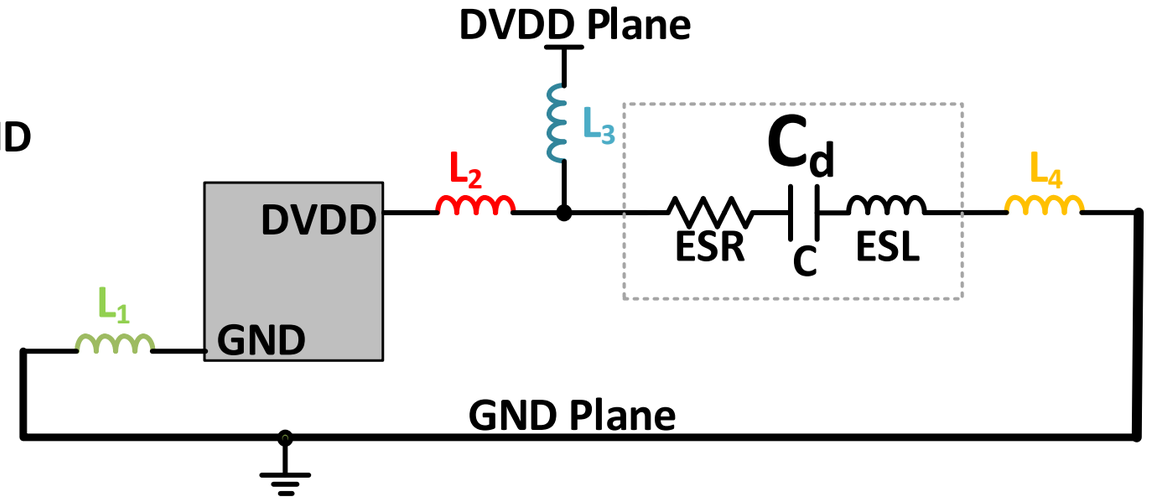
Schematic Design



Layout



Circuit including parasitics



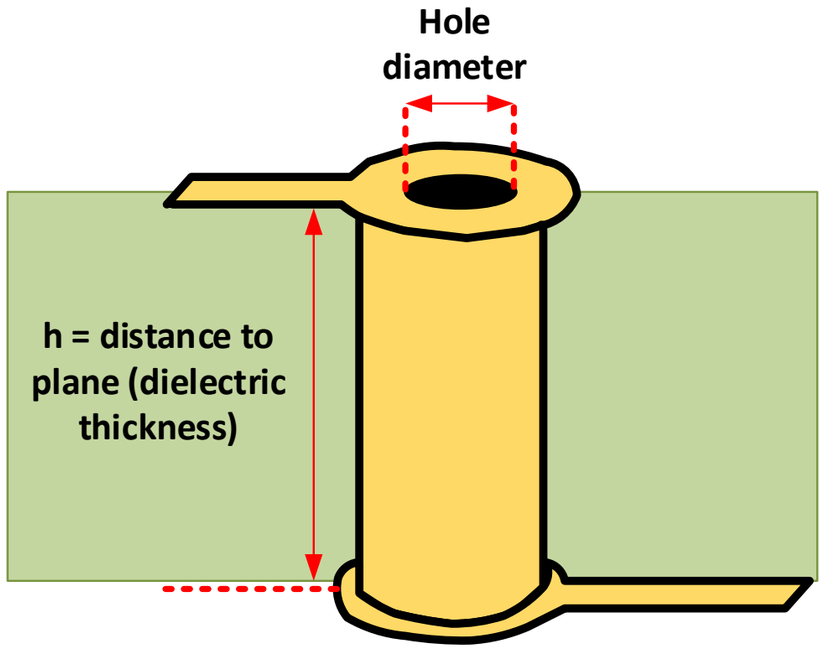
via inductance

Via inductance		
Drill hole (mil)	**h - Distance to Plane (mil)**	**Inductance - FR4**
12	9	0.0959nH
12	62	1.26782nH
16	9	0.08273nH
16	62	1.17729nH
20	9	0.07253nH
20	62	1.10706nH

Note 1: 9 mil is typical pre-preg thickness, 62 mil is typical two layer board thickness.
Note 2: 12 mil is typical minimum drilled via hole size.

Via Inductance

- Reducing dielectric thickness (h) significantly reduces inductance
- Using larger vias also helps incrementally
- Multiple vias are parallel inductors, so two similar vias will cut the inductance in half

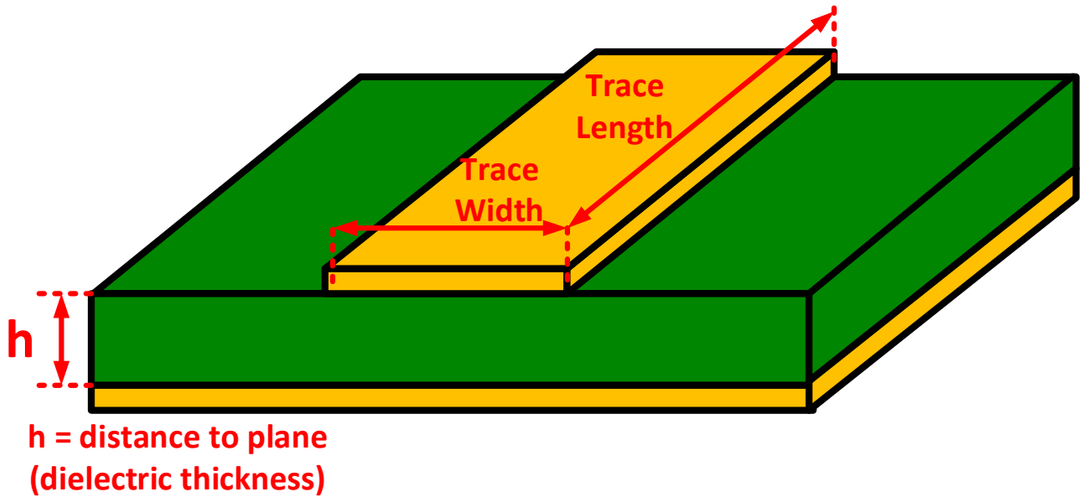


Trace inductance

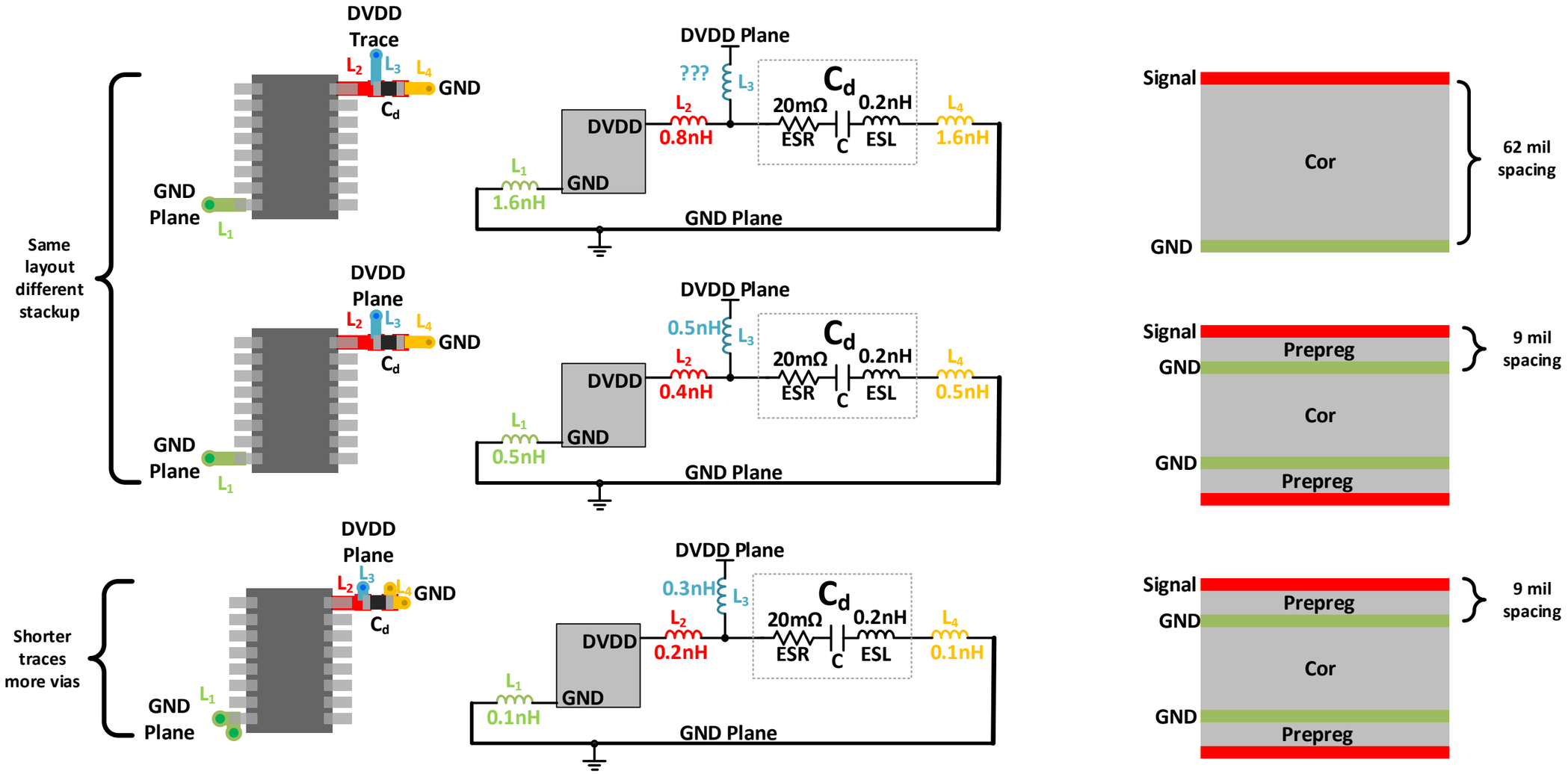
Trace inductance			
Length (mil)	**Width (mil)**	**h - Distance to Plane (mil)**	**Inductance**
100	8	9	0.9814n
100	8	62	1.960n
100	12	9	0.8065n
100	12	62	1.785n
100	20	9	0.5735n
100	20	62	1.552n
1000	20	9	5.735n
1000	20	62	15.52n

Trace Inductance

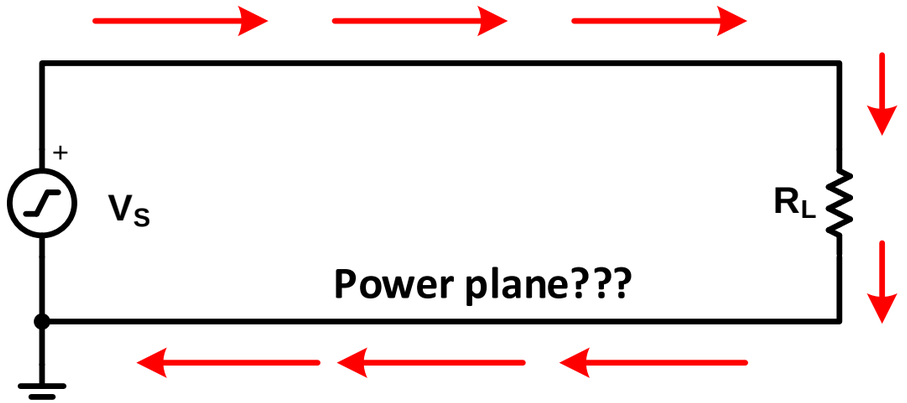
- Increasing width decreases inductance
- Decreasing the length decreases inductance
- Reducing dielectric thickness reduces inductance



Comparison of parasitic inductance and ESL

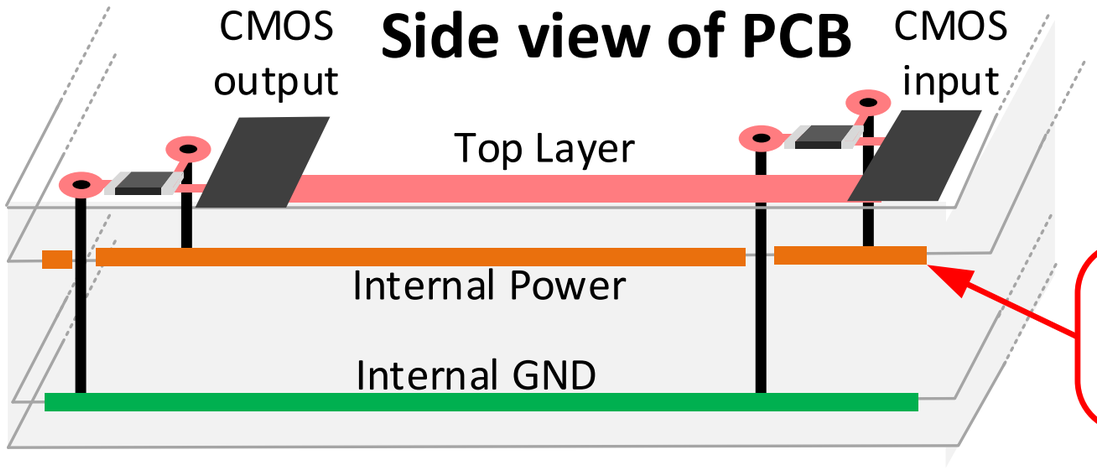


Can return current flow through the power plane?

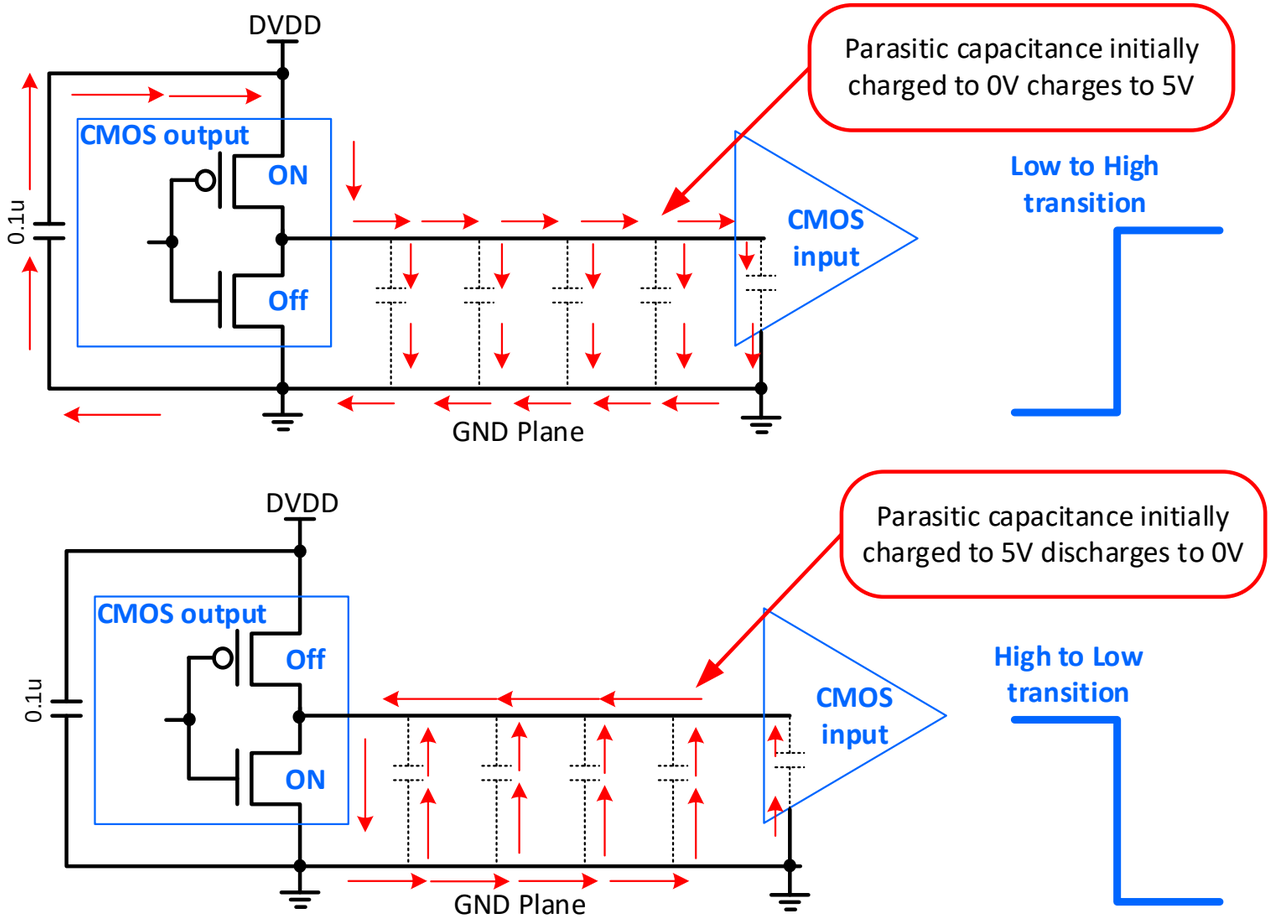


Can return current flow through the power plane?

- I seems counter intuitive that return current can flow through the power plane, but it can.
- The next two slides will show how current flows in the GND or power plane for a CMOS gate depending on which plane is adjacent to the signal path.

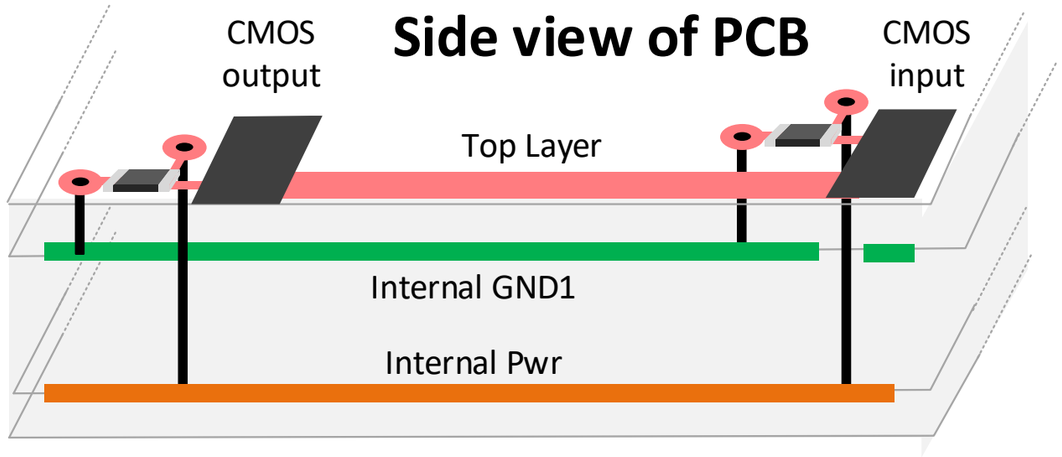


Decoupling: How does current flow in GND plane?

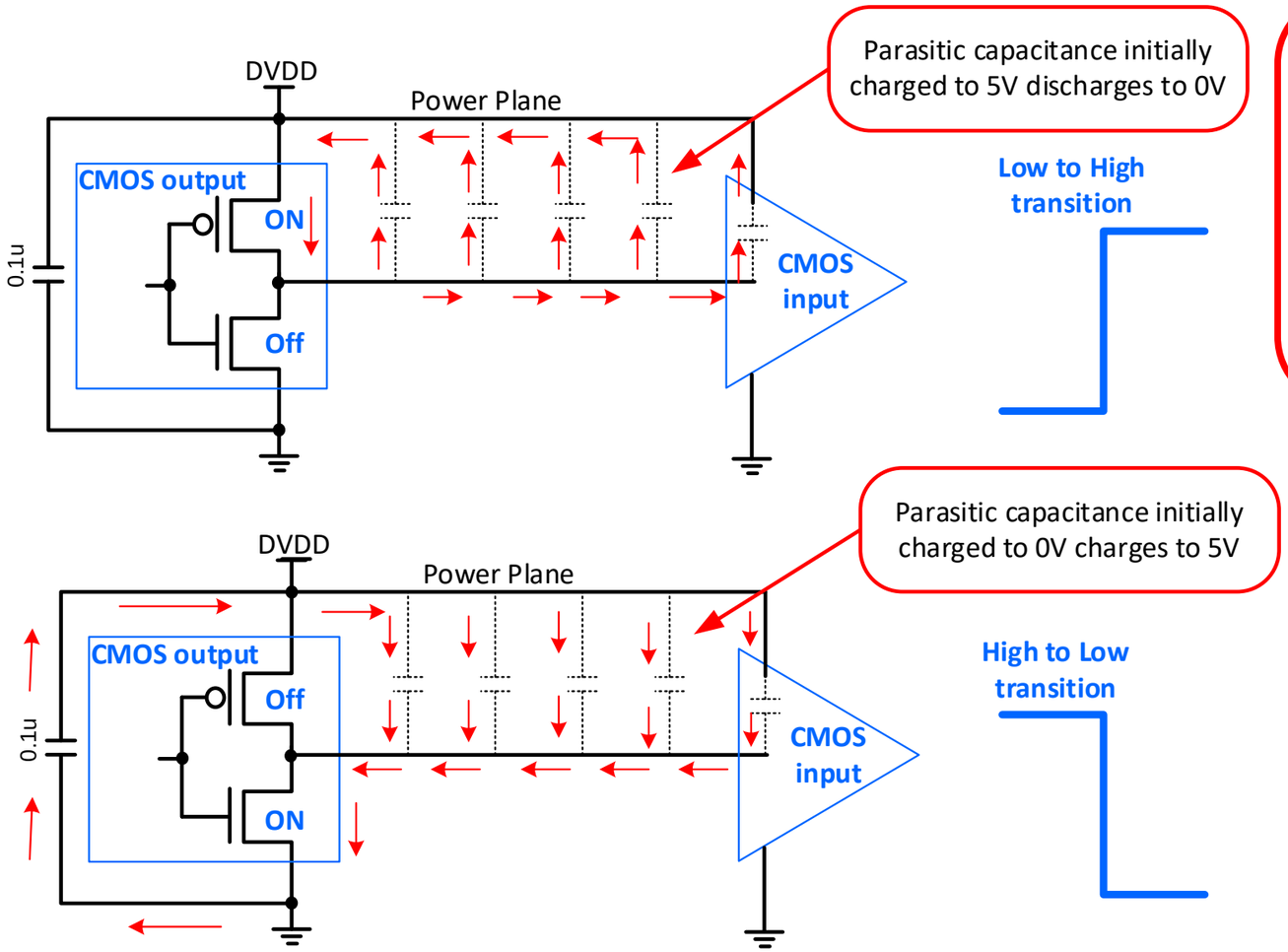


Current flow for adjacent GND Plane for microstrip

- **Low to high transition**: decoupling capacitor supplies transient current to charge parasitic capacitance of bus and CMOS input.
- **High to Low transition**: parasitic capacitance of bus discharge through the CMOS output

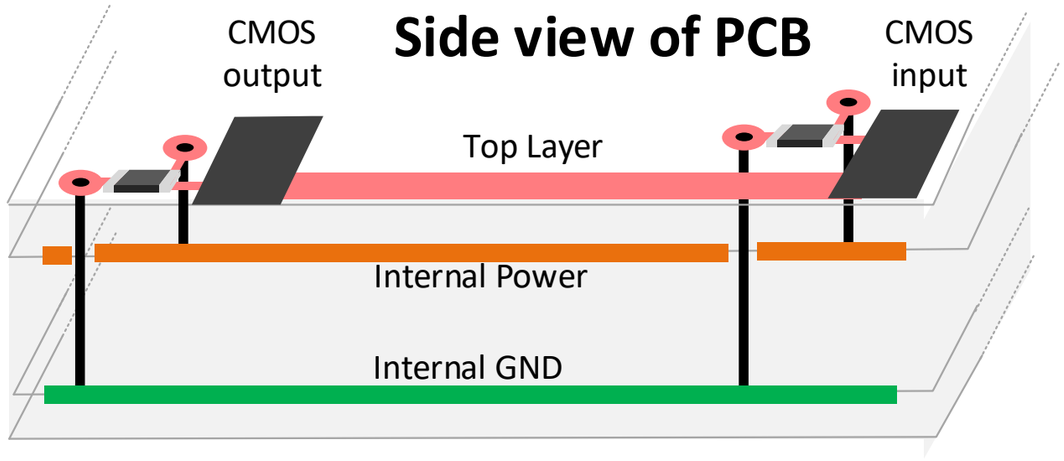


Decoupling: How does current flow in power plane?

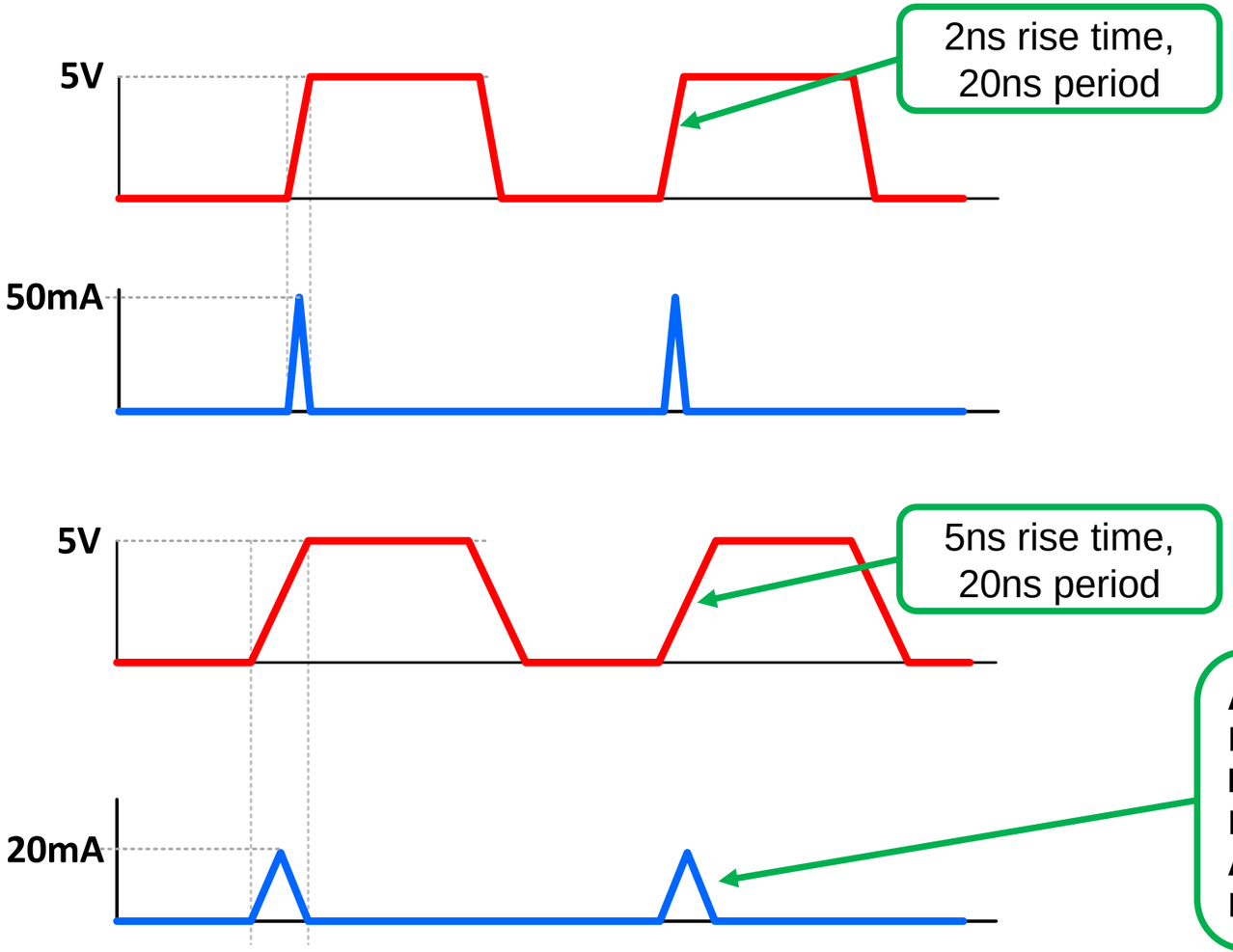


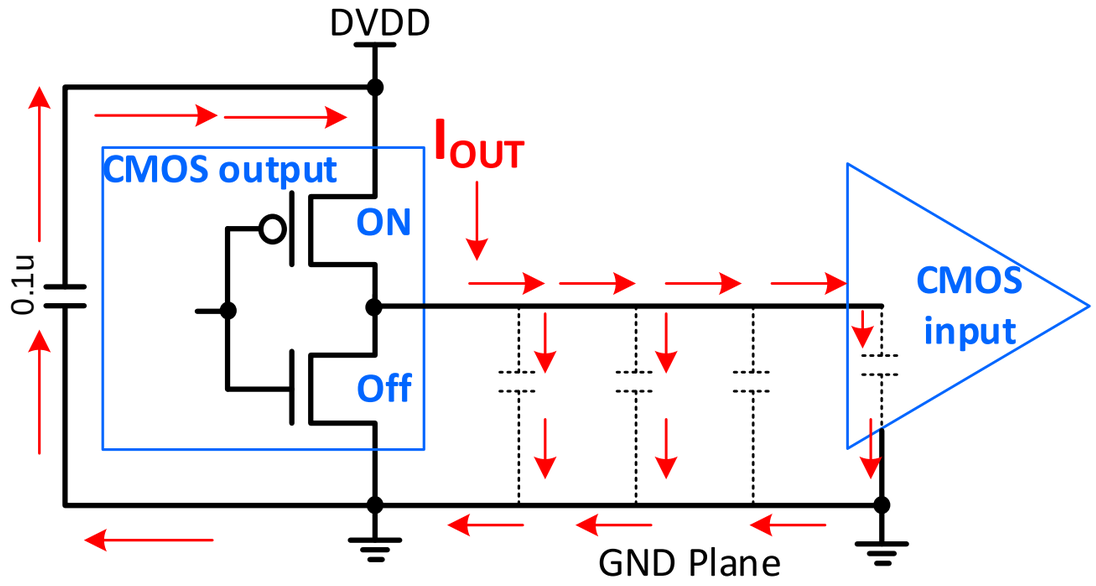
Current flow for adjacent power Plane for microstrip

- **Low to high transition**: parasitic capacitance of bus discharge through the CMOS output
- **High to Low transition**: decoupling capacitor supplies transient current to charge parasitic capacitance of bus and CMOS input.



How much current does the decoupling deliver?



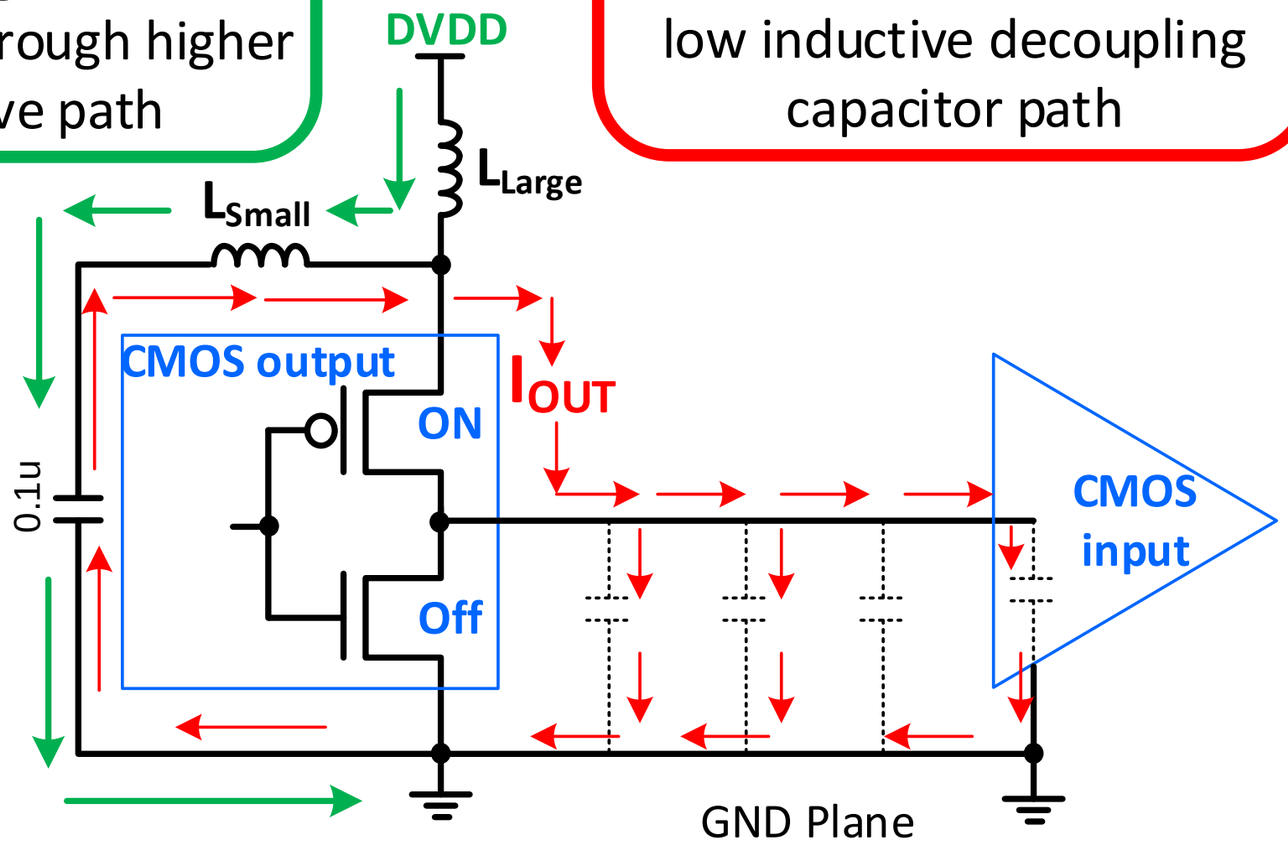


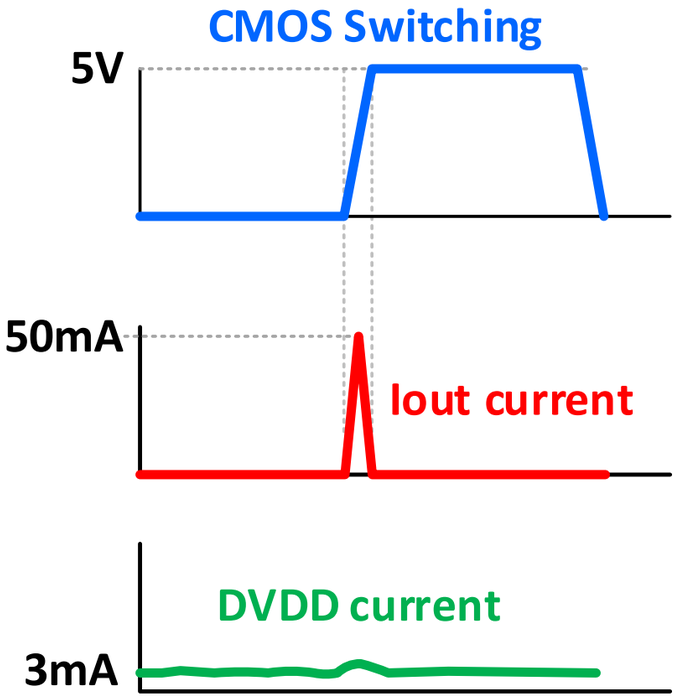
Average current during 5ns transition:
$I_x = \Delta Q/\Delta t = C\cdot \Delta V/\Delta t = 10pF \cdot 5V / 5ns = 10mA$
Peak current assuming isosceles triangle
$Ipk = 2I_x = 20mA$
Average current in period:
$I_{avg\_per} = \Delta Q/\Delta t = C\cdot \Delta V/\Delta t = 10pF \cdot 5V / 20ns = 3mA$

The supply doesn't provide the transient current

DVDD Slowly Recharge Decoupling between transients through higher inductive path

Iout Digital switching gets fast transient response from low inductive decoupling capacitor path





Thanks for your time!
Please try the quiz.

Quiz: Decoupling capacitors

1. (True/False) Using a large and small value decoupling capacitor is a good way to improve decoupling because the small value decoupling capacitor will be optimal for high frequency. For example, connecting a 0.1uF and a 0.001uF capacitor in parallel is a good combination for better high frequency decoupling.
   a) True
   b) False

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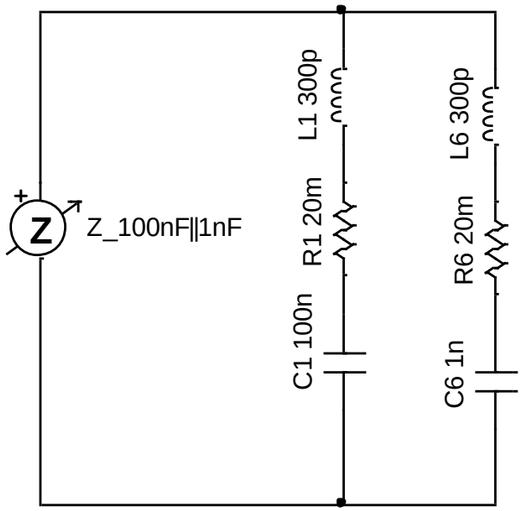
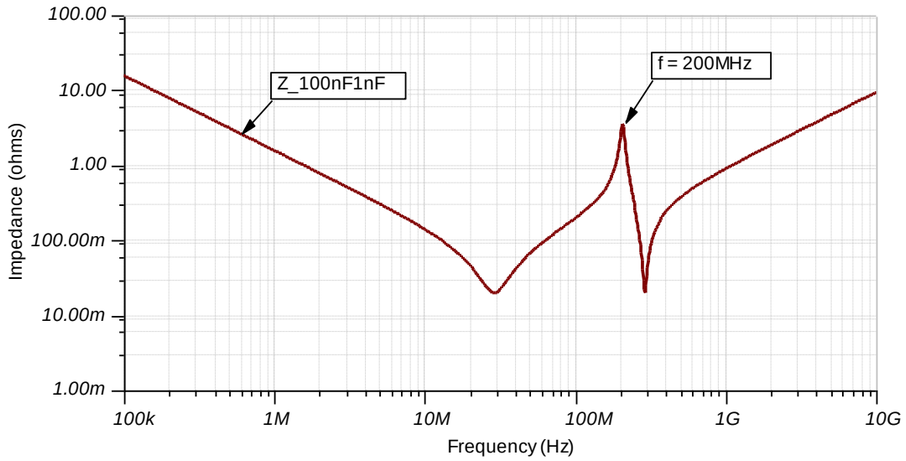
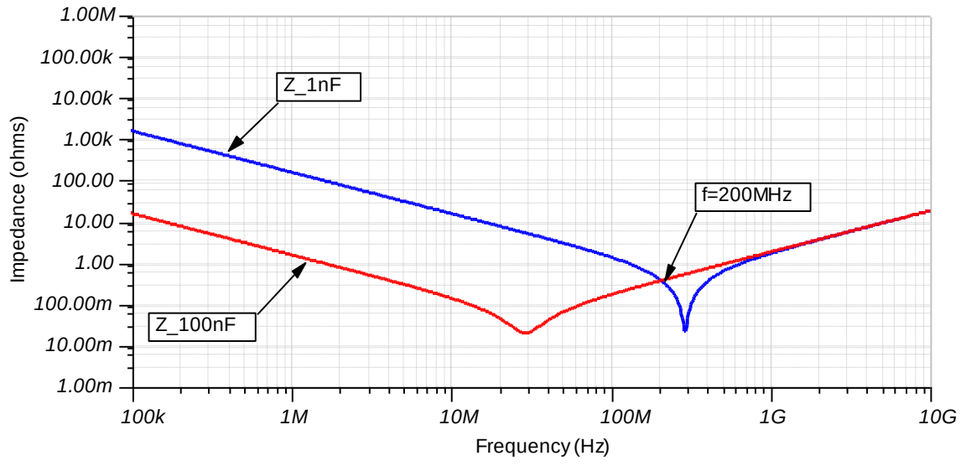






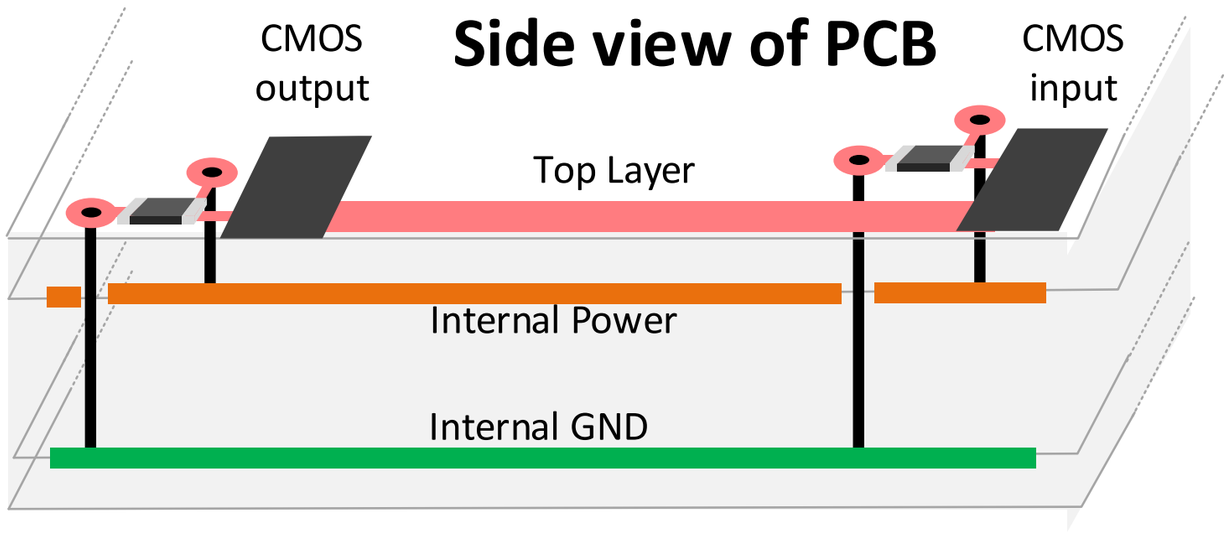
Quiz: Decoupling capacitors

2. (True/False) For low inductance, it is better to place multiple small via than one large one. For example, two 12mil via would have lower inductance than one 20mil via.
   a) True
   b) False

3. (True/False) The thickness of the dielectric between the decoupling capacitor and ground plane will impact the decoupling effectiveness.
   a) True
   b) False

Quiz: Decoupling capacitors

4. (True/False) For the layout below, when a signal is being transmitted from the CMOS output to the input, the return current will flow in the ground plane (GND).
   a) True
   b) False



Thanks for your time!