What is Clock and Data Recovery (CDR) ?

TI Precision Labs – HSSC

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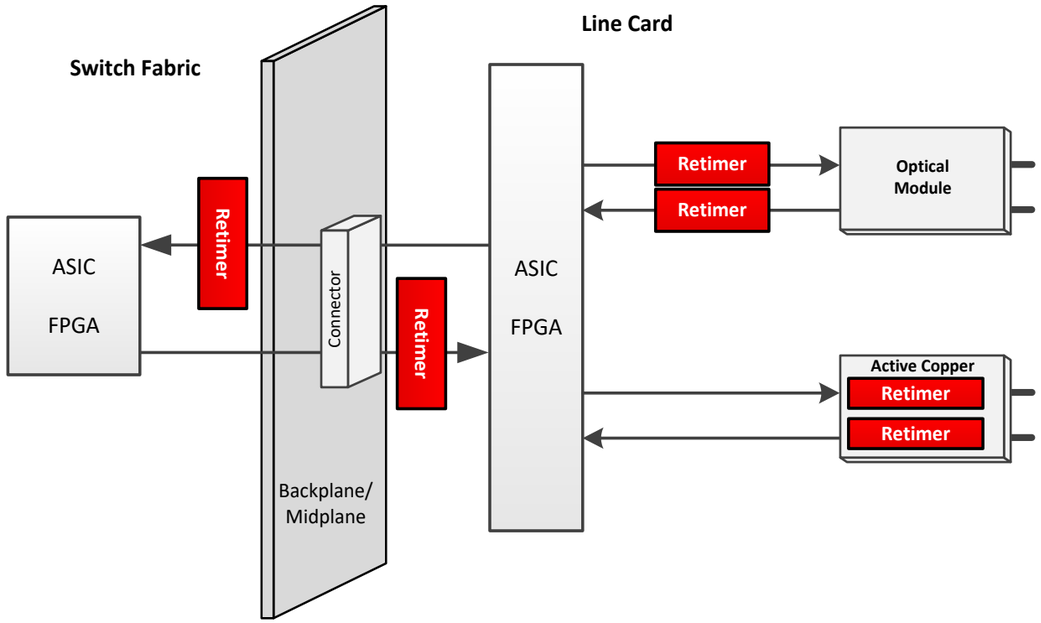
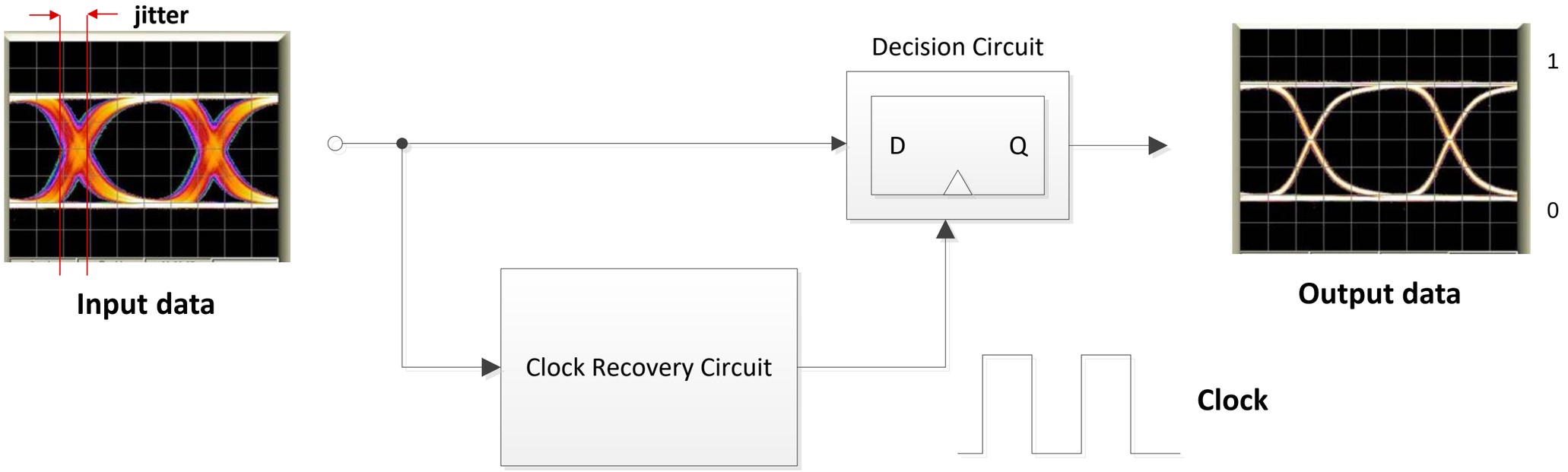
Why are CDR retimers important?



Example retimer system, enterprise networking switch

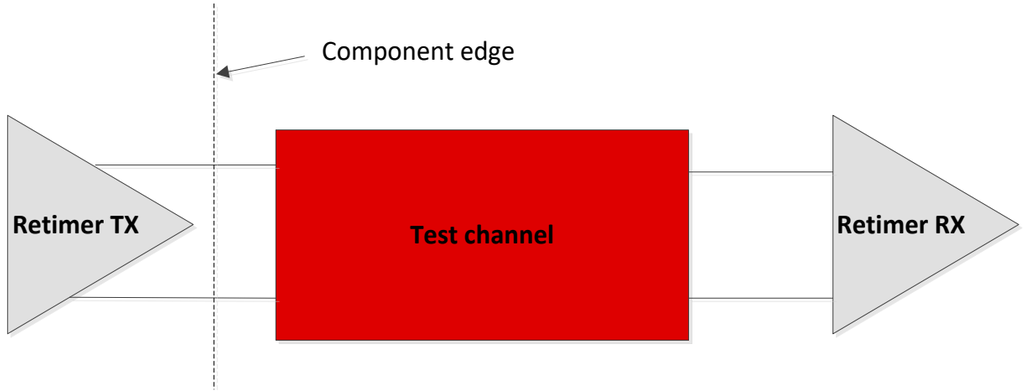
Clock and data recovery (CDR) in retimers reduce noise and jitter in data signals, extend system link reaches and lower achievable bit error rates and enable system compliance to high-speed standard specifications.

What function do CDRs perform in retimers?

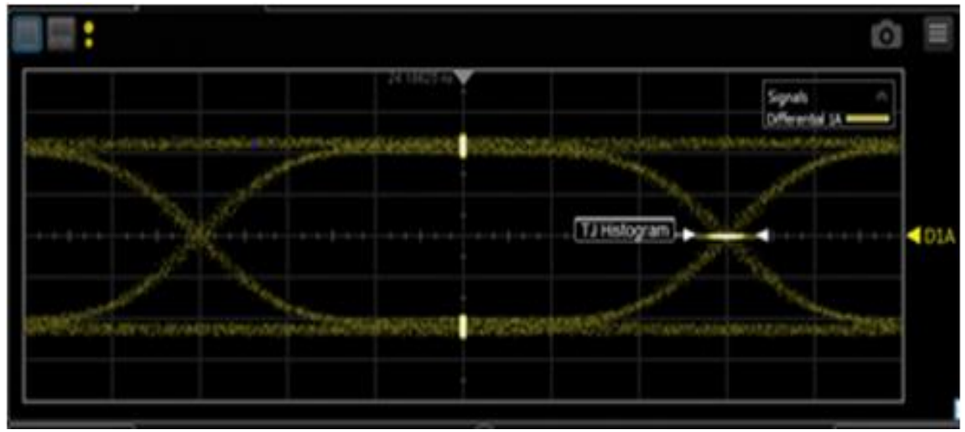


Simplified diagram of a CDR based retimer

Retimer with CDR Tx output jitter

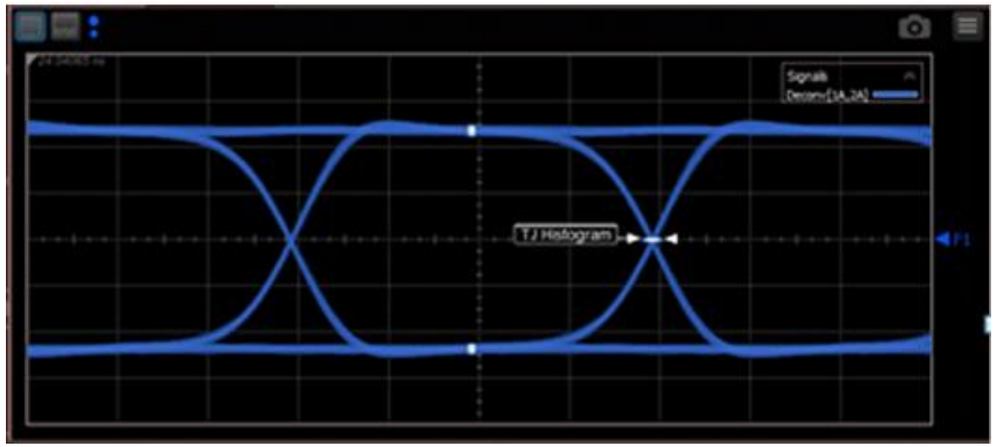


Raw data, CDR bypassed



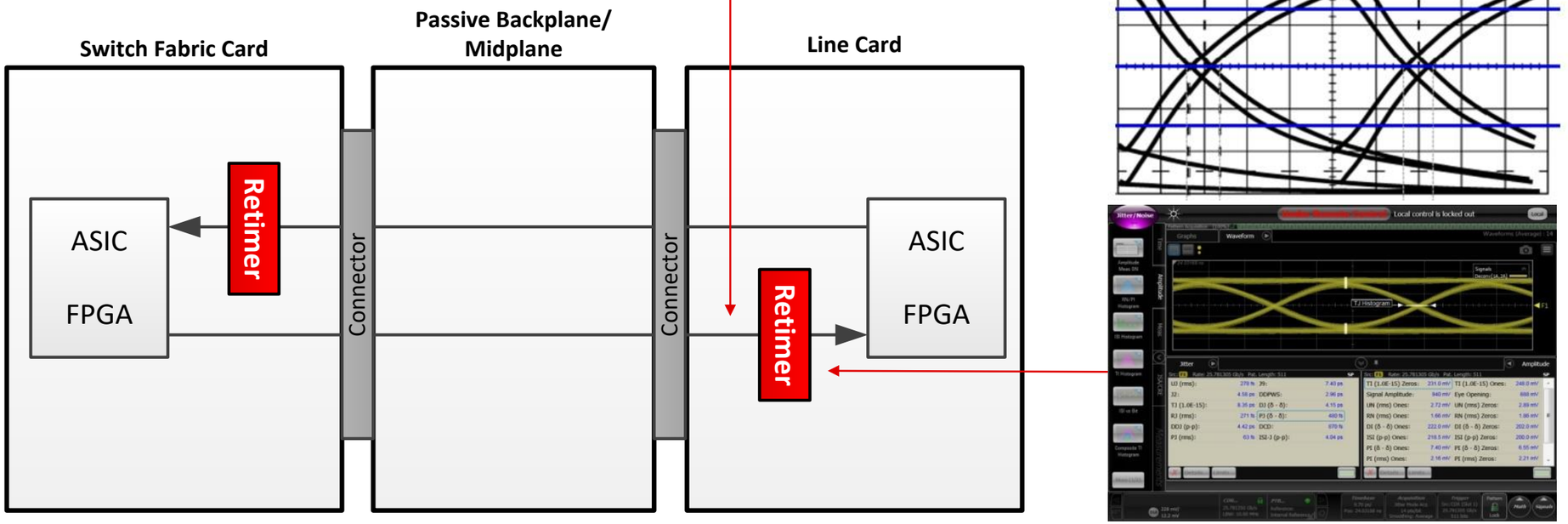
Total jitter = 13.0ps

Retimed data, CDR enabled



Total jitter = 7.15ps

Choosing a retimer based on CDR performance



Backplane system with retimers

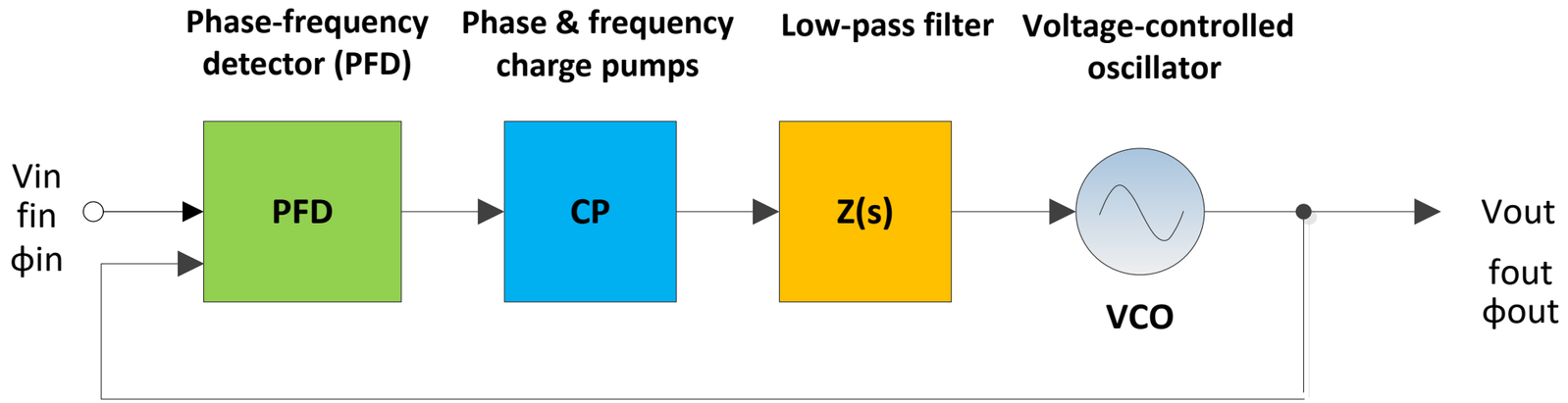
Jitter metrics

- How much jitter stress can CDR handle
- How much jitter propagates to its output

CDR lock behavior

- Data rates supported
- Lock consistency and stability over operating conditions

CDR lock acquisition in a retimer

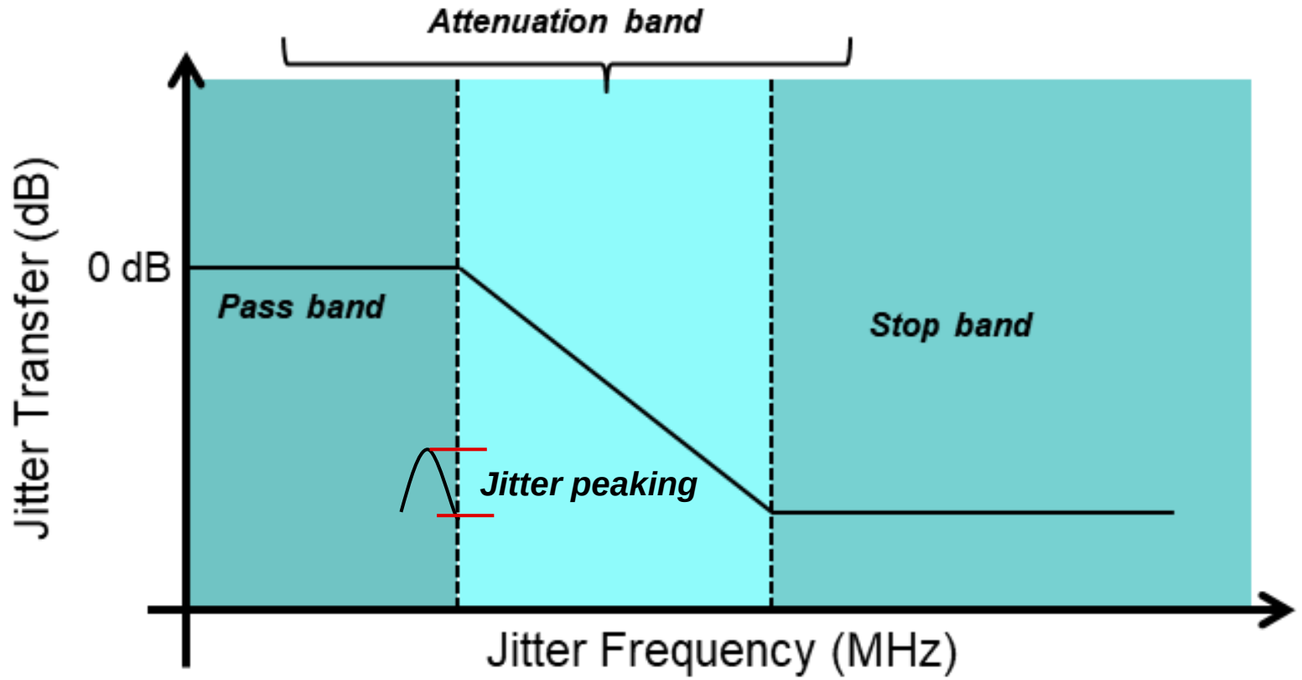


Type II PLL: phase and frequency detection

When the CDR is in locked condition, it meets the following criteria:

- Input and output phase are synchronized; $d\varphi_{out}/dt - d\varphi_{in}/dt = 0$ (φ is phase)
- $f_{out} = f_{in}$ (f is frequency)
  - f_{out} linearly tracks the control voltage (Vcont)
  - Average Vout that tracks small changes in input phase -> $\Delta\varphi$

CDR metric: jitter transfer (JXFR)



Parameters of interest

- CDR loop bandwidth
- Pass band, attenuation band and stop band
- Jitter peaking

- Output jitter as a function of input jitter frequency
- May be expressed as: **JXFR = $|Jitter_{Out}(f) / Jitter_{in}|(f)|$**

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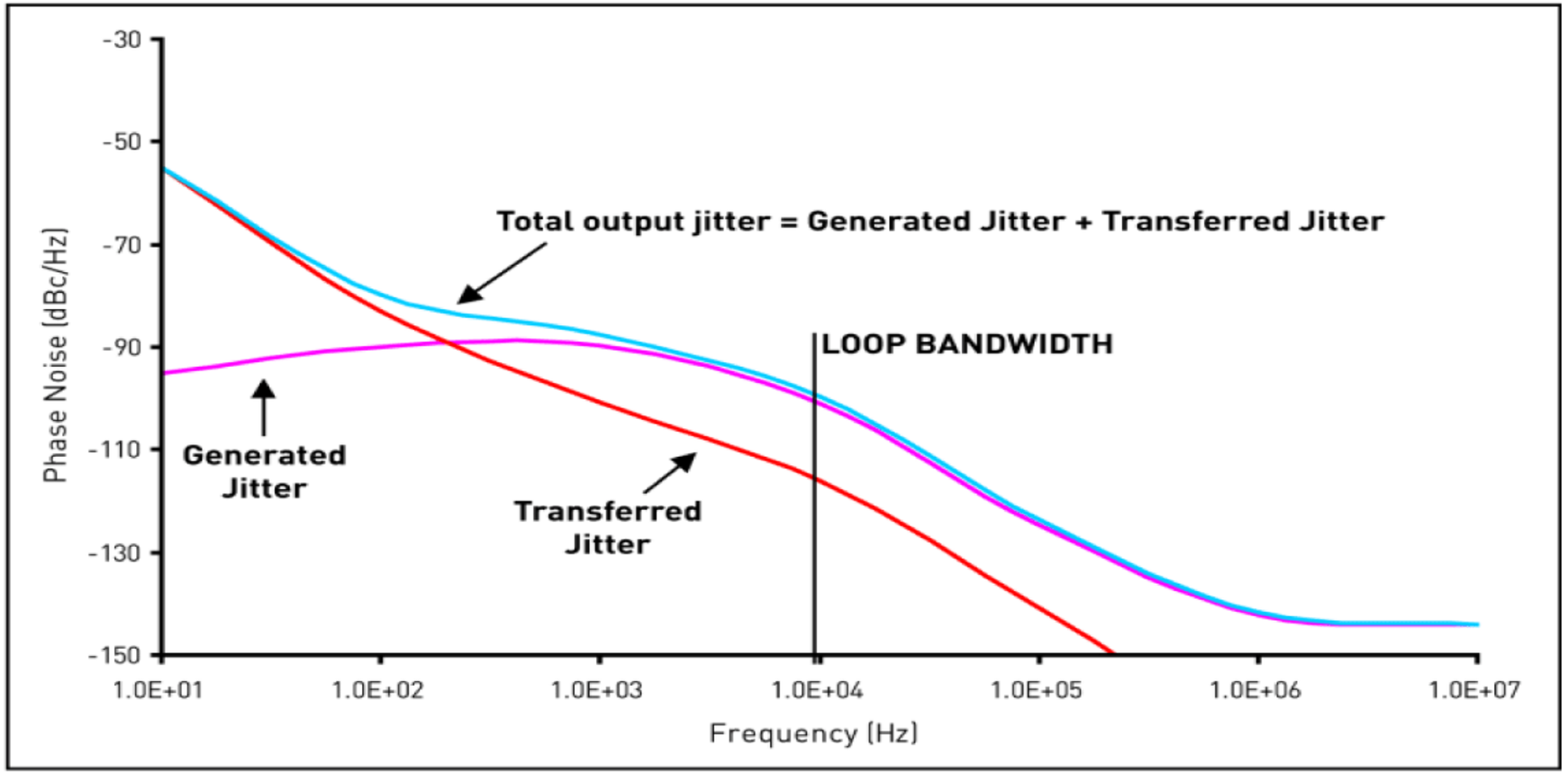
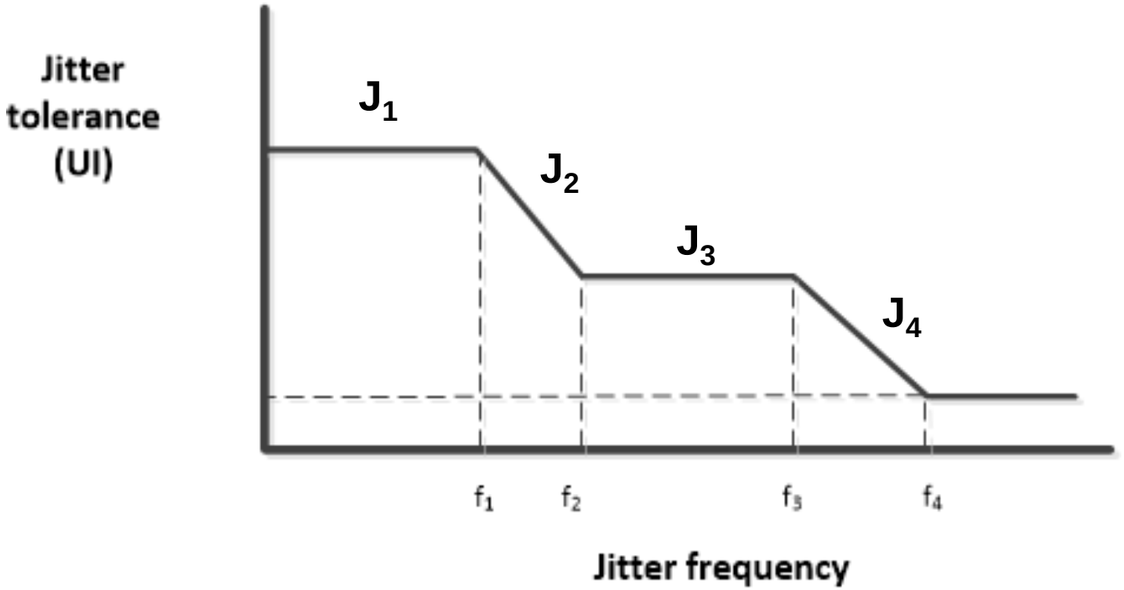
CDR metric: jitter generation

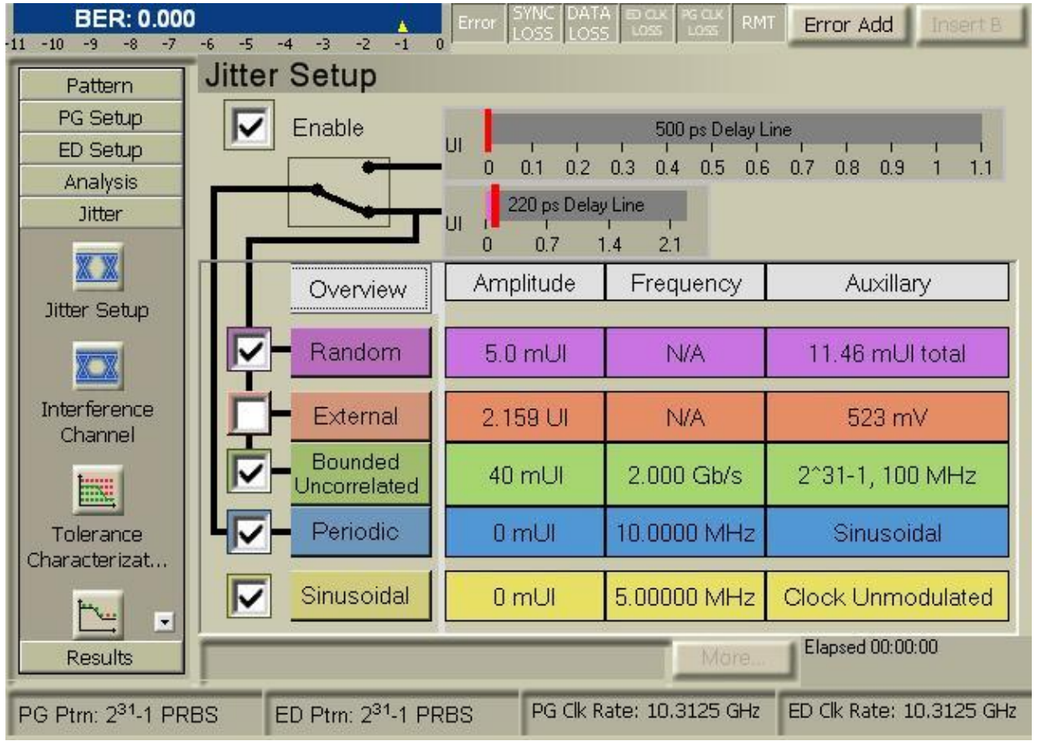


- Amount of output jitter for jitter free input data, as a function of frequency
- Jitter generation is a result of the CDR device intrinsic noise parameters

CDR metric: jitter tolerance (JTOL)



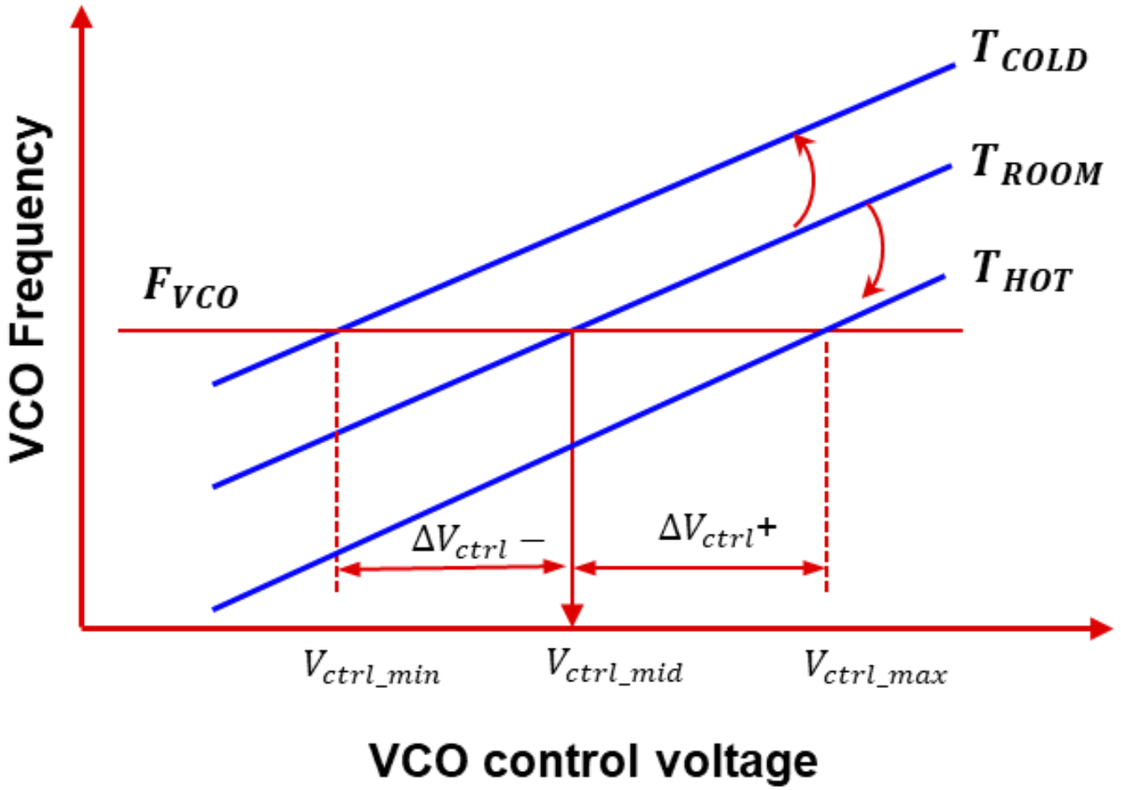
Representation of jitter tolerance mask used by standards



Example setup window for data generator with jitter stress

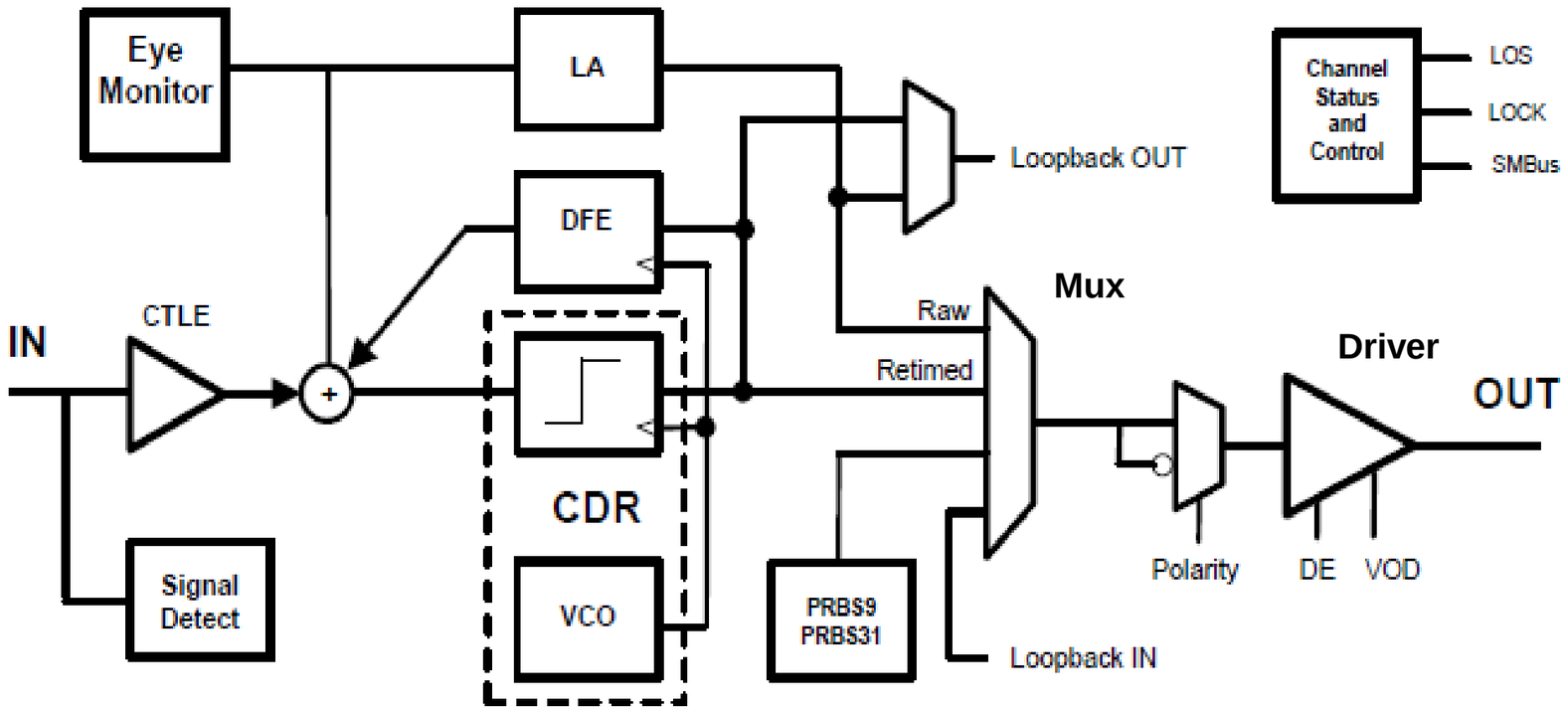
- Amount of input jitter that can be applied to the CDR without increasing bit error rate (BER)
- The higher the JTOL, the more link margin available to the system

CDR metric: temperature lock range (TLR)



- TLR is the operating temperature range for which CDR can reliably maintain lock
- The larger the TLR, the more robust and versatile the retimer

Functional block diagram of a 10Gbps retimer



In addition to the CDR, retimers may also implement input equalization, output equalization & system diagnostic features.