

How gain impacts ADC FSR, noise, and dynamic range

TIPL 4256

TI Precision Labs – ADCs

Created by Chris Hall & Bryan Lizon

Presented by Alex Smith

ADC full-scale range (FSR)

ADC w/ no integrated gain

ADS8900B FSR (20-bit SAR ADC)

PARAMETER	MIN	TYP	MAX	UNIT
ANALOG INPUT				
FSR	Full-scale input range (AINP – AINM)	-V _{REF}	V _{REF}	V

ADCs w/ integrated gain

ADS8691 FSR (18-bit SAR ADC)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
ANALOG INPUTS				
Full-scale input span (AIN_P to AIN_GND)	Input range = $\pm 3 \times V_{REF}$	-12.288	12.288	V
	Input range = $\pm 2.5 \times V_{REF}$	-10.24	10.24	
	Input range = $\pm 1.5 \times V_{REF}$	-6.144	6.144	
	Input range = $\pm 1.25 \times V_{REF}$	-5.12	5.12	
	Input range = $\pm 0.625 \times V_{REF}$	-2.56	2.56	
	Input range = $3 \times V_{REF}$	0	12.288	
	Input range = $2.5 \times V_{REF}$	0	10.24	
	Input range = $1.5 \times V_{REF}$	0	6.144	
	Input range = $1.25 \times V_{REF}$	0	5.12	

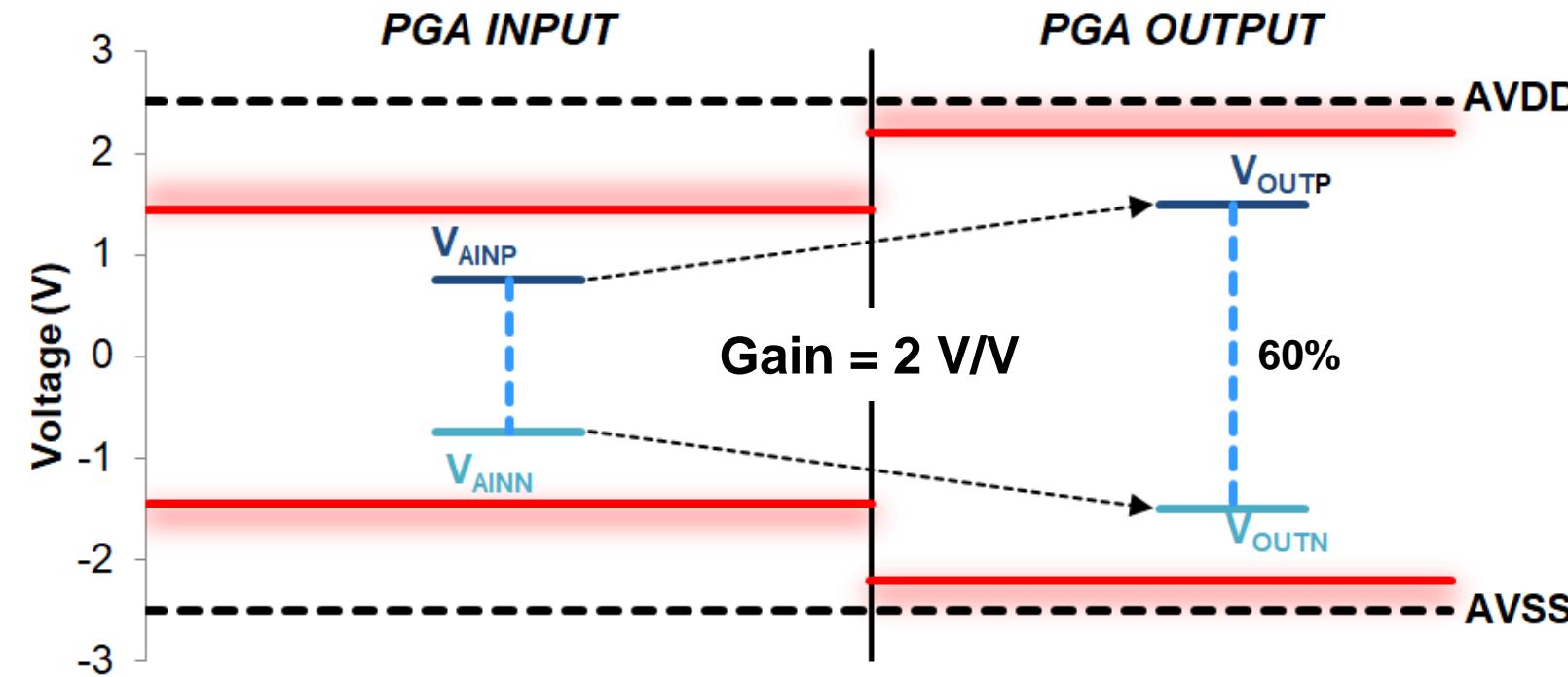
ADS124S08 FSR (24-bit delta-sigma ADC)

	NOM	UNIT
ANALOG INPUTS		
V _{IN}	V _{IN} = V _{AINP} – V _{AINN}	$\pm V_{REF} / Gain$

ADS124S08 PGA input and output range

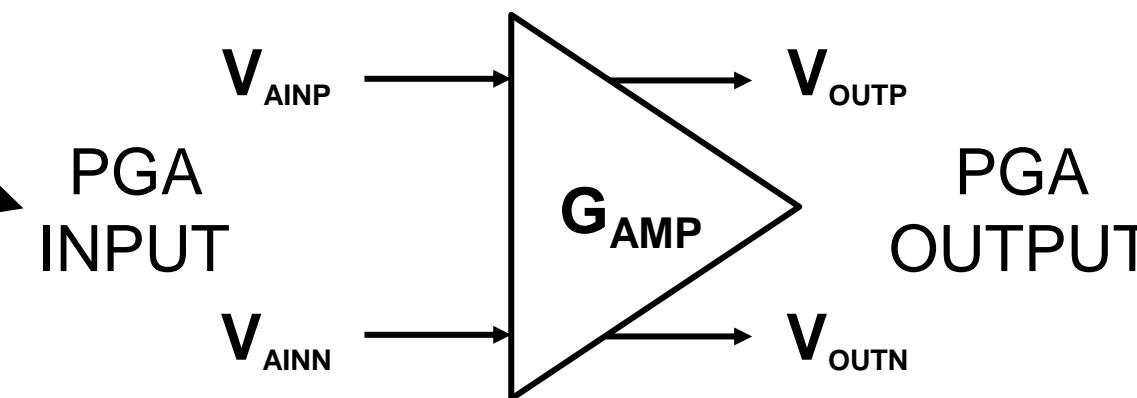
$$FSR_{ADS124S08} = \frac{\pm V_{REF}}{Gain}$$

$$V_{SIG_IN} = \pm 0.75 \text{ V}$$
$$FSR_{IN} = \pm 1.25 \text{ V}$$



$$V_{REF} = 2.5 \text{ V}$$
$$V_{SIG_OUT} = \pm 1.5 \text{ V}$$
$$FSR_{OUT} = \pm 2.5 \text{ V}$$

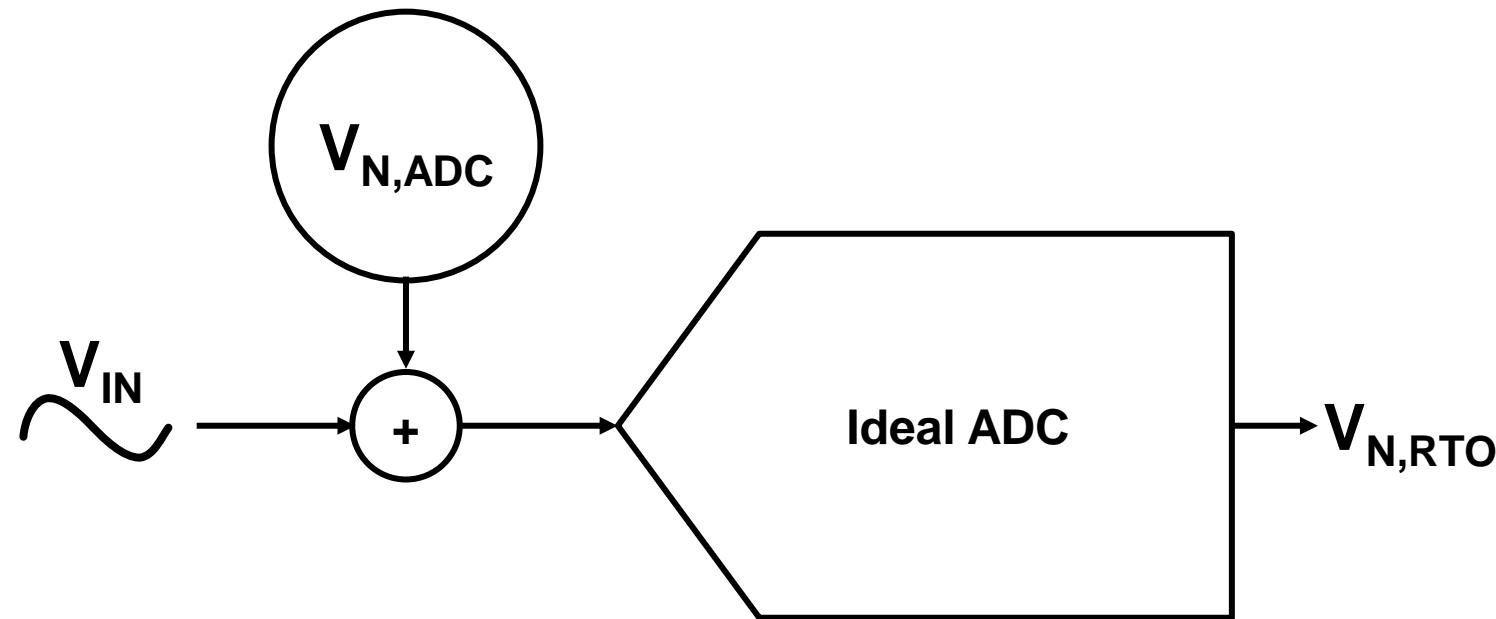
Refer both signal *and* noise to the input



To access this calculator, navigate to the ADS124S08's product folder on TI.com

Output- versus input-referred noise

Equivalent ADC Noise Model:



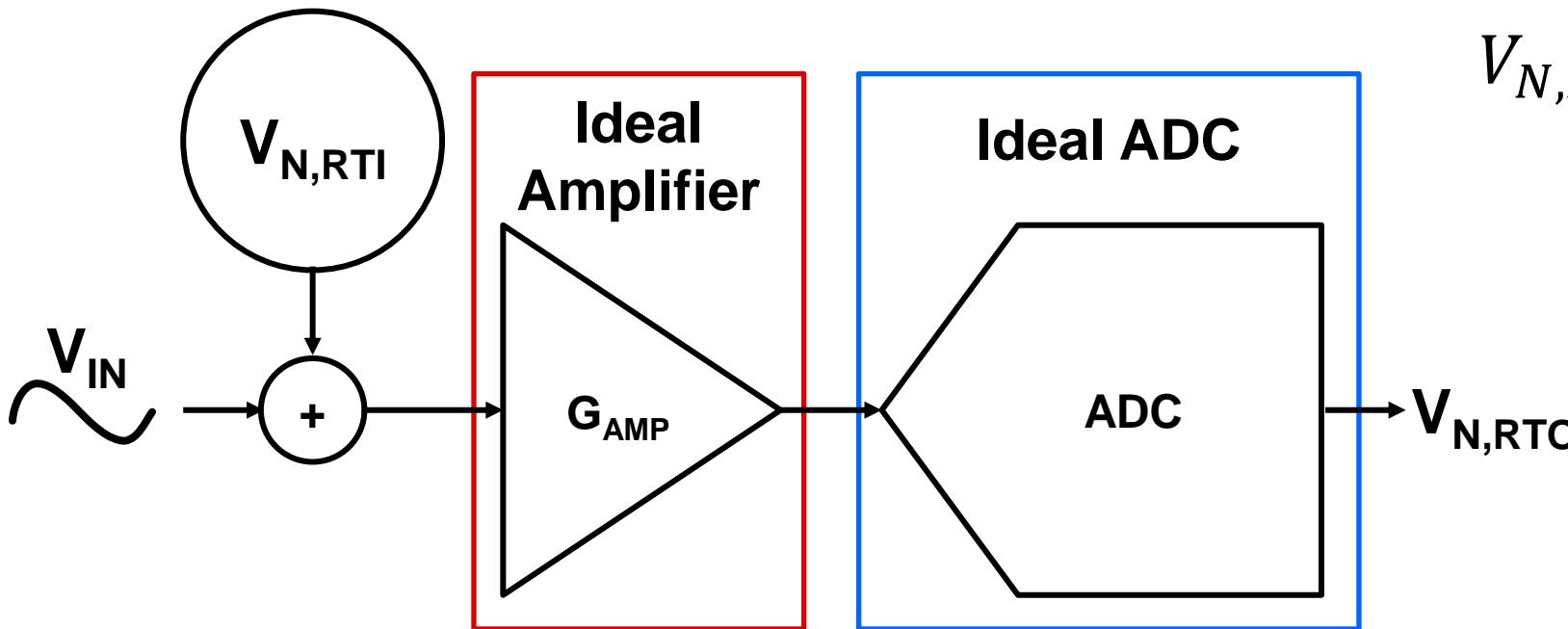
$V_{N,RTI}$ is the system's input resolution:

- If $V_{IN} < V_{N,RTI}$, the signal is below the noise floor
- Else if $V_{IN} > V_{N,RTI}$, the signal can be observed

For ADC w/ no gain, $V_{N,RTO} = V_{N,RTI} = V_{N,ADC}$

Input-referred noise for amp + ADC

Equivalent Amp + ADC Noise Model:



For ADC w/ gain, $V_{N,RTO} \neq V_{N,RTI}$

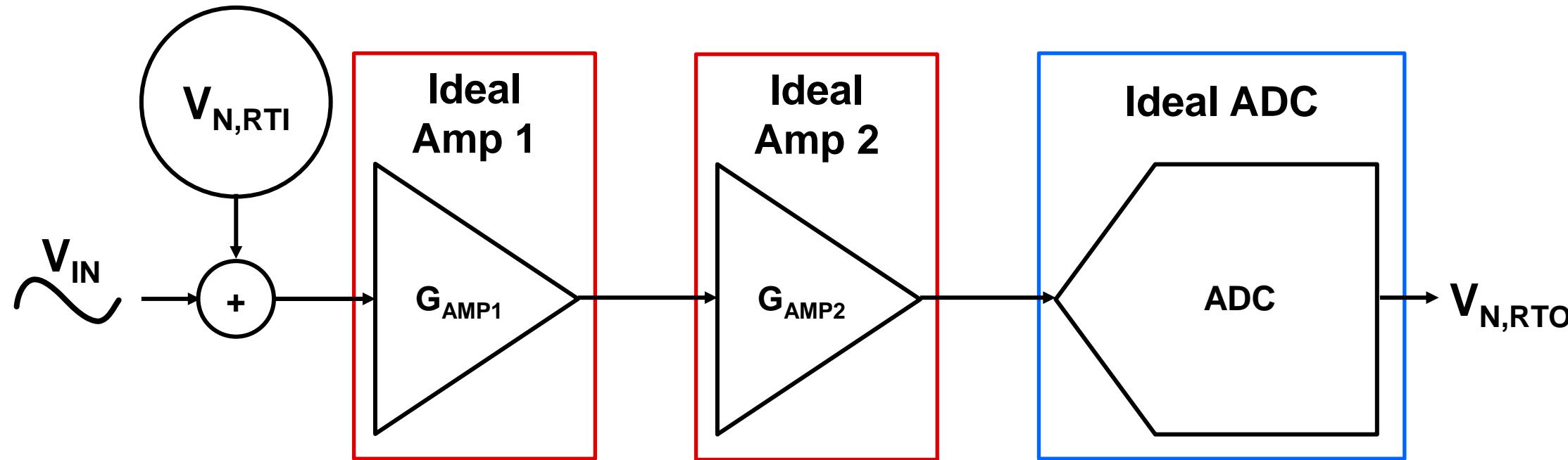
$$V_{N,RTO} = \sqrt{(V_{N,AMP(RTI)} * G_{AMP})^2 + (V_{N,ADC})^2}$$

$$V_{N,RTI} = \sqrt{(V_{N,AMP(RTI)})^2 + (V_{N,ADC}/G_{AMP})^2}$$

$G_{AMP} * V_{N,AMP(RTI)} \gg V_{N,ADC}$

Input-referred noise for 2x amps + ADC

Equivalent 2x Amplifier + ADC Noise Model:

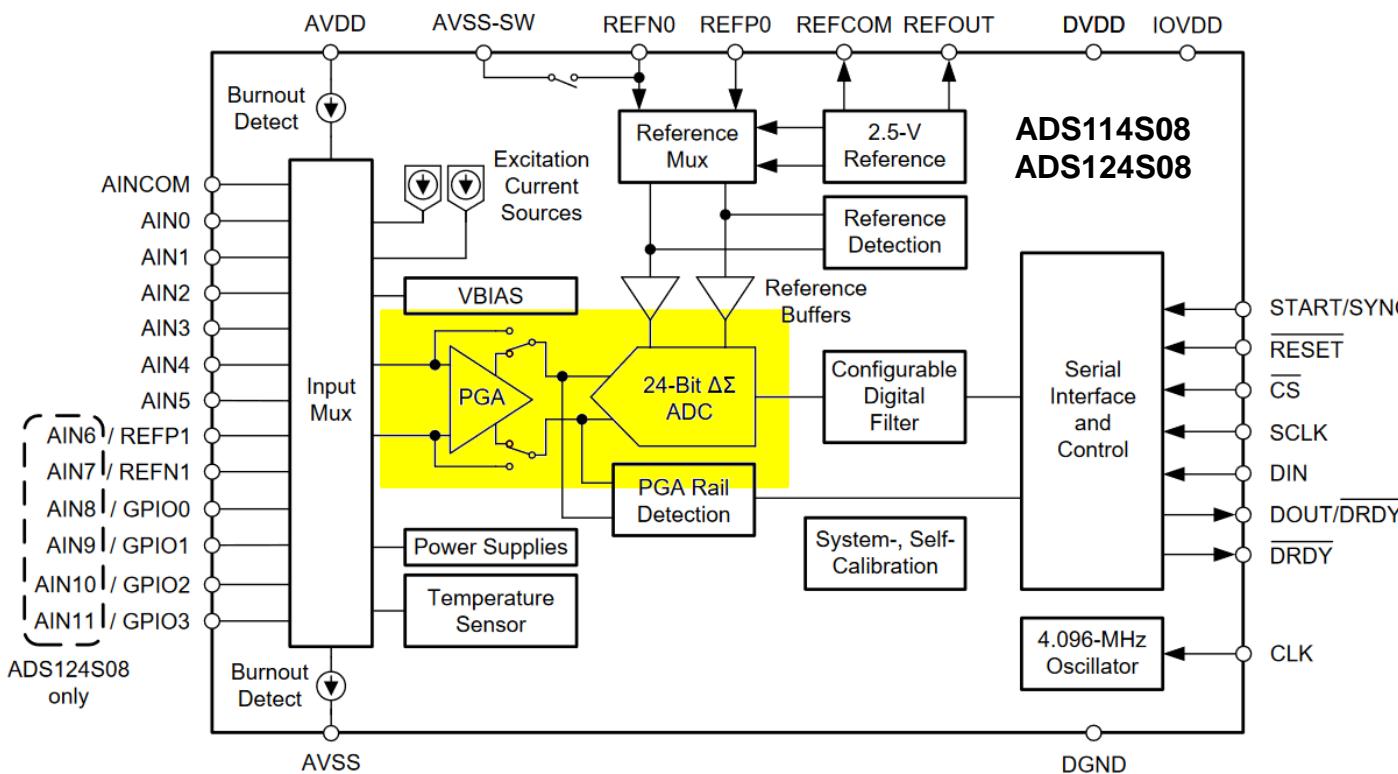


$$V_{N,RTI} = \sqrt{V_{N,AMP1(RTI)}^2 + \left(\frac{V_{N,AMP2(RTI)}^0}{G_{AMP1}} \right)^2 + \left(\frac{V_{N,ADC}^0}{G_{AMP1} * G_{AMP2}} \right)^2}$$

If $G_{AMP1} * G_{AMP2} * V_{N,AMP1(RTI)} \gg (G_{AMP2} * V_{N,AMP2(RTI)}) + V_{N,ADC}$, then $V_{N,RTI} = V_{N,AMP1(RTI)}$

Lower vs higher-resolution ADC total noise

ADS1x4S08 block diagram



16-bit ADS114S08

Parameters (Sinc 3, 60 SPS)	Gain								Units
	1	2	4	8	16	32	64	128	
Noise, RTI	76.3	38.1	19.1	9.5	4.8	2.4	1.2	0.6	µV _{RMS}

$$\frac{V_{N,G=1}}{V_{N,G=2}} = \frac{76.3 \mu V_{RMS}}{38.1 \mu V_{RMS}} = 2$$

$$\frac{V_{N,G=64}}{V_{N,G=128}} = \frac{1.2 \mu V_{RMS}}{0.6 \mu V_{RMS}} = 2$$

24-bit ADS124S08

Parameters (Sinc 3, 60 SPS)	Gain								Units
	1	2	4	8	16	32	64	128	
Noise, RTI	1.4	0.7	0.37	0.21	0.12	0.11	0.1	0.089	µV _{RMS}

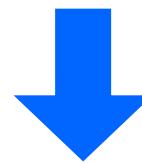
$$\frac{V_{N,G=1}}{V_{N,G=2}} = \frac{1.4 \mu V_{RMS}}{0.7 \mu V_{RMS}} = 2$$

$$\frac{V_{N,G=64}}{V_{N,G=128}} = \frac{0.1 \mu V_{RMS}}{0.09 \mu V_{RMS}} = 1.1$$

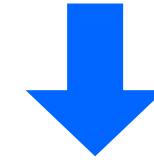
Applying the input-referred noise equation

$$V_{N,RTI} = \sqrt{(V_{N,AMP(RTI)})^2 + (V_{N,ADC}/G_{AMP})^2} \quad (nV_{RMS})$$

**Lower-resolution ADCs –
quantization noise dominates**



$$G_{AMP} * V_{N,AMP(RTI)} < V_{N,ADC}$$



- Use a higher-noise (lower \$) amp
- Larger gain if system allows

**Higher-resolution ADCs –
thermal noise dominates**



$$G_{AMP} * V_{N,AMP(RTI)} \gg V_{N,ADC}$$



- Higher gain does not reduce noise
- Use a very low noise amp

How gain affects dynamic range (effective resolution)

$$\text{Dynamic range (effective resolution)} = \log_2 \left(\frac{FSR_{RMS}}{V_{N,RMS}} \right) \text{ (bits)}$$

16-bit ADS114S08

Parameters (Sinc 3, 60 SPS)	Gain							
	1	2	4	8	16	32	64	128
Full-scale range (VREF = 2.5 V)	±2.5	±1.25	±0.625	±0.313	±0.156	±0.078	±0.039	±0.019
Noise, RTI (μV_{RMS})	76.3	38.1	19.1	9.5	4.8	2.4	1.2	0.6
Effective resolution (bits)	16	16	16	16	16	16	16	16



Increasing gain



Constant effective resolution

24-bit ADS124S08

Parameters (Sinc 3, 60 SPS)	Gain							
	1	2	4	8	16	32	64	128
Full-scale range (VREF = 2.5 V)	±2.5	±1.25	±0.625	±0.313	±0.156	±0.078	±0.039	±0.019
Noise, RTI (μV_{RMS})	1.4	0.7	0.37	0.21	0.12	0.11	0.1	0.089
Effective resolution (bits)	21.8	21.8	21.7	21.5	21.3	20.4	19.5	18.7



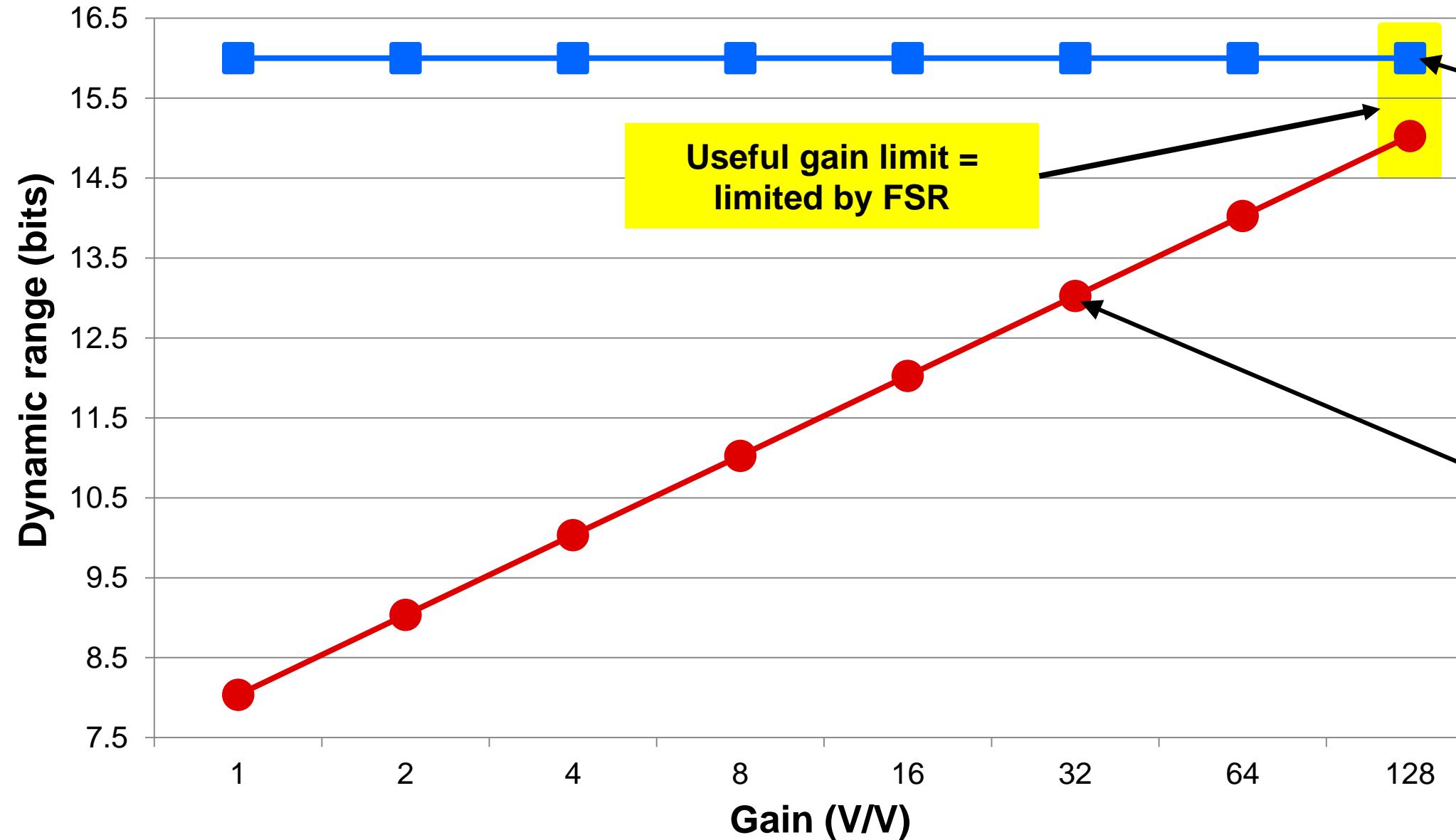
Increasing gain



Decreasing effective resolution

Dynamic range: max vs system (low resolution ADC)

ADS114S08 (16-bit) dynamic range vs gain (VREF = 2.5V)



$$V_{IN} = FSR = \frac{\pm V_{REF}}{Gain}$$

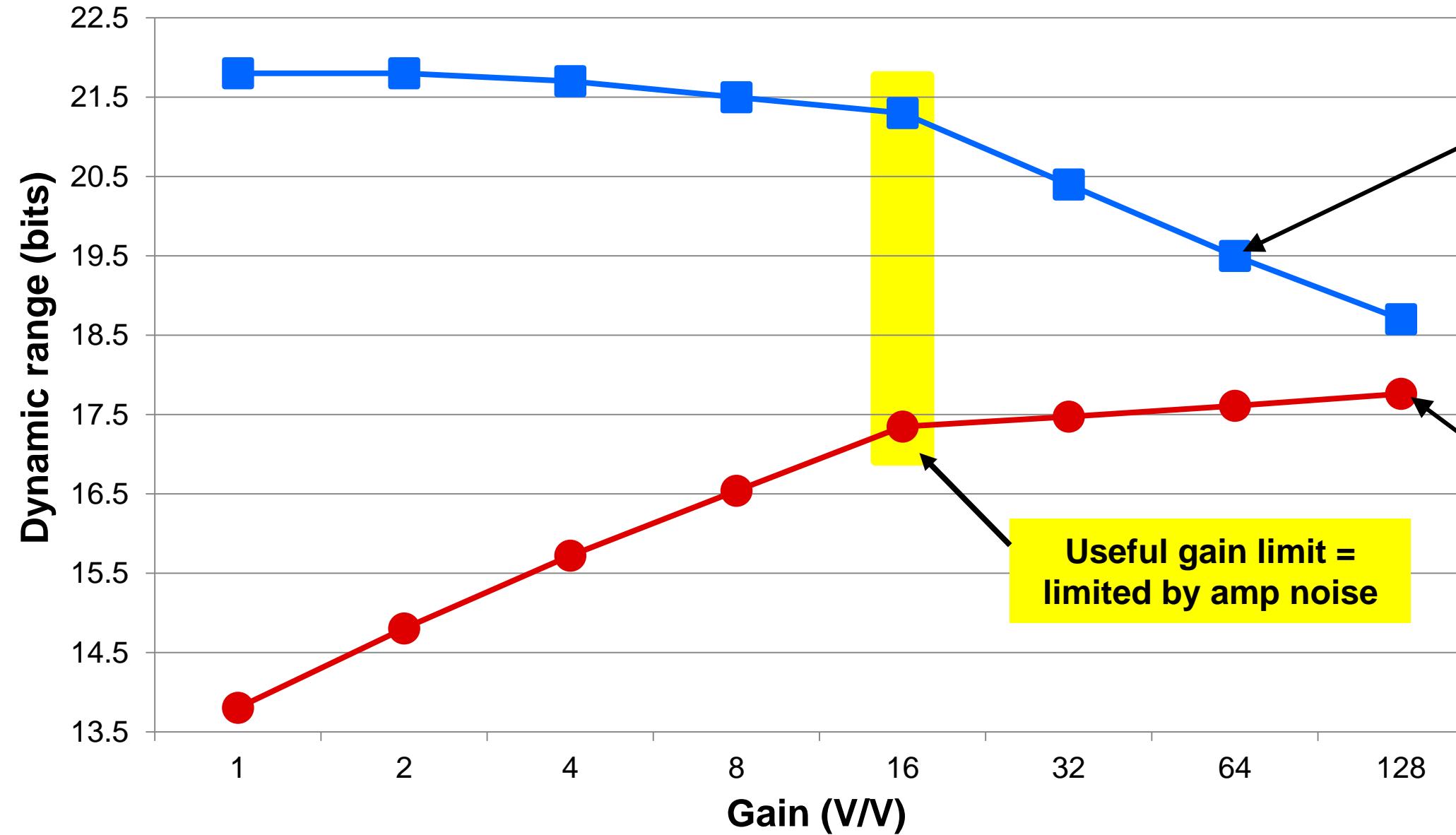
$$\begin{aligned} \text{Maximum DR} \\ = \log_2 \left(\frac{FSR_{RMS}}{V_{N,RMS}} \right) (\text{bits}) \end{aligned}$$

$$V_{IN} = 10 \text{ mV}$$

$$\begin{aligned} \text{System DR} \\ = \log_2 \left(\frac{V_{IN,RMS(RTI)}}{V_{N,RMS}} \right) (\text{bits}) \end{aligned}$$

Dynamic range: max vs system (high resolution ADC)

ADS124S08 (24-bit) dynamic range vs gain (VREF = 2.5V)



$$V_{IN} = FSR = \frac{\pm V_{REF}}{Gain}$$

$$\begin{aligned} \text{Maximum DR} \\ = \log_2 \left(\frac{FSR_{RMS}}{V_{N,RMS}} \right) (\text{bits}) \end{aligned}$$

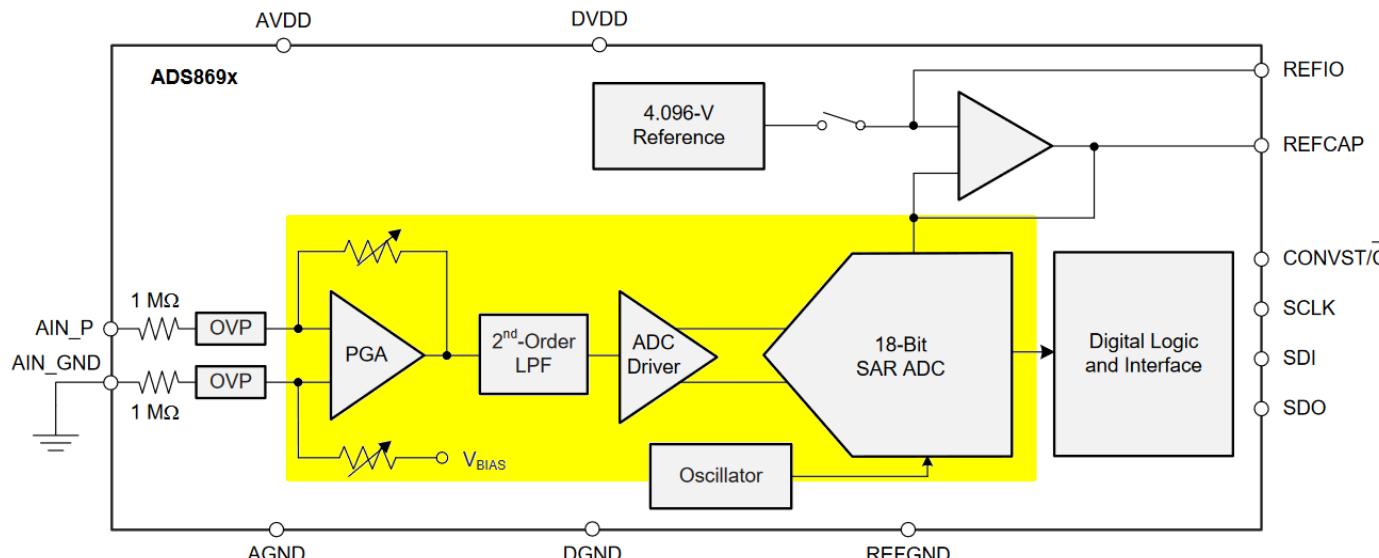
$$V_{IN} = 10 \text{ mV}$$

$$\begin{aligned} \text{System DR} \\ = \log_2 \left(\frac{V_{IN,RMS(RTI)}}{V_{N,RMS}} \right) (\text{bits}) \end{aligned}$$

How gain affects dynamic range (SNR)

$$\text{Dynamic range (SNR)} = 20 * \log_{10} \left(\frac{FSR_{RMS}}{V_{N,RMS}} \right) (\text{dB})$$

ADS86x1 block diagram



ADS86x1 datasheet SNR values (dB)

FSR	Increasing resolution → Increasing SNR			
	ADS8661 (12-bit)	ADS8671 (14-bit)	ADS8681 (16-bit)	ADS8691 (18-bit)
±3 * V _{REF}	73.5	84.5	92	92.5
±2.5 * V _{REF}	73.5	84.5	92	92.5
±1.5 * V _{REF}	73.5	84.25	91.5	91.5
±1.25 * V _{REF}	73.5	84.25	91.5	91.5
±0.625 * V _{REF}	73.5	84	90	90

Increasing gain Constant SNR SNR decreases by 0.5 dB SNR decreases by 2 dB SNR decreases by 2.5 dB

**Thanks for your time!
Please try the quiz.**

Quiz: How gain impacts ADC FSR, noise & DR

1. When is an external amplifier most effective at improving the system noise performance?
 - a) For lower resolution devices
 - b) For higher resolution devices
 - c) Using an amplifier cannot improve noise performance.

Quiz: How gain impacts ADC FSR, noise & DR

1. When is an external amplifier most effective at improving the system noise performance?
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 - b) For higher resolution devices
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Quiz: How gain impacts ADC FSR, noise & DR

2. When will increasing the gain of an amplifier driving an ADC cause system noise RTI to decrease?
 - a) When amplifier noise is the dominant noise source.
 - b) When ADC noise is the dominant noise source.
 - c) Increasing gain will always decrease system noise RTI
 - d) Increasing gain will never decrease system noise RTI

Quiz: How gain impacts ADC FSR, noise & DR

2. When will increasing the gain of an amplifier driving an ADC cause system noise RTI to decrease?
 - a) When amplifier noise is the dominant noise source.
 - b) When ADC noise is the dominant noise source.
 - c) Increasing gain will always decrease system noise RTI
 - d) Increasing gain will never decrease system noise RTI

Quiz: How gain impacts ADC FSR, noise & DR

3. In the table below, the effective resolution is approximately the same for gains of 1V/V to 16V/V. For gains of 32V/V and higher, the effective resolution drops off quickly. Which of the following statements is not true.
- a) For the low gain ranges the ADC noise is dominant, so the ratio of FSR and noise remain the same.
 - b) For higher gain ranges the amplifier noise is dominant, so FSR decreases but noise stays constant.
 - c) For higher gain ranges the ADC noise is dominant causing the effective resolution to decrease.

Parameters (Sinc 3, 60 SPS)	Gain							
	1	2	4	8	16	32	64	128
Full-scale range (V _{REF} = 2.5 V)	±2.5	±1.25	±0.625	±0.313	±0.156	±0.078	±0.039	±0.019
Noise, RTI (μ V _{RMS})	1.4	0.7	0.37	0.21	0.12	0.11	0.1	0.089
Effective resolution (bits)	21.8	21.8	21.7	21.5	21.3	20.4	19.5	18.7

$$\text{Effective resolution} = \log_2 \left(\frac{FSR_{RMS}}{V_{N,RMS}} \right) \text{ (bits)}$$

Quiz: How gain impacts ADC FSR, noise & DR

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Parameters (Sinc 3, 60 SPS)	Gain							
	1	2	4	8	16	32	64	128
Full-scale range (V _{REF} = 2.5 V)	±2.5	±1.25	±0.625	±0.313	±0.156	±0.078	±0.039	±0.019
Noise, RTI (μ V _{RMS})	1.4	0.7	0.37	0.21	0.12	0.11	0.1	0.089
Effective resolution (bits)	21.8	21.8	21.7	21.5	21.3	20.4	19.5	18.7

$$\text{Effective resolution} = \log_2 \left(\frac{FSR_{RMS}}{V_{N,RMS}} \right) \text{ (bits)}$$

How gain impacts ADC FSR, noise, and dynamic range

TIPL 4256

TI Precision Labs – ADCs

Created by Chris Hall & Bryan Lizon

Presented by Alex Smith



Hello, and welcome to the TI Precision Labs module covering how gain impacts ADC full-scale range, noise and dynamic range. This module covers the topics of ADC full-scale range versus input signals, input- and output-referred noise, total noise performance for single- and dual-stage amplifier systems, how gain affects lower resolution and higher resolution ADCs, and finally the impact gain has on dynamic range parameters.

The goal of this presentation is to understand how adding an amplifier to your signal chain affects the overall system performance. A follow-on presentation will apply these principles to several design examples.

Let's begin by discussing ADC full-scale range

ADC full-scale range (FSR)

ADC w/ no integrated gain

ADS8900B FSR (20-bit SAR ADC)

PARAMETER	MIN	TYP	MAX	UNIT
ANALOG INPUT				
FSR	Full-scale input range (AINP – AINM)	-V _{REF}	V _{REF}	V

ADCs w/ integrated gain

ADS8691 FSR (18-bit SAR ADC)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
ANALOG INPUTS				
	Input range = $\pm 3 \times V_{REF}$	-12.288	12.288	V
	Input range = $\pm 2.5 \times V_{REF}$	-10.24	10.24	
	Input range = $\pm 1.5 \times V_{REF}$	-6.144	6.144	
	Input range = $\pm 1.25 \times V_{REF}$	-5.12	5.12	
	Input range = $\pm 0.625 \times V_{REF}$	-2.56	2.56	
	Input range = $3 \times V_{REF}$	0	12.288	
	Input range = $2.5 \times V_{REF}$	0	10.24	
	Input range = $1.5 \times V_{REF}$	0	6.144	
	Input range = $1.25 \times V_{REF}$	0	5.12	

ADS124S08 FSR (24-bit delta-sigma ADC)

	NOM	UNIT
ANALOG INPUTS		
V _{IN}	V _{IN} = V _{AINP} – V _{AINN}	$\pm V_{REF} / Gain$



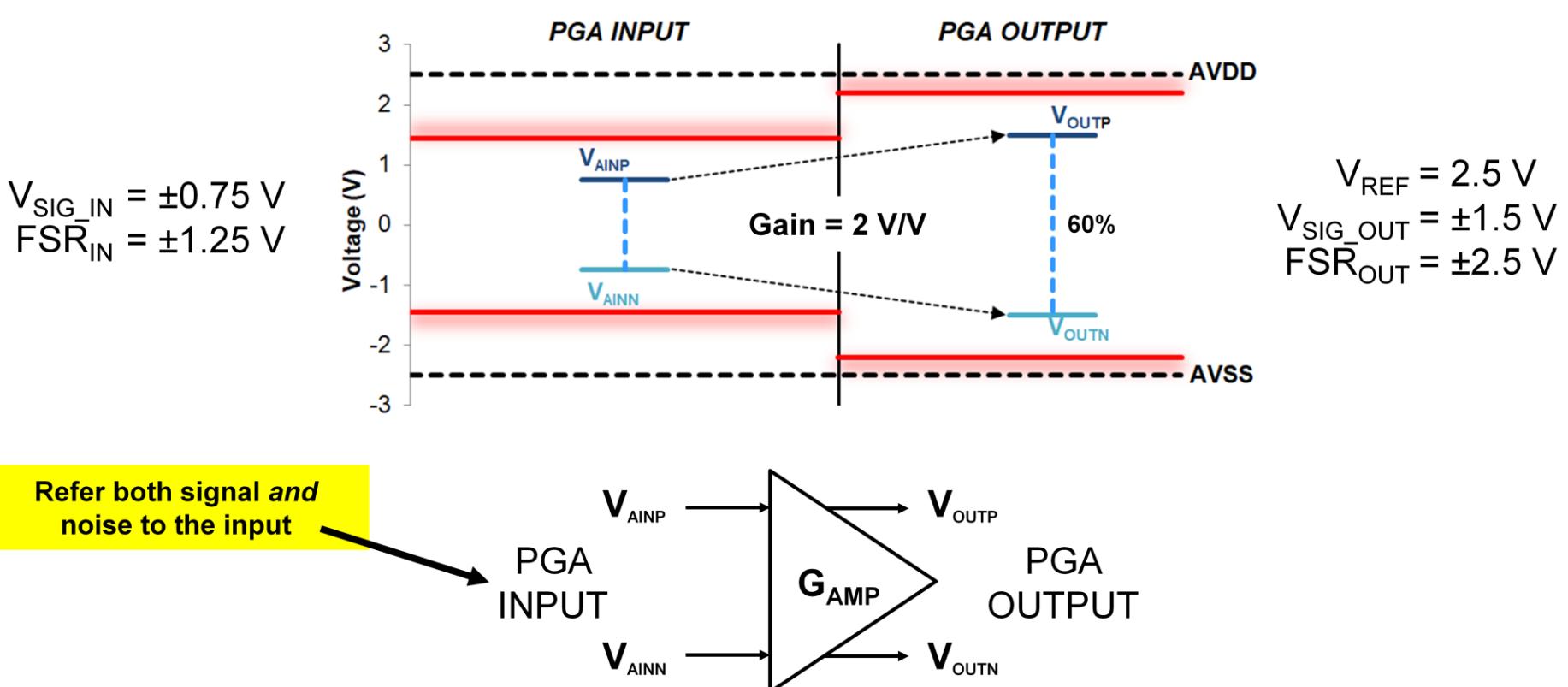
The full-scale range, or FSR, of an ADC represents the maximum input signal the device can accept and is related to the reference voltage, V_{REF}. For example, the table on the left shows the FSR for the ADS8900B, a 20-bit SAR ADC with fully differential inputs and no integrated gain stage. This device has an allowable FSR of plus or minus V_{REF} as shown. While this FSR is typical of many ADCs, other ranges are possible. In some cases, the reference voltage may have a fixed scaling factor such as two times V_{REF} or one-half times V_{REF}. In other cases, the FSR might be single-ended, such as zero volts to V_{REF}. The ultimate takeaway here is that without an integrated amplifier or buffer, the ADC's FSR and input signal are limited only by the ADC's reference voltage.

If you use an ADC with an integrated gain stage, or if you add an amplifier to your system, the FSR equation changes. Shown on the right are the FSR settings for two ADCs with integrated gain. On top is the ADS8691, an 18-bit SAR ADC, while on the bottom is the ADS124S08, a low speed 24-bit delta-sigma ADC. Each ADC's FSR includes a scaling factor that reflects the device gain. For the ADS8691, the scaling factor is numeric and corresponds to the different input ranges shown assuming V_{REF} equals 4.096 volts, while the ADS124S08 just uses the variable "gain" in its FSR equation since this ADC includes eight programmable gain settings. Both devices show that larger gains equate to smaller allowable ADC input ranges. This makes sense intuitively, since amplifiers are often used to gain up small input signals and use more of an ADC's FSR.

Finally, it is important to note that these FSR values are referred to the input, not output, of the ADC. You can use the ADS124S08's online, Excel-based calculator tool to visualize why this distinction is necessary.

ADS124S08 PGA input and output range

$$FSR_{ADS124S08} = \frac{\pm V_{REF}}{Gain}$$



To access this calculator, navigate to the ADS124S08's product folder on TI.com



The plot shown here is taken from the ADS124S08's online calculator tool and highlights the input and output range of the ADC's integrated PGA. Recall that the ADS124S08's FSR is plus or minus VREF divided by gain, as shown in the top right, and that this value is referred to the PGA's input, FSR_{IN} . To find the FSR at the PGA output, FSR_{OUT} , you would multiply this value by the amplifier gain such that FSR_{OUT} just equals plus or minus VREF.

Assuming a 2.5 volt VREF and an example input signal, V_{SIG_IN} , of plus or minus 750 mV, the maximum gain you could use is 2 volts per volt as shown. This results in plus or minus 1.25 volts for FSR_{IN} , represented by the red lines on the left, and plus or minus 2.5 volts for FSR_{OUT} , represented by the red lines

on the right. **The signal at the** PGA's output, V_{SIG_OUT} , is the input voltage multiplied by the gain. As shown, V_{SIG_OUT} equals plus or minus 1.5 volts and corresponds to the blue lines on the right. Given that you are using plus or minus 1.5 volts of the total available plus or minus 2.5 volts, you are using 60% of the ADC's available full-scale range.

There are two important takeaways from this information. First, this combination of settings does not allow you to use 100% of the ADC's FSR, though you can adjust system parameters such as the input signal, circuit gain and the reference voltage if your system required it. For example, you could instead use a 3 V reference that enables a gain of 4 V/V and 100% utilization. However, you can view the Precision Labs module on voltage reference noise to learn why this is not always beneficial. Moreover, you don't want to

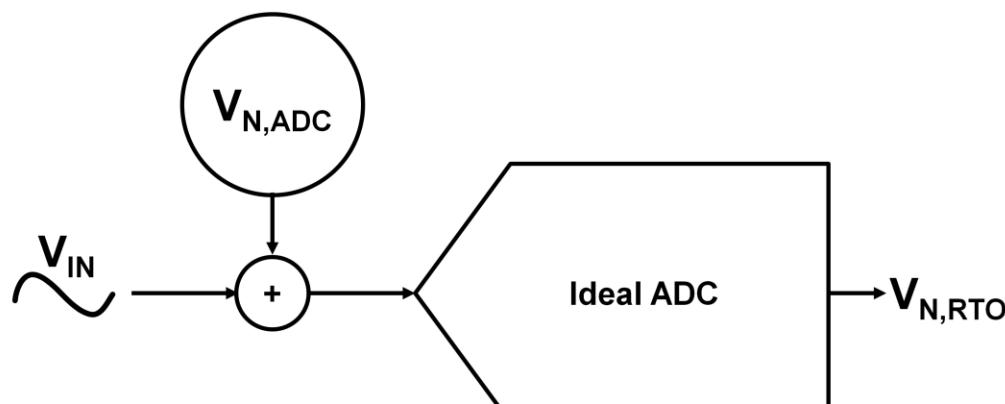
overrange the amplifier, so some margin is always recommended. And, many systems do not require 100% utilization, so adjusting your settings or applying more gain might actually cause more problems than it solves.

Second, ensure that when you calculate system performance specifications you are using noise and input signal levels from the same measurement point in the circuit. As you can see, this module emphasizes that FSR is defined at the amplifier's input, not output. Many engineers mistakenly use datasheet noise parameters that are input-referred while choosing a signal that is scaled by the gain. This is incorrect and yields invalid results. Instead, refer both your noise and signal levels to the input.

Let's now discuss the difference between input and output-referred noise, and how you determine each

Output- versus input-referred noise

Equivalent ADC Noise Model:



$V_{N,RTO}$ is the system's input resolution:

- If $V_{IN} < V_{N,RTO}$, the signal is below the noise floor
- Else if $V_{IN} > V_{N,RTO}$, the signal can be observed

For ADC w/ no gain, $V_{N,RTO} = V_{N,RTI} = V_{N,ADC}$



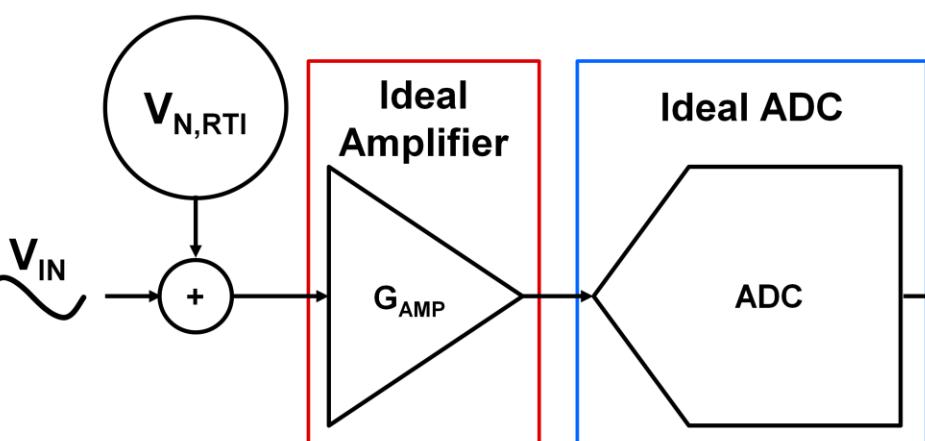
If you watched the Precision Labs module on ADC noise measurements, you'd recall that noise is measured at the output of converter by observing the code variations for a constant input. As its name implies, this is called output-referred noise, and is labelled as $V_{N,RTO}$ in the image shown here. However, this is generally not the noise value reported in datasheets, nor is it the type of noise used in the dynamic range equations shown previously. That noise is input-referred, and is labelled here as $V_{N,RTI}$. For an ADC with no gain stage, the output-referred noise is equal to the input-referred noise which is equal to the ADC's noise, labeled as $V_{N,ADC}$. So why do you want to talk about noise referred to the input instead of the output?

The equivalent ADC noise model shown here helps illustrate why this is important. Here we have separated our noisy ADC into a "noiseless" or ideal ADC preceded by a noise voltage source. The magnitude of this voltage source is equal to the ADC's input-referred noise. Now, you can quickly compare an applied input signal relative to the system noise: if the input signal amplitude is greater than the input-referred noise, you will be able to observe it. Otherwise, your signal will be buried in the noise and you won't.

Now, let's analyze how this model changes when you add an amplifier to your signal chain

Input-referred noise for amp + ADC

Equivalent Amp + ADC Noise Model:



For ADC w/ gain, $V_{N,RTO} \neq V_{N,RTI}$

$$V_{N,RTO} = \sqrt{(V_{N,AMP(RTI)} * G_{AMP})^2 + (V_{N,ADC})^2}$$

$$V_{N,RTI} = \sqrt{(V_{N,AMP(RTI)})^2 + (V_{N,ADC}/G_{AMP})^2}$$

$G_{AMP} * V_{N,AMP(RTI)} \gg V_{N,ADC}$

 TEXAS INSTRUMENTS

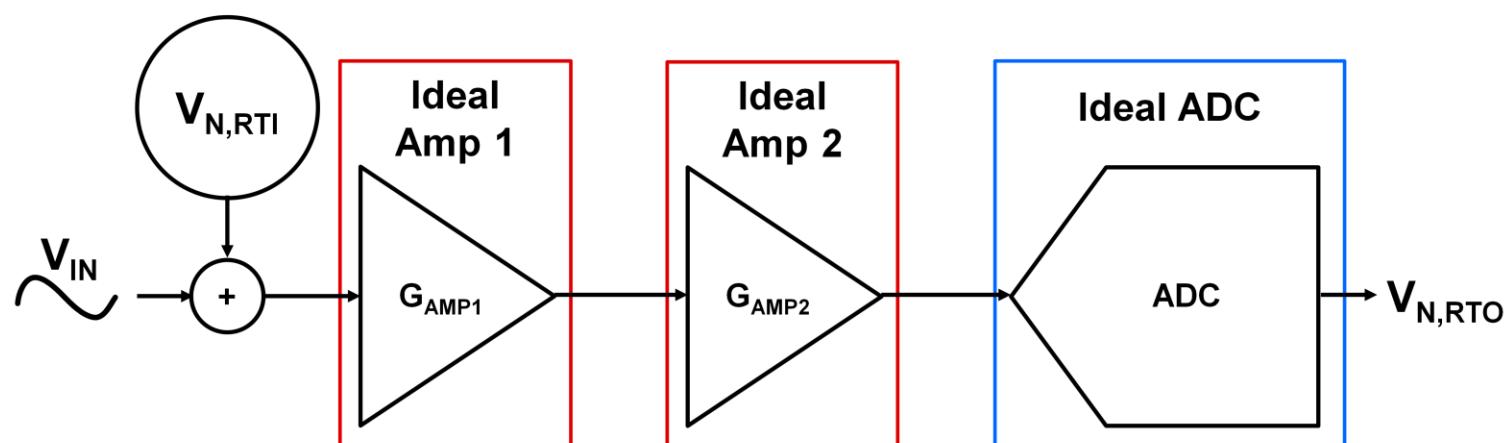
Here is the same ADC model shown on the previous slide, though we have added an amplifier at the ADC's input. Note that while this amplifier is shown as a discrete component, this same analysis can be applied to an ADC with an integrated amplifier, such as the ADS124S08 or ADS8691 used at the beginning of this module. We have modelled the amplifier similarly to the ADC as an ideal amplifier with no noise. Like the previous slide, both the amplifier and ADC noise are referred to the input to create one combined noise source called $V_{N,RTI}$. Combining noise sources helps simplify your analysis by easily allowing you to determine if your ADC-plus-amplifier signal chain has enough resolution for your application.

The equation on the top right shows how to calculate the output-referred noise of this simple signal chain. Note that the amplifier noise is scaled by its gain, G_{AMP} . To refer the output noise to the input, you need to divide each individual noise term by the circuit gain. The equation for the input-referred noise is shown on the bottom right. As you can see, the amplifier gain divides out from the amplifier noise term while the ADC noise is now divided by the amplifier's gain. This is a powerful and useful result. If the amplifier has a high gain, the ADC noise becomes negligible and the total input-referred noise is only dependent on the amplifier's noise, which is constant at a specific bandwidth. This is true whether or not the amplifier is integrated into the ADC or is a discrete component.

Now let's analyze what happens if you add an additional amplifier to your signal chain

Input-referred noise for 2x amps + ADC

Equivalent 2x Amplifier + ADC Noise Model:



$$V_{N,RTI} = \sqrt{V_{N,AMP1(RTI)}^2 + \left(\frac{V_{N,AMP2(RTI)}}{G_{AMP1}}\right)^2 + \left(\frac{V_{N,ADC}}{G_{AMP1} * G_{AMP2}}\right)^2}$$

If $G_{AMP1} * G_{AMP2} * V_{N,AMP1(RTI)} \gg (G_{AMP2} * V_{N,AMP2(RTI)}) + V_{N,ADC}$, then $V_{N,RTI} = V_{N,AMP1(RTI)}$

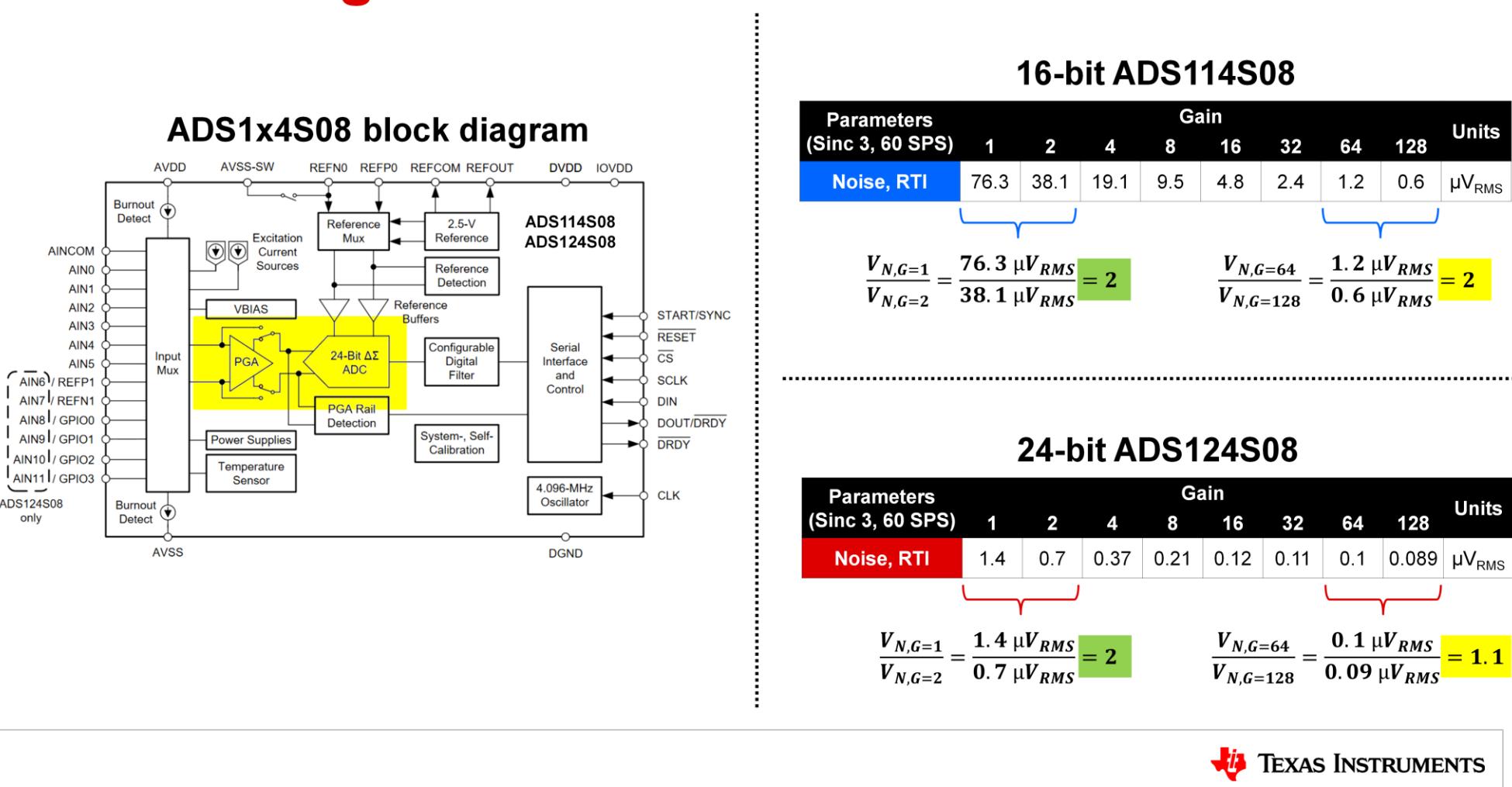


For example, what if you had a buffer plus a gain amplifier, or a single-ended-to-differential conversion stage requiring two op amps?

If you add another amplifier to the signal chain, you combine all of the noise sources into one as before. And like the single-stage amplifier example shown on the previous slide, you need to divide by the amplifier's gain. However, each amplifier can have a different gain factor, so each term in the input-referred noise equation is divided by the *product* of both amplifier gains. This leaves only the first-stage amplifier's noise with no dependence on gain as shown. Therefore, the second amplifier and the ADC noise terms effectively approach zero, given the condition that at least the first amplifier has a large gain. This leaves the system's input-referred noise dependent on only the first amplifier's noise, just like in the previous example. Therefore, choose a first-stage amplifier with low noise and a large gain whenever possible for both single- and multistage amplifier configurations.

While this is practical information for higher-resolution ADCs where the ADC noise is already small, do the same principles apply to lower-resolution ADCs?

Lower vs higher-resolution ADC total noise



To analyze the difference in total noise between lower- and higher-resolution ADCs, let's look at the 16-bit ADS114S08 and the 24-bit ADS124S08, two low-speed delta sigma ADCs. From the block diagram on the left, you can see that these ADCs are identical other than their resolutions, and they integrate the same PGA with the same noise. This makes it very easy to see the effect ADC resolution has on the overall system noise as gain is applied.

On the right are the input-referred noise tables for each device, with the 16-bit ADC on the top and the 24-bit ADC on the bottom. The noise shown here is measured at a data rate of 60 samples per second using the sinc 3 filter, though the same analysis applies to other combinations of settings as well.

If you take the ratio of the input-referred noise at a gain of 1 and a gain of 2, you get approximately 2 for each ADC as highlighted in green. Conversely, if we take this same ratio for gains of 64 and 128, the 16-bit ADC still has a noise ratio of 2, while the 24-bit ADC now has a noise ratio of approximately 1. These results are highlighted in yellow.

On the next slide we will discuss why this happens

Applying the input-referred noise equation

$$V_{N,RTI} = \sqrt{(V_{N,AMP(RTI)})^2 + (V_{N,ADC}/G_{AMP})^2} \text{ (nV}_{RMS}\text{)}$$

Lower-resolution ADCs –
quantization noise dominates



$$G_{AMP} * V_{N,AMP(RTI)} < V_{N,ADC}$$



- Use a higher-noise (lower \$) amp
- Larger gain if system allows

Higher-resolution ADCs –
thermal noise dominates



$$G_{AMP} * V_{N,AMP(RTI)} \gg V_{N,ADC}$$



- Higher gain does not reduce noise
- Use a very low noise amp



First, recall the simplified input-referred noise equation for an amplifier plus ADC system, restated here at the top of this slide. Second, recall that the amplifier noise only dominates when it's much greater than the ADC noise or the gain is extremely large. Given these conditions, you can see that for the 16-bit, lower resolution ADC, high levels of quantization noise overpower the amp noise, so you never really “see” the amp noise in the measurement. Each time you reduce the full-scale range by 2, the quantization noise reduces by a factor of 2 as well. But the ADC noise remains above the level of the amplifier noise, such that the condition on the left is true. Therefore, you could use a higher noise amplifier or a larger gain to help reduce noise further compared to the ADC by itself.

Comparatively, the opposite is true for higher-resolution ADCs, where the amp noise begins to dominate at high gains and the system noise RTI becomes constant. In these cases, using higher gains results in no system noise benefit, and you must use very low-noise amplifiers to realize the benefits of your higher-resolution ADC's low noise floor. You can approximate the point at which the noise of a high-gain amplifier starts to dominate your signal chain at the 16-bit level, though this is not always true. To be certain, you should always perform the necessary noise calculations based on the information provided in this module to estimate how an amplifier's noise will affect your ADC.

Now that we have discussed both full-scale range and noise, we can apply this information to understand how gain affects dynamic range performance for lower- and higher-resolution ADCs

How gain affects dynamic range (effective resolution)

$$\text{Dynamic range (effective resolution)} = \log_2 \left(\frac{FSR_{RMS}}{V_{N,RMS}} \right) \text{ (bits)}$$

16-bit ADS114S08

Parameters (Sinc 3, 60 SPS)	Gain								
	1	2	4	8	16	32	64	128	
Full-scale range (VREF = 2.5 V)	±2.5	±1.25	±0.625	±0.313	±0.156	±0.078	±0.039	±0.019	
Noise, RTI (μV_{RMS})	76.3	38.1	19.1	9.5	4.8	2.4	1.2	0.6	
Effective resolution (bits)	16	16	16	16	16	16	16	16	

Increasing gain



Constant effective resolution



24-bit ADS124S08

Parameters (Sinc 3, 60 SPS)	Gain								
	1	2	4	8	16	32	64	128	
Full-scale range (VREF = 2.5 V)	±2.5	±1.25	±0.625	±0.313	±0.156	±0.078	±0.039	±0.019	
Noise, RTI (μV_{RMS})	1.4	0.7	0.37	0.21	0.12	0.11	0.1	0.089	
Effective resolution (bits)	21.8	21.8	21.7	21.5	21.3	20.4	19.5	18.7	

Increasing gain



Decreasing effective resolution

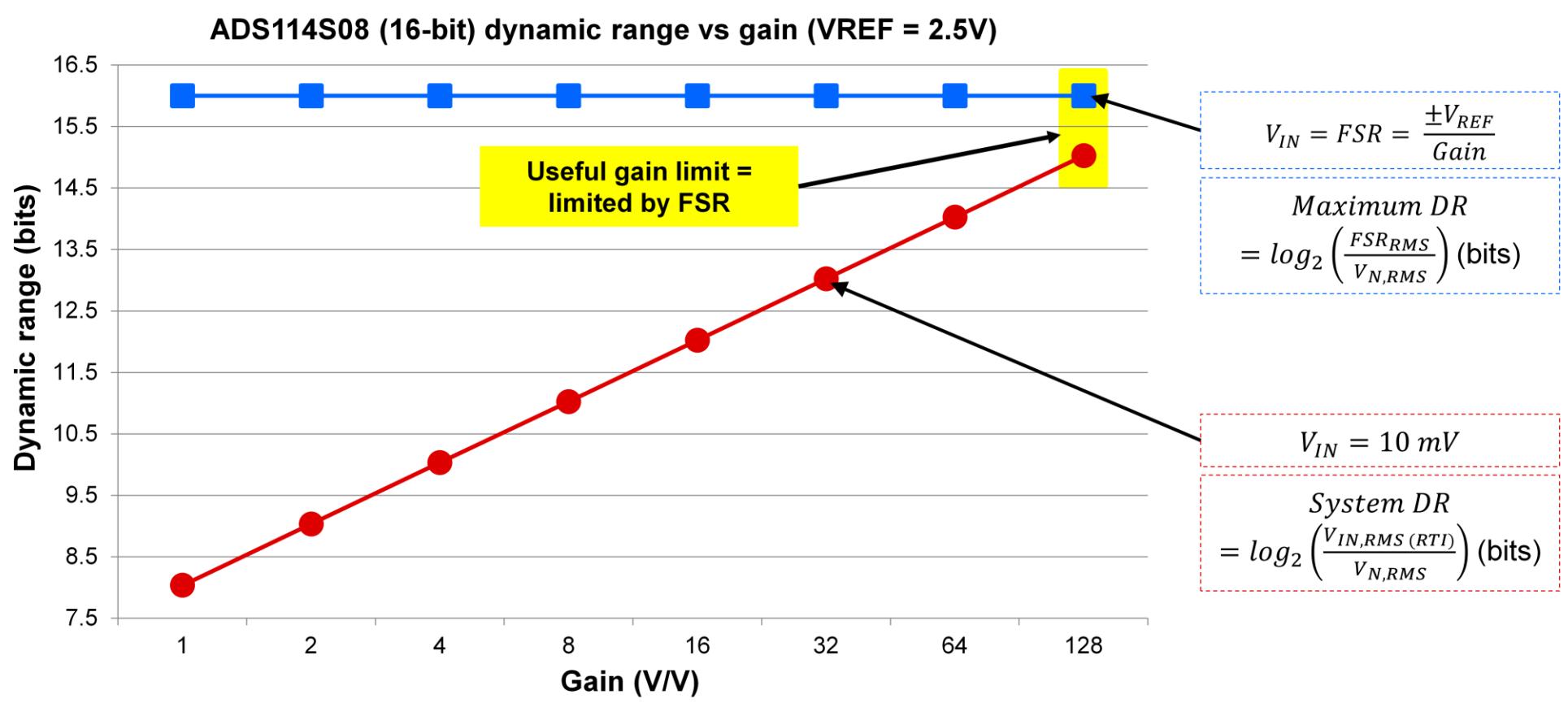



Recall from the Precision Labs module on noise measurement methods and parameters that dynamic range is a category of measurement types. One such dynamic range measurement is effective resolution, which is defined by the equation at the top of this slide. This parameter is a ratio of the ADC's full-scale range to the RMS noise, the two topics we previously discussed throughout this presentation.

The tables in the center of this slide include the full-scale range, input-referred noise, and dynamic range for the two ADCs introduced during the discussion on lower vs higher resolution ADCs. You can see that as the gain increases for the 16-bit ADC on the left, the dynamic range remains constant at 16 bits. However, for the 24-bit ADC on the right, the effective resolution is a maximum of 21.8 bits at a gain of one, and tends to decrease as gain increases. As a reminder, these devices both include the same low-noise PGA, though the results would be the same if these amplifiers were instead external, discrete components.

Given the results on this slide, should you conclude that gain should be avoided for higher-resolution ADCs but not for lower-resolution ADCs? Fortunately this is not the case, and the next two slides will explain why.

Dynamic range: max vs system (low resolution ADC)



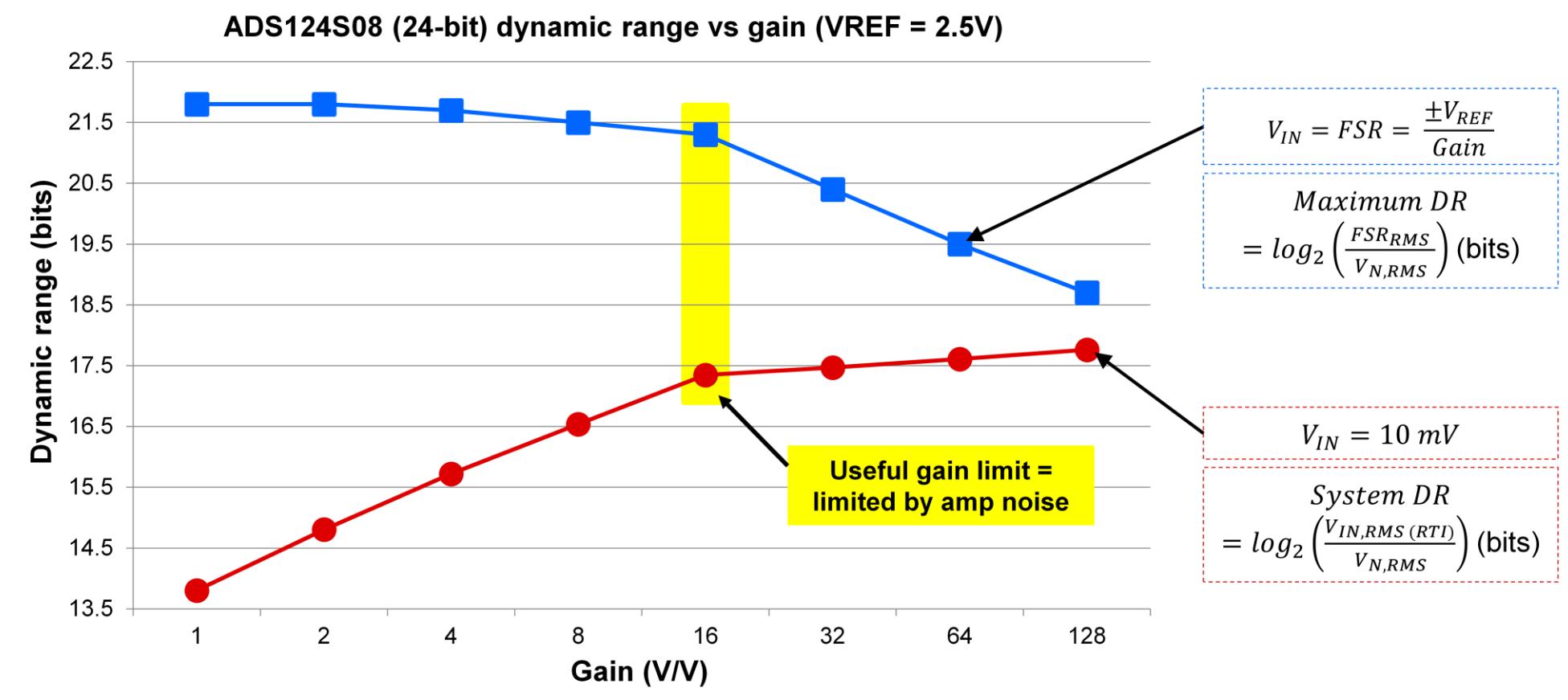
It is important to remember that datasheet dynamic range values tend to demonstrate the best possible ADC performance at the given conditions using the maximum input signal. If you applied a signal smaller than the maximum, for example zero to ten millivolts, applying gain is essential to get the best noise performance and improve your dynamic range.

The blue line shown here plots the dynamic range values for the 16-bit ADS114S08 shown in the previous slide. This line represents the maximum achievable dynamic range at the given conditions using the maximum input signal of plus or minus VREF divided by gain, where VREF is 2.5 volts. As the table revealed, this is just a constant value of 16 bits since the noise is not limited by the PGA in this case.

The red line represents the system dynamic range performance versus gain when applying a 10 millivolt signal to the ADC. The dynamic range equation used to plot this line is shown in the bottom right. Note that the system dynamic range trends toward the maximum dynamic range as the gain increases, illustrating how applying gain to your system can reduce noise and improve dynamic range. In this case, a *useful gain limit* is set by the ADC's full-scale range such that using a gain greater than 128 would amplify your input signal beyond the ADC's allowable FSR. We explore why it can be beneficial, or even necessary, to use a larger gain with a lower-resolution ADC in a subsequent Precision Labs video.

Let's now review the same plots for a higher-resolution ADC.

Dynamic range: max vs system (high resolution ADC)



As in the previous slide, the blue line shown here plots the datasheet dynamic range values for the 24-bit ADS124S08. This line represents the maximum achievable dynamic range at the given conditions using the maximum input signal of plus or minus VREF divided by gain, where VREF is 2.5 volts. Unlike the blue plot on the previous slide however, the dynamic range here tends to decrease as gain increases, with a notable acceleration around a gain of 16.

The red line represents the system dynamic range performance versus gain when applying a 10 millivolt signal to the ADC. The dynamic range equation used to plot this line is shown in the bottom right. Similar to the plot on the last slide, the system dynamic range trends toward the maximum dynamic range as the gain increases, reiterating that applying gain to your system can reduce noise and improve dynamic range for both lower- and higher-resolution systems. However, note that the system dynamic range performance begins to flatten at a gain of 16, similar to the inflection point on the blue plot. This is the ADS124S08's useful gain limit. Unlike the lower-resolution ADC, this limit is reached when the amplifier noise begins to dominate, resulting in constant system noise. You could increase the gain beyond this point until you reached the FSR limit, but this provides no meaningful noise reduction or dynamic range improvement. This is important to understand when choosing an amplifier for your ADC, or deciding if more gain is required for an ADC that already has an integrated amplifier. We explore this topic in more detail with design examples in the next Precision Labs video.

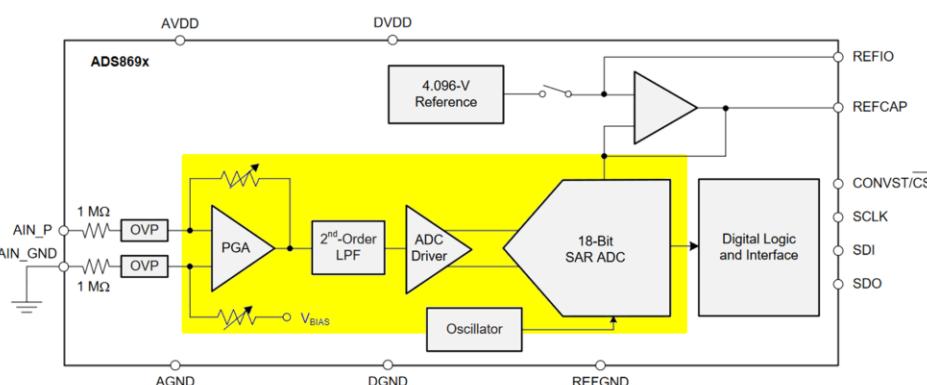
Finally, while our discussion so far has focused on low-speed delta sigma

ADCs, these same principles apply to wideband delta-sigma and SAR ADCs as well.

How gain affects dynamic range (SNR)

$$\text{Dynamic range (SNR)} = 20 * \log_{10} \left(\frac{FSR_{RMS}}{V_{N,RMS}} \right) (\text{dB})$$

ADS86x1 block diagram



ADS86x1 datasheet SNR values (dB)

FSR	Increasing resolution			
	ADS8661 (12-bit)	ADS8671 (14-bit)	ADS8681 (16-bit)	ADS8691 (18-bit)
$\pm 3 * V_{REF}$	73.5	84.5	92	92.5
$\pm 2.5 * V_{REF}$	73.5	84.5	92	92.5
$\pm 1.5 * V_{REF}$	73.5	84.25	91.5	91.5
$\pm 1.25 * V_{REF}$	73.5	84.25	91.5	91.5
$\pm 0.625 * V_{REF}$	73.5	84	90	90

Increasing gain
 Constant SNR
 SNR decreases by 0.5 dB
 SNR decreases by 2 dB
 SNR decreases by 2.5 dB



Shown here are the system block diagram and datasheet SNR tables for the ADS86x1 family of SAR ADCs. Like the low-speed delta sigma ADCs we just looked at, you can see from the block diagram on the left that the ADS86x1 family of devices includes a PGA that will help illustrate how dynamic range performance changes as gain increases.

Unlike the delta-sigma ADCs we looked at however, the ADS86x1 family of ADCs specifies dynamic range using signal to noise ratio, or SNR. This parameter is defined by the equation at the top of this slide, and is a ratio of the ADC's full-scale range to the RMS noise.

On the right is a table of SNR values pulled directly from the ADC datasheets. From left to right, the ADCs are ordered by increasing resolution, while top to bottom they are sorted by decreasing FSR, which is the equivalent of increasing gain. Note that the 12-bit and 14-bit ADCs have relatively constant SNR as gain increases, while the higher-resolution devices in this family see a much larger SNR reduction from low gain to high gain. You can also see that the general rule of a 16-bit cutoff between lower and higher resolution ADCs is not necessarily true for this family, as the PGA noise begins to dominate even at the 16-bit level. This is why it is always important to perform the necessary calculations to determine the impact your amplifier has on your overall system noise.

You can review the next video in the Precision Labs series for several practical

design examples that explore the information presented in this module in more detail.

**Thanks for your time!
Please try the quiz.**



That concludes this video. Thank you for watching. Please try the quiz to check your understanding of this video's content.

Quiz: How gain impacts ADC FSR, noise & DR

1. When is an external amplifier most effective at improving the system noise performance?
 - a) For lower resolution devices
 - b) For higher resolution devices
 - c) Using an amplifier cannot improve noise performance.

Quiz: How gain impacts ADC FSR, noise & DR

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Quiz: How gain impacts ADC FSR, noise & DR

2. When will increasing the gain of an amplifier driving an ADC cause system noise RTI to decrease?
- a) When amplifier noise is the dominant noise source.
 - b) When ADC noise is the dominant noise source.
 - c) Increasing gain will always decrease system noise RTI
 - d) Increasing gain will never decrease system noise RTI

Quiz: How gain impacts ADC FSR, noise & DR

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 - c) Increasing gain will always decrease system noise RTI
 - d) Increasing gain will never decrease system noise RTI

Quiz: How gain impacts ADC FSR, noise & DR

3. In the table below, the effective resolution is approximately the same for gains of 1V/V to 16V/V. For gains of 32V/V and higher, the effective resolution drops off quickly. Which of the following statements is not true.
- a) For the low gain ranges the ADC noise is dominant, so the ratio of FSR and noise remain the same.
 - b) For higher gain ranges the amplifier noise is dominant, so FSR decreases but noise stays constant.
 - c) For higher gain ranges the ADC noise is dominant causing the effective resolution to decrease.

Parameters (Sinc 3, 60 SPS)	Gain							
	1	2	4	8	16	32	64	128
Full-scale range (VREF = 2.5 V)	±2.5	±1.25	±0.625	±0.313	±0.156	±0.078	±0.039	±0.019
Noise, RTI (μV_{RMS})	1.4	0.7	0.37	0.21	0.12	0.11	0.1	0.089
Effective resolution (bits)	21.8	21.8	21.7	21.5	21.3	20.4	19.5	18.7

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