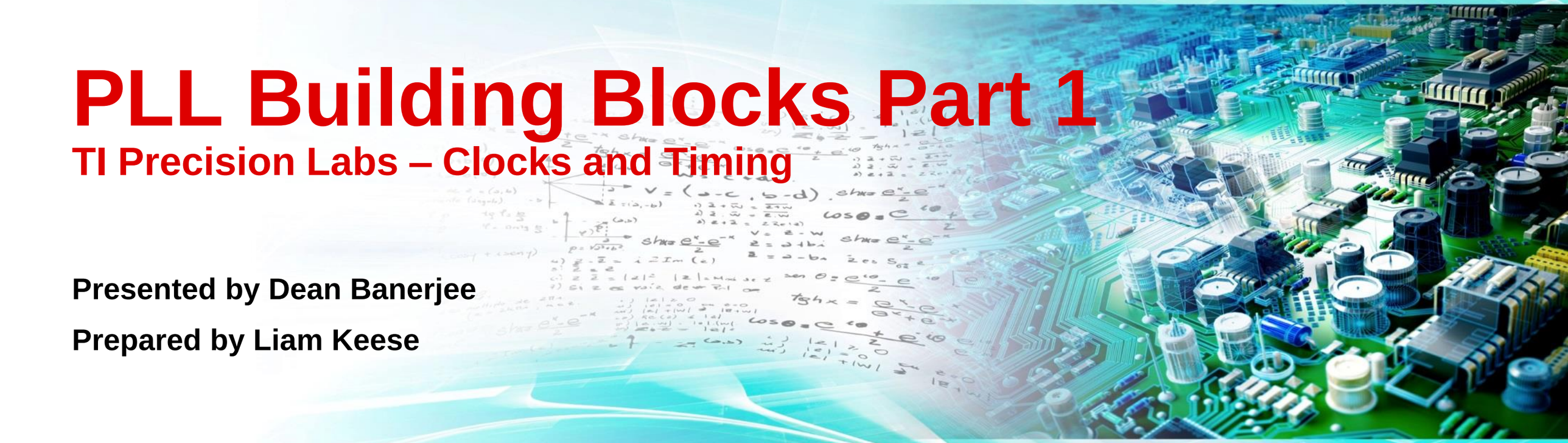
PLL Building Blocks Part 1

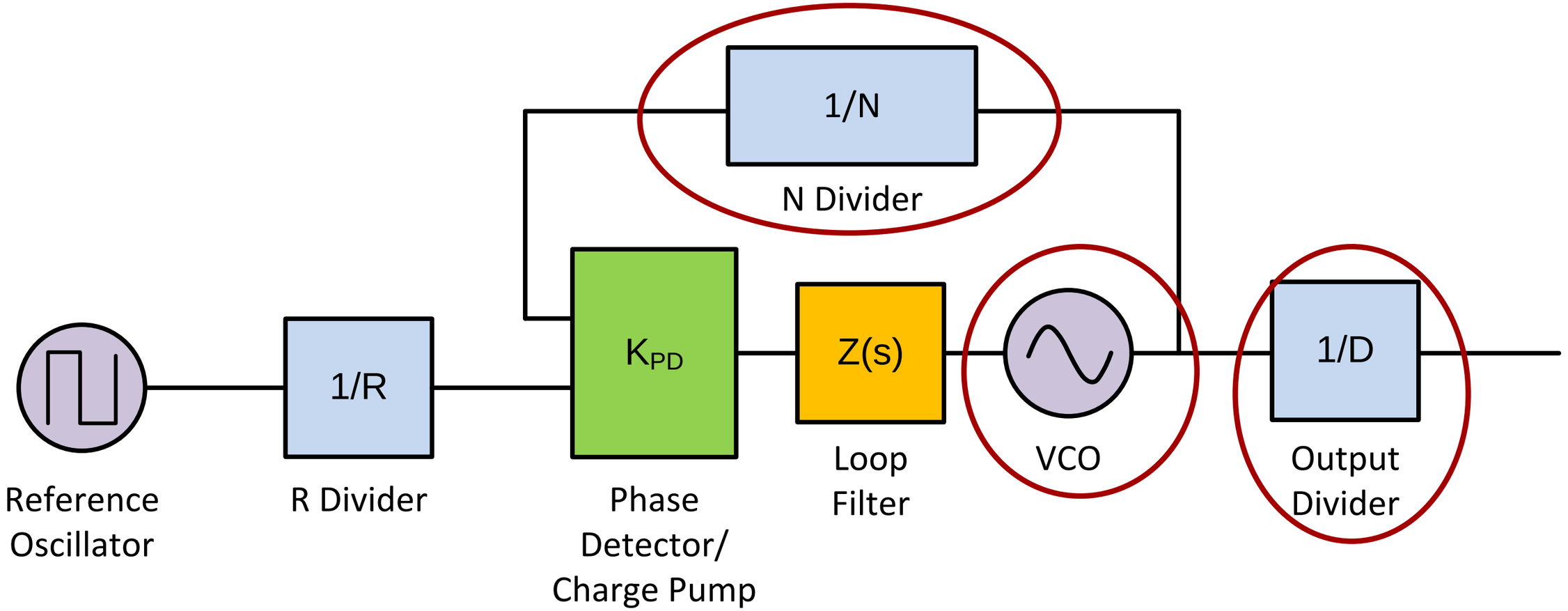
TI Precision Labs – Clocks and Timing



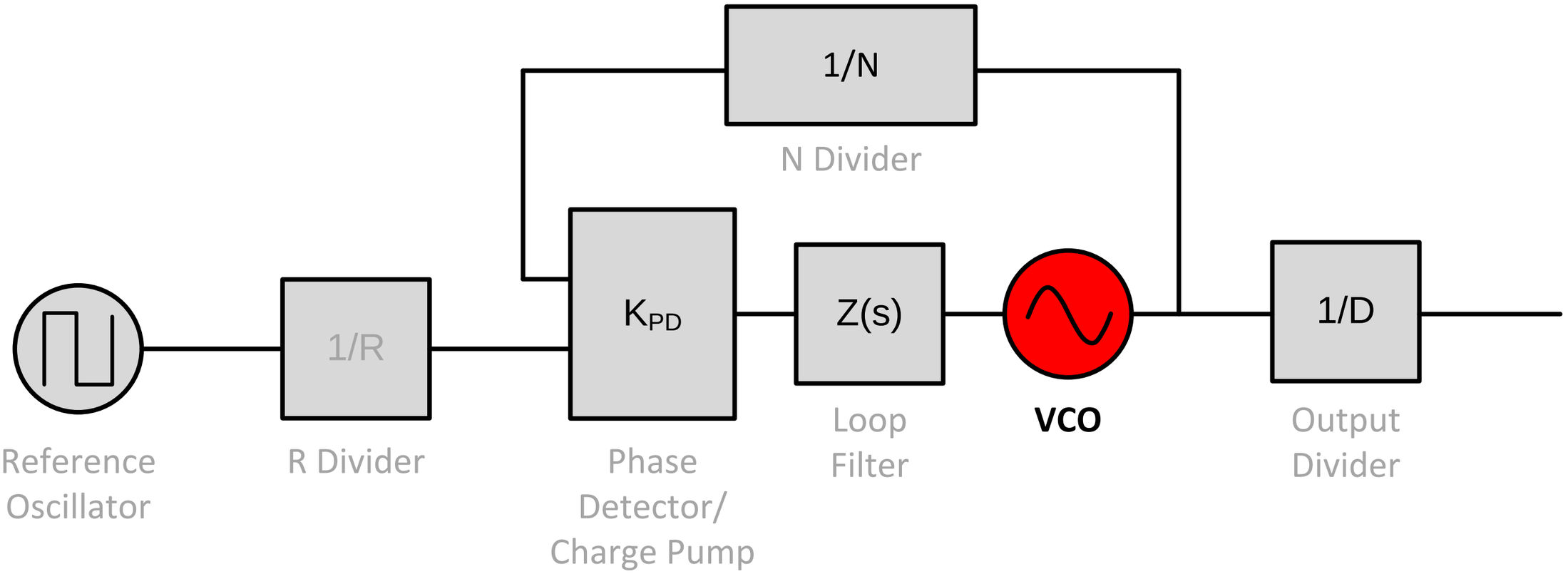
Presented by Dean Banerjee

Prepared by Liam Keese

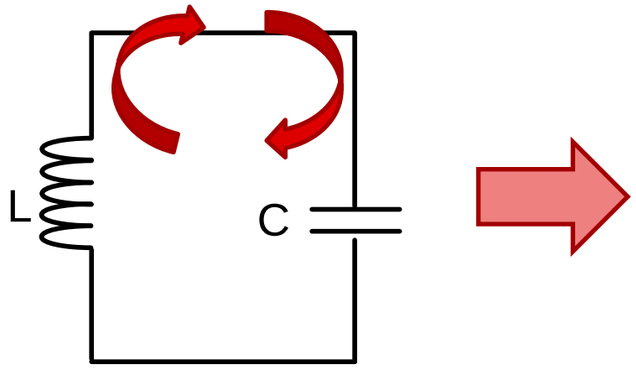
Phase lock loop (PLL) block diagram

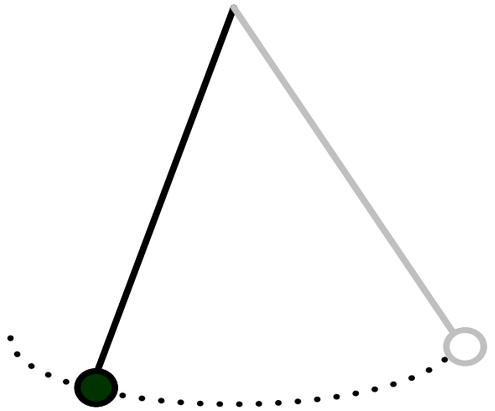


Voltage controlled oscillator (VCO)



VCO resonator





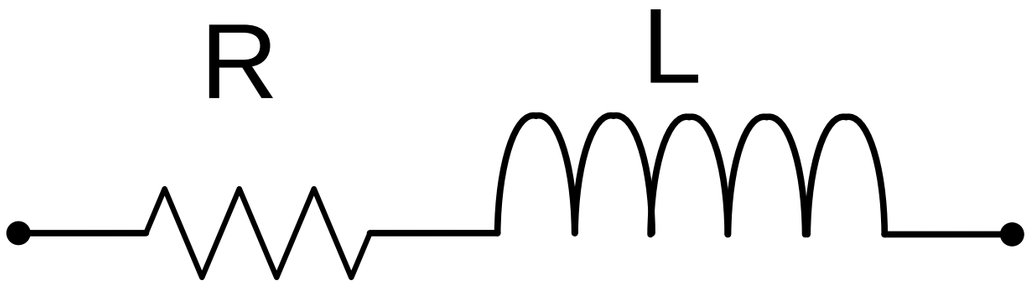
$$f = \frac{1}{2\pi\sqrt{L \cdot C}}$$

f = resonant frequency
L = inductance
C = capacitance

$$\tau = 2\pi\sqrt{\frac{L}{g}}$$

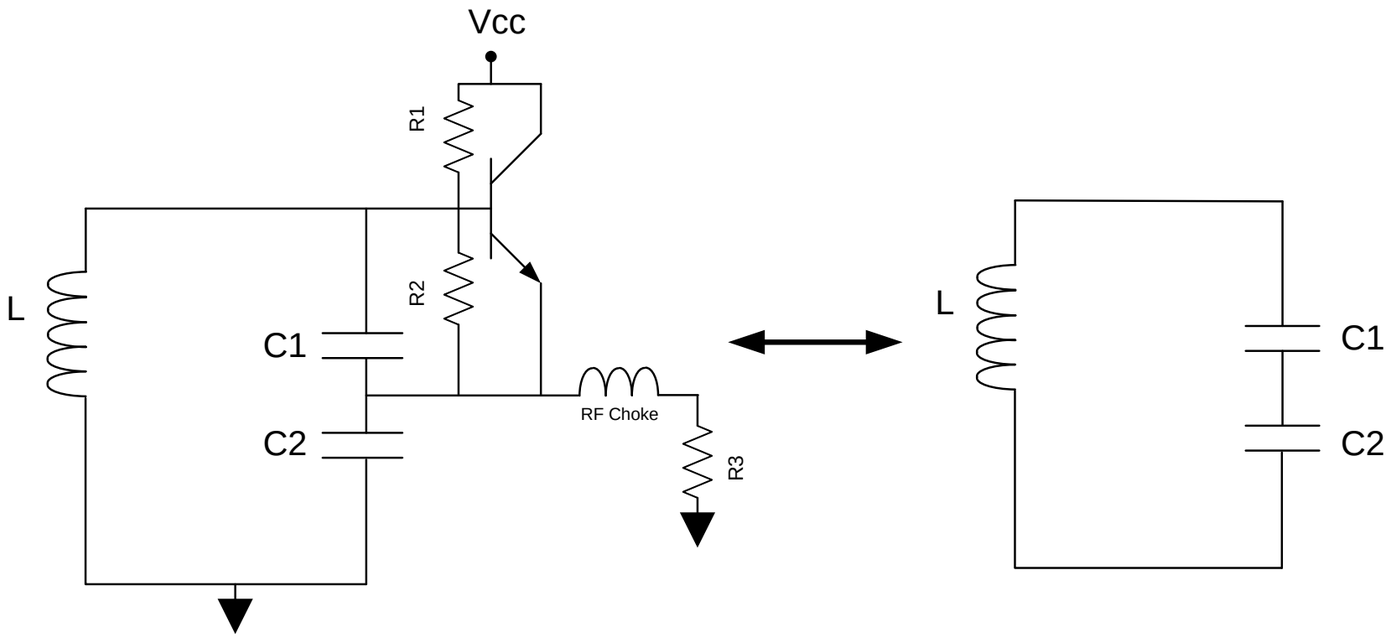
Tau = period
L = length of the pendulum
g = acceleration due to gravity

The real-world inductor



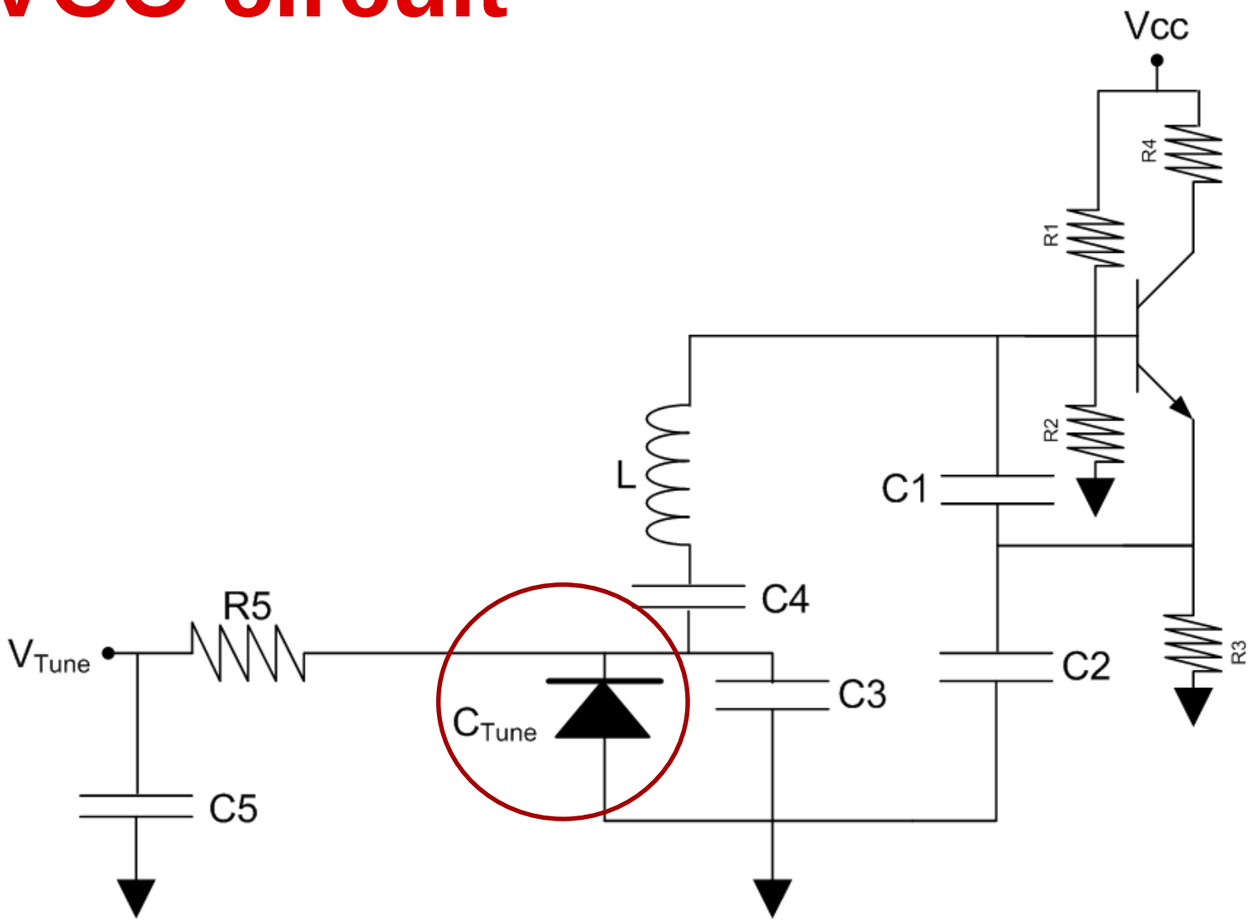
$$Q_L(f) = \frac{X_L}{R_L} = \frac{2\pi \cdot f \cdot L}{R}$$

Now add the stimulus



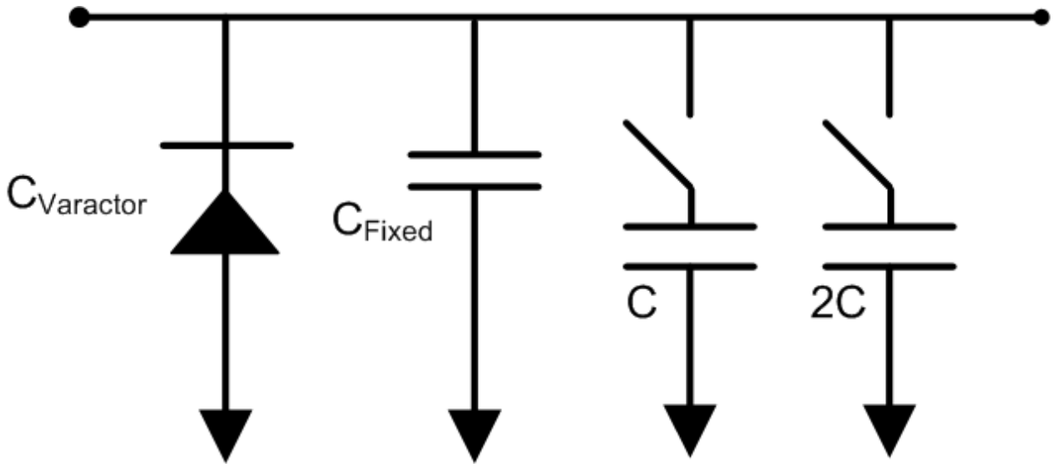
Amplified signal from emitter is lightly coupled into the circuit to sustain oscillation

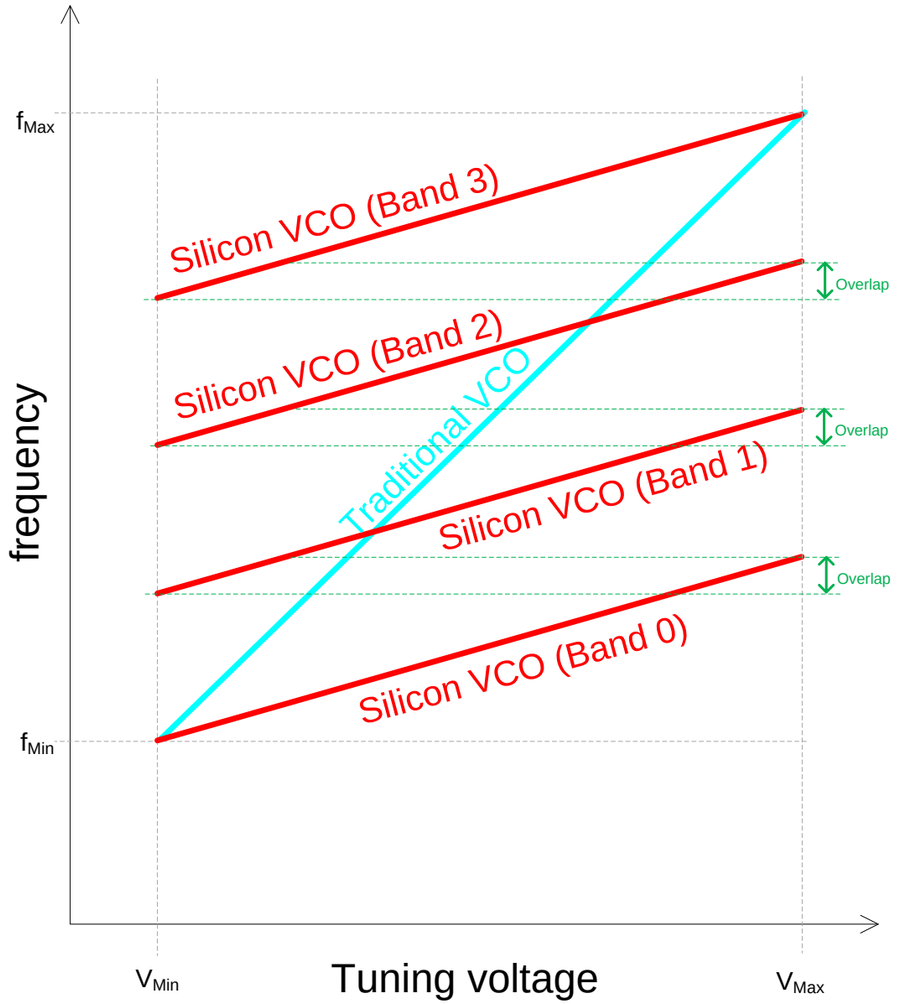
Example VCO circuit



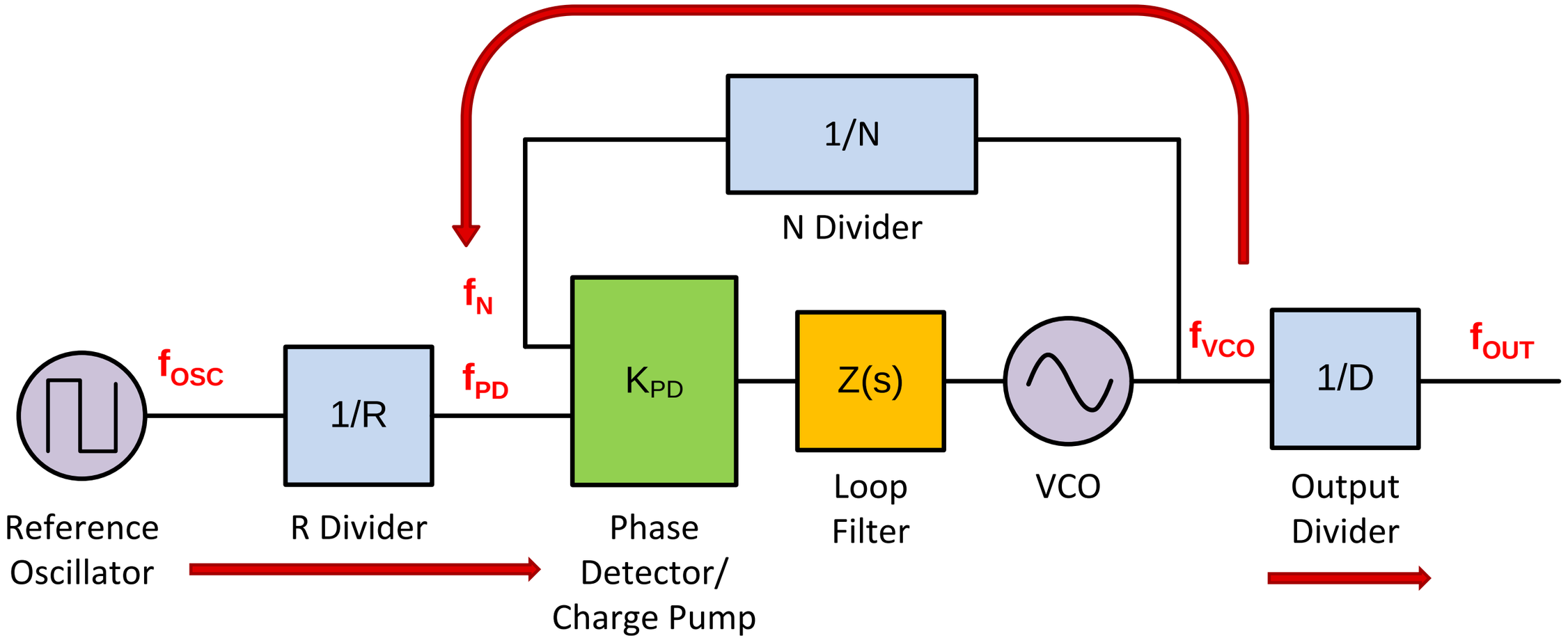
VCO tuning range

Switched Capacitor Bank



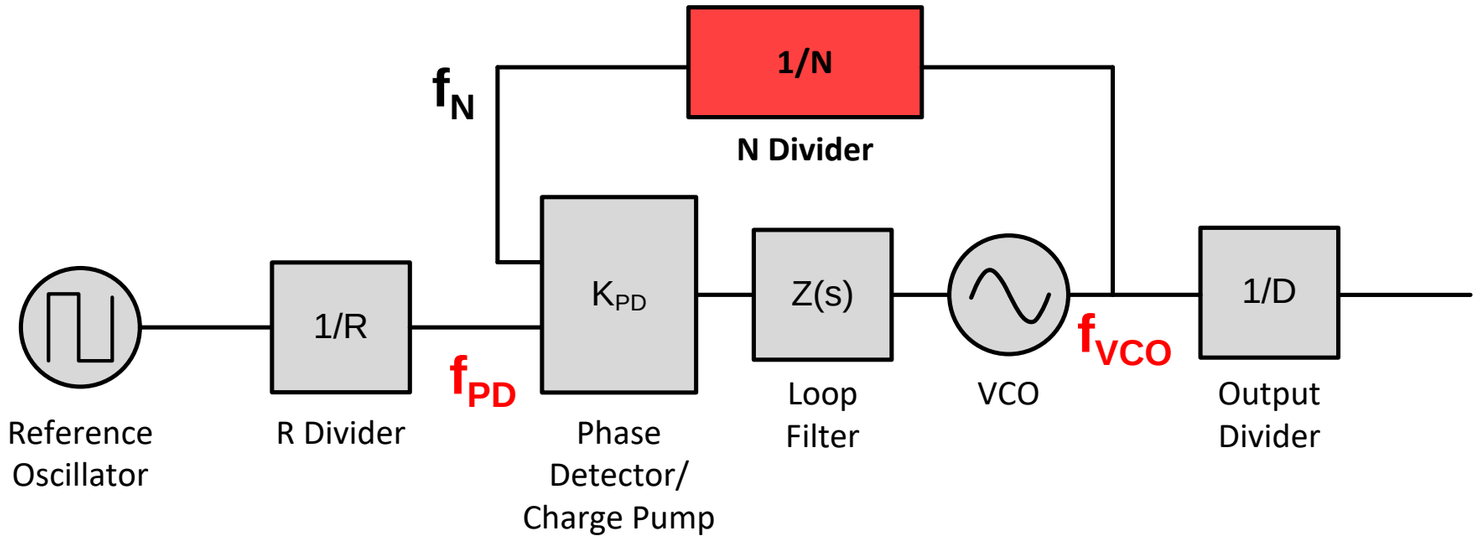


Phase lock loop overview



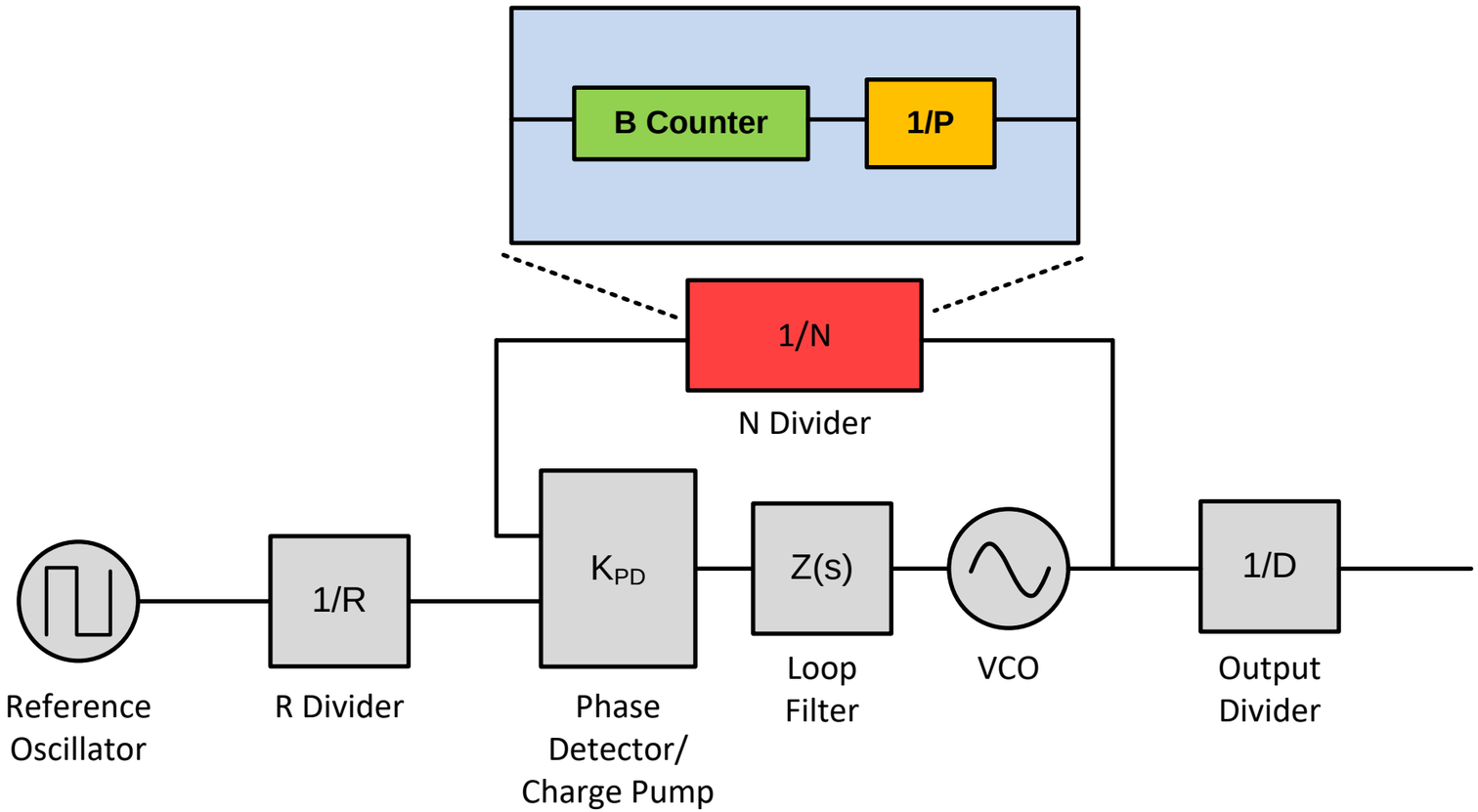
High-frequency feedback (N) divider

- **N counter value**
  - **$N = f_{VCO}/f_N = f_{VCO}/f_{PD}$**
- **Input to this counter can be high frequency**
- **Prescalers are typically inside this counter**



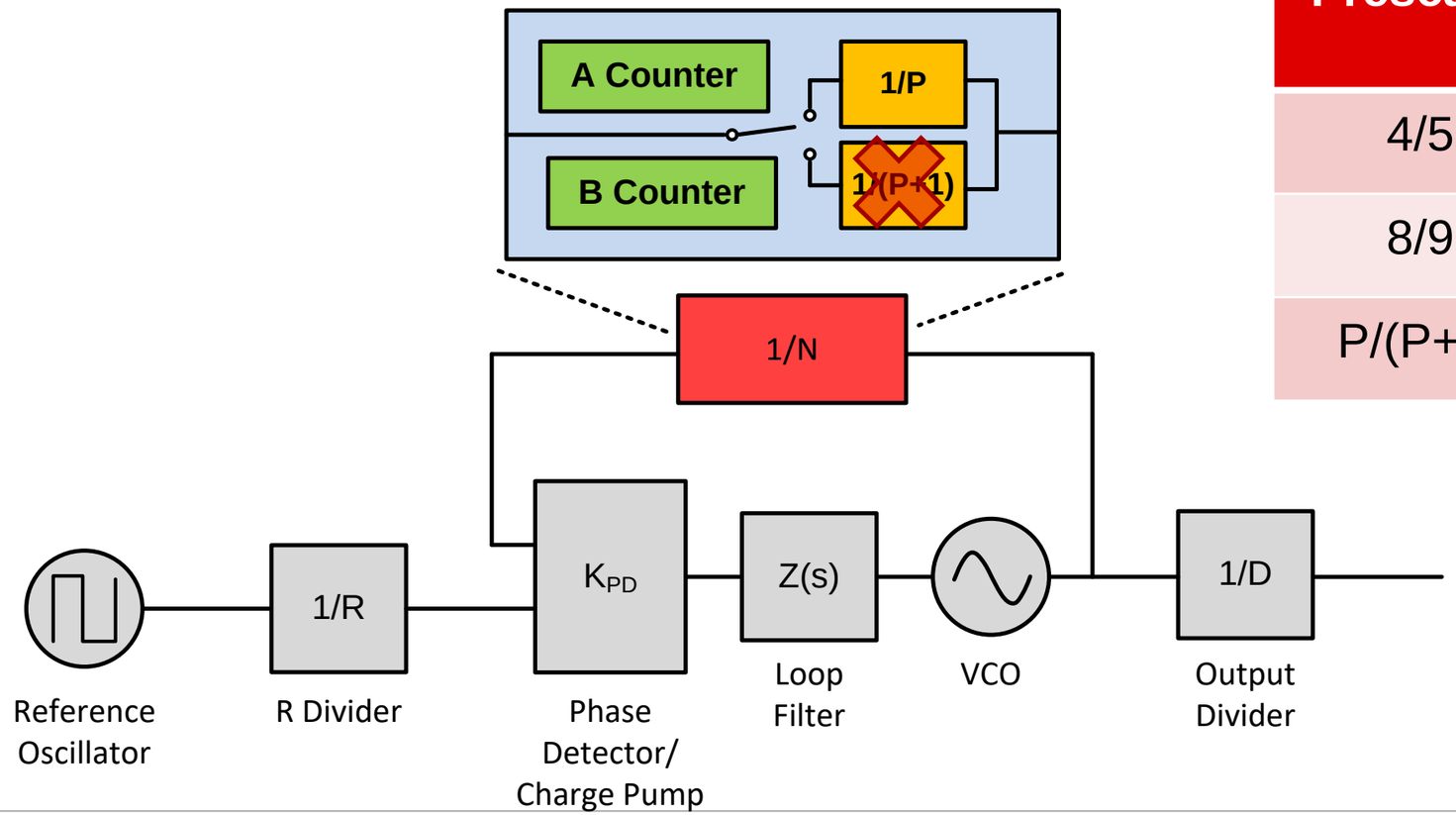
High frequency feedback (N) divider

Single Modulus Prescaler



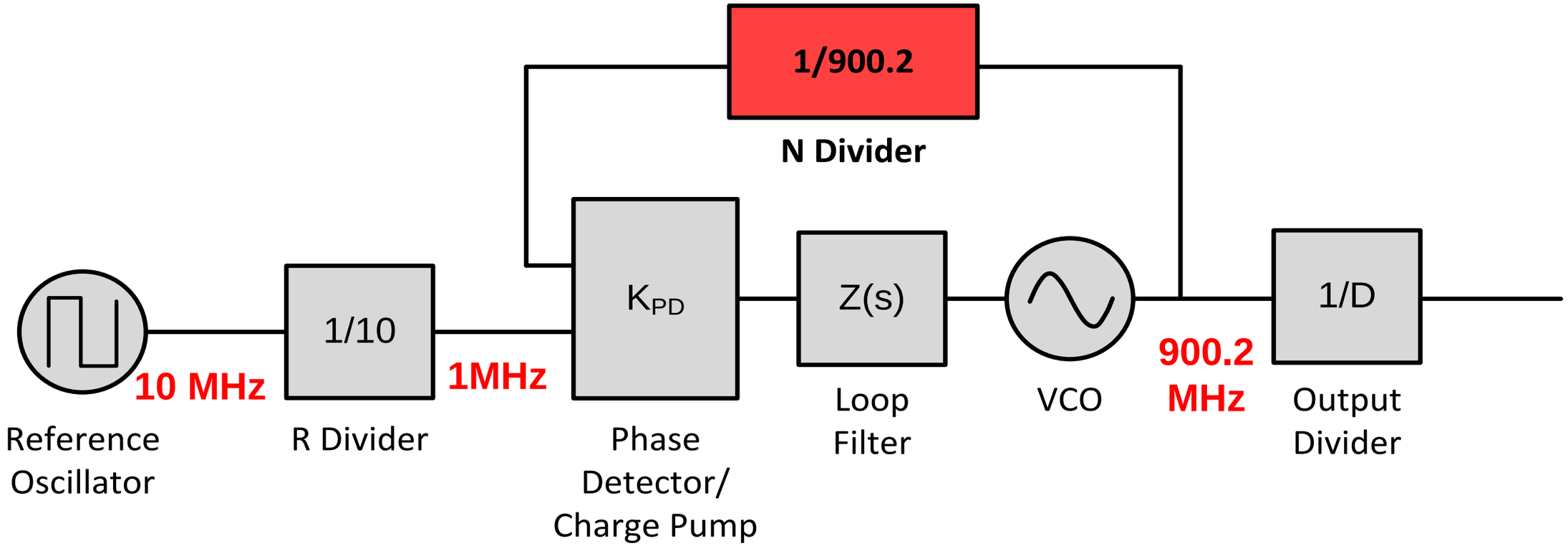
High-frequency feedback (N) divider

- **Dual modulus prescaler**
  - **N = A x (P+1) + (B-A) x P = P x B+A**



Prescaler	Minimum Continuous Divide
4/5	12
8/9	56
P/(P+1)	P x (P-1)

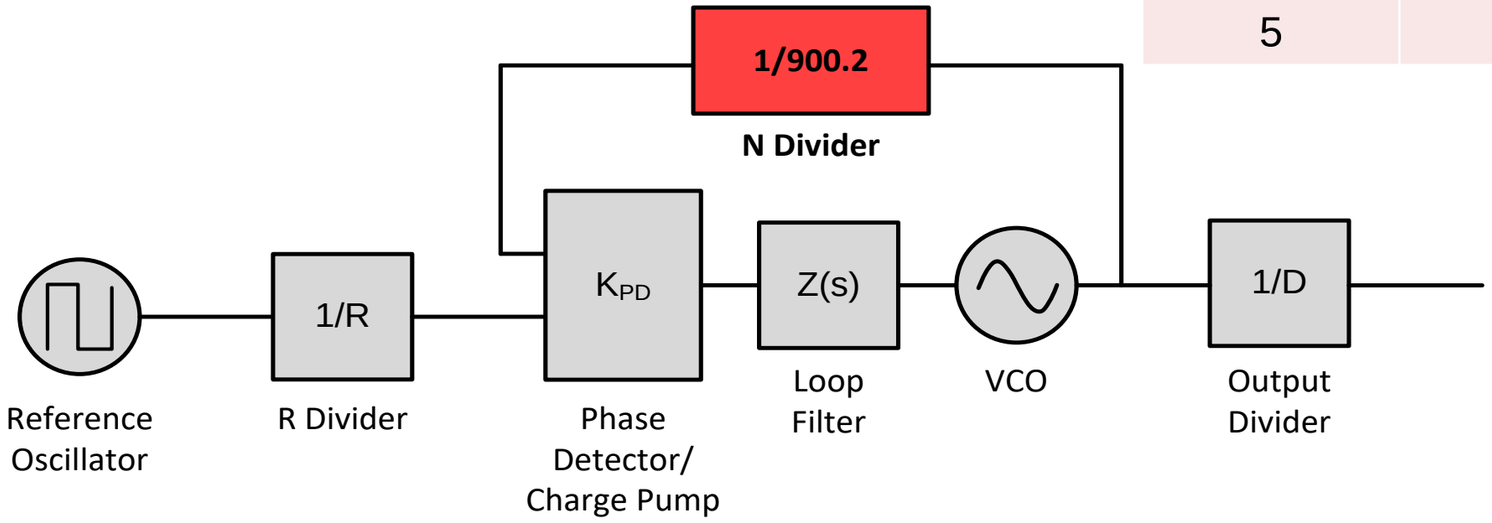
Fractional dividers (Simple 1st order modulator)



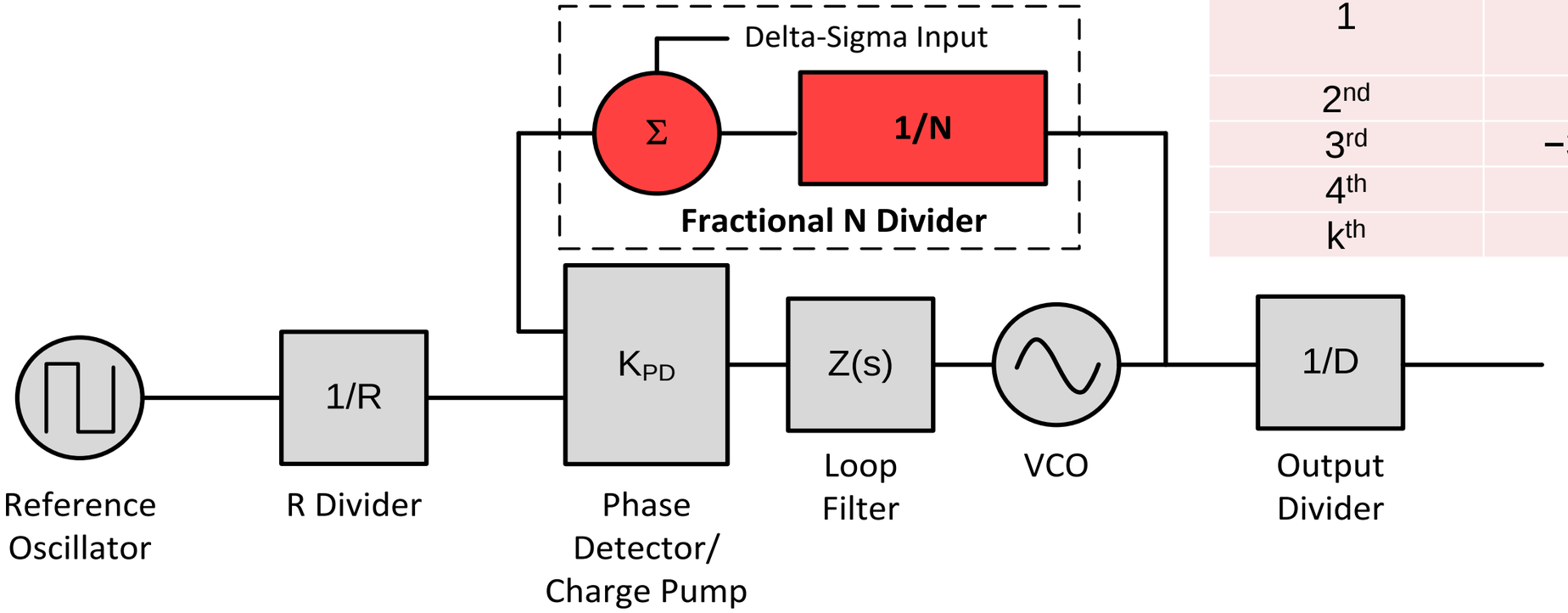
Fractional dividers (Simple 1st order modulator)

Fractional divide timing error

Phase Detector Cycle	Accumulator (Cycles)	N Value	Time for Rising Edge for Dividers (ns)	
			Actual	Desired
1	0.2	900	999.7778	1000
2	0.4	900	1999.5557	2000
3	0.6	900	2999.3335	3000
4	0.8	900	3999.1113	4000
5	0	901	5000.0000	5000



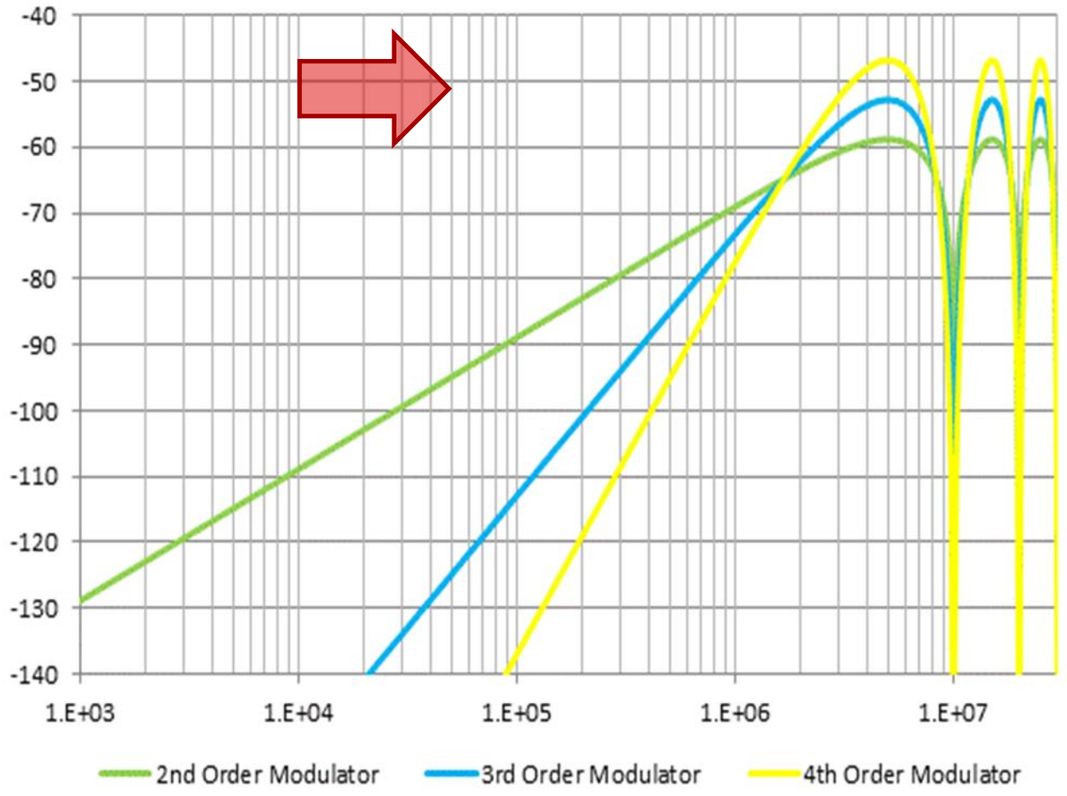
Fractional dividers (High-order modulators)



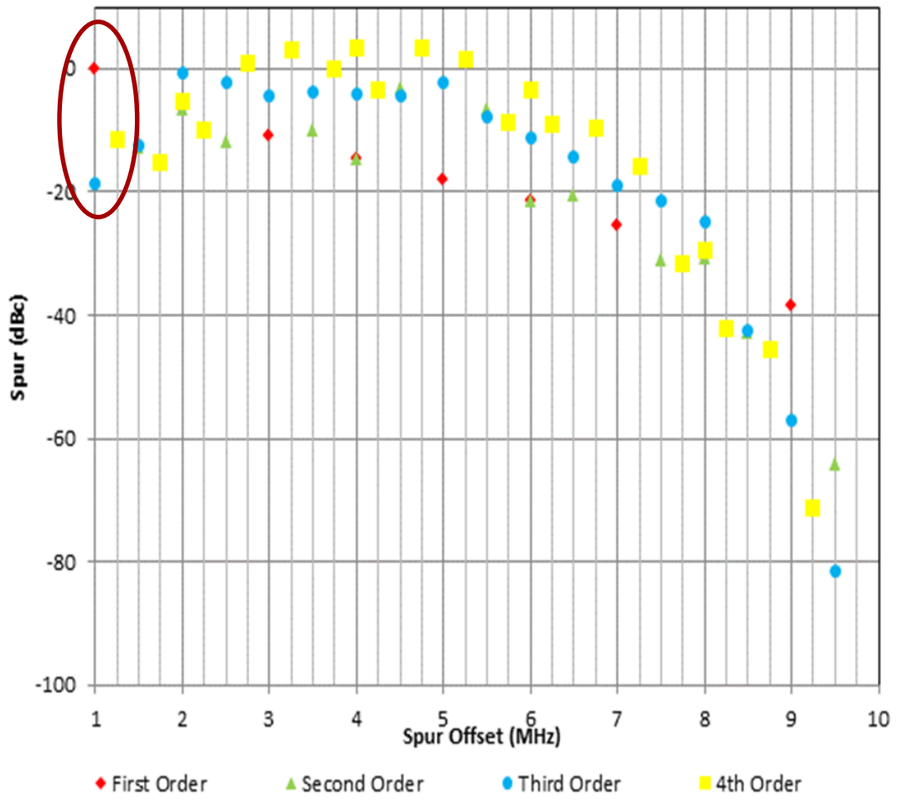
Delta-Sigma Order	Delta-Sigma Input
1	0,1
2^{nd}	−1, 0, 1,2
3^{rd}	−3, −2, −1, 0, 1, 2, 4
4^{th}	−7, ... , +8
k^{th}	-2^k -1, ... , 2^k

Fractional dividers performance (f_{PD} = 10 MHz)

Spur and Fractional Noise Shaping



Spur Example for fraction of 1/10



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Short Quiz

1. **True or False:**

The relationship between f_{VCO} (VCO frequency), f_{PD} (phase detector frequency), f_n (N divider output frequency) is $f_{VCO}/f_N = f_{VCO}/f_{PD} = N$

Short Quiz

1. True or False:

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Short Quiz

2. Choose one:

Which techniques can be used to increase VCO tuning range?

(a) Fractional N divider

(b) Switchable capacitor or inductor array

(c) Output divider

Short Quiz

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Which techniques can be used to increase VCO tuning range

(a) Fractional N divider

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Short Quiz

3. True or False:

A fractional N modulator decreases the noise generated at higher frequencies.

Short Quiz

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A fractional N modulator decreases the noise generated at higher frequencies

Short Quiz

4. Choose all that apply:

Which of below statements apply when using a dual modulus prescaler?

a) Counter will divide by (P+1) A times

b) B < A

c) N= P x B+A

Short Quiz

4. Choose all that apply:

Which of below statements apply when using a dual modulus prescaler?

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TEXAS INSTRUMENTS