

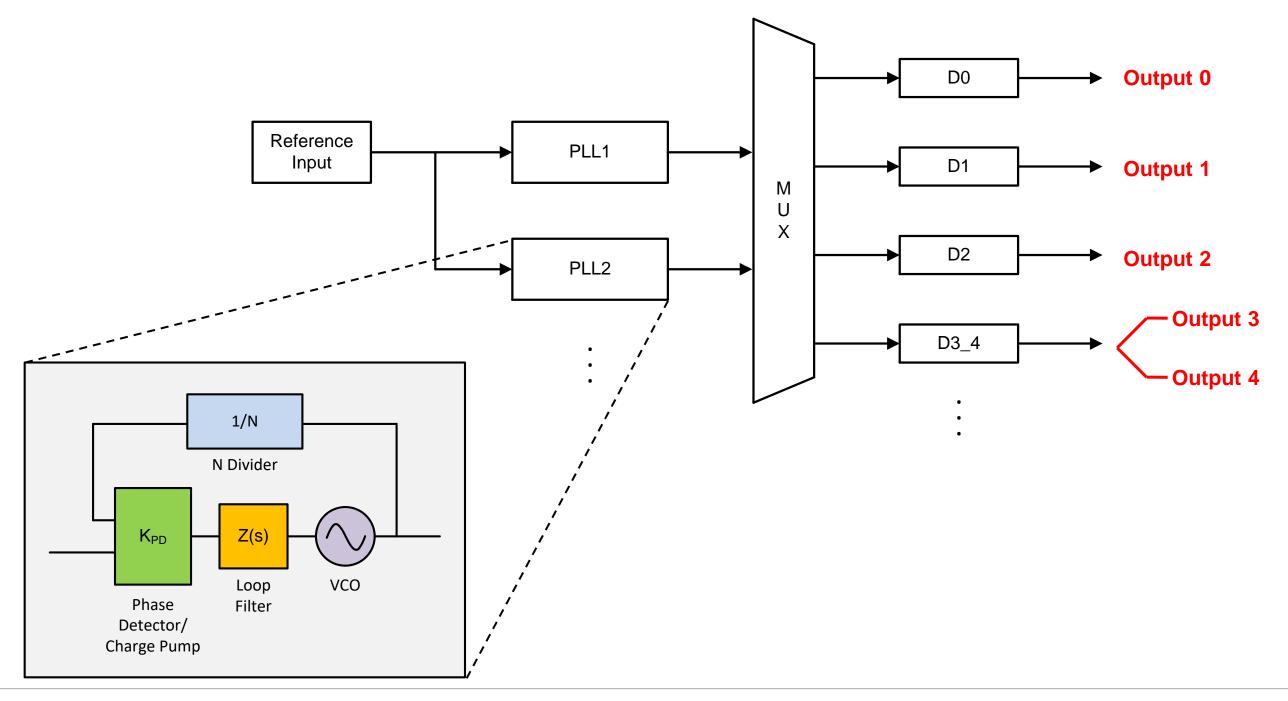
considerations

Presented by Rob Rodrigues

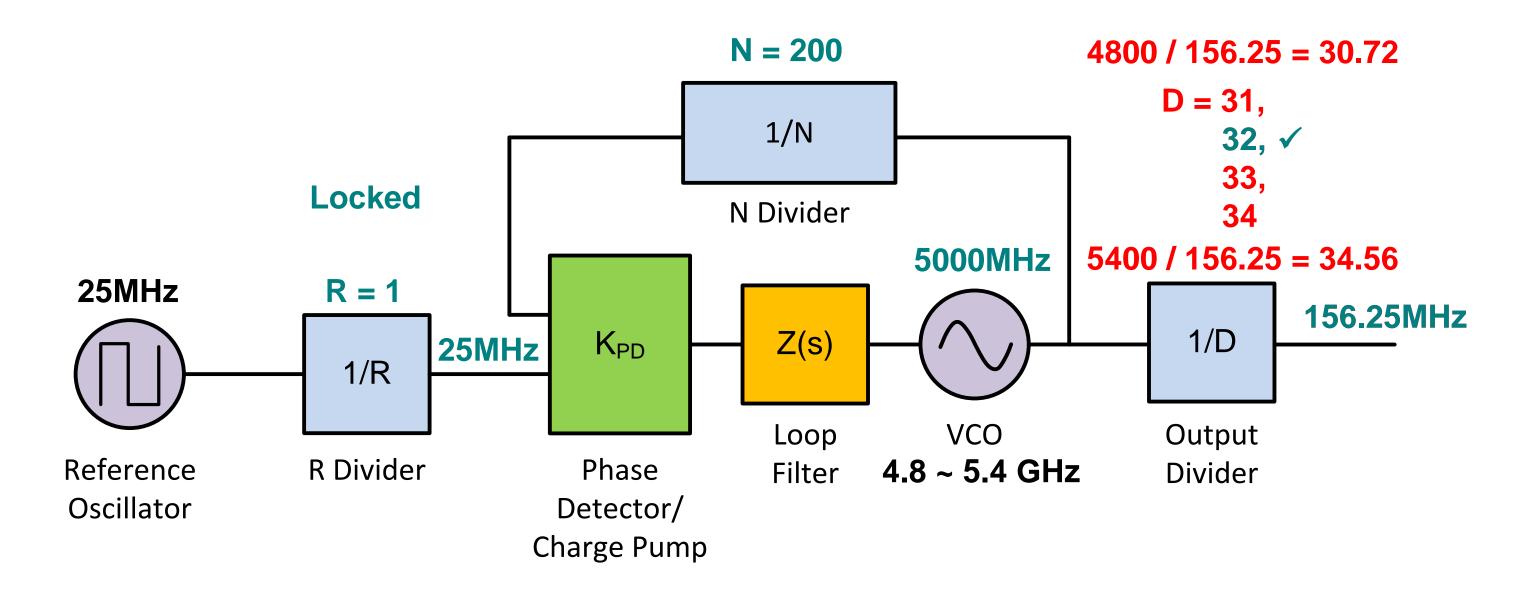
Prepared by Hao Zheng



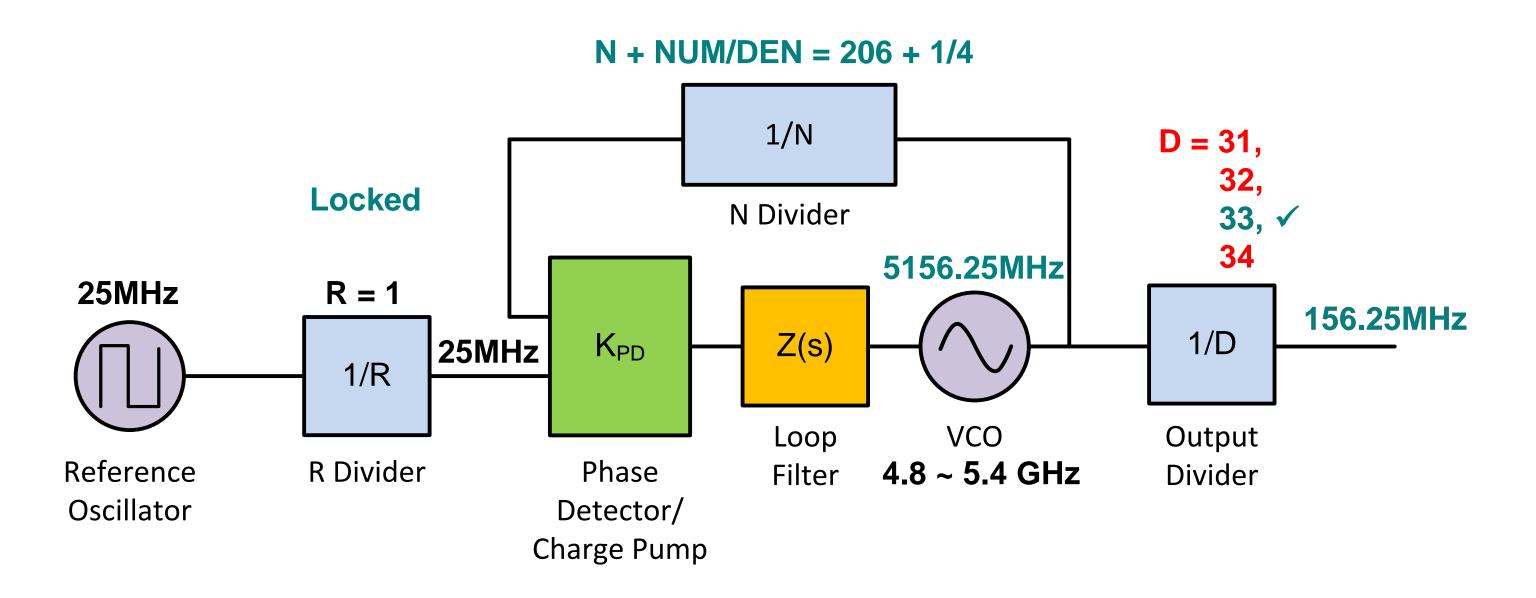
Clock generator overview



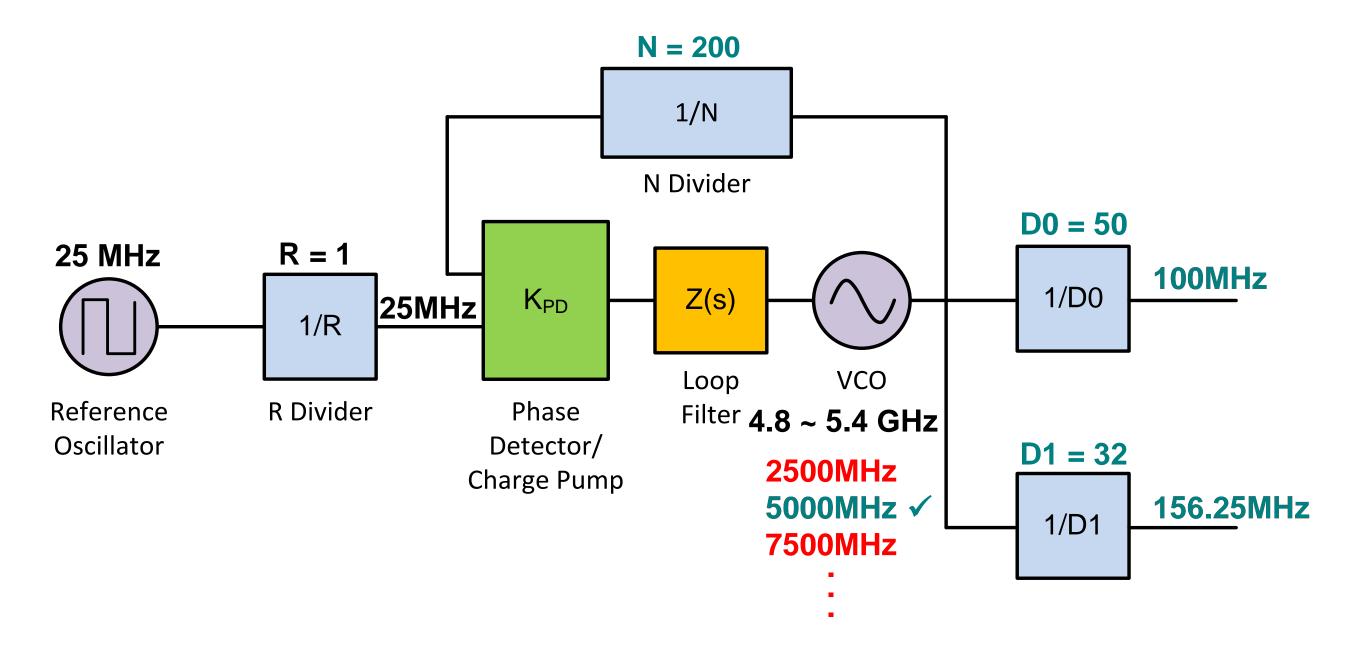
Frequency calculation



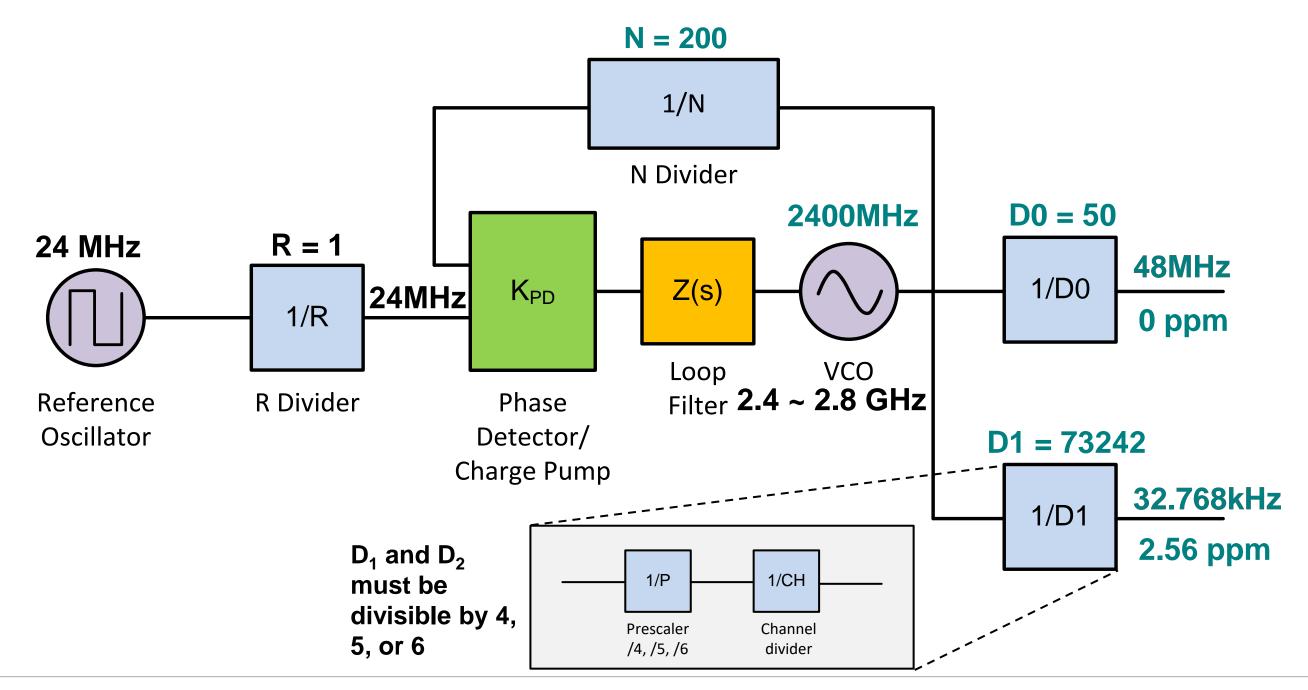
Frequency calculation (cont.)



One PLL, two output frequencies



One PLL, two output frequencies (cont.)



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The relationship between f_{VCO} (VCO frequency), D (output divider value) and f_{out} (output frequency) is $f_{out} = f_{VCO} * D$

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2. Choose one:

The relationship between f_{PD} (phase detector frequency), N (N divider value), NUM (numerator of fractional divider), DEN (denominator of fractional divider) and f_{VCO} for fractional PLL is

(a)
$$f_{VCO} = f_{PD} * (N - NUM/DEN)$$
 (b) $f_{VCO} = f_{PD} * (N + NUM/DEN)$ (c) $f_{VCO} = f_{PD} / (1/N + NUM/DEN)$

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There is only one combination of reference input frequency, phase detector frequency and divider values that can generate the desired output frequency f_{out},

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4. Choose all that apply:

Which constraints determine the relationship between f_{VCO} , f_{out1} (frequency of output 1), f_{out2} (frequency of output 2) f_{VCO_min} and f_{VCO_max} for generating 0ppm outputs?

- a) f_{VCO} is common multiple of f_{out1} and f_{out2}
- b) $f_{VCO}/N = integer$
- c) $f_{VCO_min} < f_{VCO} < f_{VCO_max}$

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